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Article

A Dual-Buck-Boost DC–DC/AC Universal Converter

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Abstract: This paper proposes a universal converter that is capable of operating in three modes for generating positive dc voltage, negative dc voltage, and sinusoidal ac voltage. By controlling the duty-cycle of two half-bridges, an inductor is operated at a high frequency to control the voltage across two film capacitors that constitute a dual-buck-boost converter. Two additional half-bridges operating at a fixed state or line frequency are used to select the mode of operation. Compared to the latest universal converter in the recent literature, the proposed topology has the same switch count while reducing the number of conducting switches for inductor current and reducing the number of switches operating at high frequency. The operation of the proposed dual-buck-boost dc–dc/ac universal converter is analyzed. Experimental results are presented for validation. The power conversion efficiency of the 100 W experimental prototype modeled in PLECS is approximately 98%.

Keywords: buck-boost converter; universal converter

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1. Introduction

Power electronics is the enabling technology for the renewable energy integrated electrical power system. Along with the innovations in power semiconductor devices, there has been a dynamic evolution in power electronics technology. In recent years, the design of converter topologies that can provide a single-stage power conversion with improved compactness and efficiency has become a hot research topic.

Topologies based on the concept of charge pumps [1–3] or switched-capacitors (SCs) are popular owing to attractive features, such as voltage boosting with natural voltage balancing, in their capacitors [4]. In [5–7], an SC is used to establish the concept of virtual dc-bus that can be discharged to generate a negative voltage across the load. They can generate a symmetric 3-level ac voltage in a single-stage operation. With the ac voltage generation referenced to the negative terminal of the dc source, these topologies provide a common ground for the dc source and the ac output that is effective for mitigating the high-frequency common-mode voltage. On integrating two SCs, one of the SCs can be charged to twice the dc source voltage magnitude to enhance the voltage gain [8]. Recent attempts have been devoted to increasing the generation of the number of levels and further enhancing the voltage gain [9–15]. However, all the SC topologies suffer from some constraints inherited from the SC circuits. Current spike induced by the charging process

of SCs by virtue of their parallel connection with the dc source or other capacitors is a major drawback.

To achieve a wide range of voltage gain without a current spike for charging the switched-capacitors, buck-boost converters are popular and have been widely explored [16]. The conventional buck-boost converter is an inverting topology. Its output voltage is of the opposite polarity to the input dc source. This could be a constraint for some practical applications. Therefore, non-inverting buck-boost dc–dc converters have been developed [17]. Soft-switching techniques are also applied to reduce the converter switching loss [18,19].

In recent years, buck-boost converters capable of generating bipolar output voltage are getting more attention [20,21]. By operating the inductor with a variable duty-cycle, a sinusoidal ac voltage can be generated directly without the need of an additional low-pass filter [22]. Using a similar concept, buck-boost inverter topologies with common ac and dc ground are attempted to mitigate the leakage current for photovoltaic applications [23,24]. These topologies provide a single-stage dc–ac power conversion without using bulky electrolytic capacitor, which is attractive for improving the system reliability [25]. A comprehensive method for deriving common-ground-type buck-boost inverters is presented in [26].

The authors in [27] made the first attempt to develop buck-boost universal converters that can generate either dc or sinusoidal ac voltages. This attractive solution can be applicable for dc and ac microgrids. This new concept has inspired the development of a new topology in this paper. The main contribution of this paper is a novel universal converter topology that uses the same switch count as that used in [27] while reducing the number of conducting switches for inductor current and the number of switches operating at a high frequency. The proposed topology integrates two buck-boost converters into a single-stage topology that can be operated in various modes, which will be thoroughly discussed in Section 2. Section 3 compares the proposed topology with the latest universal converter presented in [27]. Experiment results are discussed in Section 4. Finally, Section 5 concludes the article.

2. Proposed Universal Converter

The proposed dual-buck-boost dc–dc/ac universal converter is depicted in Figure 1. By controlling the inductor L using two half-bridges, two buck-boost dc voltages V_{Cp} and V_{Cn} can be generated across capacitors C_p and C_n, respectively. Therefore, this part of the topology is termed as dual-buck-boost converter. It is supplied by a floating dc source. In the remaining circuit of the proposed topology, two low-frequency half-bridges are used to select the operating modes that are elaborated in the following sections.

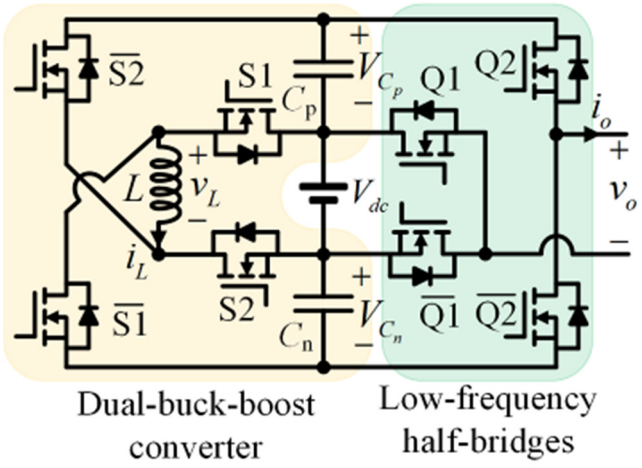


Figure 1. Proposed dual-buck-boost dc–dc/ac universal converter.

2.1. Mode 1: Generation of a Positive DC Voltage

Figure 2 shows the operating principle of the proposed universal converter operating in mode 1 for generating a positive dc voltage. The inductor L is charged by the dc source during state 1 by turning on S1 and S2. Turning off S2 during state 2 charges the capacitor C_p. The voltage across the inductor during this state is $-V_{Cp}$, as shown in Figure 2. During steady-state, the average voltage across the inductor is zero. Therefore, the voltage (V_{C_p}) V_{Cp} can be derived by considering the volt-second balance of the inductor:

$$V_{C_p} = \frac{d}{1-d} V_{dc} \tag{1}$$

where d is the duty-cycle of state 1 that charges L and (V_{dc}) V_{dc} is the dc source voltage. Notice that the voltage gain from buck to boost can be achieved by controlling the duty-cycle d, which is similar to the conventional buck-boost converter. The capacitor voltage ripple ΔV_C and the inductor current ripple ΔI_L are, respectively, written as

$$\Delta V_C = \frac{dI_o}{Cf_s} \tag{2}$$

$$\Delta I_L = \frac{dV_{dc}}{Lf_s} \tag{3}$$

where I_o denotes the average load current supplied by C_p, $f_s = 1/T_s$ is the switching frequency of the converter, and $C = C_p = C_n$.

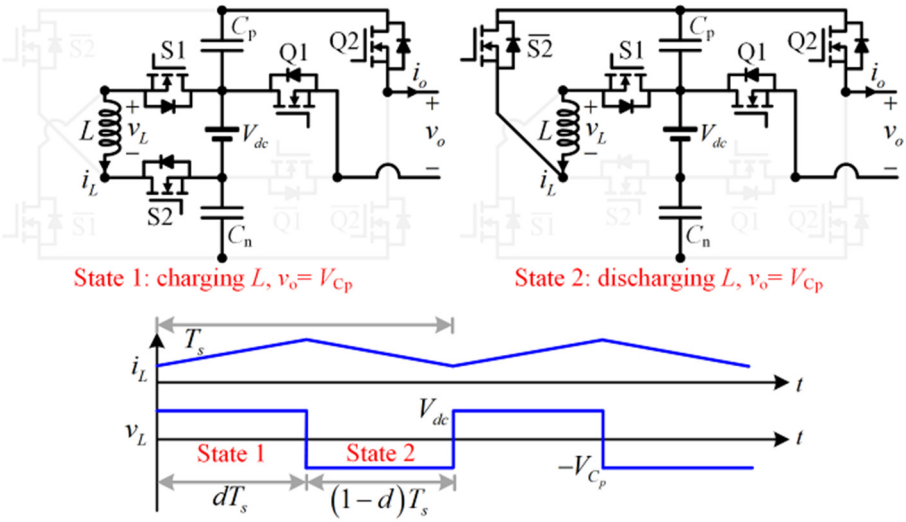


Figure 2. Switching states and key waveforms of the universal converter operating in mode 1 for generating a positive dc voltage.

2.2. Mode 2: Generation of a Negative DC Voltage

To generate a negative dc voltage, the proposed universal converter is operated in states 3 and 4, as shown in Figure 3. The operation of the inductor in mode 2 is similar to that in mode 1. However, it discharges its energy to capacitor C_n instead of C_p during state 4. Each half-bridge in the proposed topology operates in complementary mode. Therefore, the current is flowing through the on-state power MOSFETs instead of their body diode. The voltage V_{Cn} can be calculated by using Equation (1). In this mode, the top switches of both low-frequency half-bridges are turned off. The output terminals are clamped across the capacitor C_n in opposite polarity, thereby generating a negative voltage, i.e., $v_o = -V_{Cn} = -dV_{dc}/(1-d)$.

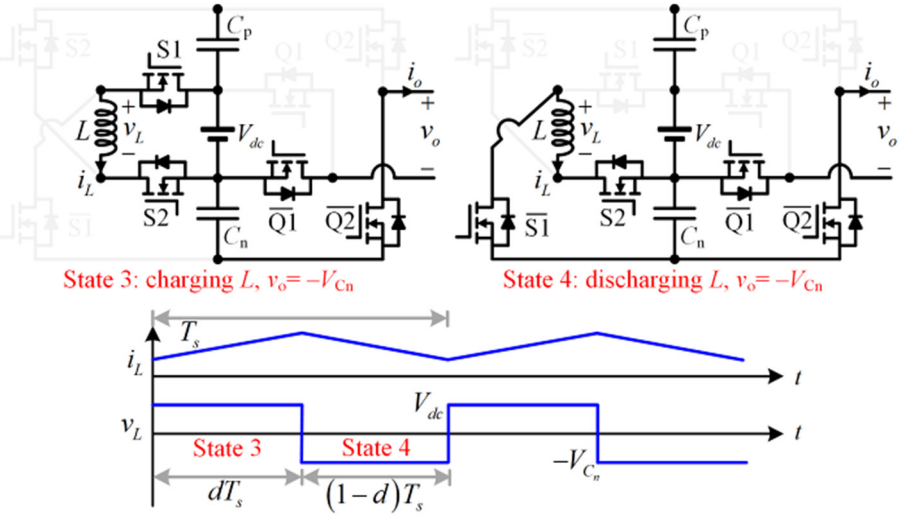


Figure 3. Switching states and key waveforms of the universal converter operating in mode 2 for generating a negative dc voltage.

2.3. Mode 3: Generation of a Sinusoidal AC Voltage

A sinusoidal ac voltage can be generated by operating the proposed universal converter in modes 1 and 2 for generating positive and negative half-cycles, respectively. The ac output voltage can be written as

$$v_o = \hat{V}_{o,1}\sin(\omega t) = \begin{cases} V_{C_p}, 0 \le \omega t \le \pi : \text{Mode 1} \\ -V_{C_n}, \pi \le \omega t \le 2\pi : \text{Mode 2} \end{cases} \tag{4}$$

where $\hat{V}_{o,1}$ denotes the amplitude of the ac voltage. Considering the voltage gain of the buck-boost converter in Equation (1), the following relationship can be obtained:

$$\left|\hat{V}_{o,1}\sin(\omega t)\right| = \frac{d}{1-d}V_{dc} \tag{5}$$

Notice that a sinusoidal ac voltage can be generated directly by controlling the proposed universal converter with a time-varying d written as

$$d = \frac{|G\sin(\omega t)|}{1+|G\sin(\omega t)|} \tag{6}$$

where $G = \hat{V}_{o,1}/V_{dc}$ denotes the voltage gain taking the ratio of the amplitudes of the ac voltage and the dc source voltage. The pulse width modulation (PWM) scheme for mode 3 is summarized in Figure 4. In this figure, G = 1 is considered to show the key waveforms and PWM signals. The feasible range of voltage gain is similar to the conventional buck-boost converter with G = 1.5 or 2 commonly reported in the literature. To reduce the voltage ripple in the output voltage, a high switching frequency relative to the output frequency should be considered. In this work, the switching frequency is 10 kHz, which is 200 times higher than the output frequency of 50 Hz.

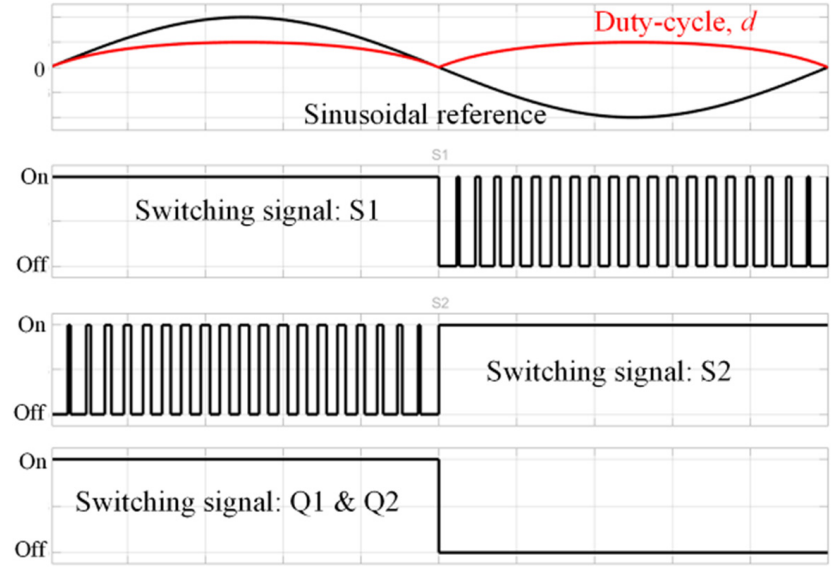


Figure 4. Pulse width modulation scheme of the universal converter operating in mode 3 ($G = 1$) for generating a sinusoidal ac voltage.

3. Comparison with the Latest Topology

The concept of a buck-boost dc–dc/ac universal converter was first introduced in [27]. This latest topology, as depicted in Figure 5, is considered for comparison to justify the advantages of the proposed topology. The switching states of both topologies are summarized and compared in Table 1. Although the total switch count of both topologies is equal and their operating principle is similar, the proposed topology has a lesser number of conducting switches for the inductor current during states 2 and 4, which implies lower conduction loss. To charge the inductor during dT_s and discharge it for the remaining period $(1 - d)T_s$, there are four switches in [27] operating at a high frequency. The proposed topology reduces the number of switches operating at a high frequency to only two in both modes 1 and 2. This is advantageous for reducing the switching loss.

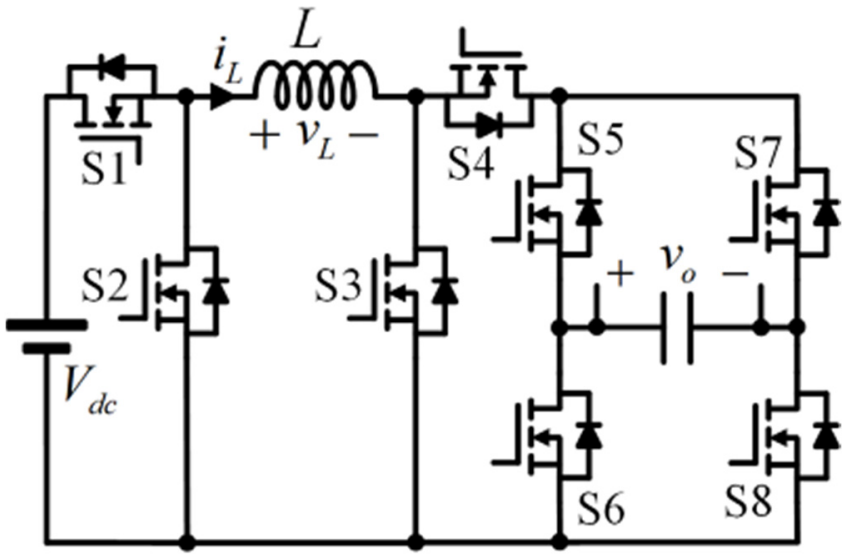
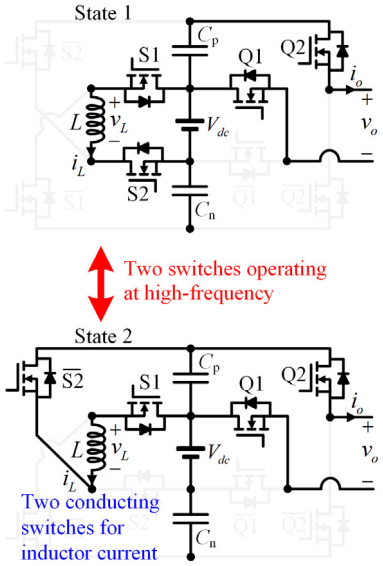
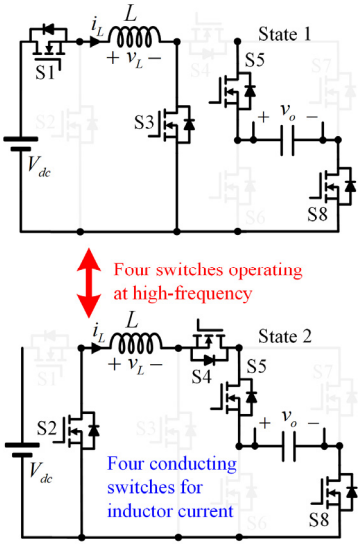
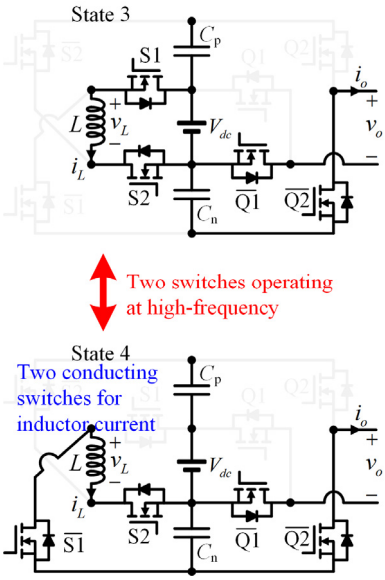
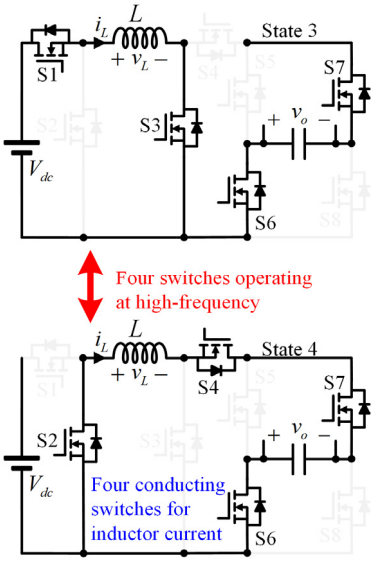


Figure 5. Buck-boost dc–dc/ac universal converter introduced in [27].

Table 1. Comparison between the proposed topology and the latest universal converter presented in [27].

Mode	Proposed Topology	Topology Presented in [27]
1		
2		

4. Experimental Results

The proposed topology was implemented as depicted in Figure 6. Experimental tests were carried out in different operating modes. The following parameters were considered: V_{dc} = 100 V, $C_p = C_n$ = 20 µF, L = 700 µH, f_o = 50 Hz, f_s = 10 kHz, and load resistance = 100 Ω. The proposed universal converter was constructed using eight silicon carbide power MOSFETs (C3M0120090D) according to the schematic in Figure 1.

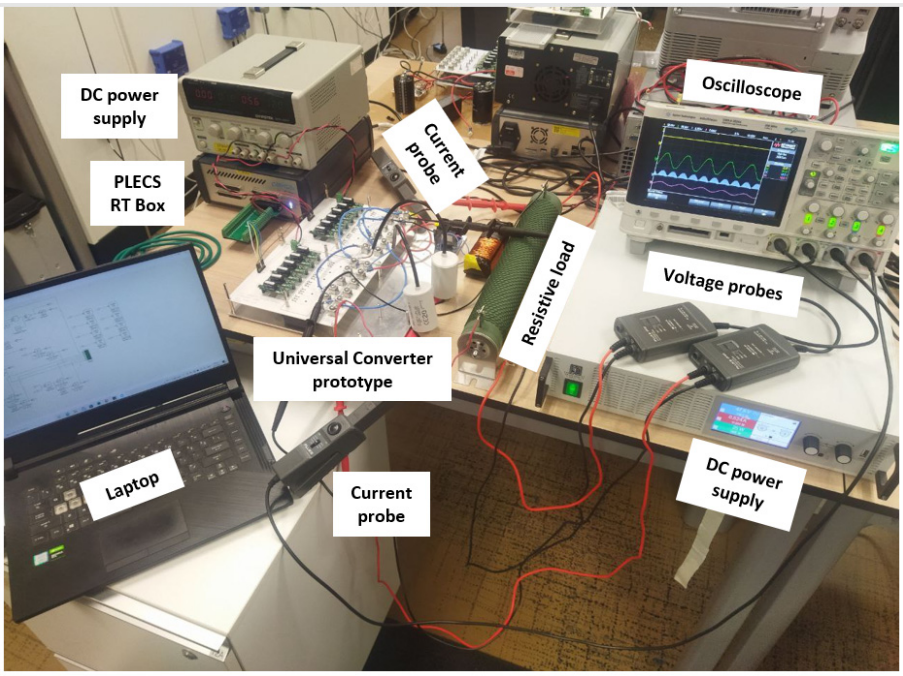


Figure 6. Experimental setup.

The experimental results show a good agreement with the analysis that justifies the operation of the proposed topology. Figures 7 and 8 show the steady-state response of modes 1 and 2 at $d = 0.5$, respectively. With $d = 0.5$, the output voltage is 100 V and -100 V for mode 1 and mode 2, respectively. The voltage C_p resembles the output voltage v_o in mode 1, while the voltage C_n corresponds in opposite polarity to v_o in mode 2. The inductor voltage and the current are the same in both modes.

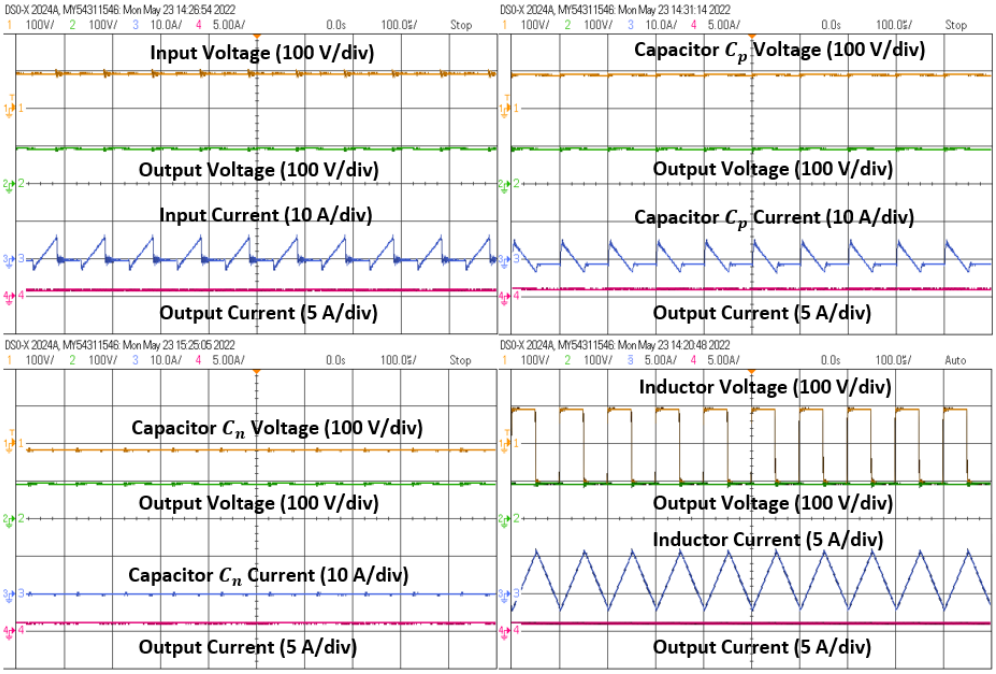


Figure 7. Steady-state response of mode 1 at $d = 0.5$.

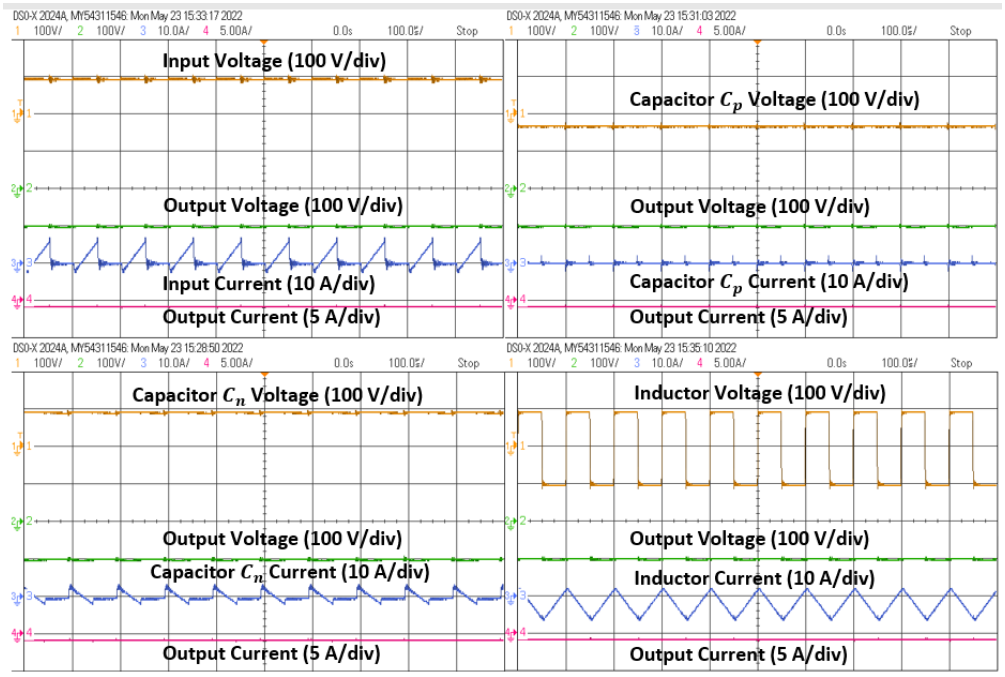


Figure 8. Steady-state response of mode 2 at d = 0.5.

Figures 9 and 10 show the steady-state response of mode 3 at G = 1 and 1.5, respectively. By controlling the duty-cycle of the proposed topology dynamically, the voltage across C_p and C_n is controlled to generate positive and negative half-cycles, respectively. It can be observed in Figure 9 that the output voltage is sinusoidal, with a peak value of 100 V. For G = 1.5, the voltage and current across the passive components are increased by 1.5 times. The sine waveforms of the output voltage and output current validate the ac operation of the proposed topology.

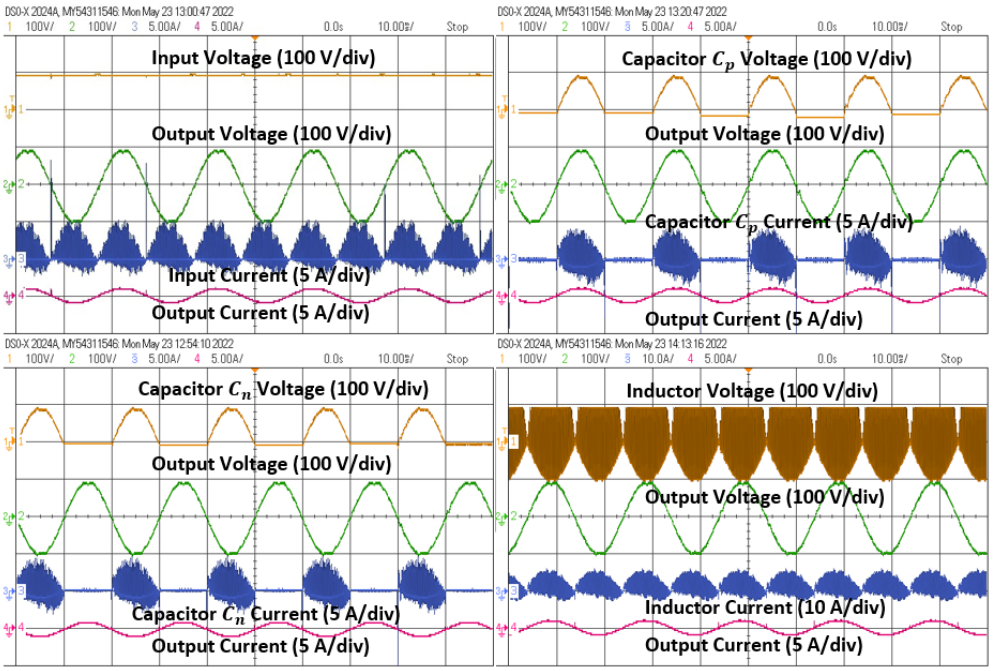


Figure 9. Steady-state response of mode 3 at G = 1.

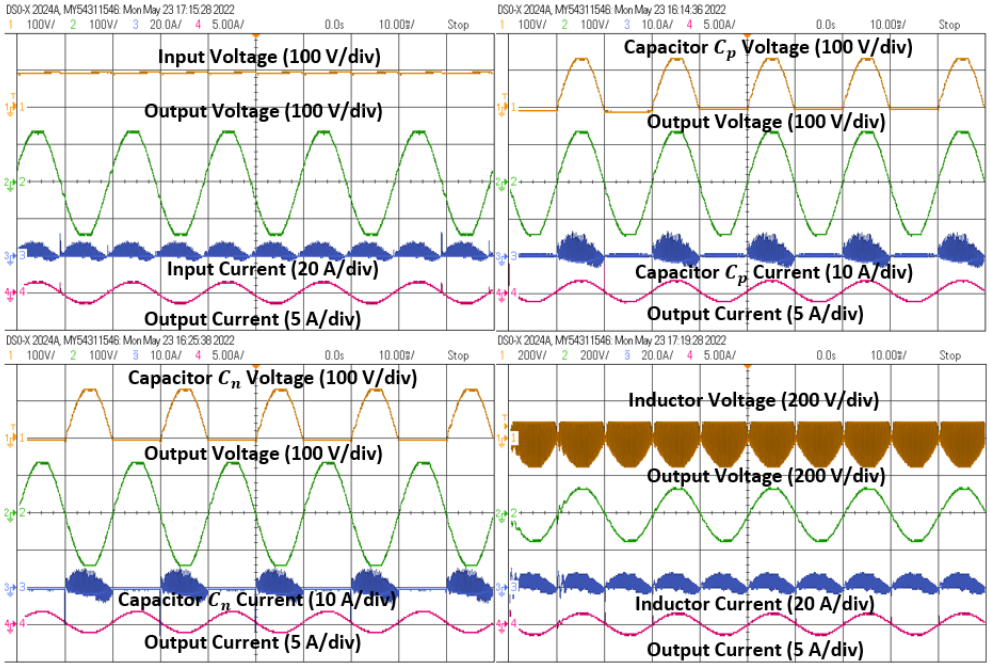


Figure 10. Steady-state response of mode 3 at G = 1.5.

The transient response of mode 3 from G = 1 to 1.5 is presented in Figure 11. When the gain changes from 1 to 1.5, the converter reacts accordingly and the change in the corresponding voltage and current magnitudes is observed. All experimental results are in good agreement with the theoretical analysis. The voltage stress values of S1 − $\overline{S1}$, S2 − $\overline{S2}$, Q1 − $\overline{Q1}$, and Q2 − $\overline{Q2}$ half-bridges are $V_{dc} + V_{Cn}$, $V_{dc} + V_{Cp}$, V_{dc}, and $V_{dc} + V_{Cp} + V_{Cn}$, respectively. To analyze the efficiency of the proposed universal converter, thermal modeling in PLECS was used to simulate the experimental prototype. The power loss distribution of each operating mode is summarized in Figure 12. Due to symmetric operation, the same power conversion efficiency of 97.9% is obtained for both modes 1 and 2. The efficiency of mode 3 is 97.6%.

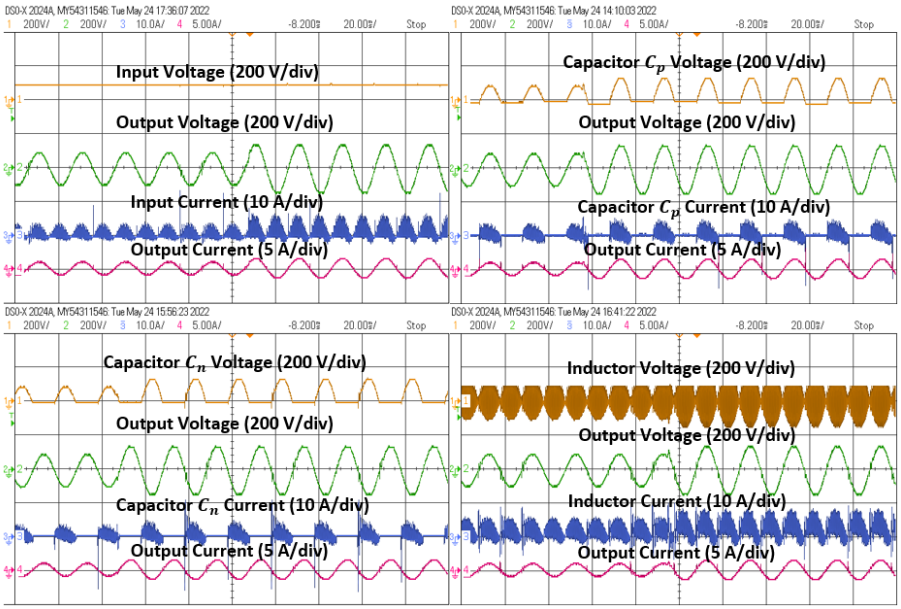
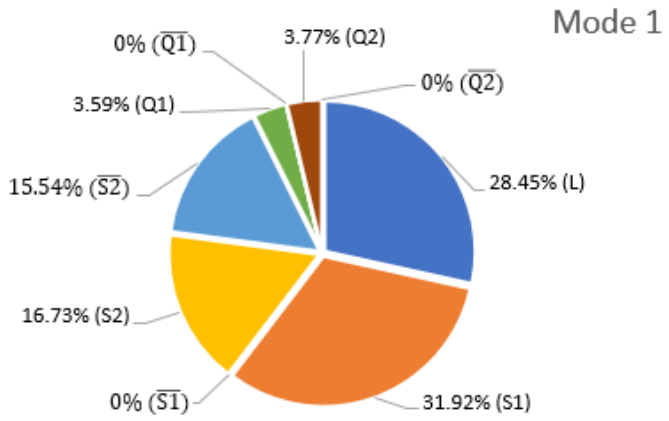
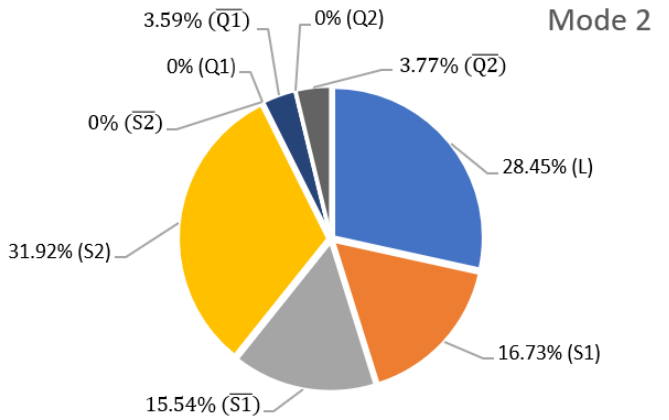


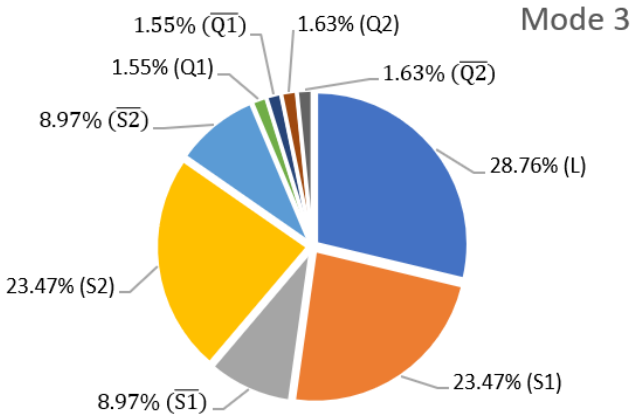
Figure 11. Transient response of mode 3 from G = 1 to 1.5.



(**a**)



(**b**)



(**c**)

Figure 12. Power loss distribution of the experimental prototype operating in: (**a**) mode 1 at $d = 0.5$ (efficiency = 97.9%), (**b**) mode 2 at $d = 0.5$ (efficiency = 97.9%), and (**c**) mode 3 at $G = 1.0$ (efficiency = 97.6%).

5. Conclusions

In this paper, a novel dual-buck-boost dc–dc/ac universal converter is presented. By using two half-bridges, one inductor, and two film capacitors, two buck-boost converters are integrated into a single-stage topology. It can be operated to generate positive dc voltage, negative dc voltage, or sinusoidal ac voltage, with the operating modes selected by controlling two additional half-bridges. This attractive feature makes the proposed topology suitable for both dc–dc and dc–ac applications at low power levels. Experimental results in both steady-state and transient response have verified the feasibility of the proposed topology. The efficiency of the experimental prototype was analyzed by modeling the power devices in PLECS. High efficiency, of approximately 98%, was achieved for all operating modes.

Author Contributions: Conceptualization, S.S.L.; methodology, S.S.L. and Y.R.O.; supervision, S.S.L. and S.C.; resources, S.C.; software, formal analysis, investigation, and writing—original draft preparation, Y.R.O.; writing—review and editing, S.S.L., C.S.L., M.M.C., N.V.K., R.B. and Y.P.S. All authors have read and agreed to the published version of the manuscript.

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