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A Common-Ground-Type Five-Level Inverter with Dynamic Voltage Boost

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Abstract: Today, transformerless inverters (TIs) are widely applicable in different solar photovoltaic (PV) grid-connected applications owing to their promising features, such as higher efficiency and power density. However, high-frequency common-mode voltage (CMV) in these topologies can result in high leakage current, electromagnetic interference, and lack of safety, reducing the whole system's reliability. To resolve the problems associated with TIs, this paper proposes a novel hybrid switched capacitor (SC)-based common-ground (CG) transformerless inverter (TI) topology, which can be applied in grid-connected photovoltaic (PV) applications. The boost inductor is integrated to achieve continuous input current and dynamic voltage gain. In addition, the proposed circuit comprises nine switches and two SCs with a single input DC source. It can generate five-level AC voltage with voltage boosting within a single-stage DC–AC power conversion. The working principles of the proposed topology, circuit description, and control technique are presented. Furthermore, the proposed inverter is comprehensively compared with other five-level TIs to show its superiority. Finally, a laboratory prototype is developed and tested to validate the practical viability of the proposed configuration.

Keywords: common-ground inverters; self-balancing; switched capacitors; transformerless inverters; voltage boost

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1. Introduction

In recent decades, transformerless inverters have developed significantly due to their attractive features, including higher efficiency, compact size, lower cost, and high power density, for many renewable energy applications—particularly for small-scale grid-connected PV systems [1–3]. However, the leakage current in these inverters is the main concern. Therefore, it becomes more critical to employ certain dedicated switching techniques [4–6] and inverter configurations, resulting in reduced efficiency and increased control complexity.

In the literature, many topological structures have been proposed to mitigate the concerns of leakage currents, such as AC and DC decoupling-based circuit configurations. The (HERIC) topology based on the AC decoupling method proposed in this paper is the most popular and efficient of this type, and the DC coupling topologies include H5 and different types of H6 [7,8]. However, the leakage current problem still exists in these inverters. In addition, conduction losses and the lack of voltage-boosting ability in the inverter operation are the biggest drawbacks of such inverter topologies.

Another alternative solution is to employ neutral-point-clamped (NPC) inverters that maintain the common-mode voltage (CMV) constant, thereby mitigating the leakage current to an acceptable range. In addition, the power quality increases by enhancing the number of output voltage levels. In this category, the inverter structures such as active neutral-point-clamped (ANPC) [9,10], t-type [11–14], and flying capacitor (FC)-based [15] are the most developed and efficient topologies. An impedance-source-based five-level inverter was proposed recently in [16]. The main drawbacks of this inverter are its limited voltage gain, high number of components, and leakage current. Therefore, EMI filters are used to minimize high-frequency variation in CMV, leading to an increase in the cost of the inverter. However, in these topologies, the inverter's maximum AC output voltage is half of the DC-link voltage, requiring a two-stage power processing structure that incorporates an additional boost converter for low-voltage PV applications.

Alternatively, a common-ground (CG) TI possessing the ability to eliminate the issue of high-frequency common-mode voltage that causes leakage current is a new approach to fulfil the requirements of grid-connected renewable energy sources—especially PV sources. In recent times, SCMLIs based on the common-ground concept to mitigate leakage current have been popular in the literature [17–22]. A new 5-L CG-type inverter was proposed in [17], with two SCs, six switches, and a diode applicable to PV systems. However, extra sensors are required to balance the SC voltages.

Recently, five-level CG topologies with integrated boost converters have been presented in [18,19]. In [18], boosted output voltage gain was achieved, and the voltage stress was minimized, but the switch count was high. In addition, the voltage gain was limited, i.e., $4V_{in}$ with more switches. A new 5L-boost-ANPC inverter [19] with a similar approach was developed, retaining the advantages of the former while significantly increasing the voltage gain with a lower switch requirement. The concept of common ground in transformerless inverters has further motivated researchers to design improved topologies. From the above discussion, it can be concluded that limited voltage gain and discontinuous input current factors are the key constraints of the recent topologies. To integrate voltage boosting while generating multilevel AC voltage simultaneously, switched-capacitor topologies based on the common-ground concept to mitigate leakage current are popular and widely explored in the literature [16–29]. Despite using a low switch count, they have the following drawbacks: (1) discontinuous DC source (input current), and (2) static voltage gain depending on the number of switched capacitors used in the topology. These drawbacks are serious concerns that hinder their practical application.

Considering the above, this study proposes a new five-level boost inverter to solve the aforementioned limitations with zero leakage current capability. The contributions of the proposed topology are listed as follows:

1. Achieves continuous input current suitable for interfacing with renewable energy sources.
2. Enhances voltage gain with an integrated boost converter and single-stage DC–AC conversion.
3. Eliminating the issue of high-frequency common-mode voltage that causes leakage current.
4. Compared to the latest similar topologies, the proposed inverter achieves higher voltage gain while reducing the switch count.

Section 2 presents the circuit configuration of the inverter and its operation. A complete comparative analysis with other inverters is presented in Section 3. Section 4 presents the simulation and experimental results to validate the inverter's performance. Finally, the conclusions of this paper are provided in Section 5.

2. Proposed Five-Level Common-Ground Boost Inverter

Figure 1 shows the circuit configuration of the proposed five-level boost inverter, termed "5-Level single-stage common-ground boost inverter (5L-S^2CGBI)". Considering the switched capacitor cell integrated into the proposed inverter's topology, the number of

voltage levels is increased from 3 to 5, and the boosting feature is enhanced. Here, nine switches with antiparallel diodes, a single boost inductor, and two capacitors are employed. Since the grid's neutral point is directly connected to the negative rail of the input source, both the AC and DC sides of the inverter are clamped to the same potential. Regarding this, the CMV of the inverter is kept constant, and the leakage current concern is mitigated. Both of the capacitors (C_1 and C_2) are inherently charged and discharged by the boost inductor at high frequency and balanced without any additional control technique or circuitry, as both of the capacitors are connected in parallel at least once in every switching cycle. Figure 2 illustrates the operating modes of the inverter. Only three power switches (S_2, S_8, and S_9) block the maximum voltage level, while the voltage stress of the remaining switches is only half of the maximum voltage level. By using three identical cells connected in parallel to a DC source, the proposed structure can be used for three-phase four-wire applications. Similar to the single-phase topology, high-frequency common-mode voltage is mitigated thanks to the common-ground structure. In addition, the three-phase four-wire structure has the advantage of supplying an unbalanced three-phase load.

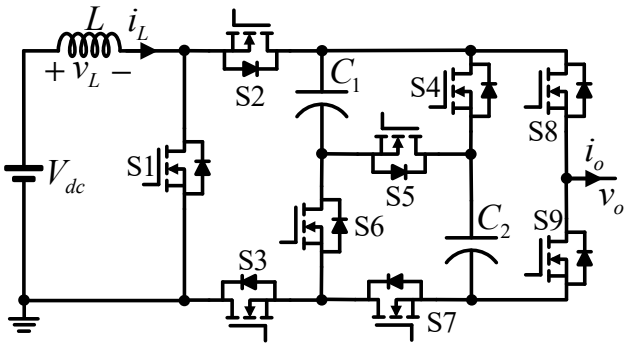

Figure 1. Circuit configuration of the proposed five-level inverter.

To better explain the operating principle of the proposed inverter, level +1 is considered as an example, as shown in Figure 2 and Table 1. Level +1 comprises two operating states: the inductor charging state and the inductor discharging state, as detailed in Figure 2c,d, respectively. When switch S_1 is turned on, the inductor is charged by the DC source, as shown in Figure 2c, while the switches S_3, S_4, S_6, S_7, and S_8 are switched on to achieve the +1 level. For the discharging mode, the operating state is depicted in Figure 2d. For this state, S_1 is switched off, and S_2 is switched on while the same switches S_3, S_4, S_6, S_7, and S_8 conduct. To avoid continuously discharging C_2 during the -1 and -2 levels, the redundant state for [-1 | C] can be used to charge the capacitor.

Table 1. Switching states of the proposed inverter.

State	Power Switches									Inductor
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	
[0]	1	0	1	1	0	1	1	0	1	Charging
	0	1	1	1	0	1	1	0	1	Discharging
[+1]	1	0	1	1	0	1	1	1	0	Charging
	o	1	1	1	0	1	1	1	0	Discharging
[−1]	1	0	1	0	1	1	0	0	1	Charging
	0	1	1	0	1	1	0	0	1	Discharging
	1	1	0	1	0	1	1	0	1	Charging
[−2]	1	1	0	0	1	0	0	0	1	Charging
[+2]	1	0	1	0	1	0	1	1	0	Charging

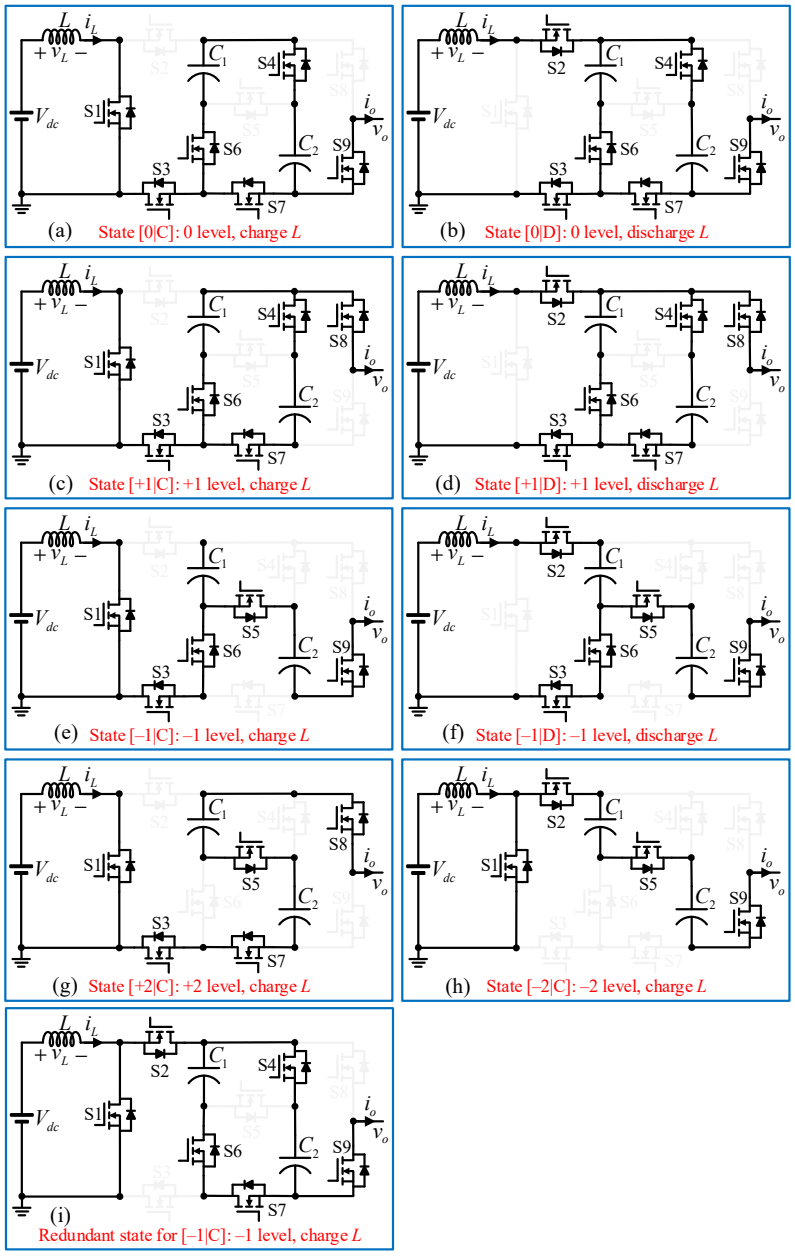

Figure 2. Different modes of operation of the proposed inverter.

The inductor is simultaneously charged in every switching period with a constant duty cycle (D) that boosts the capacitor's voltage across C_1 and C_2, and the average voltage across capacitors C_1 and C_2 is obtained as follows:

$$V_{c1} = V_{c2} = \frac{V_{dc}}{1 - D} \tag{1}$$

Therefore, the maximum voltage level ($V_{\max}$) is the sum of the capacitor's voltage and can be given as follows:

$$V_{\max} = V_{c1} + V_{c2} = \frac{2V_{dc}}{1 - D} \tag{2}$$

By controlling the value of M, the peak of the output voltage can be obtained as follows:

$$V_o = MV_{\max} = \frac{2MV_{dc}}{1 - D} \tag{3}$$

where M is the modulation index (M) with a corresponding minimum $D_{\min}$ that can be determined as follows:

$$D_{\min} = 2M - 1 \tag{4}$$

Therefore, the gain of the proposed inverter considering the D is related to the AC output voltage and the DC source voltage, and it can be determined as follows:

$$G = \frac{Vo}{V_{dc}} = \frac{2M}{1 - D} \tag{5}$$

As the boost inductor is charged with a constant duty cycle D, the inductor ripple current is similar to that of the classical DC–DC boost converter.

$$\Delta I_L = \frac{DV_{dc}}{Lf_s} \tag{6}$$

where f_s is the frequency of the triangular carrier. The voltage ripple of the capacitor is

$$\Delta V_C = \frac{D(1 - D)I_L}{Cf_s} \tag{7}$$

where I_L is the average inductor current.

3. Comparison with Recent 5L-CG Inverters

A comprehensive assessment of the proposed 5L-CG inverter (P) in comparison with other recently developed topologies is presented in Table 2. The proposed inverter was investigated in terms of the required numbers of power switches, diodes, inductors, capacitors, continuous DC source current and voltage-boosting features, and the common-ground ability.

Table 2. Comparative study of the proposed inverter with its counterpart topologies.

Ref.	N_{SW}	N_D	N_C	N_L	N_{level}	G	CIC	CG	η
[10] *	10	0	3	1	5	$0.5M/(1-D)$	Yes	No	NA
[19]	7	0	2	1	5	$M/(1-D)$	Yes	Yes	94.9% @ 1 kW
[16]	8	6	4	4	5	1	No	No	95.3% @ 200 W
[17]	6	1	3	0	5	1	No	Yes	95.8% @ 1.2 kW
[18]	10	0	2	2	5	4	No	Yes	97.1% @ 600 W
[20]	6	2	3	0	5	2	No	Yes	98% @ 500 W
[21]	7	2	2	0	5	2	No	Yes	98.1% @ 600 W
[22]	6	2	3	0	5	2	no	Yes	98.1% @ 600 W
P	9	0	2	1	5	$2M/(1-D)$	Yes	Yes	96% @ 1.2 kW

N_{sw} = number of switches, N_D = number of diodes, N_C = number of capacitors, N_L = number of inductors, N_{Level} = number of levels, G = gain, CIC = continuous input current, CG = common ground, η = efficiency. * Conventional two-stage five-level ANPC inverter with a frontend boost converter is considered as the benchmark.

In [16], the voltage gain was restricted to unity, a leakage current issue existed, and split LCL filters were used to reduce high-frequency variation in the CMV. The main contributions of the proposed topology compared with [19] are (1) doubling the voltage gain, i.e., the voltage gain of the proposed topology is $2M/(1 - D)$, and (2) improving the dynamics of the capacitor voltage, whereas in [19] the second capacitor is balanced at the fundamental frequency (50/60 Hz), which has slow transient dynamics. The proposed inverter offers many advantages when compared with [18,20–22], such as (1) achieving continuous input current, whereas the input current of these inverters is discontinuous in

nature, and (2) achieving higher and dynamic voltage boosting gain, while the voltage gain of [18] is limited to four and that of [20–22] is limited to two.

4. Simulation and Experimental Results

A low-scale laboratory prototype was developed to verify the feasibility of the proposed inverter, as shown in Figure 3a. The list of parameters used in the measurement process for both simulations and experiments is given in Table 3. The following parametric values were set corresponding to the inverter prototype: V_{in} = 24 V, load at R = 100 Ω and R = 100 Ω, L = 200 mH with a power factor of 0.85, L = 3 mH, fs = 5 kHz, M = 0.8, and D = 0.8. The values of C_1 and C_2 were set to 1200 µF with voltage ratings of 250 V. The level-shifted pulse-width modulation (LS-PWM) with a switching frequency of 5 kHz was considered to control the inverter and was implemented using the dSPACE 1104 controller.

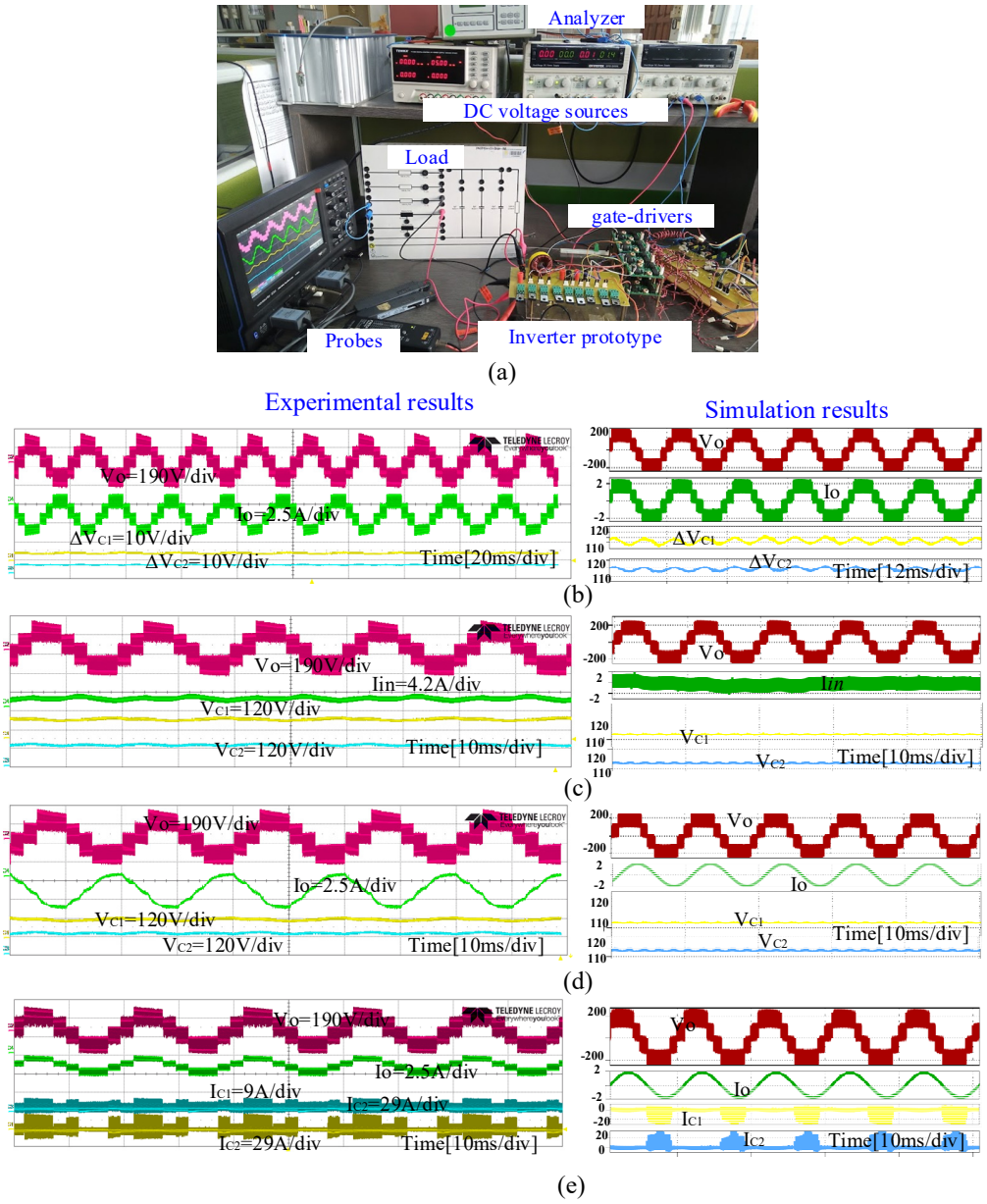

Figure 3. (**a**) Experimental setup, and steady-state experimental and simulation results for R-load (R = 100 Ω); (**b**) C_1 and C_2 voltage ripple; (**c**) input current and capacitors' voltage ripple, and steady-state results for RL-load (R = 100 Ω, L = 200 mH); (**d**) C_1 and C_2 voltage; (**e**) C_1 and C_2 charging current.

Table 3. Type and description of the parameters used in analysis and measurement.

Element	Type	Description
Input DC voltage (V_i)	-	24 V
Modulation index (M)	-	0.8
Duty cycle (D)	-	0.8
Switching frequency (f_s)	-	5 kHz
Operating frequency (f_o)	-	50 Hz
Power switches	IRGP35B60PDPBF-IGBT	600 V/60 A, R_{On} = 22 mΩ
Controller	dSPACE	DS1104
Switching frequency	5 kHz	-
C_1 and C_2	ALC70A102EH450 -electrolytic capacitors	1200 µF, 450 V
Boost inductor	Ferrite core	3 mH
Load	Resistor and inductor	R = 100 Ω & RL = 100 Ω + 200 mH
Gate driver	TLP250	IC chip

Figure 3b–e show the experimental and simulation results obtained in the steady state of the inverter's operation. Here, the output voltage and current five-level staircase waveforms were obtained without using output filters. Meanwhile, the peak fundamental output voltage reached nearly 192 V, which is eight times the input voltage. The voltage waveforms across C_1 and C_2 are illustrated in Figure 3c to verify the balanced voltage of the SCs. As can be observed, the SCs are balanced around 120 V. Figure 3b,e display the input DC source and the capacitor's current waveforms, respectively. For the non-unity power factor at R = 100 Ω, L = 200 mH; the corresponding output voltage waveform is shown in Figure 3d. It is obvious that the proposed inverter is suitable for reactive power capability in grid-connected PV applications. Figure 4 shows the experimental voltage and the current spectra of the output voltage. It can be seen that the low-order harmonics are removed, and other higher-order harmonics are placed around the multiple integrals of switching frequency.

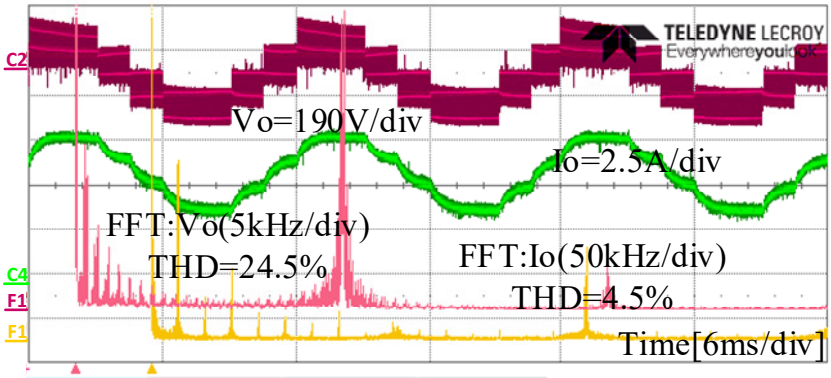

Figure 4. Experimental frequency spectra and THD.

To further investigate the feasibility of the inverter in dynamic modes of operation, it was tested for both load and modulation index variations. The measured experimental waveforms under the load variation from (R = 100 Ω, L = 200 mH) and the modulation index variation (M = 0.8 to M = 0.4) are captured in Figure 5a,b, respectively. It can be observed that the output voltage waveforms are unaffected during both the load transient and the modulation index transient. The results confirm that the proposed inverter is able to adapt to sudden variations in modulation index and load. The efficiency and loss

distribution among the power components of the proposed CG inverter were analyzed over a wide range of output power with PLECS simulation software, as shown in Figure 6. Here, the value of the input voltage was set to 100 V. In addition, the conduction, switching, and ripple losses were taken into consideration for efficiency evaluation. The thermal modeling of the semiconductor devices was developed from the datasheet of the IKY75N120CH3 module. Efficiency as high as 96% was achieved at 1230 W, which was mainly attributed to its single-stage power conversion feature. It can be observed that the conversion efficiency of the proposed inverter is above 91% over a wide range of output power.

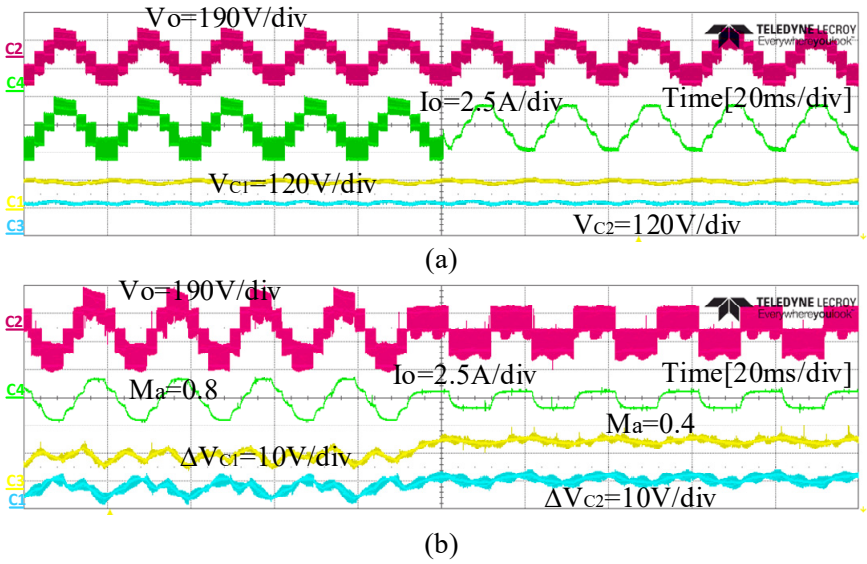

Figure 5. Step response with variation of (**a**) load from RL-load (R = 100 Ω, L = 200 mH) to R-load (R = 100 Ω), and of (**b**) modulation index from M = 0.8 to M = 0.4.

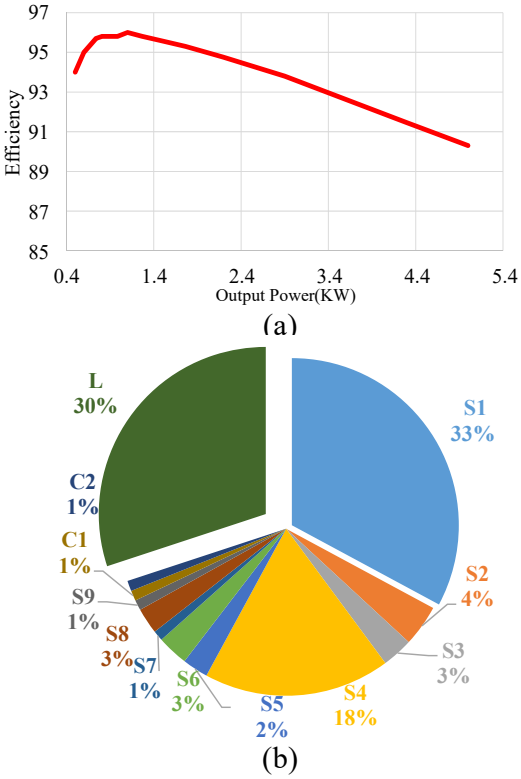

Figure 6. (**a**) Efficiency curve; (**b**) loss distribution among power components.

5. Conclusions

This paper proposes a five-level inverter based on the common-ground concept with single-stage power conversion for renewable energy applications. The proposed topology is equipped with an integrated boost converter in such a way as to achieve high gain. In addition, the common ground provided between the DC and AC terminals totally eliminates the leakage current due to CMV, making it very suitable for transformerless applications. The boost inductor is integrated into the proposed topology to achieve dynamic voltage gain and continuous input current. In addition, the proposed circuit comprises nine switches and two SCs with a single DC input source. It can generate five-level AC voltage with voltage boosting within a single-stage DC–AC power conversion. The working principles of the proposed topology, circuit description, and control technique are provided to show the operation of the inverter circuit. Comparative assessment against its recently introduced counterpart topologies verified its merits of high voltage gain and continuous input current. Furthermore, the accurate operation and performance of the proposed topology were confirmed and analyzed through simulations and experimental results. The feasibility of the proposed inverter was verified through steady-state and dynamic-state experimental results. The attractive features of the proposed topology, such as high voltage gain and continuous DC source current, make it an attractive alternative for transformerless PV applications.

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