Disturbance Rejection Based Control Strategy for Single-Phase AC-DC Converter with Ripple Voltage Estimation Capability

***Abstract*—This paper presents a robust control scheme for a single-phase grid-connected five-level AC-DC power converter. The primary objective is to achieve superior dynamic performance in realizing the regulated DC bus voltage under external disturbances and generating high-quality grid current at the same time. The proposed control approach includes a new filter-less DC bus ripple voltage estimator and a simple technique to remove this ripple from the measured DC bus voltage. This method presents fast dynamic performance in estimating the DC value of the bus voltage during transients and completely removes this ripple from the measured voltage. Consequently, it enables reducing the grid current distortion and improves the dynamic performance in achieving the regulated DC bus voltage. In this paper, a sliding-mode control (SMC) incorporated with an extended-state observer (ESO) is proposed as the external voltage control loop. This controller dynamically calculates the control input (i.e., active power reference) for the internal current tracking controller. The proposed SMC-ESO approach asymptotically rejects the external disturbances, and thus, significantly improves the dynamic performance during system uncertainties. Moreover, a finite control set-model predictive control algorithm is derived as the inner current controller to track their references while balancing the DC-bus capacitor voltages. Simulation and experimental studies are conducted to verify the proposed control scheme.**

***Index Terms*— disturbance rejection, active power, double-frequency ripple, grid-connected converter, model predictive control, observer, power quality, single-phase.**

I. Introduction

SINGLE-PHASE voltage-source converters (VSCs) are the main component enabling the integration of electric vehicles (EVs), energy storages (ESs), and renewable energy sources (RESs) into the grid. These converters can be employed as the active front end (AFE) rectifier as well as to control power factor to provide ancillary services when required [1-4]. The design of a robust control system for these converters is of great importance to the interfacing of the EVs and ESs into the power grid. In a single-phase power conditioning system, the DC-bus voltage plays a significant role in the power flow between the grid and the DC side source or load. It is also responsible for shaping the generated grid current. The DC bus voltage control is a challenging task due to the presence of the double-grid frequency pulsating power component that flows through the DC-side of the converter. This pulsating power causes double-line frequency voltage ripple in the DC bus voltage. The presence of this voltage ripple in the DC bus is inherent in both inverters and rectifiers [5-7].

The measurement of this ripple voltage in a feedback control system degrades the generated grid current quality by adding additional harmonic. Therefore, this ripple must be removed for high-quality power conversion. A low bandwidth filter must be designed to filter out this low frequency ripple term completely [8], which introduces a high phase delay in the voltage control loop. As a result, the control performances in achieving the regulated DC bus voltage is affected during transients. Therefore, a high bandwidth is desired to achieve fast transient performances in regulating the bus voltage, and thus, have to make a trade-off between the conflicting constraints such as grid current quality and dynamic performances [5]. The coupled inductor and loop compensator based approaches are presented in [9-11]. However, these approaches require a high order filter with poles and zeros at low frequencies. Several active filter based techniques have been introduced in [7, 12-17]. Nevertheless, these techniques require additional energy storage devices and converters in the DC side, which increases the cost and control complexity, and decreases the overall efficiency. To remove this ripple, a notch filter (NF) and finite impulse response (FIR) filter tuned at 2ω are reported in [5], and [18], respectively. However, a low bandwidth must be selected during filter design for complete elimination of this ripple, which result in slower dynamic response during transients.

To settle the conflicting constraints of grid current distortion and dynamic performance, there is essential for the new technique, which can achieve low-harmonic distortion of the grid current, while realizing fast dynamic performance. This paper introduces a new filter-less approach to remove this ripple from the measured DC bus voltage. This work analyzes the DC bus voltage and provides an expression of the DC bus ripple voltage component. Instead of using additional filter or hardware, the new controller uses the phase locked loops (PLLs) information to calculate this ripple voltage. The estimated ripple is then added with the measured DC bus voltage to obtain the DC component of the bus voltage. Since the proposed approach eliminates the need for filter or additional hardware, thus, it enables the voltage control loop design that overcomes the trade-off among the conflicting constraints, and improves the transient performance without distorting the generated grid current.

Another important control objective is to self-support the DC bus voltage under disturbances such as sudden variation of the active power drawn by the converters due to the sudden load changes. The bus voltage regulation is usually done by the outer voltage controller, where a feedback loop is used to

updates the control input (active power reference). Numerous control techniques have been reported in the literature to achieve this control objective. The most commonly employed methods are PI based controllers due to their simple structure. These controllers employ PI with constant gain parameters for both of the outer voltage controller and inner current controller [19]. Several PI based methods have been reported in [10, 20-25]. The performance of these methods depend on the PI controller gain parameters that need to be updated during the different operating conditions. However, most of these methods did not consider these variations. Thus, the dynamic performance will be affected by the use of constant PI gain parameters during different operating conditions. A PI-based method presented in [10], which considers the both conflicting constraints, such as the grid current quality and the dc-bus voltage fluctuations. However, this method causes a distorted grid current at low bus capacitor value. To reduce the DC bus voltage fluctuations during external disturbances, the feedforward control approaches are reported in [21, 26, 27]. These methods feed forward the DC load current or external power to reduce the voltage fluctuation. However, these methods requires additional sensors to measure the load current or external power, which increases the cost and decreases the reliability. Nevertheless, these approaches increase the grid current harmonics due to the coupling between the DC and AC sides. The major drawback of the PI based strategy is that the dynamic and steady state performances depend on the tuning of PI gain parameters in both outer voltage controller and inner current tracking controller. Therefore, the overall system behavior will be affected by the use of fixed PI parameter during external disturbances.

The other commonly studied approaches are direct power control (DPC) [28], Fuzzy control based DPC [29], and model predictive DPC [30, 31]. Among these methods, the predictive control method provides the best performance. However, the parameter sensitivity is the major problem of the predictive control methods [19, 30]. Recently, several advance methods have been proposed in three-phase applications to improve control performance such as model predictive power control [32], model predictive current control [33], model predictive DPC [34], fuzzy logic based MPC [35], sliding mode MPC [19], multi-vector MPC [36], and disturbance observer based MPC [37]. These control methods are usually governed by the conventional PI-based outer control loop. Therefore, the control performance of these methods still suffer in terms of poor dynamic behavior or overshoot during system parameter uncertainties. Moreover, these control approaches are not studied in single-phase applications. Thus, it much desired to design an advanced control method to improve the dynamic and steady state performance against the disturbances, and system parameter fluctuations.

In order to overcome the limitations of the existing methods, this paper proposes a sliding mode control (SMC) incorporated with an extended state observer (ESO) as the outer voltage controller. The SMC-ESO significantly improves the dynamic and steady state performance in the presence of disturbances. The available literature shows that single-phase applications employs traditional three-level H-bridge converter. In contrast, this paper adopted five level T-type converter in order to achieve improved grid current quality. Furthermore, it reduces the required voltage rating of the semiconductor devices and EMI filter size. However, multilevel voltage generation will be affected due to the use of series connected capacitor in the converter structure if further control action is not taken into account. In this work, a finite control set model predictive control (FCS-MPC) algorithm is derived to track the desired current reference signal calculated via the proposed DC bus voltage controller. Moreover, a cost function is formulated to have balanced voltage across the series connected capacitors

II. System Model and Problem Statement

A. Analysis of the DC bus voltage// DC-bus Modeling

The presence of double grid frequency AC voltage ripple component on the top of the DC bus voltage is inherent in a single-phase grid-connected AC-DC power converter. Since a feedback loop is used to regulate the DC bus voltage, this ripple component modulates the generated output current of the converter when it is not filtered properly. Consequently, the converter current is distorted by this ripple component. This ripple voltage should be managed properly in order to avoid the adverse effect on the control performances such as slow dynamic performance during transients and increased harmonic content in the generated grid current. The DC value of the bus voltage and its double grid frequency ripple component can be calculated by the balance of the input power and the output power of the converter as presented next.

The grid voltage $v_g(t)$ and current $i_g(t)$ are assumed as

$$v_g(t) = V_m \sin(\omega t) \quad (1)$$

$$i_g(t) = I_m \sin(\omega t + \varphi) \quad (2)$$

where V_m and I_m are the peak values of the input voltage and current of the converter, respectively, ω is the angular frequency and φ is the phase angle difference between the grid voltage and current.

The instantaneous input power at the grid-side can be obtained as follows:

$$P(t) = v_g(t) i_g(t) = \frac{V_m I_m}{2}\cos\varphi - \frac{V_m I_m}{2}\cos(2\omega t + \varphi) \quad (3)$$

The ripple voltage Δv is small compared to the DC component of the bus voltage when a large capacitor is used in the DC bus. Thus, the input power $P(t)$ operates at approximately constant voltage. Ignoring the instantaneous power of the grid-side filter and lossless power stages, the output current is calculated as

$$i_0(t) \cong \frac{P(t)}{V_{dc}} = \frac{V_m I_m}{2V_{dc}}\cos\varphi - \frac{V_m I_m}{2V_{dc}}\cos(2\omega t + \varphi) \quad (4)$$

The AC part of $i_o(t)$ flows through the DC bus capacitor C and the DC part flows through the load resistor R_L.

The current through the bus capacitor can be expressed as

$$C\frac{dv_{dc}(t)}{dt} = i_o(t) - \frac{v_{dc}(t)}{R_L} \quad (5)$$

Multiplying both side of (5) by $v_o(t)$, we have

$$Cv_{dc}(t)\frac{dv_{dc}(t)}{dt} = P(t) - \frac{v_{dc}^2(t)}{R_L} \quad (6)$$

From (6), it can be concluded that, the power flowing into the bus capacitor C is the difference between the input power and the power consumed by the load resistor R_L.

The energy stored in the bus capacitor is given as

$$E(t)=\frac{1}{2}Cv_{dc}^2(t) \quad (7)$$

Thus, the power flowing through the bus capacitor C can be written as

$$\frac{dE(t)}{dt}=Cv_{dc}(t)\frac{dv_{dc}(t)}{dt} \quad (8)$$

Substituting (7) and (8) in (6), we have

$$\frac{dE(t)}{dt}=P(t)-\frac{2E(t)}{R_LC} \quad (9)$$

The solution of this first order linear differential equation is given as

$$E(t)=E(0)e^{-\frac{2t}{R_LC}}+e^{-\frac{2t}{R_LC}}\int_0^t e^{\frac{2\tau}{R_LC}}P(\tau)d\tau \quad (10)$$

Considering the grid voltage and current are in phase and substituting (10) in (7), the expression for the DC bus voltage can be expressed as follows:

$$v_{dc}(t)=\sqrt{\frac{2\left(E(0)e^{-\frac{2t}{R_LC}}+e^{-\frac{2t}{R_LC}}\left(\frac{CV_mR_LI_m\left(e^{\frac{2t}{R_LC}}-1\right)}{4}-\frac{I_mV_m\left(\frac{k}{2}\right)+\frac{C^2R_L^2\omega e^{\frac{2t}{R_LC}}\sin(2\omega t)}{2}}{2\left(C^2R_L^2\omega^2+1\right)}\right)\right)}{C}} \quad (11)$$

where $k=CR_L\left(e^{\frac{2t}{R_LC}}\cos(2\omega t)-1\right)$

A typical bus voltage waveform during turn-on is shown in Fig. 1, which is obtained from (11). It can be observed that, the bus voltage waveform consists of double grid frequency ripple, steady-state DC part and transient part. In a closed loop control system, the measured DC bus voltage should be filtered to estimate the DC part of the bus voltage in order to avoid harmonic distortion in the generated grid current by this ripple voltage. Moreover, the filtering method should provide a fast dynamic performance in calculating the DC part during transient with zero steady-state error.

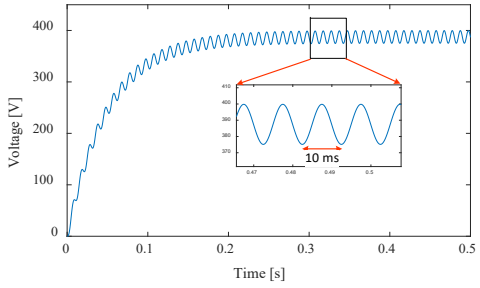

Fig. 1. DC bus voltage waveform during turn-on transient, as given by (11).

B. Dynamic System Model

The circuit structure of the single-phase five-level AC-DC converter under consideration is shown in Fig. 2. The adopted converter is connected into the power grid by means of a smoothing inductor L with an equivalent parasitic series resistor r. The DC bus consists of two series connected capacitors C_1 and C_2, and a resistive load R_L. The sudden variation in active power drawn by the converter is achieved by step change in the load resistance R_L. In this paper, the step variations of the load resistance R_L is considered as the unknown external disturbance to the converter.

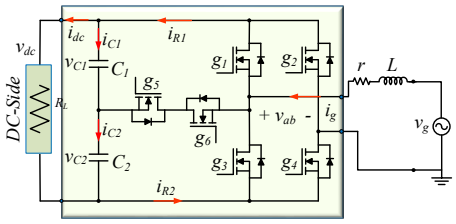

Fig. 2. Topology of the adopted single-phase five-level T-type converter.

The grid current $i_g(t)$ and the DC bus series connected capacitor voltages ($v_{c1}(t)$ and $v_{c2}(t)$) dynamics can be written via the following equations:

$$L\frac{di_g(t)}{dt}=v_g(t)-v_{ab}(t)-i_g(t)r \quad (12)$$

$$C_1\frac{dv_{C_1}(t)}{dt}=i_{R_1}(t)-i_{dc}(t)=i_{R_1}(t)-\frac{v_{dc}(t)}{R_L} \quad (13)$$

$$C_2\frac{dv_{C_2}(t)}{dt}=i_{R_2}(t)-i_{dc}(t)=i_{R_2}(t)-\frac{v_{dc}(t)}{R_L} \quad (14)$$

where v_{ab} is the converter voltage, i_{R1} and i_{R2} are the internal current of the converter and i_{dc} represents the DC bus load current.

The grid voltage (v_g), the converter voltage (v_{ab}), the inductor current (i_L) and the capacitor voltage (v_c) can be decomposed in their d and q components at the power grid frequency (ω_o). Thus, the system dynamics model can be expressed as follows:

$$\frac{di_d}{dt}=\frac{v_d}{L}-\frac{v_{abd}}{L}-\frac{r}{L}i_d+i_q\omega_o \quad (15)$$

$$\frac{di_q}{dt}=\frac{v_q}{L}-\frac{v_{abq}}{L}-\frac{r}{L}i_q-i_d\omega_o \quad (16)$$

$$\frac{C}{2}\frac{dv_c}{dt}=\frac{v_{abd}i_d+v_{abq}i_q}{2v_{dc}}-\frac{v_c}{R_L} \quad (17)$$

The system expressed in (15)-(17) is nonlinear system consists of three state variables i_d, i_q and v_{dc} and two control input v_{abd} and v_{abq}. The grid voltage is oriented to d-axis in synchronous reference frame. For simplification, the parasitic resistance r is neglected in this analysis. When the system is at the equilibrium point, (15)-(17) can be simplified as follows:

$$v_{abd}=v_d+i_q\omega_oL \quad (18)$$

$$v_{abq}=-i_d\omega_oL \quad (19)$$

$$\frac{v_{dc}^2}{R_L} = \frac{v_d i_d}{2} \quad (20)$$

From (18)-(20), it can be concluded that the DC bus voltage depends on the *d*-axis component (i_d) of the grid current. The *q*-axis component of the grid current (i_q) controls the power factor. For unity power factor operation, the *q*-axis component must be set to zero (i.e. $i_{q=0}$).

C. Modeling Uncertainties

Usually some assumptions are made during system modeling to simplify the controller design. These assumptions includes ignoring parasitic resistance of the smoothing inductor, switching losses, DC bus capacitance variation, and external disturbances due to the load variations. However, the simplified system model is not accurate, and hence, differ from the actual system behavior under different operating conditions. As a result, it affects the DC bus voltage controller. Thus, these system uncertainties should be considered to design a robust controller.

IV. Proposed Control Scheme

The proposed control approach is presented in this section. The control aims are to improve the steady-state and transient performances in realizing the regulated DC bus voltage under unexpected external disturbances, while achieving highest grid current quality. The controller design is based on the cascaded structure. The block diagram of the controller is illustrated in Fig. 3. It consists of an outer voltage controller and an inner current controller. The outer voltage regulation loop consists of a sliding mode controller (SMC), an extended state observer (ESO), and a DC bus voltage ripple estimator. The ESO is designed to estimate the disturbances to the converter, and an SMC is employed in parallel to the ESO to calculate the reference active power value for the inner current controller. In this paper, a filter-less method is used to estimate the DC value of the bus voltage. The proposed method provides fast transient performance in estimating the DC value of the bus voltage. Besides, the inner current tracking controller is designed based on a finite control set-model predictive control (FCS-MPC) algorithm. A five-level T-type converter is employed in this work. However, the generation of multilevel voltages will be affected if voltage unbalancing issue of this converter is not taken into account during controller design. To overcome this control problems, an FCS-MPC algorithm is derived to track the current references and maintain balanced voltages across the DC bus capacitors.

A. Proposed ripple voltage estimation method

In the proposed method, the DC bus ripple voltage is calculated based on the estimated quantities obtained from the phase locked loops (PLLs). The estimated ripple is then added with the measured DC bus voltage to get the DC component of the bus voltage. From (4), the current through the DC bus capacitor can be written as follows:

$$C\frac{dv_{dc}(t)}{dt} = -\frac{V_m I_m}{2V_{dc}}\cos(2\omega t + \varphi) \quad (21)$$

where $v_{dc}=V_{dc}+\Delta v$.

By integrating (21), the magnitude of the ripple voltage component can be approximated as:

$$\Delta v \cong \frac{V_m I_m}{4V_{dc}\omega C} \quad (22)$$

Therefore, the bus voltage and its ripple component can be approximated as follows:

$$v_{dc}(t) \approx V_{dc,avg} + \frac{V_m I_m}{4V_{dc,avg}\omega C}\sin(2\omega t + \varphi) \quad (23)$$

where $V_{dc,avg}$ is the average bus voltage.

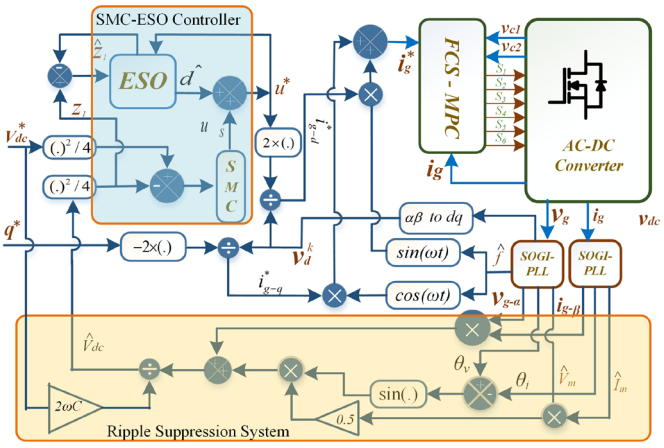

Fig. 3. Control system of the T-type AC-DC converter

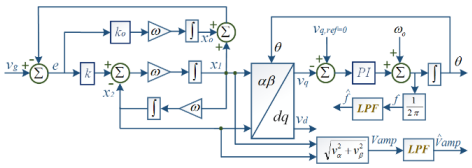

Fig. 4. Block diagram of the SOGI-PLL

According to (23), the value of $\sin(2\omega t+\phi)$, the magnitude of the grid voltage (V_m) and current (I_m) are required to estimate the ripple component of the DC bus voltage. In the proposed method, the α component of the grid voltage ($v_{g\text{-}\alpha}$) and the β component of the grid current ($i_{g\text{-}\beta}$) are multiplied to generate the twice of the grid frequency component.

By multiplying $v_{g\text{-}\alpha}(t)$ and $i_{g\text{-}\beta}(t)$, we have

$$V_m \sin(\omega t) \times I_m \cos(\omega t + \varphi) = \frac{V_m I_m}{2}\sin(2\omega t + \varphi) - \frac{V_m I_m}{2}\sin(\varphi) \quad (24)$$

Thus, the ripple component can be calculated by adding $(V_m.I_m/2)\sin\phi$ in (24) and multiplying by $1/(2V_{dc,avg}\omega C)$.

To evaluate the dynamic performance of the proposed approach in tracking the DC value of the bus voltage, two transients conditions are introduced in the DC-bus voltage. The obtained result is then compared with the existing approaches (low pass filter (LPF) and notch filter (NF)). As can be observed from Fig. 5 that the proposed method can estimate the DC value of the bus voltage faster than the existing methods.

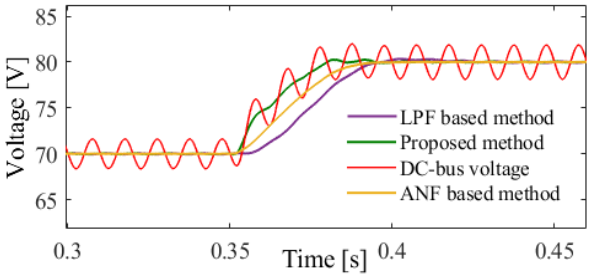

Fig. 5. The performance comparison of different DC bus ripple suppression methods.

B. Sliding mode control

According to (20), an inherent relationship is present between the DC bus voltage and the *d*-axis component of the grid current. In other words, the DC bus voltage depends on the active power value. In this paper, an SMC is designed to calculate the reference active power value.

1. Sliding surface

The sliding surface S is chosen as a linear combination of the two state variables, i.e.,

$$S = \alpha_1 x_1 + \alpha_2 x_2 \quad (25)$$

where α_1, and α_2 represent the sliding coefficients.

The controlled state variables are defined as the DC-link voltage error x_1, and the integral of the voltage errors x_2, which can be expressed as follows:

$$x_1 = V_{dc} - V_{dc,ref} \quad (26)$$

$$x_2 = \int (V_{dc} - V_{dc,ref})dt \quad (27)$$

Thus, the sliding surface is given as

$$S = \alpha_1 (V_{dc} - V_{dc,ref}) + \alpha_2 \int (V_{dc} - V_{dc,ref})dt$$

$$= \lambda (V_{dc} - V_{dc,ref}) + \int (V_{dc} - V_{dc,ref})dt = 0 \quad (28)$$

where λ is a positive constant, and defined as $\lambda = \alpha_1/\alpha_2$.

The parameter λ should be tuned in order to achieve optimized results in terms of settling time, steady state error, and overshoot.

The time derivative of (28) is given as

$$\dot{S} = \lambda \dot{V}_{dc} + (V_{dc} - V_{dc,ref}) \quad (29)$$

2. Control law

Rearranging (6), the expression for the input power in the DC bus is given as:

$$P_{dc}(t) = C v_{dc}(t) \frac{dv_{dc}(t)}{dt} + \frac{v_{dc}^2(t)}{R_L} \quad (30)$$

where the input power $P_{dc}(t)$ is the summation of the power flowing into the DC bus capacitor C (i.e. $Cv_{dc}(t)\frac{dv_{dc}(t)}{dt}$) and the power consumed by the load resistor R_L(i.e. $\frac{v_{dc}^2(t)}{R_L}$).

Considering lossless system, the input active power $P(t)$ of the converter is equal to the power $P_{dc}(t)$ in the DC bus. Thus, the control law is designed as:

$$u = \begin{cases} P^+(t), & S > 0 \\ P^-(t), & S < 0 \end{cases} \quad (31)$$

where $P^+(t)$ and $P^-(t)$ denotes the instantaneous input active power when the sliding variable reach different sides of the sliding surface S, respectively, and u denotes the control law.

Therefore, (20) can be rewritten as:

$$\frac{dv_{dc}(t)}{dt} = \frac{u}{CV_{dc}} - \frac{V_{dc}}{R_L C} + \delta \quad (32)$$

where δ presents the uncertainty disturbance in the DC bus voltage.

The bound of the external disturbance, ρ, is considered as $|\delta| \leq \rho < 1$, i.e. ρ is a positive constant. Thus, the control output is given as follows:

$$u_S = \left[\left(\frac{1}{R_L C} - \frac{1}{\lambda} \right) V_{dc} + \frac{1}{\lambda} V_{dc,ref} - \rho . sign(S_V) \right] C \quad (33)$$

C. Observer

In SMC, the control law is designed according to the system model. However, the dynamic performance is still affected with the SMC due to the system parameter uncertainties (e.g. external load variation). In order to overcome the limitations of the SMC, an ESO is designed which is applied in parallel to the SMC to calculate the reference active power to have improved dynamic performance during system uncertainties. In the proposed control scheme, an ESO is designed that estimates the load power and compensates the system disturbances such as the external load variation and plant dynamic variation. Thus, the control output of the proposed scheme is given as:

$$u = u_S + \hat{d} \quad (34)$$

where u_S is the SMC controller output obtained from (33), and $\hat{d}$ is the observed value obtained from the ESO.

From (17), the capacitor voltage dynamic can be written as

$$\frac{C}{2}\frac{dv_{dc}}{dt} = \frac{1}{v_{dc}}\left(p^* - p_t\right) \quad (35)$$

where $p^* = \frac{v_{abd} i_d + v_{abq} i_q}{2}$, $p_t = \frac{v_{dc}^2}{R_P} + \frac{v_{dc}^2}{R_L}$, and R_P is the equivalent resistance connected in parallel to the load resistor R_L, which represents the switching losses of the converter.

Defining a new variable $z_1 = \frac{(v_{dc})^2}{4}$, (35) can be rewritten as

$$C\frac{dz_1}{dt} = u - d(t) \quad (36)$$

where $d(t) = p_t = z_2$, $p^* = u$, and the disturbance z_2 is considered as an extended state.

The derivative of z_2 is denoted h, and can be expresses as:

$$\frac{dz_2}{dt} = h(t) \quad (37)$$

Thus, the linear ESO is designed as follows:

$$C\dot{\hat{z}}_1 = u - \hat{z}_2 + \beta_1\left(z_1 - \hat{z}_1\right) = u - \hat{z}_2 + \beta_1 e \quad (38)$$

$$\dot{\hat{z}}_2 = -\beta_2\left(z_1 - \hat{z}_1\right) = -\beta_2 e \quad (39)$$

where $e = z - \hat{z}$, β_1 and β_2 are the positive gain parameters of the ESO, $\hat{z}_1$ and $\hat{z}_2$ are the estimated values of z_1 and z_2, respectively.

The error dynamics are given by

$$C\dot{e} = -\beta_1 e - e_d \quad (40)$$

$$\dot{e}_d = h(t) + \beta_2 e \quad (41)$$

where $\dot{f}_t = h(t)$ denotes the load power change rate, and $e_d = d - \hat{d}$.

The systems expressed in (40) and (41) can be rewritten as:

$$\begin{bmatrix} \dot{e} \\ \dot{e}_d \end{bmatrix} = \begin{bmatrix} -\frac{\beta_1}{C} & -\frac{1}{C} \\ \beta_2 & 0 \end{bmatrix} \begin{bmatrix} e \\ e_d \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} h(t) \quad (42)$$

To make the error dynamics converge to the equilibrium point, the value of the gain parameters β_1 and β_2 are required to be chosen so that the polynomial of (42) i.e. $\lambda^2 + (\beta_1/C)\lambda + \beta_2/C$ is Hurwitz stable. Finally, the estimated disturbance to the converter $\hat{d}$ is added to the control output obtained from the SMC controller to obtain the reference active power value.

B. FCS-MPC

In order to predict the grid current and the DC bus capacitor voltages, (12)-(14) are converted into discrete time form which are obtained by employing the Euler's discretization technique, as given below:

$$i_g[k+1] = \left(1 - \frac{rT_s}{L}\right) i_g[k] + \left(v_g[k] - v_{ab}[k]\right)\frac{T_s}{L} \quad (43)$$

$$v_{C_1}[k+1] = v_{C_1}[k] + \frac{T_s}{C_1} i_{R_1}[k] - \frac{T_s}{C_1} i_{dc}[k] \quad (44)$$

$$v_{C_2}[k+1] = v_{C_2}[k] + \frac{T_s}{C_2} i_{R_2}[k] - \frac{T_s}{C_2} i_{dc}[k] \quad (45)$$

The output voltage of the converter (v_{ab}) is obtained from Table I for different switching states. The internal current of the converter (i_{R1} *and* i_{R2}) can be obtained from the grid current measurement (i_g) data for individual switching states, as shown in Table I. As a results, the unnecessary current measurements can be avoided, which reduces the cost and complexity of the system. In the proposed system, the current reference of the converter is calculated as follows [38]:

$$i_g = \frac{2p}{v_{gd}}\sin(\omega t) - \frac{2q}{v_{gd}}\cos(\omega t) \quad (46)$$

where the value of ωt is calculated from the PLL as shown in Fig. 4, p is the control output obtained from the SMC-ESO controller, q is the reference reactive power value.

In the proposed FCS-MPC control scheme, the following cost function is formulated to realize the desired grid current and balanced voltages across the DC bus capacitors.

$$g_{c.} = \left(i_g^*[k+1] - i_g[k+1]\right)^2 + \frac{p}{V_{avg}^2}\left(v_{C_1}[k+1] - v_{C_2}[k+1]\right)^2 \quad (47)$$

where the value of p is obtained from the SMC-ESO controller.

TABLE I
POSSIBLE STATES OF THE CONVERTER

	g_1	g_2	g_3	g_4	g_5	g_6	i_{R_1}	i_{R_2}	v_{ab}
$v_g>0$	0	0	0	0	0	0	i_g	i_g	$+(v_{C_1}+v_{C_2})$
	0	0	0	0	1	0	0	i_g	v_{C_2}
	0	0	1	0	0	0	0	0	0
$v_g<0$	0	0	0	0	0	0	i_g	i_g	$-(v_{C_1}+v_{C_2})$
	0	0	0	0	0	1	i_g	0	v_{C_1}
	0	0	0	1	0	0	0	0	0

II. SIMULATION AND EXPERIMENTAL RESULTS

To verify the proposed control scheme, the adopted converter with the specifications listed in Table II is tested with the grid voltage magnitude of 120 V. The DC-bus voltage reference is set to 150 V. The parameters of the observer, filter, and SMC are listed in Table II. The proposed control algorithms are implemented in a TMS320F28379D floating point DSP board. The sampling frequency is set to 50 kHz. The input current, grid voltage, output current, DC-bus voltage and load current are sampled using the internal A/D of the DSP with12 bits. The photograph of the converter prototype used for the experiment is shown in Fig. 6. To demonstrate the feasibility of the proposed control approach, two scenarios are implemented and compared with the existing approaches. In both cases, the inner current control loop remains the same to provide a base for comparison. The first test scenario consists of a step variation in the reference DC-bus voltage from 150 V to 180V. In this test case, the outer voltage and inner current control loops remain the same, and a 150 Ω load resistance is connected at the DC-bus. Fig. 7 shows the experimental results associated with the ANF and proposed DC-bus ripple estimation methods in realizing the reference voltages during this step variation. It can be seen that the settling time with the proposed method is less than the ANF based method. The proposed method requires ~50 ms with no overshoot is observed, whereas the ANF based controller requires 90 ms. The second test scenario focuses on external disturbances rejection capability. For this purpose, a step variation in the active power drawn by the converter is considered as the external disturbance, which is realized by 40% step changes in DC-bus load. In this case, the proposed ripple estimation method is used. Fig. 8 shows the experimental results associated with the SMC-ESO and traditional PI-based methods for the step-up load changes. Form the test results, it is clear that the SMC-ESO requires ~50 ms to settle at the reference voltage level and the DC-bus voltage drop is about 5 V. The same experiment is conducted during this load transient with the PI-based method, which requires 150 ms to settle at the reference voltage, and the bus voltage drop is 20 V. The similar tests were conducted for step-down load changes. The experimental waveforms are presented in Fig.

9(a) and (b) with the SMC-ESO and traditional PI-based methods, respectively. Form the results, it is clear that the SMC-ESO requires less time to settle at the reference voltage level compared with the PI-based method. The proposed method requires 55 ms, whereas, the PI method requires 145 ms. Moreover, the observed DC-bus voltage overshoot were ~10 V with the proposed method, whereas the PI based method showed ~20 V voltage overshoot.

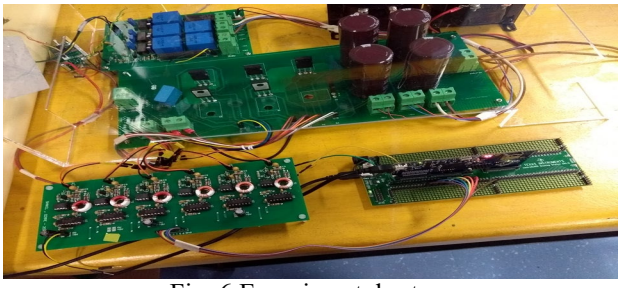

Fig. 6 Experimental setup.

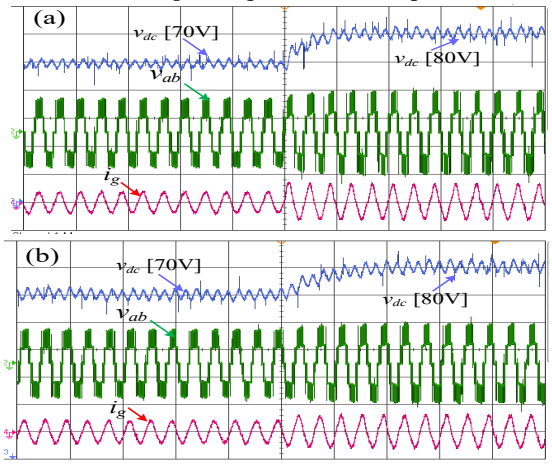

Fig. 7. Experimental results during transients, (a) Proposed DC-bus voltage estimation method, (b) ANF based DC-bus voltage estimation method.

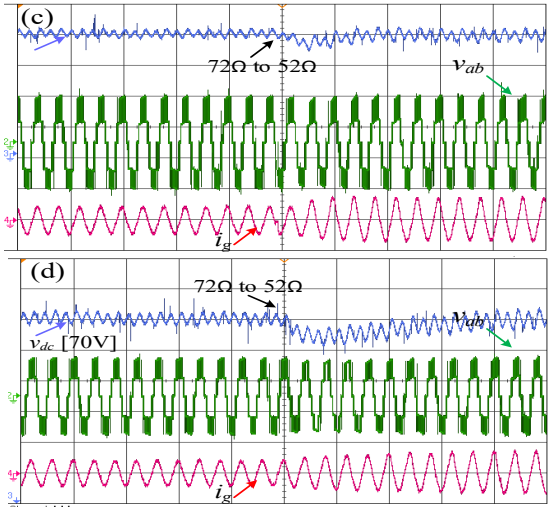

Fig.8. Experimental results during step-up load condition, (a) SMC-ESO, (b) PI-based approach.

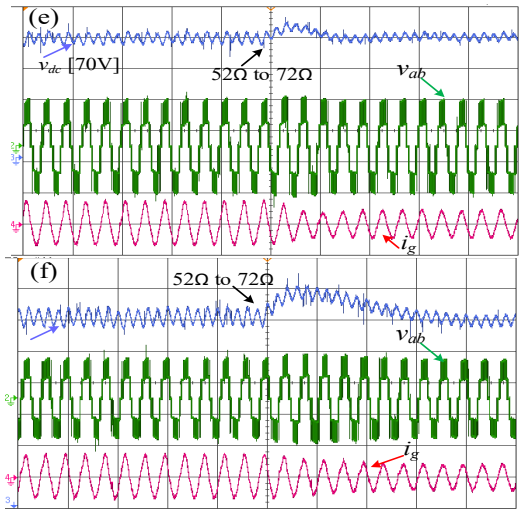

Fig.9. Experimental results during step-down load condition, (a) SMC-ESO, (b) PI-based approach.

TABLE II
SPECIFICATIONS OF THE EXPERIMENTAL SETUP

Parameters	Value	Unit
Sampling frequency	50	kHz
Maximum switching frequency	25	kHz
dc-link capacitor	2.0	mF
Filter capacitor	1.0	µF
Filter inductor	3.0	mH
Input ac voltage (V_m)	70	V
Grid Frequency	50	Hz
Main control chip	TMS320F28379D	
Voltage sensor	LV 25-P/SP5	
Current sensor	LA 25-NP	
Switch	SCT3022ALGC11	
Diode	HFA15PB60	

III. CONCLUSION

In single-phase AC-DC converters, the main challenge associated with the designing of DC bus voltage controller is the trade-off between the generated grid current quality and the DC bus voltage dynamic performance. This trade-off becomes more difficult when the DC bus ripple voltage is high due to the use of small bus capacitor. This paper provided an expression for the DC bus ripple component and introduced a filter-less method to remove this component from the measured voltage completely. Consequently, it enables in reducing the grid current distortion and presents fast dynamic performance in realizing regulated DC bus voltage during the transient. Moreover, to improve the dynamic performance during external disturbances, a robust control approach based on the SMC incorporated with an ESO was proposed as the DC-bus voltage controller. The SMC-ESO control approach presented superior dynamic performance under external disturbances compared to the traditional controller. Moreover, an FCS-MPC algorithm is derived as the inner current controller that ensured balanced voltages across the DC bus capacitors and generated five distinct voltages in the grid-side.

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