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A Family of Single-Phase Single-Stage Boost Inverters

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***Abstract*—H-bridge inverter is a common topology used for single-phase applications. Due to its limited voltage gain, a two-stage power conversion with a front-end dc-dc converter is usually adopted to accommodate the low dc source voltage. Recently, single-stage boost inverters are gaining significant interest due to their higher power efficiency and compactness. This paper presents a family of boost inverters with continuous dc source current. By the incorporation of merely a power switch and a boost inductor to the first leg of H-bridge, voltage-boosting and 3-level generation can be simultaneously achieved within a single-stage operation. All potential topologies using the same number of components are derived. An extension to generate five voltage levels with voltage gain enhancement is also proposed. The operation of the proposed boost inverters is thoroughly analyzed. Simulation and experimental results are presented for verification.**

***Index Terms*— Boost inverters, H-bridge, Multilevel inverters, Single-stage.**

I. Introduction

An H-bridge which is also referred to as the full-bridge inverter is a classical topology that has been widely used in single-phase applications. With merely four power switches, it is capable to generate three ac voltage levels while ensuring bidirectional power conversion between the dc and ac sides at the same time. An H-bridge is a buck-type inverter with its dc to ac voltage gain controllable up to unity by regulating the modulation index of the sinusoidal pulse-width modulation (PWM). For applications that require voltage-boosting such as grid-connected renewable energy or energy storage systems, a front-end dc-dc boost converter is usually mandatory to provide a sufficient dc-link voltage for the H-bridge inverter [1], [2]. A main downside of this two-stage power conversion structure is its low efficiency due to the high loss dissipation across the boost converter. The efficiency can be improved by making use of two paralleled front-end boost converters so that the interleaving operation between the two converters [3], [4] provides equal power sharing to reduce the losses in the dc-dc stage.

Instead of improving the two-stage topologies, significant research has been devoted to establishing single-stage inverters that inherit high voltage-boosting capability. In [5], [6], the positive terminal of a H-bridge is disconnected to constitute two boost converters with separate dc-links. In order to prevent from dc offsets in the ac output, both converters are controlled with a sinusoidal varying duty-cycle that not only generates a differential ac voltage, but also enables their dc voltages to counteract each other at the same time. It is important to note that the generation of accurate differential ac voltage between the two dc-links is highly complicated, rendering the design of control scheme for this topology challenging [7]. Moreover, the circulating current is another major concern that needs to be addressed.

Impedance source inverters are another type of single-stage topologies that also gain popularity in recent years [8]. The earliest impedance source inverter introduced in 2003 is referred to as a Z-source inverter [9]. As its name implies, a Z-shaped impedance network is integrated into the dc-link of the conventional voltage source inverter. Note that a shoot-through state is introduced when both switches in the same phase leg are ON, thereby allowing the impedance network to operate with a boosted dc-link voltage. Despite the drawbacks such as a discontinuous input current and the need of several passive components for the impedance network, this pioneering contribution has inspired substantial related research works. A comprehensive review concerning the developments of impedance source inverters can be found in [10]–[12].

Recently, a distinctive family named split-source inverter (SSI) that features simplicity, high compactness, continuous input dc current, and continuous dc-link voltage has been explored [13]–[17]. It requires the incorporation of only one

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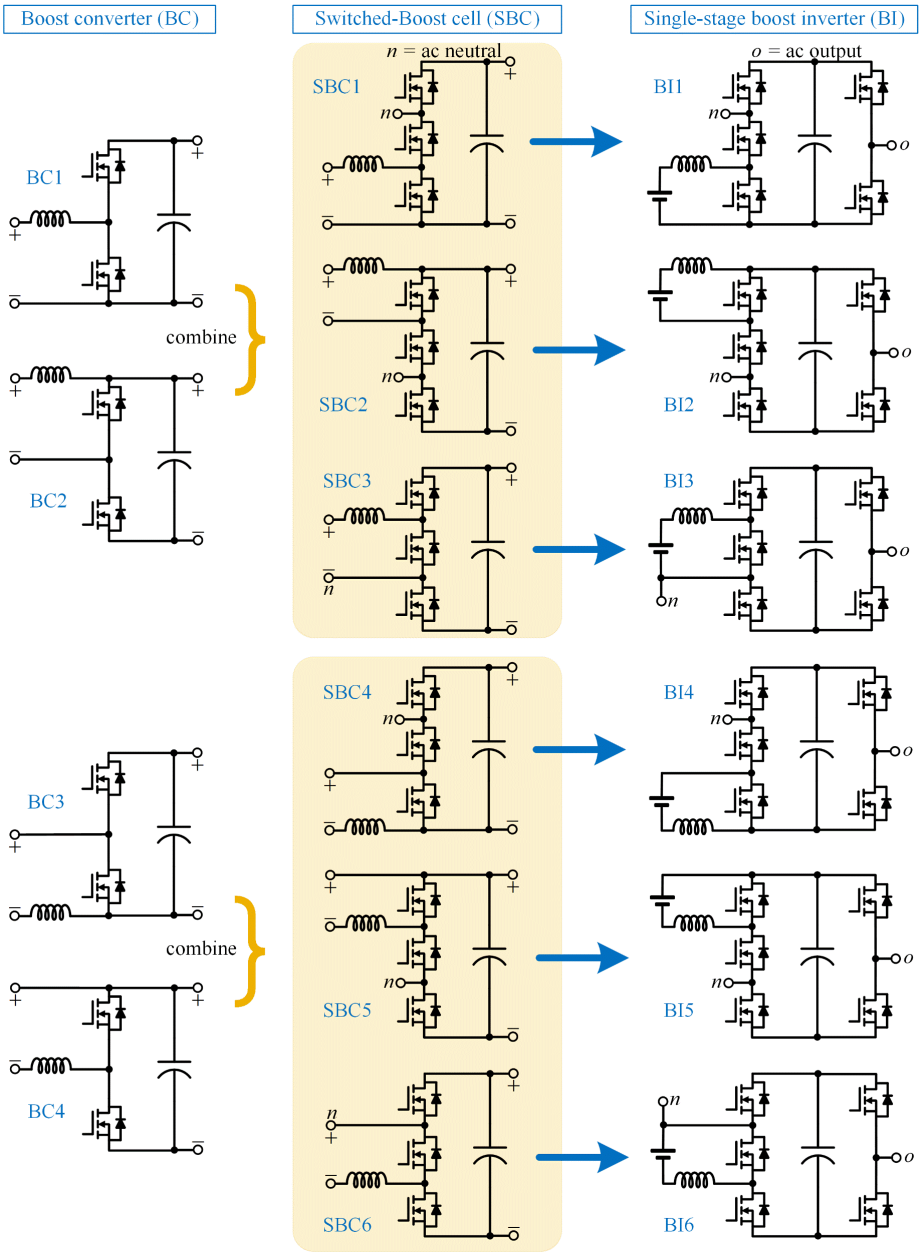

Fig. 1. Derivation of single-phase single-stage 3-level boost inverters.

inductor, one capacitor, and two diodes into the H-bridge inverter. The single-stage configuration which encompasses a boost converter, and a H-bridge inverter permits concurrent accomplishment of dc-link voltage-boosting and ac voltage generation. The first topology introduced in [13] is later denoted as SSI in [14] to better reflect the circuit structure. A more compact design can be attained by relocating the dc source with the utilization of a commercial device that comprises two common-cathode diodes [18]. All the earlier SSIs, however, exhibit common shortcomings such as high-frequency commutations of diodes, aggravated harmonics which are induced by the variable charging duty-cycle of the boost inductor, and incapability of bidirectional power conversion.

A latter study improves the SSI by replacing the two diodes with two power MOSFETs [19]. With both the power MOSFETs operate in synchronous rectification mode at the line frequency, the modified SSI mitigates the high-frequency commutation of diodes and achieves bidirectional power flow. Besides, the presented hybrid quasi-sinusoidal and constant pulse-width modulation (PWM) scheme is able to provide a constant charging duty-cycle for the boost inductor. It is also worth noting that the operations of the two H-bridge legs are effectively decoupled. One leg is responsible for inductor charging and dc-link voltage control while the other leg is responsible for ac voltage generation according to the sinusoidal PWM.

A single-phase SSI topology that allows bidirectional power flow with reduced component count is presented in [20]. While preserving all the inherent merits of earlier SSIs, this so-called simplified SSI (S^3I) exhibits the highest compactness in the SSI family. Voltage boost function and three voltage levels generation are attained within a single-stage operation by

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merely the incorporation of an additional power switch into the first leg of a H-bridge. However, this topology suffers from high-frequency common-mode voltage that is not feasible for applications such as photovoltaic (PV) system.

By using the same number of components, all potential topologies for single-stage boost inverters are derived in this paper. Some of the topologies in this boost inverter (BI) family have been presented in the literature while the remaining are novel. An extension from 3 to 5-level generation with voltage gain enhancement is also proposed. The remainder of this article is organized as follows. In Section II, the BI family is introduced. Section III presents an extension to generate 5 voltage level and enhance voltage gain. Section IV compares the proposed topology with the state-of-the-art 5-level inverters. Simulation and experimental results are discussed in Section V. Finally, Section VI concludes the article.

II. Three-Level Boost Inverters

Fig. 1 depicts the derivation of the boost inverter (BI) family. Four basic topologies of dc-dc boost converter are considered, and they are termed as BC1 to BC4. By combining BCs with similar circuit structure for their dc source and boost inductor, a total of 6 switched-boost cells (SBC1 to SBC6) are obtained. In each SBC, a power switch is inserted into the half-bridge that introduces a new switching state for controlling the voltage of ac neutral. Six topologies of boost inverter (BI1 to BI6) are established by adding a half-bridge to each respective SBC. The first (BI1) and third (BI3) topology depicted in Fig. 1 has been introduced in [20] and [21], respectively, while the remaining BIs are novel that have not been presented in the literature.

All BIs depicted in Fig. 1 can generate three voltage levels and boosting voltage gain simultaneously within a single-stage operation. They have four useful switching states as shown in Fig. 2. The boost inductor can be charged by clamping it across the dc source during all voltage levels. To boost the voltage across capacitor, the boost inductor is discharged in series with the dc source during 0-level.

To enable a single-stage dc-ac power conversion, PWM scheme depicted in Fig. 3 consists of two reference signals and a triangular carrier. A constant duty-cycle D for charging the boost inductor is obtained by comparing the constant reference V_{const} with the triangular carrier. By considering the volt-second balance of the boost inductor, the voltage across capacitor V_C is

$$V_C = \frac{1}{1-D} V_{dc} . \tag{1}$$

Simultaneously, a sinewave reference is used to control the ac output with the amplitude of fundamental voltage is

$$\hat{V}_{on,1} = MV_C = \frac{M}{1-D} V_{dc} \tag{2}$$

where $M = \hat{V}_{\text{sine}} / \hat{V}_{\text{tri}}$ is the modulation index. In this PWM scheme, the modulation index and constant duty-cycle are coupled for achieving voltage boosting and ac voltage generation simultaneously in a single-stage operation. The minimum value for constant reference is given by the peak of sinewave reference. Therefore, the minimum constant duty-cycle is equal to the inverter modulation index, $D_{\min} = M$.

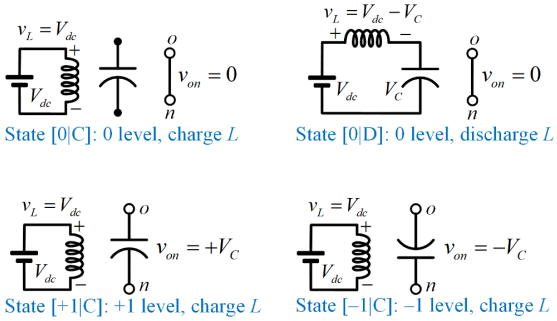

Fig. 2. Generalized switching states of 3-level boost inverters.

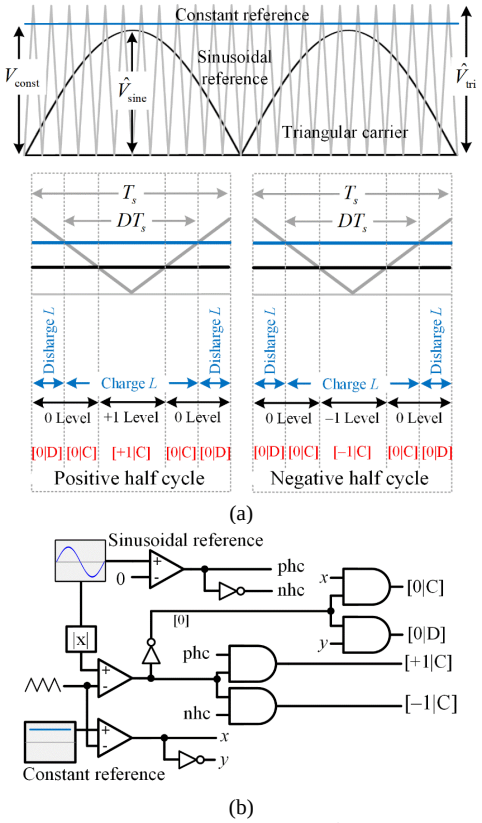

Fig. 3. Pulse-width modulation (PWM) scheme of 3-level boost inverters: (a) key waveforms, (b) PWM unit.

The ripple of capacitor voltage and ripple of inductor current consists of double-line-frequency and high-frequency components. A comprehensive ripple analysis can be referred to [20]. Considering sinusoidal ac current, the capacitor voltage ripple ΔV_C and inductor current ripple ΔI_L can be respectively written as

$$\Delta V_C = \frac{M\hat{I}_{o,1}}{4\pi f_o C} + \frac{D(1-D)I_L}{Cf_s} \tag{3}$$

$$\Delta I_L = \frac{M\hat{I}_{o,1}(1-D)}{16\pi^2 f_o^2 LC} + \frac{DV_{dc}}{Lf_s} \tag{4}$$

where $\hat{I}_{o,1}$ is the amplitude of fundamental ac current, I_L is the average dc source or inductor current, f_o is the fundamental ac frequency, f_s is the frequency of the triangular carrier, L is inductance and C is capacitance.

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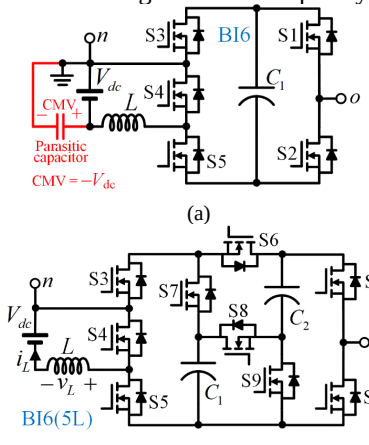
III. Extended 5-Level Topology with Voltage Gain Enhancement

All BIs depicted in Fig. 1 have the same component count and operating principle summarized in Fig. 2. The location of ac neutral point that determines the inverter common-mode voltage (CMV) is their main distinctive feature. The ac neutral point of BI1, BI2, BI4 and BI5 is separated from the dc source by a switch. Due to the switching of this switch, high-frequency CMV is introduced.

Among the novel 3-level BIs in Fig. 1, BI6 has an attractive structure with its ac neutral is directly connected to the positive terminal of the dc source. This implies that the neutral point voltage with respect to any dc source terminals is constant without high-frequency CMV. As shown in Fig. 4(a), the CMV across the parasitic capacitor is $-V_{dc}$, which is constant. It prevents the risk of leakage current that is very feasible for applications such as photovoltaic (PV) system. Therefore, this topology is considered for further extension.

To increase the number of voltage levels from three to five, a capacitor C_2 and four power switches S6–S9 are added, as shown in Fig. 4(b). Fig. 5 shows the switching states of the extended 5-level topology (BI6(5L)). Both capacitors C_1 and C_2 are charged in parallel. Therefore, their voltage is equal. Maximum voltage levels (+2 and –2) can be generated by discharging the capacitors in series. The magnitude of these maximum voltage levels is two times of the capacitor voltage. This implies that the voltage gain of BI6(5L) is double compared to BI6 for the same D and M.

As shown in Fig. 5, the boost inductor can be charged during any voltage levels. To discharge the boost inductor during 0, +1 or –1 level that ensures a constant duty-cycle D for voltage-boosting while simultaneously generating 5-level ac voltage, a phase-shifted PWM scheme depicted in Fig. 6 is proposed. This PWM scheme not only enables a 5-level generation that reduces overall total harmonic distortion (THD) of ac output voltage, but it also improves the harmonic spectrum. Compared to BI6, the dominant harmonics of ac voltage generated by BI6(5L) is extended to twice the triangular carrier frequency. This is beneficial for reducing the power filter requirement, i.e., smaller power filter for higher cutoff frequency.



(a)

(b)

Fig. 4. Proposed boost inverters: (a) 3-level boost inverter (BI6) without high-frequency common-mode voltage, (b) extension of BI6 with 5-level generation and voltage gain enhancement.

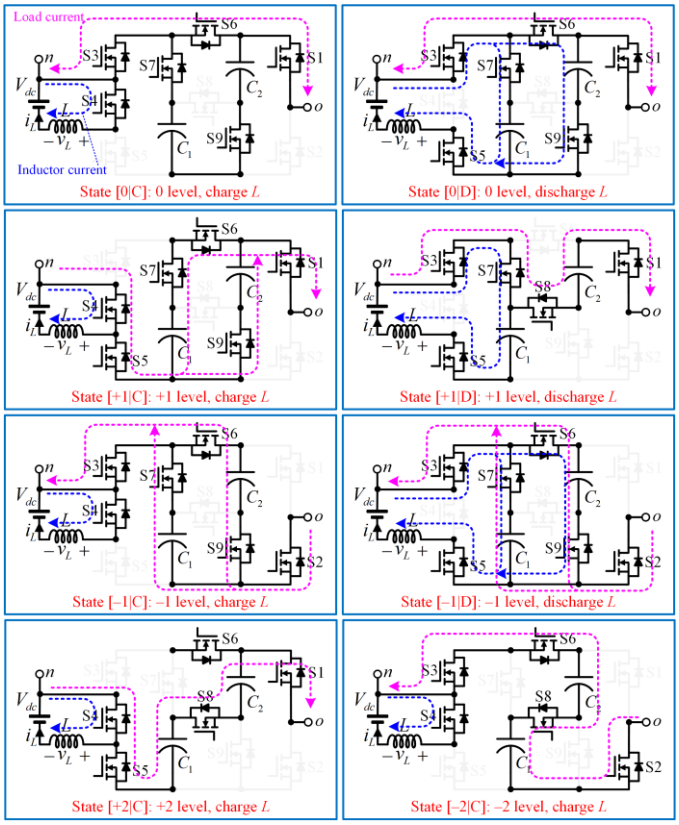
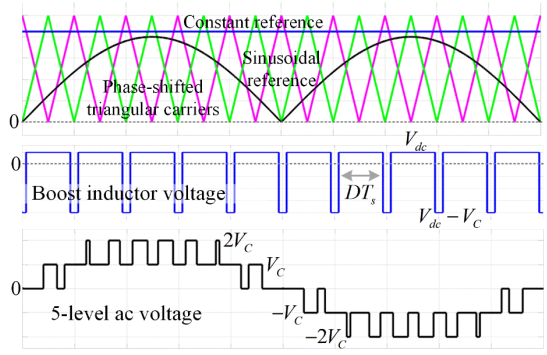
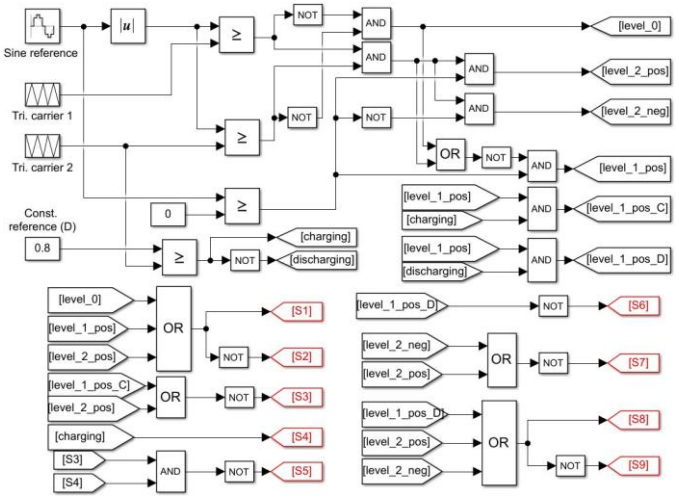


Fig. 5. Switching states of extended 5-level boost inverter (BI6(5L)).



(a)



(b)

Fig. 6. Phase-shifted PWM scheme of extended 5-level boost inverter (BI(5L)): (a) key waveforms, (b) implementation of PWM scheme.

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To design BI6(5L), $D_{\min} = M$ is considered. Modulation index M for the required voltage gain G is

$$M = \frac{G}{G+2}. \tag{5}$$

Two capacitors with the same value are considered:

$$C_1 = C_2 = C = \frac{1}{\Delta V_C}\left(\frac{M\hat{I}_{o,1}}{4\pi f_o} + \frac{D(1-D)I_L}{f_s}\right). \tag{6}$$

Finally, the value of inductor can be calculated as

$$L = \frac{1}{\Delta I_L}\left(\frac{M\hat{I}_{o,1}(1-D)}{16\pi^2 f_o^2 C} + \frac{DV_{dc}}{f_s}\right). \tag{7}$$

IV. Comparison with Existing 5-Level Boost Inverters

Table I summarizes the comparison of the proposed BI6(5L) with the state-of-the-art 5-level inverters without high-frequency CMV. The topologies presented in [22]–[25] uses lesser number of power switches. However, their major drawbacks are limited voltage gain and discontinuous dc source current. A 5-level inverter presented in [26] improved the voltage gain significantly, however, with a tradeoff of high switch count. In addition, the issue of discontinuous dc source current is not fully resolved. The capacitors of this topology are connected in series. They are individually charged by the boost inductor and requires voltage balancing control that unfortunately causes significant distortion to the inductor current due to limited redundant states. Inductor or dc source current with discontinuous and highly distorted waveform increases the overall RMS value. Referring to the superposition theorem: $I_{rms}^2 = I_{dc}^2 + I_{1,rms}^2 + I_{2,rms}^2 + \ldots$ where $I_{\rm rms}$ is the overall RMS current, $I_{\rm dc}$ is the average current, $I_{1,\rm rms}$ is the RMS current of the fundamental harmonic, etc, the overall RMS current would be significantly higher than the average current that increases power loss. This results in lower efficiency because the average power delivered by the inverter is contributed by the average current only. In addition, discontinuous dc source current is not feasible for applications such as PV system. The proposed BI6(5L) provides the best performance that achieved high voltage gain and continuous dc source current while saving one switch count compared to [26]. In addition, the number of conducting switches for inductor current in the proposed topology is also lesser than [26].

TABLE I
COMPARISON BETWEEN THE PROPOSED BI6(5L) AND THE EXISTING 5-LEVEL INVERTERS WITHOUT HIGH-FREQUENCY CMV

Topology	N_S	N_D	N_C	N_L	G	CIC
[22]	6	1	2	0	M	No
[23]	6	2	2	0	$2M$	No
[24]	7	2	2	0	$2M$	No
[25]	6	2	2	0	$2M$	No
[26]	10	0	2	1	$2M/(1-D)$	Partial
BI6(5L)	**9**	**0**	**2**	**1**	$\mathbf{2M/(1-D)}$	**Yes**

N_S = number of switches, N_D = number of diodes, N_C = number of capacitors, N_L = number of inductors, G = voltage gain, M = modulation index, D = duty-cycle, CIC = continuous input current.

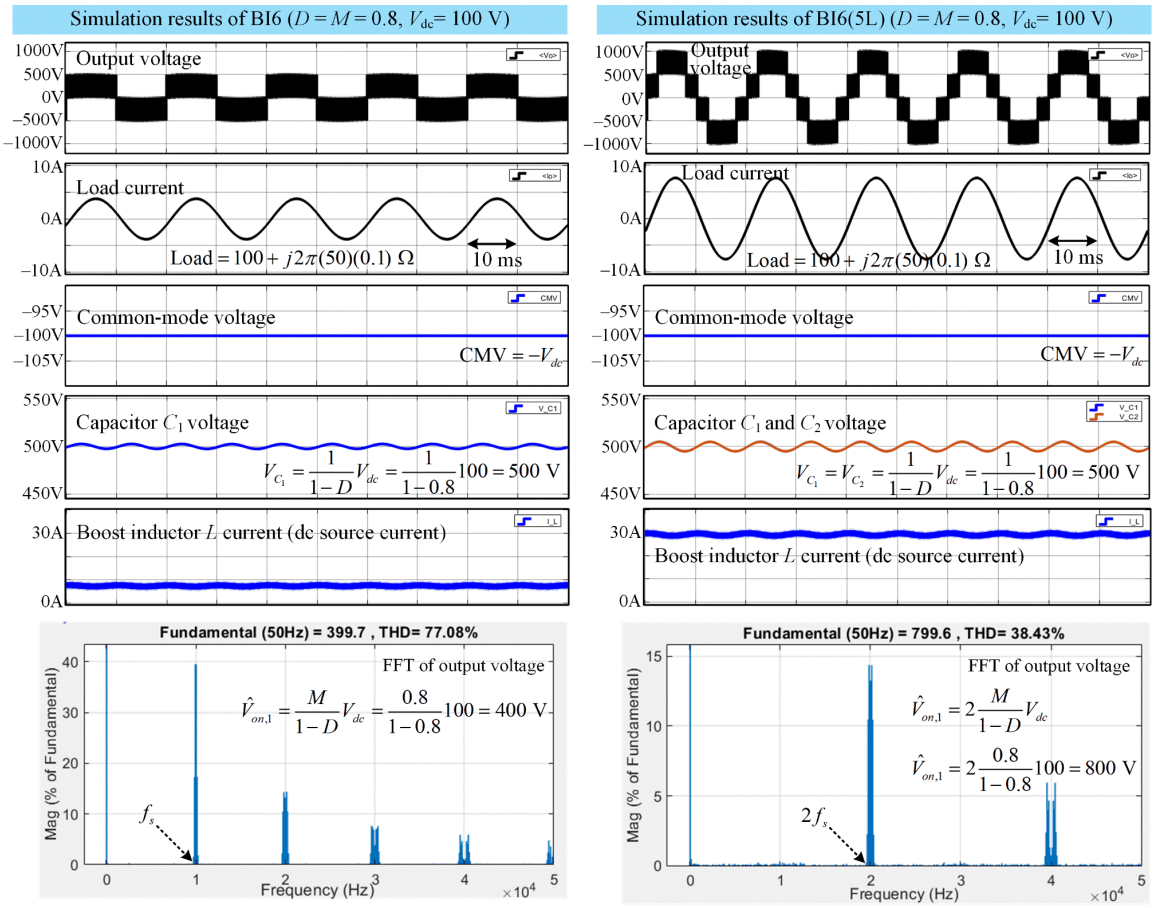

Fig. 7. Simulation results of the proposed BI6 and BI6(5L).

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V. Simulation and Experimental Results

Simulations were conducted using Matlab Simulink to verify the operation of the proposed BI6 and BI(5L). To compare the performance of both topologies, the same parameters are considered: V_{dc} = 100 V, $D = M$ = 0.8, $C_1 = C_2$ = 1000 µF, L = 1 mH, f_s = 10 kHz, f_o = 50 Hz, load resistance = 100 Ω, and load inductance = 100 mH.

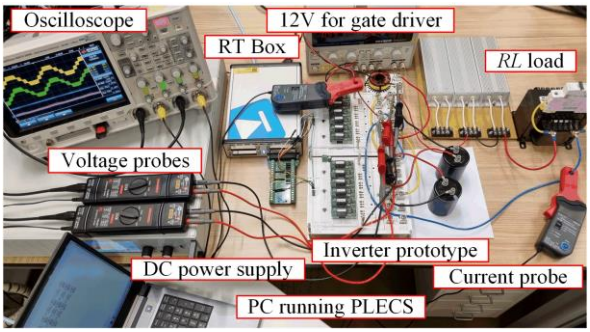
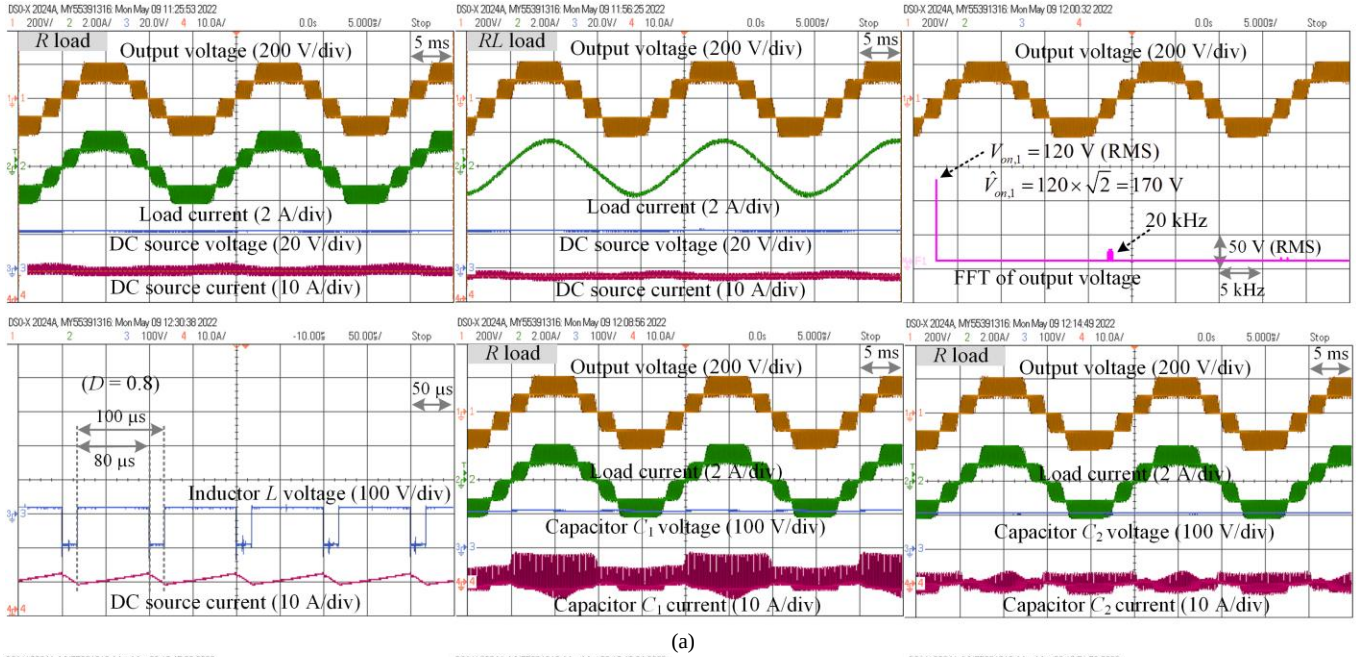
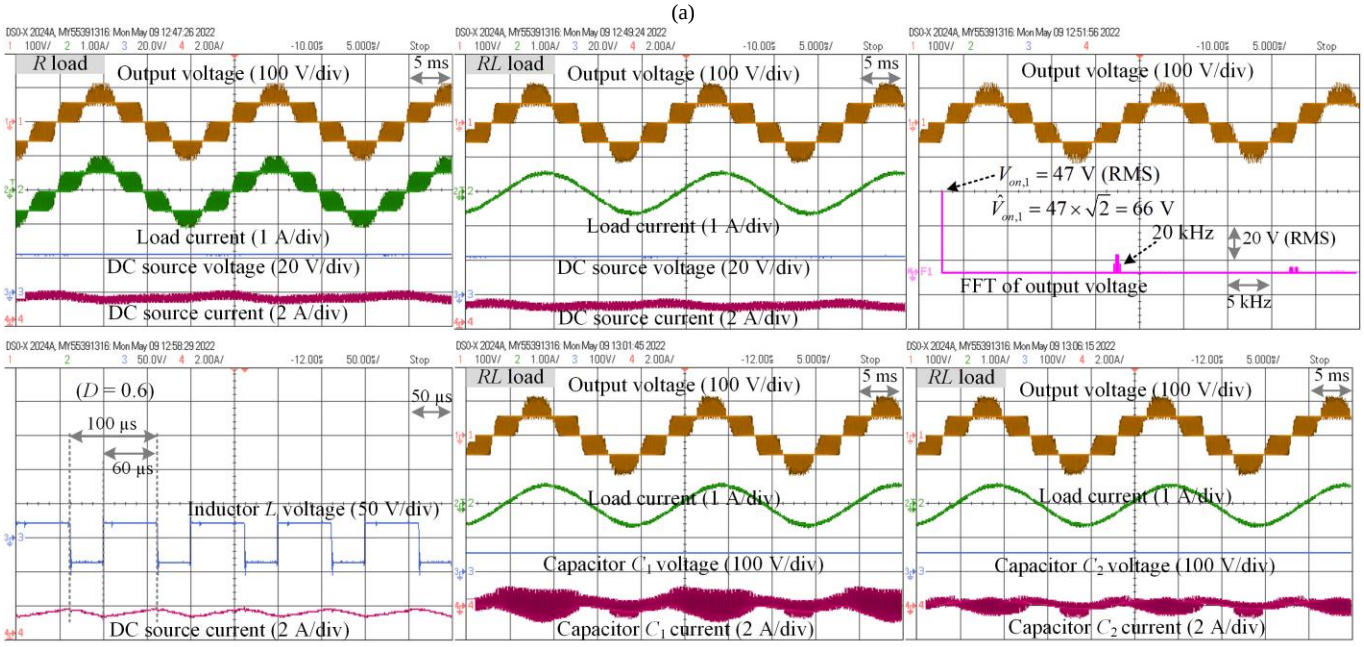


Fig. 8. Experimental setup.



(a)



(b)

Fig. 9. Measured steady-state response at: (a) $D = M$ = 0.8, and (b) $D = M$ = 0.6.

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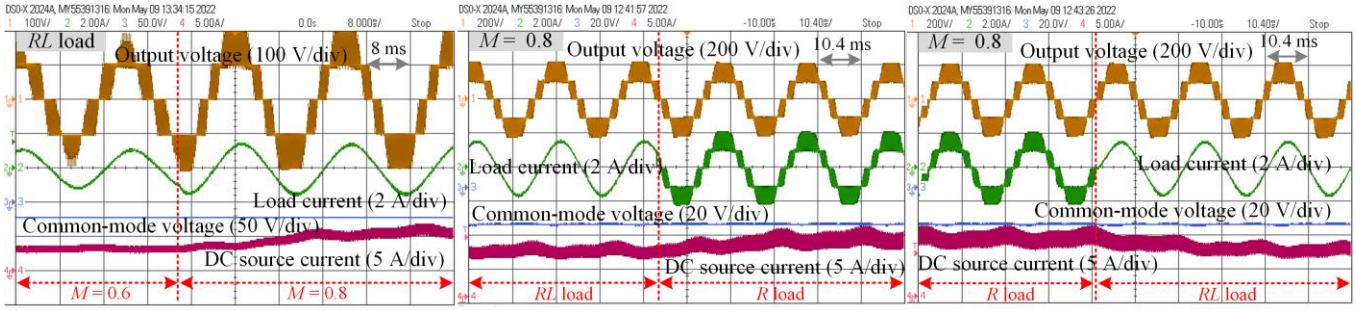

Fig. 10. Measured transient response.

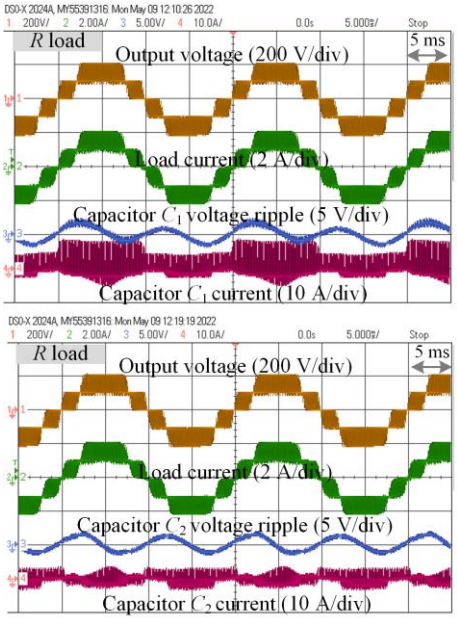

Fig. 11. Measured capacitors' voltage ripple of the proposed BI6(5L) at $M = D = 0.8$.

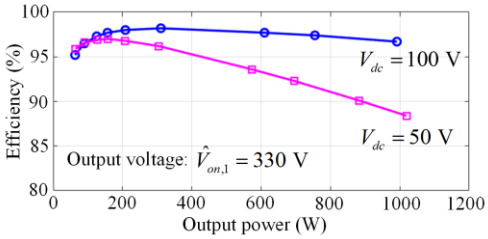

Fig. 12. Efficiency of the proposed BI6(5L).

TABLE II
SIMULATION AND EXPERIMENTAL PARAMETERS OF BI6(5L)

Parameter	Simulation	Experiment
Boost inductor, L	1 mH	1 mH
Capacitor, $C_1 = C_2 = C$	1000 µF	1000 µF
Carrier frequency, f_s	10 kHz	10 kHz
Output frequency, f_o	50 Hz	50 Hz
Input voltage, V_{dc}	100 V	22 V
Output voltage, $\hat{V}_{on,1}$ (at $D = M = 0.8$)	800 V	176 V
Output power, P_o	2914 W	200 W

By charging the boost inductor with a constant duty-cycle of 0.8, the voltage of each capacitor in both topologies is boosted to 500 V. Three symmetrical voltage levels are generated by BI6 between 500 V and –500 V with the amplitude of fundamental component is 400 V. The BI6(5L) has clear improvement that generates two additional voltage levels, i.e., +1000 V and –1000 V. With the same modulation index of 0.8, the amplitude of fundamental ac voltage generated by BI6(5L) is 800 V, double compared to BI6. Consequently, the output power of BI6(5L) in Fig. 7 is 2914 W which is 4 times higher than 730 W of BI6. In addition, the fast Fourier transform (FFT) of ac voltage shows that the dominant harmonics of BI6(5L) are concentrated at 20 kHz that is twice compared to 10 kHz of BI6. In addition, the harmonics magnitude and overall THD of BI6(5L) are significantly lower that can improve the load current quality. These significant improvements are achieved while retaining the advantages of BI6 such as constant CMV without high-frequency component and continuous dc source current.

For further verification, a low power (200 W) proof-of-concept experimental prototype for BI6(5L) was implemented using Silicon Carbide MOSFETs (C3M0120090D) that have on-state resistance of 120 mΩ. The experimental prototype depicted in Fig. 8 was implemented to verify the operation of the proposed topology. The same parameters in simulation study were used except V_{dc} was reduced to 22 V to ensure the dc source current is within 10-A current limit of the power supply. Table II summarizes the simulation and experimental parameters of BI6(5L). Phase-shifted PWM scheme presented in Fig. 6 was implemented in PLECS and switching signals were generated in real-time using the RT Box controller.

Fig. 9(a) shows the measured steady-state response at $D = M = 0.8$ under both R and RL load. It is clearly seen that the dc source or boost inductor L current is continuous. Zoomed-in to this current shows the charging and discharging duration of the inductor is 80 µs and 20 µs, respectively, that confirms the operating duty-cycle (0.8) and frequency (10 kHz). The average voltage across both C_1 and C_2 are boosted to 110 V. By connecting these capacitors in series during [+2|C] state, the maximum voltage level generated by the BI6(5L) at $D = 0.8$ is 220 V which is 10 times higher than the dc source voltage. Five symmetrical voltage levels are observed in the ac output voltage between 220 V and –220 V. The fundamental component of the ac voltage is 120 V rms, as reflected by the spectrum captured from the fast Fourier transform (FFT) analysis. This observation matches well with the theoretical finding, and it is only slightly less than the calculated value of 124 V rms. The

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measured voltage gain is 170/22 = 7.7 which is very close to the theoretical value of 8. The dominant harmonics of ac voltage are concentrated at 20 kHz that shows a good agreement with the theoretical analysis and simulation results.

Experiments were repeated for $D = M = 0.6$ with the steady-state responses are summarized in Fig. 9(b). The inductor L is charged by the dc source for 60 µs and discharging to the capacitors for the remaining period in each switching cycle. Continuous inductor current is ensured while boosting the dc source voltage from 22 V to 55 V across each capacitor. The ac output voltage consists of five symmetrical voltage levels between 110 V and –110 V. The measured peak of fundamental ac voltage is 66 V that verified the theoretical value: $\hat{V}_{on,1} = 2MV_{dc}/(1–D) = 2(0.6)(22)/(1–0.6) = 66$ V.

Fig. 10 shows the transient response of the BI6(5L) prototype. The increase in modulation index increases the magnitude of load current due to higher magnitude ac voltage. The load current changes instantly when the load is switched from R to RL load and vice-versa. The 5-level waveform of the output voltage is maintained without any deterioration during the load transient. The common-mode voltage between the negative terminal of dc source and ac neutral is constant, i.e., –22 V. This verified the capability of the proposed BI6(5L) in mitigating high-frequency common-mode voltage.

The voltage ripple of capacitors C_1 and C_2 was also measured, as shown in Fig. 11. The ripple waveforms are in phase and similar because the capacitors are charged in parallel that balances their voltage naturally. The measured voltage ripple is approximately 3 V that is slightly higher than 2.4 V calculated using (3). Fig. 12 continues to investigate the efficiency of the proposed topology by modeling the experimental prototype in simulation. Considering a peak ac output voltage of 330 V and dc source voltages of 100 V and 50 V, peak efficiency exceeding 98% can be achieved. The efficiency decreases with power level and more apparent reduction is observed for 50 V due to higher dc source current.

VI. Conclusion

A family of six 3-level BIs is derived in this paper. They are the most compact topologies for single-phase single-stage boost dc-ac power conversion that consists of only five power switches, one capacitor and one inductor. One of the 3-level BIs without high-frequency CMV is further extended to generate five voltage levels. The proposed BI6(5L) also enhances voltage gain in addition to retaining the benefit of continuous dc source current. In addition, a phase-shifted PWM scheme is proposed that enables the simultaneous generation of five voltage levels and voltage-boosting within a single-stage operation and extends the frequency of dominant harmonics in ac voltage. Good agreement between analysis, simulation and experimental results has verified the operation and feasibility of the proposed BI6 and BI(5L).

References

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, 2005.

[2] A. Sangwongwanich, Y. Yang, and F. Blaabjerg, "A Sensorless Power Reserve Control Strategy for Two Stage Grid-Connected PV Systems," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8559–8569, 2017.

[3] Z. Zhao, M. Xu, Q. Chen, J.-S. (Jason) Lai, and Y. Cho, "Derivation, Analysis, and Implementation of a Boost Buck Converter-Based High Efficiency PV Inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1304–1313, 2012.

[4] Z. Zhao, J.-S. Lai, and Y. Cho, "Dual-Mode Double Carrier Based Sinusoidal Pulse Width Modulation Inverter With Adaptive Smooth Transition Control Between Modes," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 2094–2103, 2013.

[5] R. O. Caceres and I. Barbi, "A Boost DC–AC Converter: Analysis, Design, and Experimentation," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134–141, 1999.

[6] M. Jang, M. Ciobotaru, and V. G. Agelidis, "A Single-Phase Grid Connected Fuel Cell System Based on a Boost-Inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 279–288, 2013.

[7] P. Sanchis, A. Ursæa, E. Gubía, and L. Marroyo, "Boost DC–AC Inverter: A New Control Strategy," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 343–353, 2005.

[8] J. Ma, H. Liu, J. Chen, Y. Li, and P. C. Loh, "A Family of Coupled Dual Winding Impedance-Source Inverters with Continuous Input Currents and No DC-Link Voltage Spikes," *IEEE J. Emerg. Sel. Top. Power Electron.*, 2020.

[9] F. Z. Peng, "Z-Source Inverter," *IEEE Trans. Ind. Appl.*, vol. 39, no. 2, pp. 504–510, 2003.

[10] O. Ellabban and H. Abu-Rub, "Z-Source Inverter: Topology Improvements Review," *IEEE Ind. Electron. Mag.*, vol. 10, no. 1, pp. 6–24, 2016.

[11] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-Source Networks for Electric Power Conversion Part I: A Topological Review," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 699–716, 2015.

[12] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, and S. Yang, "Impedance-Source Networks for Electric Power Conversion Part II: Review of Control and Modulation Techniques," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1887–1906, 2015.

[13] H. Ribeiro, A. Pinto, and B. Borges, "Single-stage DC-AC converter for photovoltaic systems," in *IEEE Energy Conversion Congress and Exposition*, 2010, pp. 604–610.

[14] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three-Phase Split-Source Inverter (SSI): Analysis and Modulation," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7451–7461, 2016.

[15] L. A. Rodrigues, G. S. da Silva, and F. B. Grigoletto, "Control of Split-Source Cascaded Multilevel Inverter (SS-CMI) for Single-Phase Grid-Connected Photovoltaic Systems," in *IEEE PES Innovative Smart Grid Technologies Conference - Latin America (ISGT Latin America)*, 2019.

[16] A. Nahavandi, M. Roostaee, and M. R. Azizi, "Single Stage DC-AC Boost Converter," in *7th Power Electronics, Drive Systems & Technologies Conference*, 2016, pp. 362–366.

[17] F. Akbar, H. Cha, H. F. Ahmed, and A. A. Khan, "A Family of Single-Stage High-Gain Dual-Buck Split-Source Inverters," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1701–1713, 2020.

[18] A. Abdelhakim, P. Mattavelli, P. Davari, and F. Blaabjerg, "Performance Evaluation of the Single-Phase Split Source Inverter Using an Alternative DC–AC Configuration," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 363–373, 2018.

[19] S. S. Lee and Y. E. Heng, "Improved Single-Phase Split Source Inverter With Hybrid Quasi-Sinusoidal and Constant PWM," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2024–2031, 2017.

[20] S. S. Lee, A. S. T. Tan, D. Ishak, and R. Mohd-Mokhtar, "Single-Phase Simplified Split Source Inverter (S3I) for Boost DC–AC Power Conversion," *IEEE Trans. Ind. Electron.*, vol. 66, no. 10, pp. 7643–7652, 2019.

[21] X. Hu, P. Ma, B. Gao, and M. Zhang, "An Integrated Step-Up Inverter Without Transformer and Leakage Current for Grid-Connected Photovoltaic System," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9814–9827, 2019.

[22] F. B. Grigoletto, "Five-Level Transformerless Inverter for Single-Phase Solar Photovoltaic Applications," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 4, pp. 3411–3422, 2020.

[23] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A New Transformer-Less Five-Level Grid-Tied Inverter for Photovoltaic Applications," *IEEE Trans. Energy Convers.*, vol. 35, no. 1, pp. 106–118, 2020.

[24] R. Barzegarkhoo, Y. P. Siwakoti, and F. Blaabjerg, "A New Switched-Capacitor Five-Level Inverter Suitable for Transformerless Grid-

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Connected Applications," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8140–8153, 2020.

[25] R. Barzegarkhoo, Y. P. Siwakoti, N. Vosoughi, and F. Blaabjerg, "Six-Switch Step-up Common-Grounded Five-Level Inverter with Switched-Capacitor Cell for Transformerless Grid-Tied PV Applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 2, pp. 1374–1387, 2021.

[26] R. Barzegarkhoo, S. S. Lee, Y. P. Siwakoti, S. A. Khan, and F. Blaabjerg, "Design, Control, and Analysis of a Novel Grid-Interfaced Switched-Boost Dual T-Type Five-Level Inverter With Common-Ground Concept," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8193–8206, 2021.

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