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Selective Harmonic Elimination Technique for a 27-Level Asymmetric Multilevel Converter

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Abstract: In this paper, we present an implementation of selective harmonic elimination modulation technique in a 27-Level asymmetric multilevel converter. The main issue in this kind of converters is the generation of the gating patterns to obtain an optimized AC voltage waveform. State-of-the-art solutions use deep mathematical analysis in the frequency domain by means of the Fourier series, but they are mainly applied for two-level or symmetric multilevel converters. On the other hand, the modulation for asymmetric multilevel converters is mainly focused on nearest level control or nearest vector control. In this work, we propose a novel modulating technique that takes advantage of the switching angles optimization for a 27-level waveform. In fact, different set of solutions are obtained and presented in order to define the modulation index as well as the value of the switching angles for the multilevel waveform. A modulation index sweep was performed for the entire operating region of the converter, where it can be observed that the number of levels decreases when the modulation index is low, which are calculated in order to minimize the total harmonic distortion (THD) of the resulting voltage waveform. In order to validate the proposal, these results for different modulation indexes values are simulated, obtaining a THD < 5% for a modulation index $0.75 < M < 1.0$. Finally, a small scale proof-of-concept prototype is implemented in order to validate the proposal.

Keywords: DC–AC power conversion; multilevel power converters; total harmonic distortion



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1. Introduction

DC/AC converters are widely used in power electronics systems, such as motors, renewable energy sources, active power compensation, virtual inertia emulation, among others [1–3]. One of the main concerns in this field is the generation of harmonics in the AC waveforms due to commutation in the semiconductors, particularly with low switching frequency. An attractive alternative to mitigate the effects of the undesired harmonics produced by pulse width modulation (PWM) techniques is the use of multilevel converters [4–6], which have been an extended solution to power conversion in different fields. Additionally, they are able to achieve a high number of power levels with low dv/dt .

Among multilevel converters, a growing trend is the use of asymmetric multilevel converters [7–9], which are characterized for using isolated and unequal DC sources to generate a high amount of levels, according to the number of power semiconductors and the asymmetry ratio [10]. Indeed, these converters, with the same amount of semiconductors as their symmetric equivalent, can achieve a higher number of levels and reduce the switching harmonics.

The generation of the gating patterns of the asymmetric converters are usually made with fundamental switching frequency PWM techniques such as the nearest level control (NLC) approach [11] or the nearest vector control (NVC) technique [12], which have been extensively documented in technical literature [13,14]. Among the features of these approaches, it is possible to mention the flexibility of the switching patterns, the low computational complexity, and the suitability for multiphase multilevel applications [15]; however, there is a common drawback related to the spread harmonic content through the frequency spectrum.

Aimed to improve the performance of these methods, in terms of the undesired harmonic content, it is possible to optimize the resulting AC waveform using the selective harmonic elimination (SHE) technique, the most important advantage of which over other existing techniques is the generation of an optimized gating pattern that avoids the presence of certain harmonics that may activate undesired system/load resonances. Most of the existing previous works use SHE for symmetric multilevel converters [16–18]; nevertheless, it is difficult to find technical literature related to this technique applied to asymmetric topologies.

This approach is suitable for systems where low frequency harmonics are harmful due to potential resonances with other devices connected to the point of common coupling (PCC) [19]. Considering this, all the applications with grid-tied converters should consider useful the results provided in this paper.

The implementation of the SHE technique can offer significant advantages over other approaches, mainly related to the distribution of the harmonic components along the resulting spectrum. It is possible to consider this modulating technique in order to improve the performance of the passive active filters [20] because the complete elimination of certain particular harmonics is ensured, which is the main task of such filters.

The main contribution of this article lies in the systematic development of a SHE method applied to an asymmetric converter, which allows to generate the optimal gating patterns for different modulating indexes. The obtained switching angles ensure the absence of specific harmonic components, while the THD is minimized. The application of this technique to an asymmetric inverter is also a novelty, considering that SHE is mainly used for symmetric multilevel converters.

2. Overall System Model

SHE technique is a PWM-based modulation, where the switching angles are calculated in order to define the moment when power switches are commutated. The main characteristic of this technique is that it allows to eliminate completely specific harmonic content of the output waveform due to a mathematical analysis in the frequency domain using Fourier series. Among the advantages of this technique, it allows size reduction of power filters as low-order harmonics elimination can be done [21,22].

This technique is implemented in the 27-level (3^n , where n is the number of CHBs connected in series on the same phase) asymmetric multilevel converter presented in Figure 1. The topology considers three types of single-phase power cells connected in cascade: high power cell (HPC), medium power cell (MPC), and low power cell (LPC). Each one considers different voltage levels in the DC side, which follow the 1:3:9 ratio to minimize the redundant states [23] and therefore generate low harmonic content in the resulting output waveform.

Due to the asymmetrical voltage distribution, the HPC that commutates at low frequency (50/60 Hz) handles most of the converter power while MPC and LPC which switching frequency are higher than HPC, only manage a reduced portion of the inverter energy. This power–frequency relation is meant to reduce the power losses of the converter, as deeply explained in [24,25].

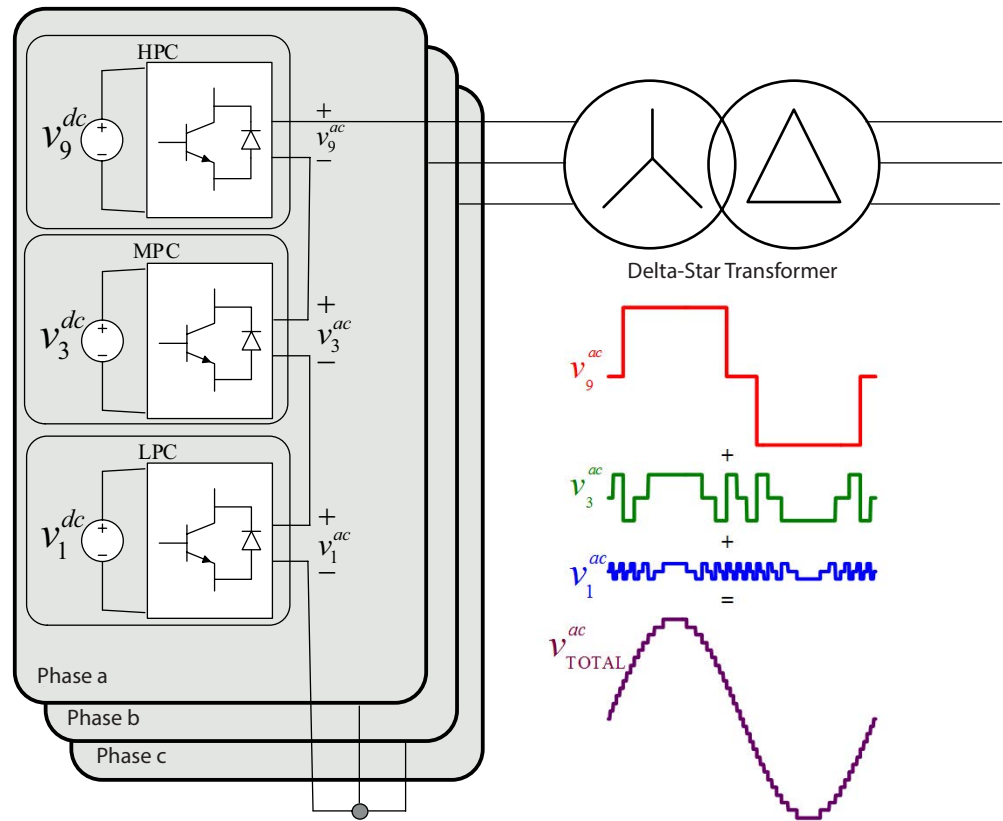


Figure 1. 27-level asymmetric multilevel converter (HPC: high power cell, MPC: medium power cell, LPC: low power cell).

To implement the SHE technique, the quarter-wave symmetry is used in order to reduce the amount of equations. This means that it is necessary to find the switching angles of the first quadrant. The rest of the angles are calculated using quarter-wave symmetry [26].

The general Fourier series equation of a periodic signal is given by [27]:

$$V(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} (a_n \cos(n\omega_0 t) + b_n \sin(n\omega_0 t)) \tag{1}$$

where $V(t)$ is the output waveform. For sake of simplicity, only seven levels are considered for this explanation, as shown in the staircase waveform of Figure 2; however, the presented analysis is also valid for a 27-level output. For the latter, V_{DC} has to be considered as the DC input of the LPC.

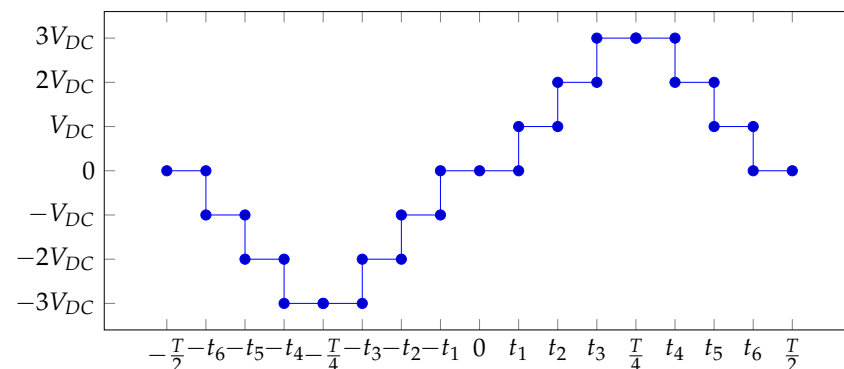


Figure 2. Output waveform for seven levels.

Due to the quarter-wave symmetry, $a_0 = 0$ and $a_1 = 0$, for instance, the cosine component is equal to zero, so only b_n component is present, and it is defined as follows:

$$b_n = \frac{2}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} f(t) \sin(n\omega_0 t) dt \tag{2}$$

Taking the Equation (2), and decomposing it in an integral by sections results in:

$$b_n = \frac{2}{T} \left(\int_{-\frac{T}{2}}^{-\frac{T}{4}} f(t) \sin(n\omega_0 t) dt + \int_{-\frac{T}{4}}^0 f(t) \sin(n\omega_0 t) dt + \int_0^{\frac{T}{4}} f(t) \sin(n\omega_0 t) dt + \int_{\frac{T}{4}}^{\frac{T}{2}} f(t) \sin(n\omega_0 t) dt \right) \tag{3}$$

Due to the quarter-wave symmetry, it is necessary to integrate the section from 0 to $\frac{T}{4}$, according to the waveform presented in Figure 3. Then, b_n is four times the value for that section.

$$b_n = \frac{2}{T} 4 \int_0^{\frac{T}{4}} f(t) \sin(n\omega_0 t) dt \tag{4}$$

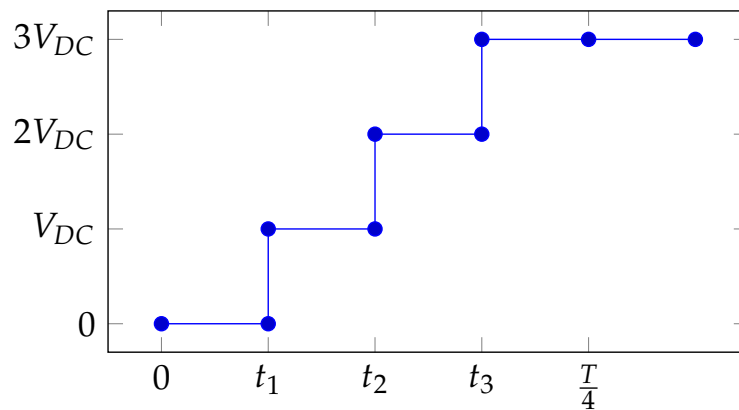


Figure 3. First quarter wave of the example signal.

Taking (4) and rewriting it as an integral by sections of $f(t_n)$:

$$b_n = \frac{8}{T} \left(\int_0^{t_1} f(0) \sin(n\omega_0 t) dt + \int_{t_1}^{t_2} f(t_1) \sin(n\omega_0 t) dt + \int_{t_2}^{t_3} f(t_2) \sin(n\omega_0 t) dt + \int_{t_3}^{\frac{T}{4}} f(t_3) \sin(n\omega_0 t) dt \right) \tag{5}$$

The first section of (5) is zero, due to $f(0) = 0$. The values of $f(t_1)$, $f(t_2)$, and $f(t_3)$ are known.

$$b_n = \frac{8}{T} \left(-V_{DC} \frac{1}{n\omega_0} \cos n\omega_0 t \Big|_{t_1}^{t_2} - 2V_{DC} \frac{1}{n\omega_0} \cos n\omega_0 t \Big|_{t_2}^{t_3} - 3V_{DC} \frac{1}{n\omega_0} \cos n\omega_0 t \Big|_{t_3}^{\frac{T}{4}} \right) \tag{6}$$

$$b_n = \frac{8}{T} \left(\frac{-V_{DC}}{n\omega_0} [\cos n\omega_0 t_2 - \cos n\omega_0 t_1] - \frac{2V_{DC}}{n\omega_0} [\cos n\omega_0 t_3 - \cos n\omega_0 t_2] - \frac{3V_{DC}}{n\omega_0} [\cos n\omega_0 \frac{T}{4} - \cos n\omega_0 t_3] \right) \tag{7}$$

In the Equation (7), $\cos(n\omega_0 \frac{T}{4})$ is equal to zero. Furthermore, factorizing by $\frac{V_{DC}}{n\omega_0}$ and adding similar terms, the following equation is obtained:

$$n\omega_0 b_n = \frac{8V_{DC}}{Tn\omega_0} [\cos n\omega_0 t_1 + \cos n\omega_0 t_2 + \cos n\omega_0 t_3] \quad (8)$$

Considering that $\theta_n = \omega t_n$ and, on the other hand, $\omega = \frac{2\pi}{T}$, it results in:

$$b_n = \frac{4V_{DC}}{n\pi} [\cos n\theta_1 + \cos n\theta_2 + \cos n\theta_3] \quad (9)$$

The Equation (9) describes the fundamental and the harmonics of the output waveform for the 7-level converter. From this equation, the fundamental is expressed equal to M , and the harmonics, which are equal to 0, to eliminate them.

Although it is true that this system describes the multilevel output of 7 levels, it is possible to use it to express the 27 levels of the converter that this work refers to.

Considering n as the amount of switching angles and b_n as the magnitude of the n th harmonic component, the Equation (9) can be generalized as follows [27]:

$$b_n = \frac{4V_{DC}}{n\pi} \sum_{n=1}^N \cos(n\theta_n) \quad (10)$$

where N is the number of switching angles for each quarter (number of variables), α_n represents the n th switching angle and V_{DC} as the DC voltage of the LPC, In addition, the switching angle variable is changed from θ to α in order to continue with the standard nomenclature used in the literature.

The N equations of (10) have N variables (switching angles): $\alpha_1, \alpha_2, \dots, \alpha_N$; thus, the system can be solved. With N angles, the fundamental component can be set according to the modulation index M and $N - 1$ harmonic components can be eliminated, with N equal to the number of equations of the system. In this way, the equations system's first equation is equaled to the modulation index, due to the latter corresponds to the fundamental component, and the rest of the coefficients are equaled to zero in order to eliminate the undesired harmonics. Considering this, the amount of equations is:

$$N = \frac{L - 1}{2} \quad (11)$$

In this case, for the 27 level asymmetric inverter ($L = 27$), the amount of equations is $E_q = 13$; thus 12 harmonics can be eliminated. The resulting system is shown in (12).

$$\begin{aligned} \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \dots + \cos(\alpha_{12}) + \cos(\alpha_{13}) &= \frac{M\pi}{4} \\ \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \dots + \cos(5\alpha_{12}) + \cos(5\alpha_{13}) &= 0 \\ \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \dots + \cos(7\alpha_{12}) + \cos(7\alpha_{13}) &= 0 \\ \vdots & \\ \cos(35\alpha_1) + \cos(35\alpha_2) + \cos(35\alpha_3) + \dots + \cos(35\alpha_{12}) + \cos(35\alpha_{13}) &= 0 \\ \cos(37\alpha_1) + \cos(37\alpha_2) + \cos(37\alpha_3) + \dots + \cos(37\alpha_{12}) + \cos(37\alpha_{13}) &= 0 \end{aligned} \quad (12)$$

The first equation describes the fundamental, and the rest of them describe the harmonics h of the asymmetric multilevel converter output waveform. The harmonics are equaled to zero using the SHE technique. The main objective of solving this system is to find the switching angles that eliminate the undesired harmonics, while the fundamental component is kept equal to the modulation index M .

It is important to highlight the nonlinear nature of the system as it has multiple solutions. Solving this equations system has two peculiarities: first, the solution for this system has to be subject to some constraints. Particularly, the solutions need to be higher than 0 and less than $\pi/2$; the switching angles need to increase between the range, i.e.,

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \dots < \alpha_{13} < \pi/2. \quad (13)$$

In order to solve this system, a cost function must be minimized. This function is the *THD*, considering the first 51 harmonics [28].

$$THD = \frac{100}{E} \sqrt{\sum_{k=2}^{51} (V_k)^2} \quad (14)$$

In the Equation (14), E is the fundamental component amplitude of the AC output waveform, and V_k is the amplitude of k th harmonic voltage. The flowchart summarizing the SHE procedure can be seen in Figure 4. The first optimization for this problem is made considering a modulation index $M = 1$; this first result leads to the solution vector expressed as switching angles, which can be found in Table 1. Note that for different values of M , different solution vectors (i.e., switching angles vector) are calculated.

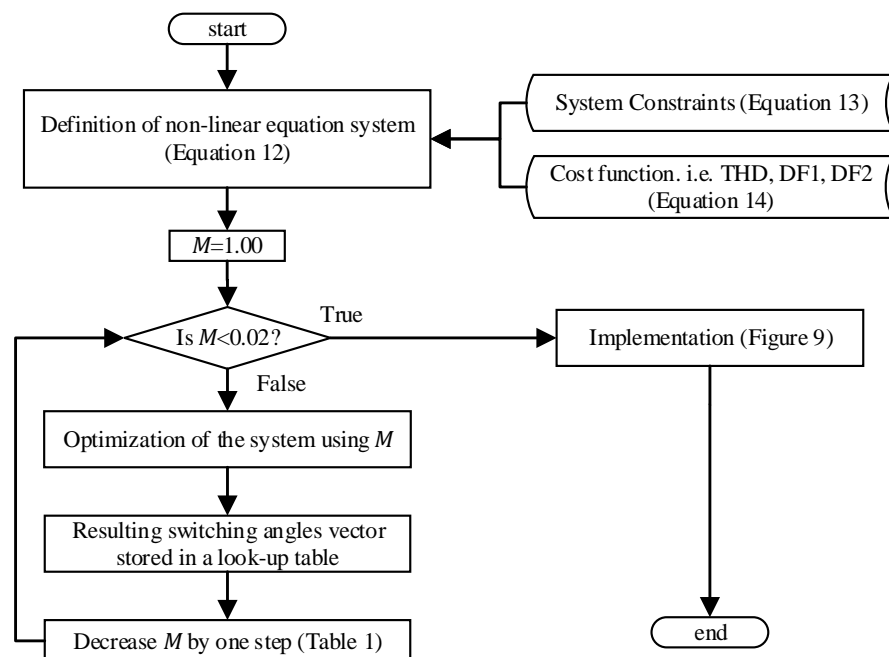


Figure 4. SHE modulation flowchart.

Table 1. Switching angles for SHE technique ($M = 1$).

Angle	Radians	Angle	Radians
α_1	0.0589	α_8	0.6146
α_2	0.1019	α_9	0.7529
α_3	0.1974	α_{10}	0.8173
α_4	0.2922	α_{11}	0.9430
α_5	0.3815	α_{12}	1.0854
α_6	0.4266	α_{13}	1.2725
α_7	0.5322		

3. Simulation

Table 2 summarizes the main parameters for these simulations, which were entirely conducted using the software MATLAB[®]. For solving the highly nonlinear equations system considering the constraints and the cost function mentioned in Section 2, function *fmincon* is used that can solve the system considering all constraints.

Table 2. Simulation parameters.

Parameter	Value
Voltage Levels	$LPC = V_{dc}$, $MPC = 3V_{dc}$, $HPC = 9V_{dc}$
Output Voltage Frequency	50 Hz
Sampling Time	2 μ s
Output Type	Open circuit
Software	MATLAB [®]
Nonlinear solver	<i>fmincon</i>

3.1. Nearest Level Control

In order to contrast the proposal, simulations are made with traditional nearest level control. This results considers a modulation index $M = 1$. Figure 5 shows the output voltage and voltage harmonic spectrum for this approach. Certainly, there are two main concerns with this modulation: the harmonic content is widely dispersed among the spectra, and second, the low frequency harmonics are not irrelevant if they are compared to the high-frequency harmonics. On the other hand, SHE modulation can cope with this eliminating target harmonics by optimizing a cost function (i.e., *THD*) and calculating the specific switching angles.

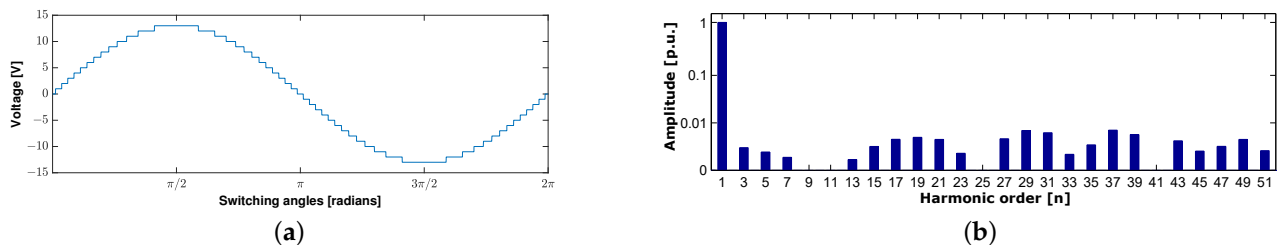


Figure 5. Simulation for 27-level multilevel converter with nearest level control: (a) output voltage, (b) voltage harmonic spectrum.

3.2. First Solution

The first solution found for the system is shown in the Table 1. For this set of angles, a modulation index of 1.0 is considered. The *THD* is considered as cost function as well. The resulting waveform is shown in Figure 6a, and its harmonic spectrum in Figure 6b.

In the first case, the proposal solution results on a waveform with a *THD* equal to 5.5826%. Even though this value is among acceptable margins, it is higher than the resulting *THD* of nearest level control [29,30]. This can be explained considering the redistribution of harmonics between the spectrum. Despite this, the resulting waveform does not have the undesired low-order harmonics, which are potentially harmful to the power system, as shown in Figure 6b.

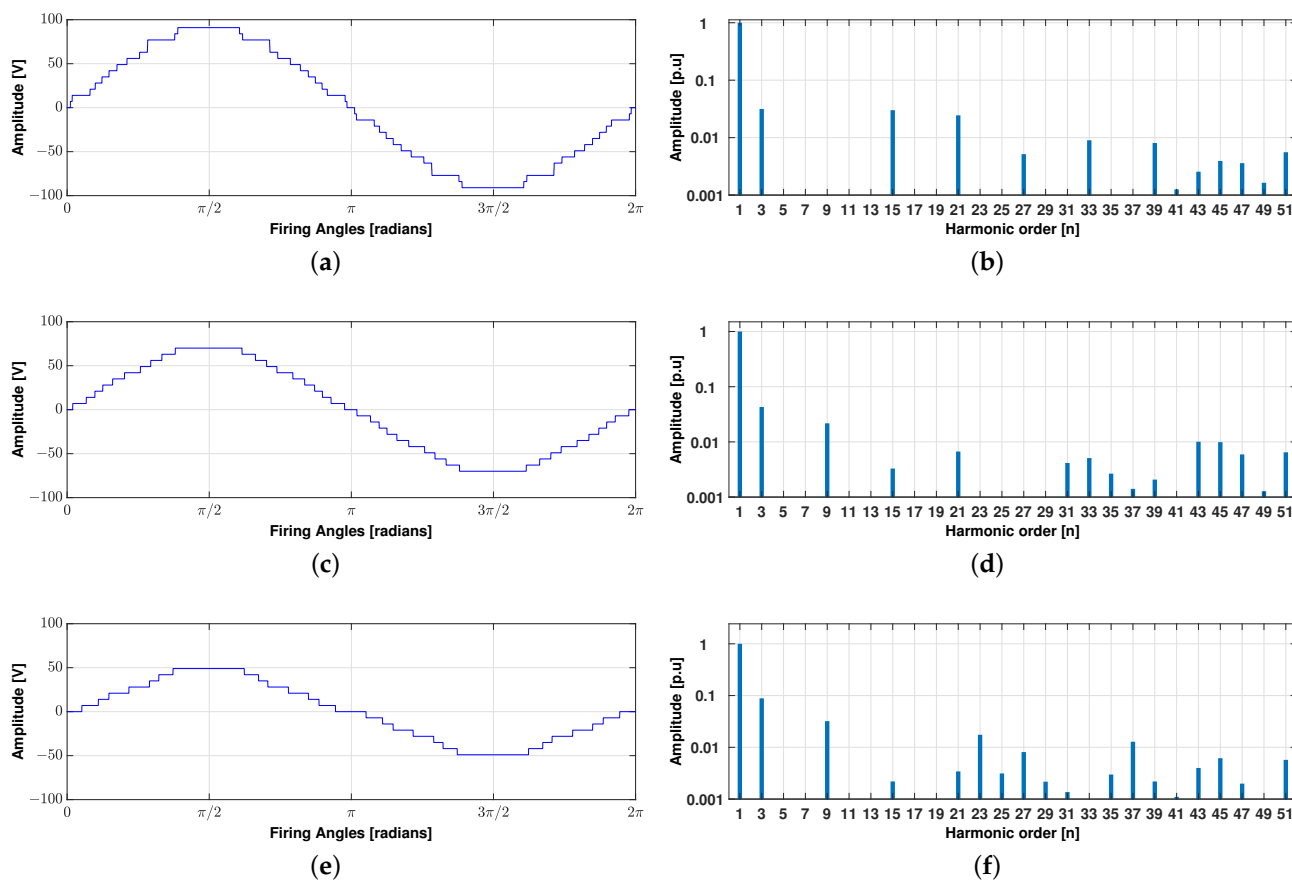


Figure 6. Waveforms: (a) Output voltage for $M = 1.00$, (b) voltage harmonic spectrum for $M = 1$, (c) output voltage for $M = 0.75$, (d) voltage harmonic spectrum for $M = 0.75$, (e) output voltage for $M = 0.50$, (f) voltage harmonic spectrum for $M = 0.50$.

3.3. Modulation Index

The modulation index M is the ratio among the fundamental frequency amplitude of a sine wave and a reference amplitude. To explain the latter, considering a fundamental amplitude of 900 V and a reference value of 1000 V, then the modulation index is equal to 0.9.

In the SHE technique, this index is essential because it determines on which values of the switching angles the number of levels of the converter need to be modified, due to other factors that need to be considered, as the resulting *THD*, or the impossibility to find a set of angles that allow to deliver the desired amount of levels for the voltage and the required fundamental amplitude [31–33].

In order to determine the modulation indexes to be used, the output voltage range is divided. In this way, different values in the modulation index can be obtained, as shown in Table 3. The first value corresponds to the modulation index equal to 1, which is the value for an output voltage of 1300 V, taking into account that the LPC has a value of 100 V, the MPC 300 V, and the HPC 900 V. The second value for the modulation index is 0.9808, and it is associated to an output voltage of 1275 V, and so on until obtaining a value of 0.0192 in the modulation index, which corresponds to 25 V.

The relation between M and the voltage is linear, so as the modulation index decreases, it also has to decrease the amount of levels on the converter output waveform, since this allows reaching the value of the voltage defined by M ; this can be seen in Figure 7. Different solutions can be found for each M , which is detailed in the next section.

3.4. Modulation Index Sweep

The modulation index sweep is the variation of the fundamental frequency amplitude of the output waveform, which may affect the amount of used levels to create the waveform. In this work, the modulation index sweep is made varying the value from 1 to 0.02 at regular intervals, as seen in Table 3.

Once the range of M is defined, using a mathematical method, the equation system is solved for all modulation index values; therefore, a set of N angles ($\alpha_1, \alpha_2, \dots, \alpha_N$) is obtained as solution for every value of M . In this work, the algorithm used to solve the system is the interior-point algorithm [34].

Table 3. Modulation index for voltage levels.

Voltage	M	Voltage	M	Voltage	M	Voltage	M
1300	1.0000	975	0.7500	650	0.5000	325	0.2500
1275	0.9808	950	0.7308	625	0.4808	300	0.2308
1250	0.9615	925	0.7115	600	0.4615	275	0.2115
1225	0.9423	900	0.6923	575	0.4423	250	0.1923
1200	0.9231	875	0.6731	560	0.4308	225	0.1731
1175	0.9038	845	0.6500	525	0.4038	200	0.1538
1150	0.8846	825	0.6346	500	0.3846	175	0.1346
1125	0.8654	800	0.6154	475	0.3654	150	0.1154
1100	0.8462	775	0.5962	455	0.3500	125	0.0962
1075	0.8269	750	0.5769	425	0.3269	100	0.0769
1050	0.8077	725	0.5577	400	0.3077	75	0.0577
1025	0.7885	700	0.5385	375	0.2885	50	0.0384
995	0.7654	675	0.5192	350	0.2692	25	0.0192

Figure 7 shows a dispersion graph with different angles in function of the modulation index. It can be observed that, from the unit modulation index, a set of 13 angles are obtained, until a modulation index of 0.95, where the amount of angles decreases to 12; therefore, an output waveform of 25 levels is generated. For an index modulation of 0.5, 7 angles are calculated, which generates an output waveform of 15 levels, as shown in Figure 7. Some interest waveforms are presented in the next section.

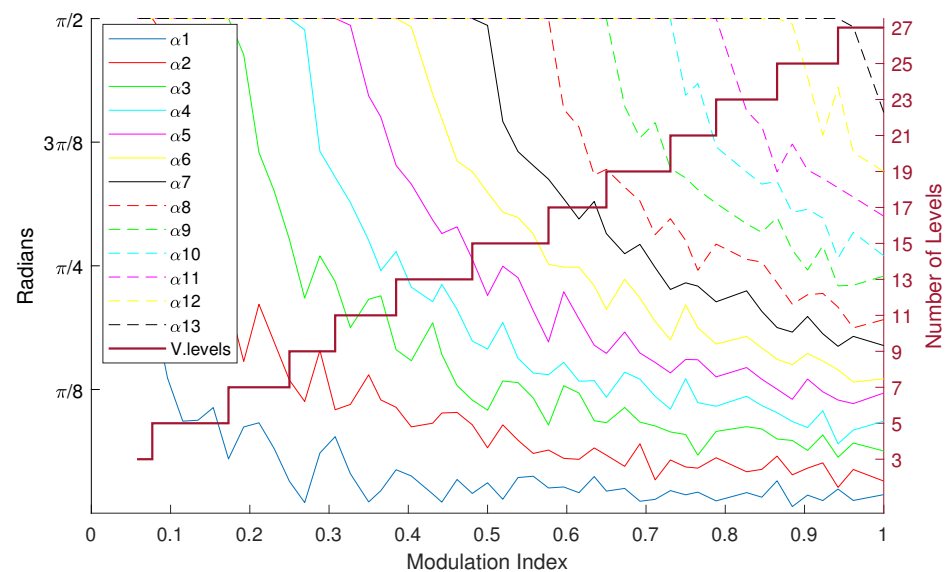


Figure 7. Switching angles for modulation index sweep.

3.5. Waveforms

In order to illustrate the differences among sets of solutions obtained due to different modulation indexes, a time-domain waveform and a frequency-domain waveforms are presented with different representative values of the modulation index M . Figure 6 shows the different results for $M = 1.00$, $M = 0.75$, and $M = 0.50$.

It can be seen that, in the first instance, with the unit modulation index, the amount of levels to be used in the converter is 27. Therefore, the harmonics to be eliminated are 12, which is shown in the harmonic spectrum of the Figure 6b. The waveform of Figure 6 shows the 27 levels for this case. When $M = 0.75$ and due to what was presented in the Section 3.4, 21 levels have to be used, limiting the amount of harmonics to be eliminated to 9, as shown in Figure 6d, and the output waveform has 21 levels, as shown in Figure 6c. Similar is the case for $M = 0.5$, where the amount of eliminated harmonics is reduced, which is directly proportional to the amount of levels of the converter, as shown in Figure 6e,f.

It is important to highlight that all waveforms for the different M values have triple harmonics. Due to the inclusion of a delta-star transformer, only the harmonics that are reflected in the secondary had to be eliminated.

Figure 8 shows the different THD values for the cases of Figure 6, which considers triple harmonics. As expected, while M decreases, the total harmonic distortion increases due to the decrease of the amount of levels in the resulting waveform, which implies fewer angles available, and therefore fewer harmonics to eliminate. Around $M = 0.7$ and greater values, the THD keeps below or at 5%, which is marked with a red line.

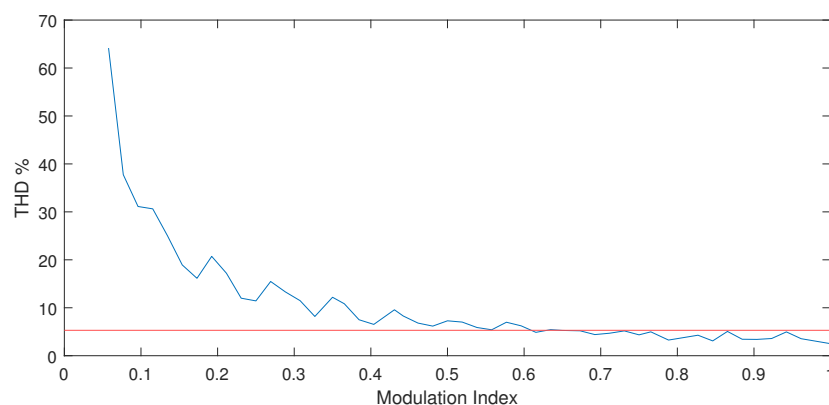


Figure 8. THD for different modulation indexes.

4. Experimental Results

The experimental results are obtained using an asymmetric multilevel converter with the following conditions:

- Array of photovoltaic (PV) panels fixed in 1:3:9 ratio, usually at 30 V, 90 V and 270 V.
- The photovoltaic panel model type is a A-255 GS (Atersa). The electrical ratings are:
 - Maximum Power (P_{mpp}): 255 Wp.
 - Open Circuit Voltage (V_{oc}): 37.83 V.
 - Short Circuit Current (I_{sc}): 8.97 A.
 - Maximum Power Voltage (V_{mpp}): 30.29 V.
 - Maximum Power Current (I_{mpp}): 8.42 A.
- Modulation Index of $M = 1.00$, $M = 0.75$ and $M = 0.50$.
- Once the waveform is generated, this is captured as an array of comma-separated values(.csv archive) to process it using MATLAB®, with a resolution of 5000 points per cycle.
- The harmonic spectrum is the result of this digital processing.
- The results are in open-circuit.
- Circuit main characteristics:

- Silicon Carbide MOSFET: rated at 1200 V and 80 m Ω . Modulation considers 1 μ s of idle switching time to prevent short-circuits.
- Insulated DC–DC converters to separate control signals and power output.
- Optical fiber receptor to command power switches, allowing fast communication and EMI/RFI immunity, among others.

The experimental implementation considers an open-loop control, where the resulting switching angles for the modulation index M sweep are calculated and saved in a look-up table. First, when a specific value of M is needed, the stored switching angles are read from the dSPACE which carries the switching angles for the different M values and also the corresponding switching sequences for the different power cells. On the second hand, the FPGA is used to safely commute the power switches, i.e., calculating the idle time for the semiconductors, ensure safety operation, and prevent short-circuits, among others. Finally, the FPGA send the switching command to the power cells through optical fiber in order to insulate the control signals from the power signals. This scheme can be seen in Figure 9.

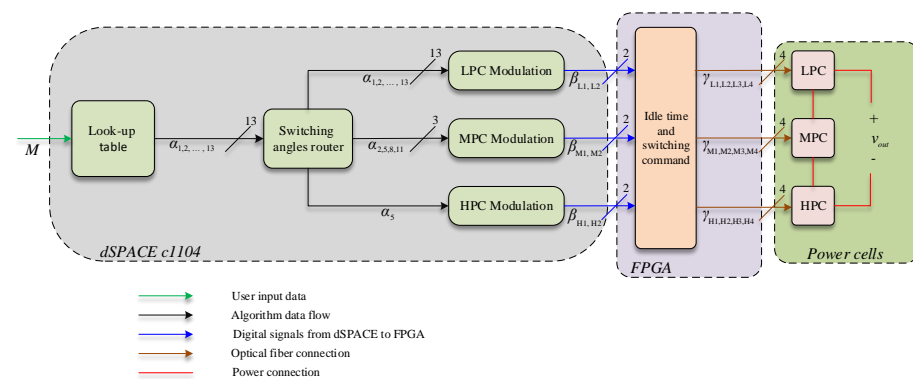


Figure 9. Control scheme for implementation.

The real converter used in this work is shown in Figure 10. First, PV panels are connected in arrays, in order to have the ratio 1:3:9 among the DC voltages sources. The first modulation index to be used is $M = 1$ and it considers traditional NLC modulation for comparison purposes. The experimental results for this traditional modulation be seen in Figure 11. The waveform is highly sinusoidal and the voltage harmonic spectrum shows a low harmonics presence. However, most of the odd nontriple harmonics are not completely eliminated; this is because the NLC technique does not consider a mathematical model that allows to calculate the switching angles for the semiconductors, i.e., they are not controlled. This does not guarantee the complete elimination of target harmonics, as SHE modulation has been proved to do.



Figure 10. Implementation for a 27-level asymmetric multilevel converter.

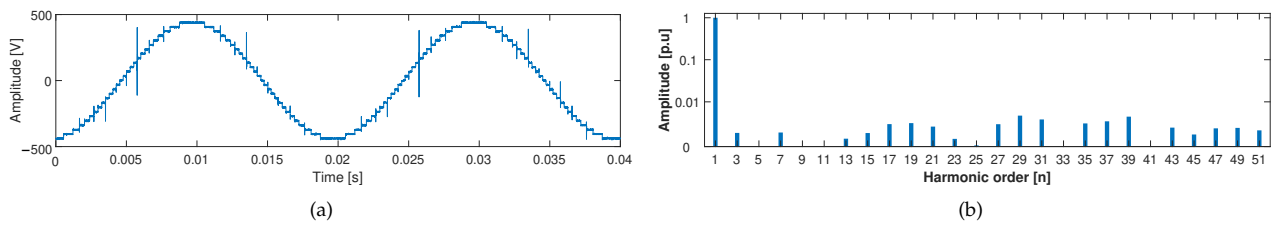


Figure 11. Waveforms: (a) Experimental output voltage for traditional nearest level control, (b) voltage harmonic spectrum for nearest level control.

The resulting waveform is shown in Figure 12, where the output waveforms for different modulation indexes are shown. The resulting signal for $M = 1$ is shown in Figure 12a,b.

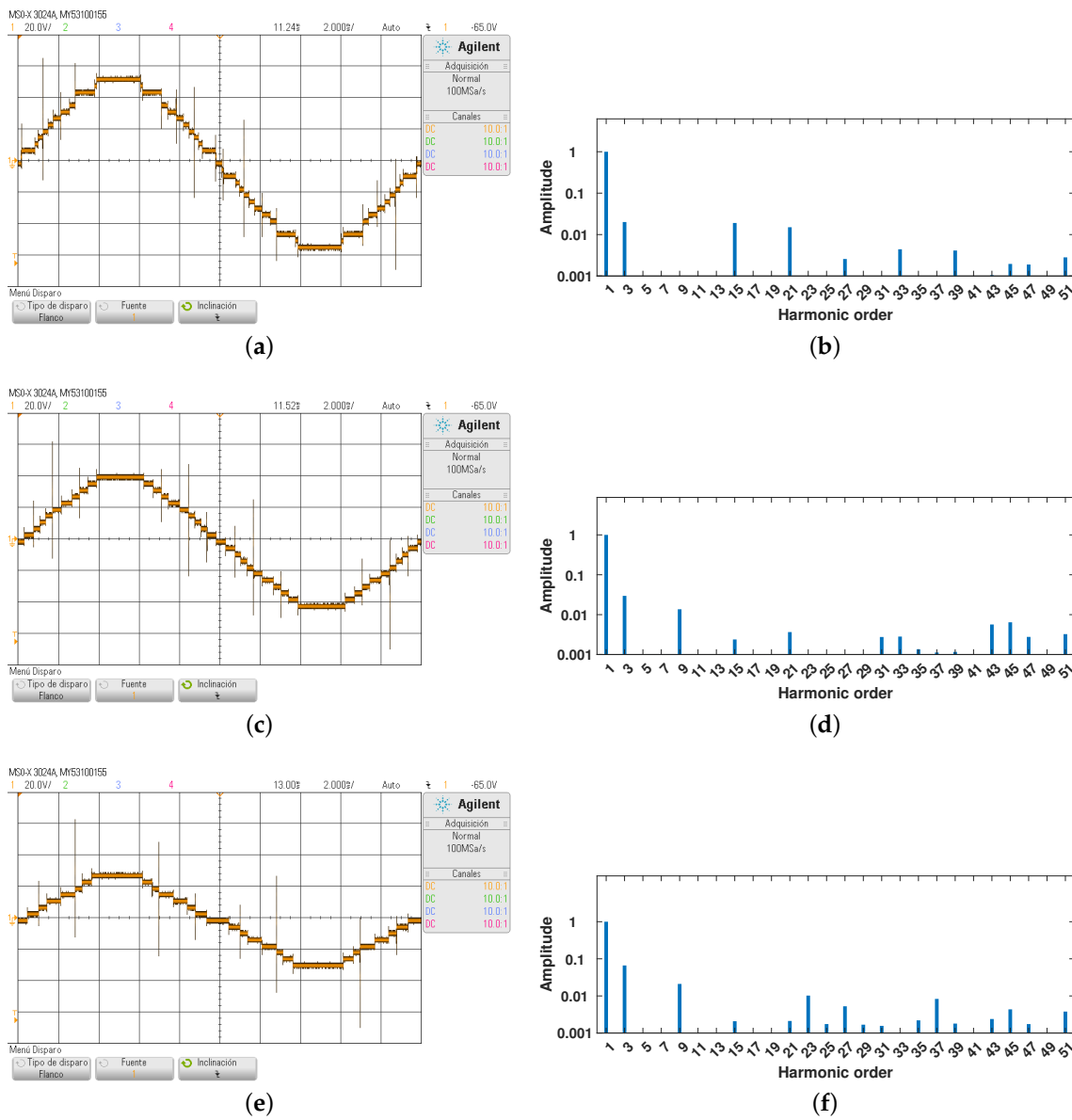


Figure 12. Waveforms for experimental implementation for different M values. (a) Output voltage for $M = 1$, (b) harmonic spectrum for $M = 1$, (c) output voltage for $M = 0.75$, (d) harmonic spectrum for $M = 0.75$, (e) output voltage for $M = 0.5$, and (f) harmonic spectrum for $M = 0.5$.

Some spikes can be observed in the waveform. They correspond to high-frequency harmonics, so they will not appear in the harmonic spectra, because it is considered up to the 51th harmonic. On the other hand, some switching angles are close from each other, leaving some voltage levels smaller than others. In the harmonic spectrum, it is observed that the harmonics to be eliminated are completely eliminated, and the triple harmonics eliminated have been eliminated unintentionally.

In Figure 12c,d, a waveform for modulation index $M = 0.75$ is shown as an experimental result. As the modulation index decreases, the voltage of the output waveform also decreases, and the amount of harmonics to eliminate is also affected. The main difference among the simulation result and experimental result for this modulation index value is the presence of high-frequency harmonics.

In Figure 12c,d, a waveform for modulation index $M = 0.75$ is shown as experimental result. As the modulation index decreases, the voltage of the output waveform also decreases, and the amount of harmonics to eliminate is also affected. The main difference among the simulation result and experimental result for this modulation index value is the presence of high frequency harmonics.

For modulation index $M = 0.5$, the output of the converter is shown in Figure 12e,f. The waveform for this case has only 15 voltage levels. Because of that just six odd nontriple harmonics are eliminated. High frequency harmonics appear, as the other results.

As shown in Table 4, THD index for simulation (THD_{SIM}) and THD index for experimental (THD_{EXP}) show almost the same results between them, which proves the proposal.

Table 4. THD for different modulation indexes.

M	THD_{SIM} (%)	THD_{EXP} (%)
1.00	2.583	2.5618
0.75	5.4579	5.4036
0.50	9.5359	10.4747

In open-circuit, the implementation verifies the simulation results, showing the expected waveforms and harmonic spectrum based on the simulations. The results are satisfying because simulation and experimental results, in the all three cases, are similar.

The 27-level asymmetric multilevel inverter if feeds an RL load in the experimental setup, an instantaneous regeneration will happen due to the phase shift between the current and load voltage. Figure 13a depicts the equivalent circuit when the current and load voltage are positive. In this condition, the peak voltage in $v_{oi}(t)$ is $V_{DC} - 2V_{sat,MOSFET}$. Contrary, when the load current is negative and the load voltage is positive (Figure 13b), the peak voltage in $v_{oi}(t)$ is $V_{DC} - 2V_{diode}$. These two facts explain why the voltage $v_{oi}(t)$ presents a displacement in the zero voltage level. Introducing a DC component, in the harmonic spectrum of the individual and total voltage. If the DC voltage is high enough, the voltages $V_{sat,MOSFET}$ and V_{diode} are negligible and will not greatly affect the THD. Finally, as the load voltage is the summation of the individual H-bridge voltages, this voltage displacement is reflected as a voltage sag in the load total voltage waveform, if DC voltages are low. This phenomenon is observed in Figure 14, where an RL load is considered with $R = 10 \Omega$ and $L = 2.5 \text{ mH}$ for the inverter modulated with SHE and $M = 1$. The voltage waveform has the expected shape similar to its open-circuit counterpart. Nevertheless, the effect of the load can be noticed by the presence of the 25th harmonic.

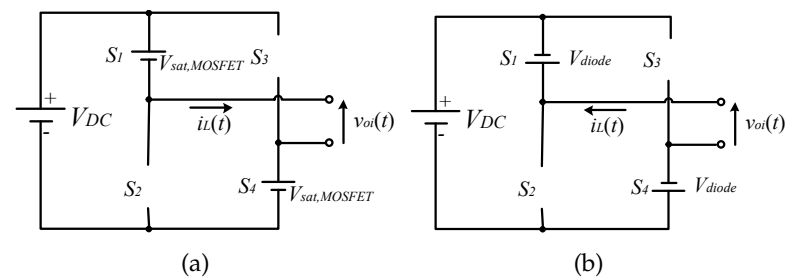
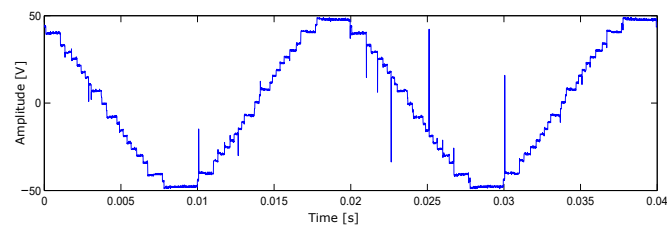
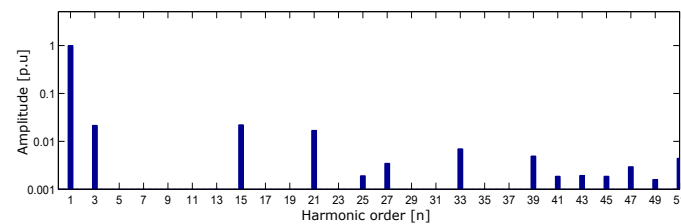


Figure 13. Equivalent circuit of an H-bridge for voltage sag analysis; (a) for positive load both voltage and current, (b) for positive load voltage and negative current.



(a)



(b)

Figure 14. Results for experimental implementation of SHE and RL load; (a) output voltage waveform, (b) voltage harmonic spectrum.

The topology used, together with the proposed modulation scheme, can be used as AC drive or reactive power compensator.

The proposed modulation scheme is integrated into the control scheme, as presented in [35–37]. The control scheme delivers to the SHE technique the modulation index and phase requirements for the required voltage waveform. In particular, due to the approach of obtaining the switching angles, where quarter-wave symmetry is used, due to this the minimum update rate is $T/4$, where T is the period of the signal. In addition, for the correct implementation of the commutation angles, a PLL is necessary and to have a sufficient number of points per period, to be able to implement the commutation angles obtained offline in the most precise way.

5. Discussion

The SHE modulation technique determines the switching angles based on a set of nonlinear equations, which are obtained from the requested predefined waveform. Due to the nonlinear nature of the resulting equations, solving them online is slow and does not allow a quick response to changes [38]. In fact, considering this issue, the switching angles are calculated offline and the solutions are stored in a look-up table within the digital control platform, in order to avoid any overload. Therefore, the main computational effort is made offline by preprocessing software.

The use of memory in DSP, FPGA, or Microlab-box type of platforms will depend on the number of angles and points that the modulation index vector have. In particular, for the modulation technique used in this work, 13 switching angles and a modulation

index vector $m = [0.00:0.01:1.00]$ are considered. Using a 64-bit codification, the resulting look-up table may use 72 kB of memory, which is certainly negligible for off-the-shelf digital control boards.

As compared with the simplest NLC technique the computational burden and memory usage of the SHE proposal is certainly higher; which is an expected trade-off between simplicity and improvement. However, if the comparison is made with methods based on Space Vector Modulation, the proposed technique is easier to implement because it only requires a small memory space to store the look-up table with the switching angles, considering that all the hard calculations are made offline. Nevertheless, it is important to highlight that computational complexity is no longer an obstacle for the existing methods due to the advance on the control hardware for power converters.

For other similar modulation techniques, to obtain the commutation angles, as a function of the modulation index, polynomial approximations of the solution trajectories angles are made. Under this approach, it is possible to decouple memory usage, but the use of resources at the level of multiplication, power operations, and additions is required.

6. Conclusions

Implementing a SHE-based modulation technique in a 27-level asymmetric multilevel converter is possible. This modulation allows generating an output phase voltage, V_{total}^{ac} , with no-odd nontriple low-frequency harmonics.

The modulation index (M) variation allows obtaining different solutions for the same system, depending on the selected amplitude of the fundamental frequency component. While M decreases, the number of switching angles and voltage levels decrease as well. Frequency domain graphs demonstrate that this diminution will decrease the number of harmonics to be eliminated in the output phase voltage, V_{total}^{ac} , and, therefore, the distortion index will increase.

The aforementioned issues can be assuaged by choosing the number of levels that provide a lower THD in each particular value of M . In fact, for $M > 0.7$, the THD stays close to or below 5%, which is verified through the experimental results.

The experimental implementation confirms the results obtained in simulations for V_{total}^{ac} . The harmonic spectra in both cases are practically the same. This is because the number of points by period is 606, obtaining a resolution of 0.59° between samples, suitable for the proposed modulation technique. Furthermore, the drop voltage in the power semiconductor is negligible.

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References

1. Ansari, S.; Chandel, A.; Tariq, M. A Comprehensive Review on Power Converters Control and Control Strategies of AC/DC Microgrid. *IEEE Access* **2021**, *9*, 17998–18015. [[CrossRef](#)]
2. Dashtaki, M.A.; Nafisi, H.; Pouresmaeil, E.; Khorsandi, A. Virtual Inertia Implementation in Dual Two-Level Voltage Source Inverters. In Proceedings of the 2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), Tehran, Iran, 4–6 February 2020; pp. 1–6. [[CrossRef](#)]

3. Dashtaki, M.A.; Nafisi, H.; Khorsandi, A.; Hojabri, M.; Pouresmaeil, E. Dual Two-Level Voltage Source Inverter Virtual Inertia Emulation: A Comparative Study. *Energies* **2021**, *14*, 1160. [[CrossRef](#)]
4. Rodriguez, J.; Lai, J.S.; Peng, F.Z. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [[CrossRef](#)]
5. Rubilar, I.; Espinoza, J.; Muñoz, J.; Morán, L. DC link voltage unbalance control in three-phase UPQCs based on NPC topologies. In Proceedings of the 2007 IEEE Industry Applications Annual Meeting, New Orleans, LA, USA, 23–27 September 2007; pp. 597–602. [[CrossRef](#)]
6. Muñoz, J.; Reyes, J.; Espinoza, J.; Rubilar, I.; Morán, L. A novel multi-level three-phase UPQC topology based on full-bridge Single-Phase Cells. In Proceedings of the IECON 2007—33rd Annual Conference of the IEEE Industrial Electronics Society, Taipei, Taiwan, 5–8 November 2007; pp. 1787–1792. [[CrossRef](#)]
7. Sathik, J.; Aleem, S.H.E.A.; Shalchi Alishah, R.; Almakhlles, D.; Bertilsson, K.; Bhaskar, M.S.; Fernandez Savier, G.; Dhandapani, K. A Multilevel Inverter Topology Using Diode Half-Bridge Circuit with Reduced Power Component. *Energies* **2021**, *14*, 7249. [[CrossRef](#)]
8. Gaisse, P.; Muñoz, J.; Villalón, A.; Aliaga, R. Improved Predictive Control for an Asymmetric Multilevel Converter for Photovoltaic Energy. *Sustainability* **2020**, *12*, 6204. [[CrossRef](#)]
9. Espinosa, E.; Espinoza, J.; Ramirez, R.; Rohten, J.; Villarroel, F.; Melin, P.; Guzman, J. A new modulation technique for 15-level asymmetric inverter operating with minimum THD. In Proceedings of the IECON 2013—39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, Austria, 10–13 November 2013; pp. 6164–6169. [[CrossRef](#)]
10. Fernández, L.D.P.; Caicedo, E.A.; Rodríguez, J.L.D. Comparative analysis of 9 levels cascade multilevel converters with selective harmonic elimination. In Proceedings of the 2015 IEEE Workshop on Power Electronics and Power Quality Applications (PEPQA), Bogota, Colombia, 2–4 June 2015; pp. 1–6. [[CrossRef](#)]
11. Busarello, T.D.C.; Pomilio, J.A.; Bubshait, A.S.; Simoes, M.G. Staircase modulation based battery storage system with Asymmetric Cascaded H-Bridge Multilevel Inverter. In Proceedings of the 2015 IEEE Power Energy Society General Meeting, Denver, CO, USA, 26–30 July 2015; pp. 1–5. [[CrossRef](#)]
12. Sreedhar, R.; Karunanithi, K.; Chandrasekar, P.; Teja, R.B. Nearest Space-Vector Control Strategy for High-Resolution Multilevel Inverters. In Proceedings of the 2021 6th International Conference for Convergence in Technology (I2CT), Maharashtra, India, 2–4 April 2021; pp. 1–6. [[CrossRef](#)]
13. Jonnala, R.B.; Eluri, N.R.; Choppavarapu, S.B. Implementation, comparison and experimental verification of nearest vector control and nearest level control techniques for 27-level asymmetrical CHB multilevel inverter. In Proceedings of the 2016 International Conference on Control, Instrumentation, Communication and Computational Technologies (ICCICCT), Kumaracoil, India, 16–17 December 2016; pp. 214–221. [[CrossRef](#)]
14. Nguyen, M.H.; Kwak, S. Nearest-Level Control Method With Improved Output Quality for Modular Multilevel Converters. *IEEE Access* **2020**, *8*, 110237–110250. [[CrossRef](#)]
15. Deng, Y.; Harley, R.G. Space-Vector Versus Nearest-Level Pulse Width Modulation for Multilevel Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 2962–2974. [[CrossRef](#)]
16. Zhao, H.; Jin, T.; Wang, S.; Sun, L. A Real-Time Selective Harmonic Elimination Based on a Transient-Free Inner Closed-Loop Control for Cascaded Multilevel Inverters. *IEEE Trans. Power Electron.* **2016**, *31*, 1000–1014. [[CrossRef](#)]
17. Siddiqui, N.I.; Alam, A.; Quayyoom, L.; Sarwar, A.; Tariq, M.; Vahedi, H.; Ahmad, S.; Mohamed, A.S.N. Artificial Jellyfish Search Algorithm-Based Selective Harmonic Elimination in a Cascaded H-Bridge Multilevel Inverter. *Electronics* **2021**, *10*, 2402. [[CrossRef](#)]
18. Padmanaban, S.; Dhanamjayulu, C.; Khan, B. Artificial Neural Network and Newton Raphson (ANN-NR) Algorithm Based Selective Harmonic Elimination in Cascaded Multilevel Inverter for PV Applications. *IEEE Access* **2021**, *9*, 75058–75070. [[CrossRef](#)]
19. Zhou, H.; Li, Y.W.; Zargari, N.R.; Cheng, Z.; Ni, R.; Zhang, Y. Selective Harmonic Compensation (SHC) PWM for Grid-Interfacing High-Power Converters. *IEEE Trans. Power Electron.* **2014**, *29*, 1118–1127. [[CrossRef](#)]
20. Flores, P.; Dixon, J.; Ortuzar, M.; Carmi, R.; Barriuso, P.; Moran, L. Static Var Compensator and Active Power Filter With Power Injection Capability, Using 27-Level Inverters and Photovoltaic Cells. *IEEE Trans. Ind. Electron.* **2009**, *56*, 130–138. [[CrossRef](#)]
21. Zhang, Y.; Li, Y.W.; Zargari, N.R.; Cheng, Z. Improved Selective Harmonics Elimination Scheme With Online Harmonic Compensation for High-Power PWM Converters. *IEEE Trans. Power Electron.* **2015**, *30*, 3508–3517. [[CrossRef](#)]
22. Pérez-Basante, A.; Ceballos, S.; Konstantinou, G.; Pou, J.; Andreu, J.; de Alegría, I.M. $(2N + 1)$ Selective Harmonic Elimination-PWM for Modular Multilevel Converters: A Generalized Formulation and A Circulating Current Control Method. *IEEE Trans. Power Electron.* **2018**, *33*, 802–818. [[CrossRef](#)]
23. Pereda, J.; Dixon, J. Cascaded Multilevel Converters: Optimal Asymmetries and Floating Capacitor Control. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4784–4793. [[CrossRef](#)]
24. Muñoz, J.; Gaisse, P.; Baier, C.; Rivera, M.; Gregor, R.; Zanchetta, P. Asymmetric multilevel topology for photovoltaic energy injection to microgrids. In Proceedings of the 2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL), Trondheim, Norway, 27–30 June 2016; pp. 1–6. [[CrossRef](#)]
25. Silva, P.; Muñoz, J.; Aliaga, R.; Gaisse, P.; Restrepo, C.; Fernández, M. On the DC/DC converters for cascaded asymmetric multilevel inverters aimed to inject photovoltaic energy into microgrids. In Proceedings of the 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand, 5–8 December 2016; pp. 1–6. [[CrossRef](#)]

26. Aguilera, R.P.; Acuña, P.; Lezana, P.; Konstantinou, G.; Wu, B.; Bernet, S.; Agelidis, V.G. Selective Harmonic Elimination Model Predictive Control for Multilevel Power Converters. *IEEE Trans. Power Electron.* **2017**, *32*, 2416–2426. [[CrossRef](#)]
27. Sinha, Y.; Nampally, A. Modular multilevel converter modulation using fundamental switching selective harmonic elimination method. In Proceedings of the 2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA), Birmingham, UK, 20–23 November 2016; pp. 736–741. [[CrossRef](#)]
28. *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)—Redline*; IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems—Redline. Institute of Electrical and Electronics Engineers: New York, NY, USA, 2014; pp. 1–213.
29. Muñoz, J.; Torres, I.; Guzmán, J.; Baier, C.; Melín, P.; Rohten, J.; Espinoza, J.; Silva, J. Selective harmonic elimination for a 27-level asymmetric multilevel converter. In Proceedings of the 2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC/I CPS Europe), Milan, Italy, 6–9 June 2017; pp. 1–5. [[CrossRef](#)]
30. Muñoz, J.; Pérez, C.; Torres, I.; Villalon, A.; Espinosa, E.; Melin, P.; Rohten, J. Multilevel Selective Harmonic Elimination for an Asymmetric Converter. In Proceedings of the 2018 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Amalfi, Italy, 20–22 June 2018; pp. 485–490. [[CrossRef](#)]
31. Yang, K.; Hao, J.; Wang, Y. Switching angles generation for selective harmonic elimination by using artificial neural networks and quasi-newton algorithm. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016; pp. 1–5. [[CrossRef](#)]
32. Khamitov, A.; Massalim, Y.; Ruderman, A. Simultaneous Selective Harmonic Elimination and Total Harmonic Distortion minimization for a single-phase two-level inverter. In Proceedings of the 2017 International Conference on Optimization of Electrical and Electronic Equipment (OPTIM) 2017 Intl Aegean Conference on Electrical Machines and Power Electronics (ACEMP), Brasov, Romania, 25–27 May 2017; pp. 735–740. [[CrossRef](#)]
33. Manohar, V.J.; Rani, I.S.; Ramana, K.V. SHE controlled CHB 7-level inverter with equal unequal DC sources using C-genetic algorithm. In Proceedings of the 2016 International Conference on Communication and Electronics Systems (ICCES), Coimbatore, India, 21–22 October 2016; pp. 1–6. [[CrossRef](#)]
34. Zorkal'tsev, V. Algorithms of the interior point method. In Proceedings of the 2017 Constructive Nonsmooth Analysis and Related Topics (dedicated to the memory of V.F. Demyanov) (CNSA), Saint Petersburg, Russia, 22–27 May 2017; pp. 1–4. [[CrossRef](#)]
35. Manoharan, M.S.; Ahmed, A.; Park, J.H. An Improved Model Predictive Controller for 27-Level Asymmetric Cascaded Inverter Applicable in High-Power PV Grid-Connected Systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 4395–4405. [[CrossRef](#)]
36. Sajadi, R.; Iman-Eini, H.; Bakhshizadeh, M.K.; Neyshabouri, Y.; Farhangi, S. Selective Harmonic Elimination Technique With Control of Capacitive DC-Link Voltages in an Asymmetric Cascaded H-Bridge Inverter for STATCOM Application. *IEEE Trans. Ind. Electron.* **2018**, *65*, 8788–8796. [[CrossRef](#)]
37. Panda, K.P.; Lee, S.S.; Panda, G. Reduced Switch Cascaded Multilevel Inverter With New Selective Harmonic Elimination Control for Standalone Renewable Energy System. *IEEE Trans. Ind. Appl.* **2019**, *55*, 7561–7574. [[CrossRef](#)]
38. Yang, K.; Feng, M.; Wang, Y.; Lan, X.; Wang, J.; Zhu, D.; Yu, W. Real-Time Switching Angle Computation for Selective Harmonic Control. *IEEE Trans. Power Electron.* **2019**, *34*, 8201–8212. [[CrossRef](#)]