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Transformer-less Grid-Tied AC Module Systems Suitable for Single-Phase Renewable Energy-Based Applications

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Abstract

Grid-tied converters/inverters with a transformerless (TL) circuit configuration are an efficient power electronics interface between the power grid and renewable energy resources, e.g., photovoltaic (PV) arrays, batteries, and fuel cells. Such a tremendous inclination to use the TL converters originates from their appropriate power density and higher rate of overall efficiency with a lower overall manufacturing cost in comparison to their transformer-based counterparts. However, detaching the galvanic isolated transformer from the converter and the grid and using the commercially available two or three-level voltage source inverters lead the following challenges/concerns: 1) Variable common mode voltage (CMV) and in turn the ground leakage current problem, 2) the need for another power processing stage to meet the minimum requirement of the grid voltage amplitude while utilizing a relatively low value of the dc input voltage, and 3) power quality enhancement issue. The aim of this thesis is to investigate the above-mentioned constrains/challenges among various developed versions of the existing TL inverters, and accordingly propose several new circuit configurations to address such issues. All the proposed converters/inverters are able to generate a multilevel staircase output voltage waveform using a single dc source leading to improve the injected power quality and reduce the need for large bulky interfaced filters. To alleviate the effect of high frequency CMV in grid-connected PV systems and to nullify the concern of leakage current, the design configuration of all the proposed topologies is either based on a common-ground circuit architecture or a mid point-clamping technique. Through the incorporation of switched-capacitor and/or switched-boost technique, all the proposed structures possess either a static or dynamic voltage conversion gain, which make them an attractive choice when the input dc source is variable and low. Extending the operating range of the grid-connected TL converters for a wide range of the input dc voltage, reduction on voltage/current stress profile of the switches, circuit extension capability to generate larger number of output voltage levels, and reduced number of required power electronics elements, i.e., switches, gate drivers, inductors, and capacitors are some other important characteristics of the proposed topologies. Since the major goal of each of the proposed TL-based grid-tied inverters/converters is to inject a tightly controlled current to the grid, the performance of all the proposed structures is governed within a closed-loop control platform. Comparative study and the design guidance of the proposed converters are developed. And finally, several simulation and experimental results are presented to prove the feasibility and correct operation of each of the proposed converters.

AUTHOR'S DECLARATION

I, *Reza Barzegarkhoo* declare that this thesis, submitted in partial fulfilment of the requirements for the award of Doctor of Philosophy, in the *Electrical and Data Engineering*, *Engineering and IT* at the University of Technology Sydney, Australia, is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis. This document has not been submitted for qualifications at any other academic institution. This research is supported by the Australian Government Research Training Program.

SIGNATURE: Production Note: Signature removed prior to publication.

[Reza Barzegarkhoo]

DATE: 20th March, 2023

PLACE: Sydney, Australia

DEDICATION

To my family, friends, and my beloved home country, Iran...

Hereby, I would like to dedicate this dissertation to my family first. During such a tough period and in specific when the COVID-19 pandemic emerged, I never had a chance to visit my family in Iran. However, I could feel their endless emotions, unconditional love, and continuous encouragement when I was struggling with each piece of this thesis content. I also would like to present this dissertation to my beloved sister and the little member of our family, *Peransa*, my sister daughter, who was born during the latest months of my PhD.

There is no doubt that without the technical support and important advice of my closed friends and the collaborators from different corner of the word, this thesis could not have such a nice outcome. With their help and support, more than 20 articles in different well-known journals and conference proceeding were published from this thesis content, which can perfectly show the importance of collaboration with developed/fresh ideas. I would like to particularly express my gratitude to my friend, Mr. Majid Farhangi who gave me his tremendous support in the UTS Power Electronics Lab.

Last but not least, I would like to dedicate all the efforts done to compile this research during my PhD to all the Iranian people living in my beloved home country. As a persian guy, I tried to do my best during my stay abroad to show our nice culture, friendly behavior, and research/team work capability to the rest of the world. I would like to dedicate this work to all the talented young researchers who are living in Iran and have this aspiration to move towards the PhD to flourish their research potential.

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I would express my deepest gratitude to my principal supervisor Dr. Yam Siwakoti for his guidance and encouragement during my study. I also would like to thank my co-supervisor, Dr. Ricardo P. Aguilera for his thorough help and advice throughout this research.
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List of Publications

Journal Articles

- **R. Barzegarkhoo**, M. Farhangi, S. S. Lee, R. P. Aguilera, F. Blaabjerg, and Y. P. Siwakoti, "A Novel Active Neutral Point-Clamped Five-Level Inverter With Single-Stage Integrated Dynamic Voltage Boosting Feature," in IEEE Transactions on Power Electronics, doi: 10.1109/TPEL.2023.3257959.

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- **R. Barzegarkhoo**, Y. P. Siwakoti and F. Blaabjerg, "Model Predictive Control of a Five-level Active Boost Neutral Point Clamped (5L-ABNPC) Inverter for Transformerless Grid-Connected PV Applications," 2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia), 2020, pp. 209-213.

- **R. Barzegarkhoo**, Y. P. Siwakoti, T. Long and F. Blaabjerg, "Five-Level Grid-Tied Inverter Employing Switched-Capacitor Cell with Common-Grounded Feature," 2020 IEEE Applied Power Electronics Conference and Exposition (APEC), 2020, pp. 3298-3303.

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Awards and Achievements

- A recipient of the prestigious Green Talent Award 2021 from the German Federal Ministry of Education and Research (BMBF). “Selected as one of 25 green-talent awardees in 2021 among more than 450 international applicants”.
- A recipient of the best paper award selected by the IEEE Industrial Electronics Society (IES) in 2022.
- A recipient of the best paper award selected by the 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG 2022), Kiel, Germany.
- A recipient of the IEEE Industrial Electronics Society Inter Chapter Paper competition with the theme of Smart Connected Community in 2021.
- Winners of the best showcase award among all the PhD candidates in School of Electrical and Data Engineering, University of Technology Sydney (UTS), Australia, Oct 2021, and Nov 2020.
- Winner of the best showcase award among all the PhD candidates in the Faculty of Engineering and IT, University of Technology Sydney (UTS), Australia, Nov 2020.
- A commendation by Faculty of Engineering and IT of UTS for the HDR 2022 team awards.
- Student Travel award to attend in ECCE 2021, Vancouver, Canada and PEDG 2022, Kiel, Germany.
- Distinguished Reviewer of IEEE Transactions on Industrial Electronics in 2020.
- Star Reviewer of IEEE journal of Emerging and Selected Topics in Power Electronics in 2022.

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Acronyms

- **PV**: Photovoltaic
- **RE**: Renewable Energy
- **APD**: Active Power Decoupling
- **MPPT**: Maximum Power Point Tracking
- **GT-ACM**: Grid-Tied-AC Module
- **LF**: Low Frequency
- **HF**: High Frequency
- **CMV**: Common Mode Voltage
- **PQE**: Power Quality Enhancement
- **CG**: Common-Ground
- **TSV**: Total Standing Voltage
- **SC**: Switched-Capacitor
- **SB**: Switched-Boost
- **LS-PWM**: Level-Shifted Pulse Width Modulation
- **PS-PWM**: Phase-Shifted Pulse Width Modulation
- **MLIs**: Multilevel Inverters
- **FC**: Flying-Capacitor
- **ANPC**: Active Neutral Point Clamped

- **ABNPC**: Active Boost Neutral Point Clamped
- **CPC**: Charge Pumped Circuit
- **MPC**: Model Predictive Control
- **DBC**: Dead-Beat Controller
- **SMC**: Sliding Mode Control
- **HCC**: Hystresis Current Control
- **FC**: Flying-Capacitor
- **FCS-MPC**: Finite-Control-Set MPC
- **CCS-MPC**: Continuous-Control Set MPC
- **VOC**: Voltage Oriented Control
- **THD**: Total Harmonic Distortion
- **PLL**: Phase Locked Loops
- **SRF**: Synchronous Reference Frame
- **GVO**: Grid Voltage Observer
- **PI**: Proportional-Integrator
- **PR**: Proportional-Resonant
- **MVS**: Maximum Voltage Stress
- **QSC**: Quasi Soft Charging
- **LDT**: Longest Discharging Time
- **RSS**: Redundant Switching State

CHAPTER 1

INTRODUCTION

1.1 Recent Advances on Grid-Tied Transformerless Inverters

The integration of intermittent renewable energy (RE)-based resources, e.g., PV arrays, fuel cells, batteries and wind turbines in power grids and the new policies of the governments to reduce the need for fossil fuels dependent energy generation have accelerated the necessity of efficient and reliable energy management in a multigeneration source network [1]. As for the low power-scaled single-phase grid-tied utilities, a PV panel is directly connected to a power electronic converter within a single or two stages operation as illustrated in Fig. 1.1. Maximum power point tracking (MPPT), active power decoupling (APD), grid current control regulation, PV voltage amplification, islanding detection and the power quality enhancements are some crucial and strict missions, which must be taken into account in designing any new breed of grid tied-AC module (GT-ACM) systems [2].

In two-stage power conversion systems, utilization of the front-end dc-dc boost or buck-boost converter is imperative as the MPPT operation even with presence of a wide varying dc link voltage in the PV string modules is facilitated [3]. Moreover, in case of having a low available dc voltage magnitude, a voltage boosting feature can be added to the entire power conversion process in order to meet the peak voltage requirement of the grid. Applying APD in single-phase grid-connected applications [4],[5], and drawing

a continuous input current from the dc source are other important missions of these front-end boost converters. Depending on the working region, size of passive elements and the demanded range of voltage boosting feature in such a front-end dc-dc converters, the overall efficiency of whole the dc to ac power conversion process is affected [6]. Such a two-stage system is usually connected to the grid via a line transformer, since it can provide a galvanic isolation between the grid and the dc-side.

On the other hand, by removing the dc-dc front-end converters in the conventional types of GT-ACM, the PV voltage that is usually between 23 to 38 V at the rated power of 160 W, has to be enhanced through either a low-frequency (LF) back-end or an embedded high frequency (HF) transformer to meet the peak amplitude voltage requirement of the grid. In both these cases, the overall conversion efficiency of the system is affected due to additional core losses of the transformer although in case of HF-transformer-based solution, the systems weight and size can be still kept low [2, 6]. The overall configuration of trasformer-based energy conversion solution has been illustrated in Fig. 1.2. In case of using an embedded HF transformer, different types of flyback dc-dc converters or any of boost-integrated isolated converter are used, while the dc-ac stage can be any types of commercially available two or three-level (3L) voltage source inverters. Herein, although the embedded HF transformer in the dc-dc stage can possess a small size, the passive components for the filter interfaced design is still large since the number of inverter output voltage levels is limited to two or three.

To improve the overall efficiency and power density of the entire system, PV grid-tied inverters with the transformerless (TL) circuit configuration have been more popular during the latest years. However, detaching the galvanic isolated transformer, while using the conventional 2L or 3L inverters in the back-end dc-ac stage contributes to the following challenges:

- Variable common mode voltage (CMV) and in turn the ground leakage current problem.
- Requiring another power processing stage to cope with meeting the minimum grid voltage amplitude requirement whilst utilizing a relatively low value of the input dc voltage.
- And power quality enhancement (PQE) issue.

The main challenge in designing a suitable TL-based GT-ACM is to take some additional measures from the grounding issues viewpoint. Here, the parasitic

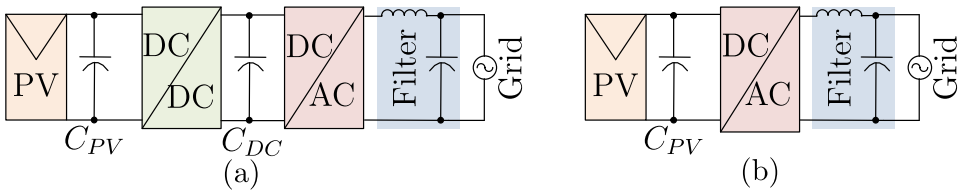


Figure 1.1: The overall configuration of power conversion system based on (a) two-stage platform, (b) single-stage platform [2].

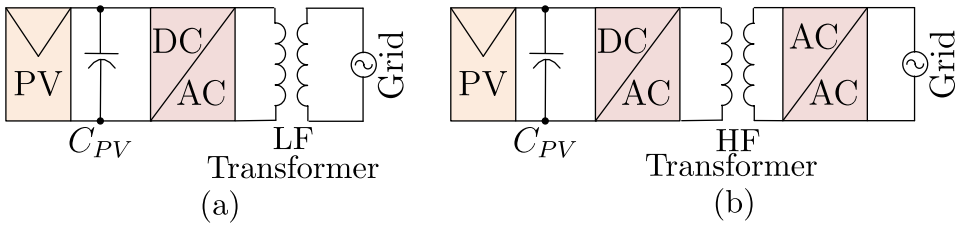


Figure 1.2: Examples of transformer-included inverter solutions based on (a) Line-frequency (LF) transformer, (b) embedded High-frequency transformer [2].

capacitance provided by the negative terminal of the PV panel, which is around 100 nF per 1 kW, causes a resonant path with the output ac side filter and therefore the leakage current is propagated through the inverter [7]. The value of the leakage current in the grid must be limited to under 30 mA based on the NEC 690 and VDE 0126-1-1 IEEE standards [8], where a leakage current over 0.3 A must trigger the break to isolate the TL-inverter from the grid. This parasitic dc current degrades the quality of the injected current and also may saturate the core of other transformers in the distribution network. Since the major element in generating the leakage current is the variable HF-CMV of the GT-ACM at the inverter side, various efforts have been recently put forward to address this issue [9]. From the topological point of view, there have been three main categories of the TL inverters with different capabilities shown in Fig. 1.3, e.g., Freewheeling-based TL-inverters, mid-point-clamped-based TL inverters and the common-ground (CG)-based TL inverters. The characteristics of different grid-tied TL inverters is assessed based on the their capability in reduction on the value of the leakage current, number of output voltage levels, and voltage boosting feature within a single or double-stage platform. Additional parameters like number of required power switches, capacitors, gate drivers, inductors, maximum blocking voltage across the switches, total standing voltage (TSV) across the switches, ability to work in boost mode with a switched-capacitor (SC) or switched-boost (SB) technique, and overall efficiency can also be considered to have a comprehensive evaluation of different topologies. In following sub-sections, each of these topological categories are briefly introduced. Moreover, the major challenges over the SC-based converters are discussed.

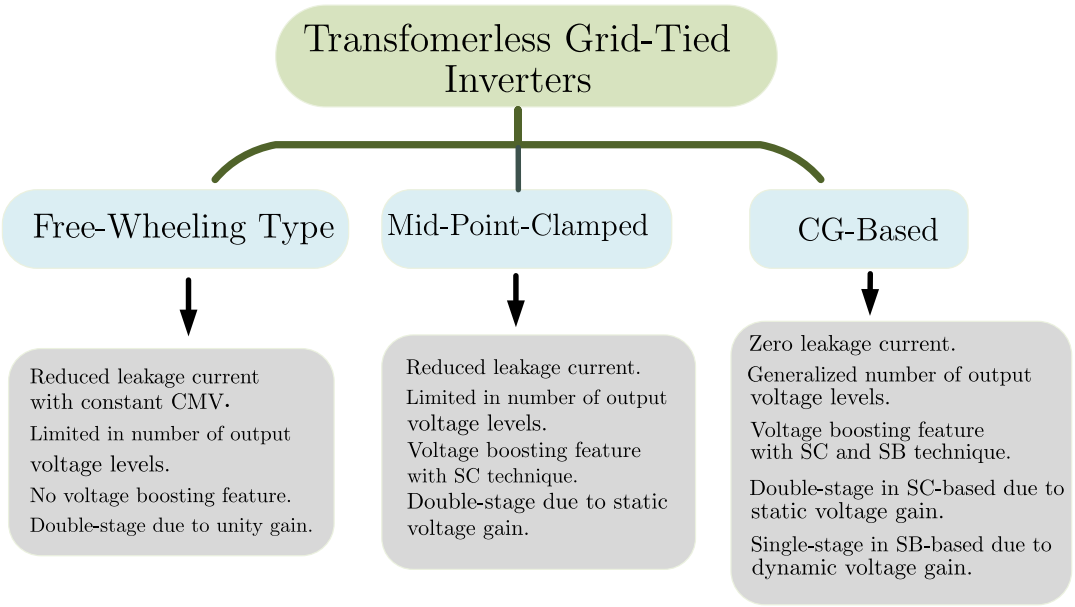


Figure 1.3: Categorization of the TL-based grid-tied inverters.

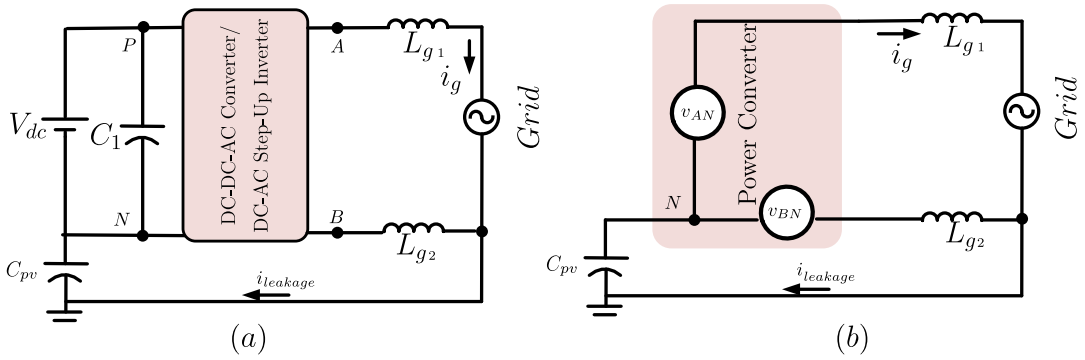


Figure 1.4: Common-mode model for single-phase grid-connected inverter: (a) Full model, (b) simplified model [10].

1.1.1 Freewheeling-Based TL-Inverters

Once the transformer is removed from the inverter and the grid, a resonant circuit between the negative terminal of the input dc source and the null of the grid is formed as shown in Fig. 1.4(a). This resonant circuit includes stray capacitance, C_{pv}, the filter inductors, L_{g1} and L_{g2}, and the leakage current, $i_{leakage}$. Here, the power converter is represented by a block with four terminals to allow a general representation of various converter topologies. On the dc side, P and N are connected to the positive and negative rail of the dc-link, respectively; while on the ac side, terminals A and B are connected to the single-phase grid via filter inductors. From the view point of the grid, the power converter block shown in Fig. 1.4(a) can be considered as voltage sources, generating voltages v_{AN} and v_{BN}. Hence, regardless of the circuit structure, this power converter

block can be simplified into the equivalent circuit, which consists of v_{AN} and v_{BN} as shown in Fig. 1.4(b) [10]. The leakage current is thus a function of v_{AN}, v_{BN}, the grid voltage, filter inductance, and the stray capacitance, C_{pv}. Since v_{AN} and v_{BN} possess HF switching functions of the inverter output voltage, the impedance of the resonant path can also be related to the switching frequency, f_{sw}. Considering $L_{g1} = L_{g2}$, in Fig. 1.4(b), the CMV can be represented as $\frac{v_{AN}+v_{BN}}{2}$, which appears across C_{pv} and can generate the leakage current.

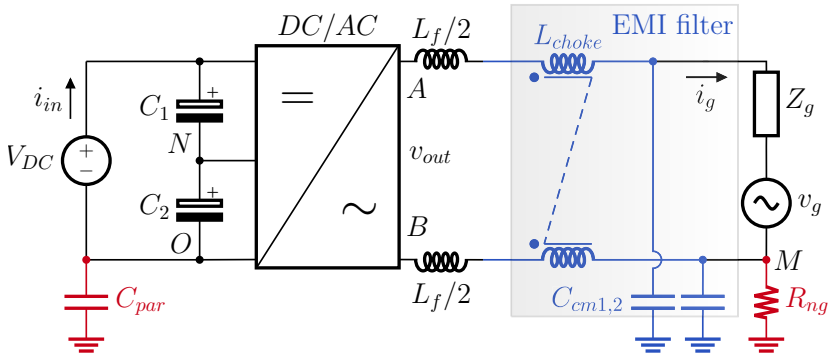


Figure 1.5: A simplified structure of the grid-connected TL inverter with CM-filter.

In case of adopting any conventional types of 2L or 3L inverters, in which their output voltage is to be measured with respect to the inverters legs voltage, i.e., terminals A and B, the CMV attenuation can be performed by employment of relatively small common-mode (CM) filters as shown in Fig. 1.5. In this case, determination of the leakage current path impedance leads to choosing the carrier/switching frequency of the pulse width modulation (PWM) signals for operating outside the resonance region. The overall CMV can also be constant during each switching instant by the means of bipolar PWM schemes and using an half-bridge based TL inverter [11]. However, such bipolar 2L output voltage causes undesirable switching losses and impacts thereby the injected grid current quality [10]. Half dc-link voltage utilization at the ac side of the inverter is another shortcoming of such a half-bridge (HB)-based circuit. Hence, as for low available dc voltage source magnitude, the system becomes two-stage and the front-end dc-dc boost converter must work within a larger value of the dc duty cycle. This causes additional power loss and can sacrify the overall conversion efficiency, thereby.

Decoupling the PV source from the ac grid during the freewheeling period in unipolar 3L-PWM schemes is one of the well-known approaches to alleviate the leakage current value. Herein, H5 [12] and HERIC [13] converter are based on a floating CMV in the freewheeling period (zero-level of the output voltage), while different types of H6 family

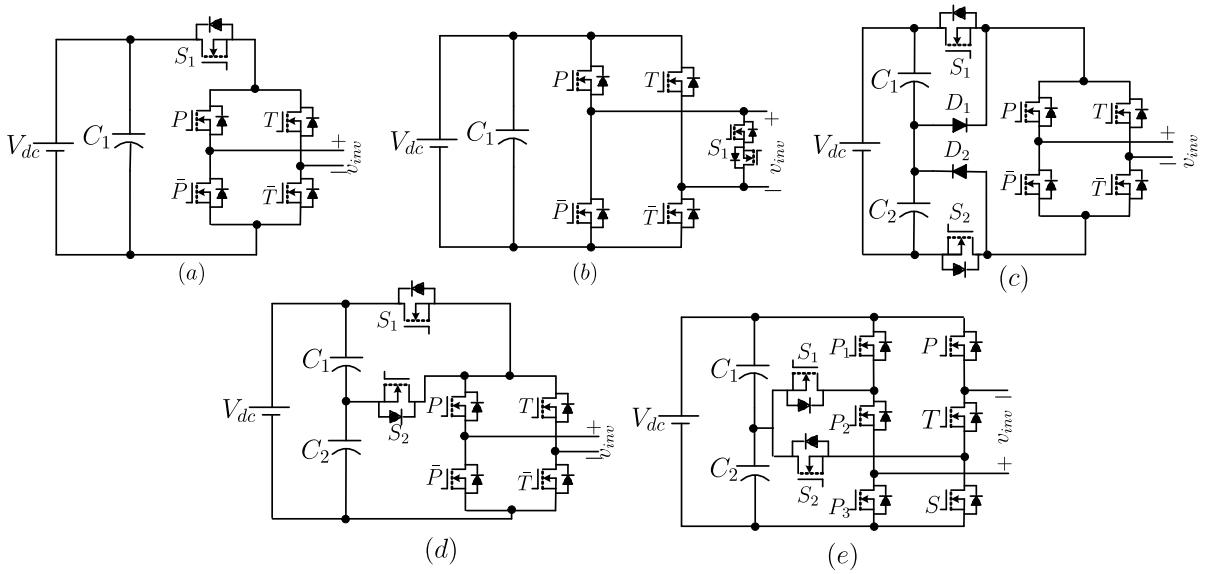


Figure 1.6: Full-bridge based topologies for TL grid-tied inverters (a) H5 [12] (b) HERIC [13] (c) H6 with DC bypass [14] (d) OH5 [17], and (e) PN-NPC [18].

[14–17], optimized H5 (OH5) [10], the positive-negative neutral point-clamped (PN-NPC) [18] and Dual buck [19] TL-inverters are able to clamp the overall CMV on the half value of the input dc source at each switching instant. Within the same concept, a new variant of H8-TL inverter has also recently been put forward [20], which is able to generate five-level (5L) output voltage waveform with a constant CMV per each switching instant. Motivated by the concept of multilevel inverters (MLIs), the inverter output filter size of the above-mentioned transformerless inverters can be reduced remarkably leading to further improving the power density/overall efficiency with a quality ac voltage waveform [21]. Herein, the 5L-inverters proposed in [22, 23] have used 12 power switches to attain all the possible output voltage levels with a constant HF-CMV. A combination of T-Type and HB leg introduces another 5L inverter in [24] in which its HF-CMV is not constant but varied within half and one-quarter of the main dc-link voltage. Some of the most well-known structures of such topologies have been depicted in Fig. 1.6 with the capability of 3L output voltage generation with relatively constant CMV. Regarding these newly developed TL inverter topologies, the leakage current can be mitigated but with the cost of employing additional power switches. Conversely, it is apparent that in case of having a low and wide varying dc voltage, all these topologies require a front-end dc-dc converter as discussed earlier. Moreover, owing to the junction parasitic capacitors of the involved power switches, the overall value of the leakage current is reduced but never totally suppressed.

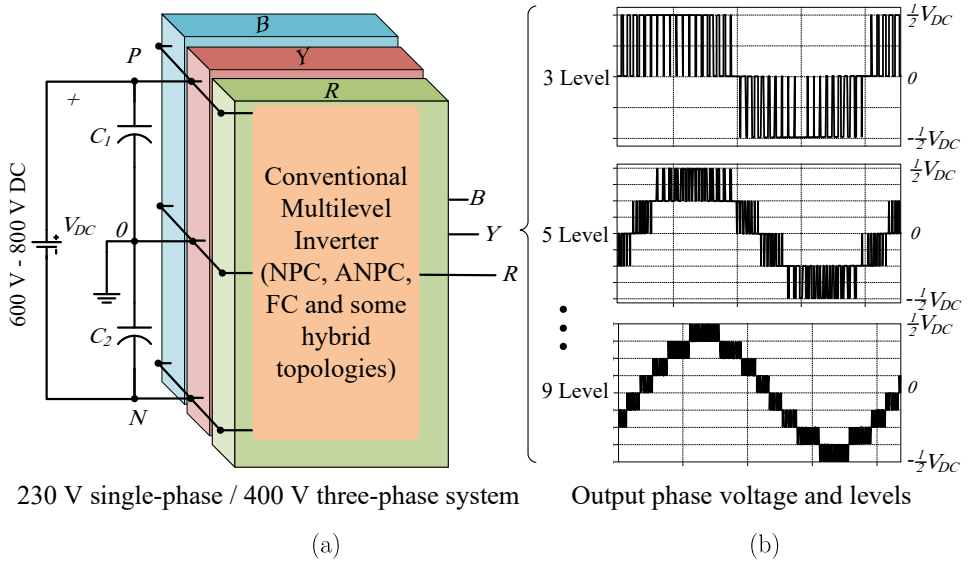


Figure 1.7: Circuit illustration of conventional TL-inverters with mid point-clamped technique [25].

1.1.2 Mid Point-Clamped TL-Based MLIs

Mid point-clamped TL-inverters with the dc-bus capacitors as the neutral point of the inverter with respect to the null of the grid are also capable of mitigating the undesirable value of the leakage current whilst generating multilevel output voltage waveform is possible. Hence, they can also improve the PQE constraints of the available grid-tied TL-based inverters. A schematic circuit diagram and the typical multilevel output voltage waveforms of such types of TL-based inverters has been illustrated in Fig. 1.7(a) and (b). In this case, HB or NPC inverters are usually utilized and the converter can be operated even for three-phase system with the single-dc source concept. Since, in the conventional types of such structures, e.g., conventional flying capacitor(FC)-MLIs, active neutral point-clamped (ANPC)-MLIs and T-Type-based MLIs, the maximum magnitude of the inverter output voltage is confined with half value of the main dc-link voltage, the PV voltage as the available dc source must be doubled through the front-end step-up dc-dc converters to meet the grid voltage amplitude requirement [11, 26]. Here, the bipolar and unipolar PWMs are, respectively, used for the HB and NPC inverters. Hence, 2L and 3L output voltage can be created for them, respectively. The advanced version of such types of TL-inverters named as active boost neutral point clamped (ABNPC) inverter can somehow address this drawback by integrating the FC and/or SC cells into the conventional basic designs of the ANPC-based TL inverters [25, 27]. Pure SC-based switching circuits contain several capacitors, power switches and/or diodes that can convert the available fixed dc-link voltage to generate multilevel voltage using a

series-parallel switching conversion technique. The integrated capacitors are charged directly through the parallel connection with another voltage source (input dc-source or another charged capacitor). A discrete output voltage can be generated by discharging the capacitor(s) in series or parallel fashion with or without the input dc-source. Such a single-stage inductorless/transfomerless switching operation creates a voltage step-up feature with a self-voltage balancing for the involved capacitors and make SC-MLIs a valuable and interesting solution for many new applications [28]. Inclusion of SC-based switching circuit techniques into the dc-dc converters have already been widely studied in the literature and commercialized in industry [28]; however, such integration for multilevel ac-voltage generation applications are emerging and worth investigating. Herein, larger number of output voltage levels, e.g., 5L, or seven-level (7L) variants can be achieved by adding a T-Section into front-end side of conventional topologies [27]; however, the voltage boosting factor of such types of TL-MLIs is still limited to a certain static value, e.g., two-times or three-times. Hence, additional front-end boost-based converter with extra active and passive elements is still needed in case of dealing with the low and wide-varying dc voltage available as the output voltage of PV panels. Therefore, the energy conversion stage of the system is still double and in turn the overall efficiency is prone to be degraded. Some of the recently proposed structures of such types of ABNPC-based TL-MLIs are depicted in Fig. 1.8(a)-(e).

The ABNPC TL-inverter shown in Fig. 1.8(a) can generate 5L output voltage with six power switches and unity voltage conversion gain. Here, the SC-integrated switches designated as P, can be either RB-IGBT or four-quadrant power switch [25], while C_{FC} is charged to the main dc-link voltage during the middle positive/negative output voltage level generation, i.e., $\pm Vdc/2$. To extend the number of output voltage levels as well as the overall voltage gain of the converter, [29] has proposed two different circuit configurations for the mid-point-clamped SC-MLIs. The first structure is illustrated in Fig. 1.8(b). C_{FC} is balanced at the input dc-source voltage through the highlighted current flowing path, while the number of inverter output voltage levels is seven with 1.5 times overall voltage conversion gain. Replacing C_{FC} and the HB-leg with a T/NPP cell constitutes to nine-level (9L) and eleven-level (11L) ABNPCs with unity and 1.5 times voltage conversion gain, respectively as shown in Fig. 1.8(c), while additional capacitors charged to half voltage value of the main dc-link voltage with the help of the highlighted T-section circuit. Integration of the SC-voltage doubler unit into a mid-point-clamped four-level (4L) inverter has also been introduced in [30, 31], while single and three-phase design of the converter are the target, respectively, as shown in Fig. 1.8(d). A unity ratio

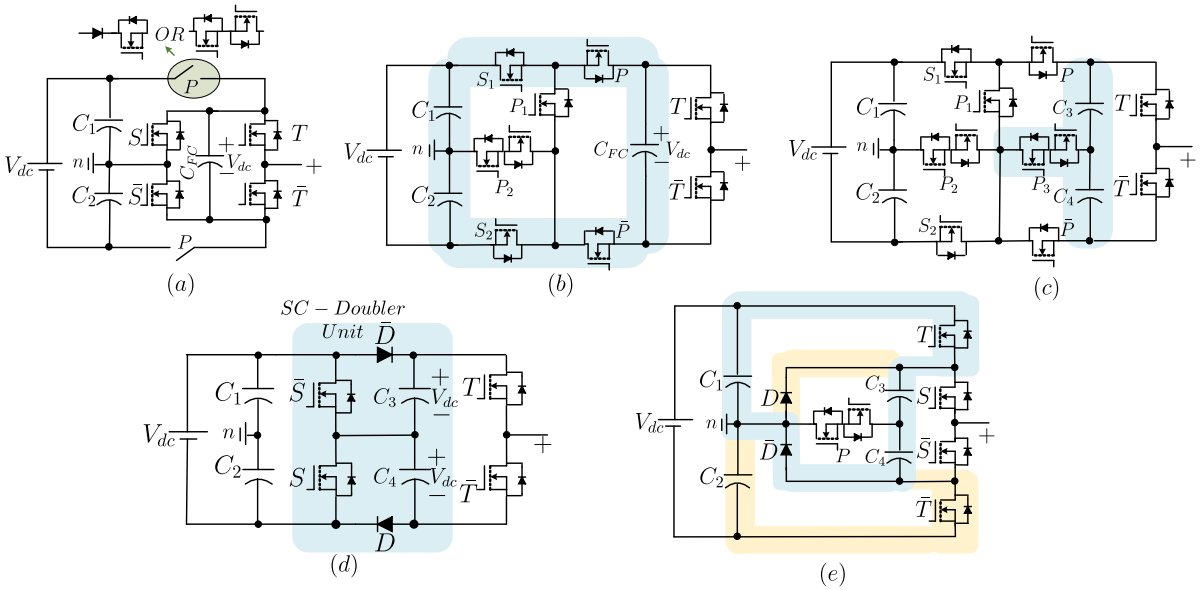


Figure 1.8: ABNPC-based TL inverters (a) 5L-ABNPC [25], (b) 7L-ABNPC [29], (c) 9L-ABNPC [29], (d) 4L-ABNPC [30], and (e) 5L-ABNPC [32].

between the number of inverter output voltage levels and number of required switches as well as a single-stage 1.5 times overall voltage conversion gain are two important features of this topology. The concept of adding an T-section cell to any conventional types of ANPCs to achieve larger number of output voltage levels with full dc-link utilization is also introduced in [27]. An example of this technique is shown in Fig. 1.8(e), where two capacitors, C_3 and C_4, with a four-quadrant power switch, P, are inserted into the conventional 3L-NPC based inverter, and five output voltage levels are achieved [32]. Regarding the blue and yellow highlighted colours in Fig. 1.8(e), it can be discerned that these two added capacitors are charged to the voltage across C_1 or C_2 through the integration of the existing diodes and the switches T and $\bar{T}$.

1.1.3 CG-Based TL-MLIs

Alternatively, CG-based TL inverters is a recently developed configuration to almost fully suppress the leakage current concerns through bypassing the CMV across C_{pv}. In this case, the negative terminal of the input dc supply and the neutral point of the grid are connected to each other; therefore, C_{pv} is short-circuited the ground leakage current is fully suppressed. The CG-based TL inverters with a unity static voltage gain have been extensively elaborated in [33–37], where a virtual dc-link capacitor is needed to be charged in one half-cycle of the grid voltage and deliver its voltage to the output in another half cycle. In such cases, the maximum number of inverter output voltage levels,

which is an important factor from PQE viewpoint, is only two or three. Regarding such a mentioned virtual dc-link capacitor, the positive and negative sequence output voltage generation principles are different and a charge pumped circuit (CPC) theory is needed to make a true AC waveform. Hence, the CPC facilitates two different current flowing paths for the CG-TL inverters during the operation in positive and negative half-cycle. In most of recently rehearsed topologies, different types of SC integrated circuit are used to form an CPC and generate output voltage levels with a single dc-source [28]. Regarding this concept, [33] presented a virtual dc bus as a CPC shown in Fig. 1.9(a), where five power switches are integrated with a unipolar PWM and 3L output voltage is achieved. Another scheme of CPC-based 3L-CGSC-based TL-inverter has been proposed in [34], yet additional power diodes are needed to provide an indirect charging operation for the virtual dc-bus through a diode-assisted CPC cell. The number of switching devices for this type of 3L-CGSC-based inverter is reduced in the presented $Siwakoti$-H inverters in [35] as shown in Fig. 1.9(b) and (c), while an extra diode has been used in Type-I of this converter and two RB-IGBTs are used in its Type-II variant. The common feature among all these mentioned 3L-CGSC-based inverters is their unity voltage conversion gain. Having taken Fig. 1.9(d) into account, a double-voltage conversion gain 3L-CGSC-based inverter is proposed in [36], while six power switches, a diode-assisted CPC cell and a series-parallel switched-capacitor (SPSC)-unit are employed. Here, C_2 and C_3 are charged to $2V_{dc}$, which is the boosted voltage value of the frond-end series-parallel SPSC unit. In this context, two other similar boost-based topologies of 3L-CGSC-based inverters are also proposed in [37, 38] with more number of power switches and elevated switch voltage stress.

Following this, [39] has merged the virtual dc-link concept of a conventional four-switch based FC-leg to realize a 5L inverter with CG-circuit feature as shown in Fig. 1.9(e). In this case, the charging/discharging operation of C_1 is realized in a fully soft fashion using the load current path similar to the FC-based MLIs. However, like other virtual dc-link based CGSC-MLIs, C_2 must be charged to peak voltage value of the inverter output voltage, which is equal to V_{dc}. Even though using only six power switches, the proposed topology does not provide voltage boosting feature. Herein, a relay, S_P with a parallel resistor, R_P, is used in the charging path of C_2 to attenuate the large charging current at the start-up moment of the operation.

Another reduced switch-count 7L-CGSC-based inverter is presented in [40] as shown in Fig. 1.9(f). Similar to the above-mentioned 5L-CGSC-based inverters presented in [44–47], this structure is also based on virtual dc-link concept, where capacitors, C_1,

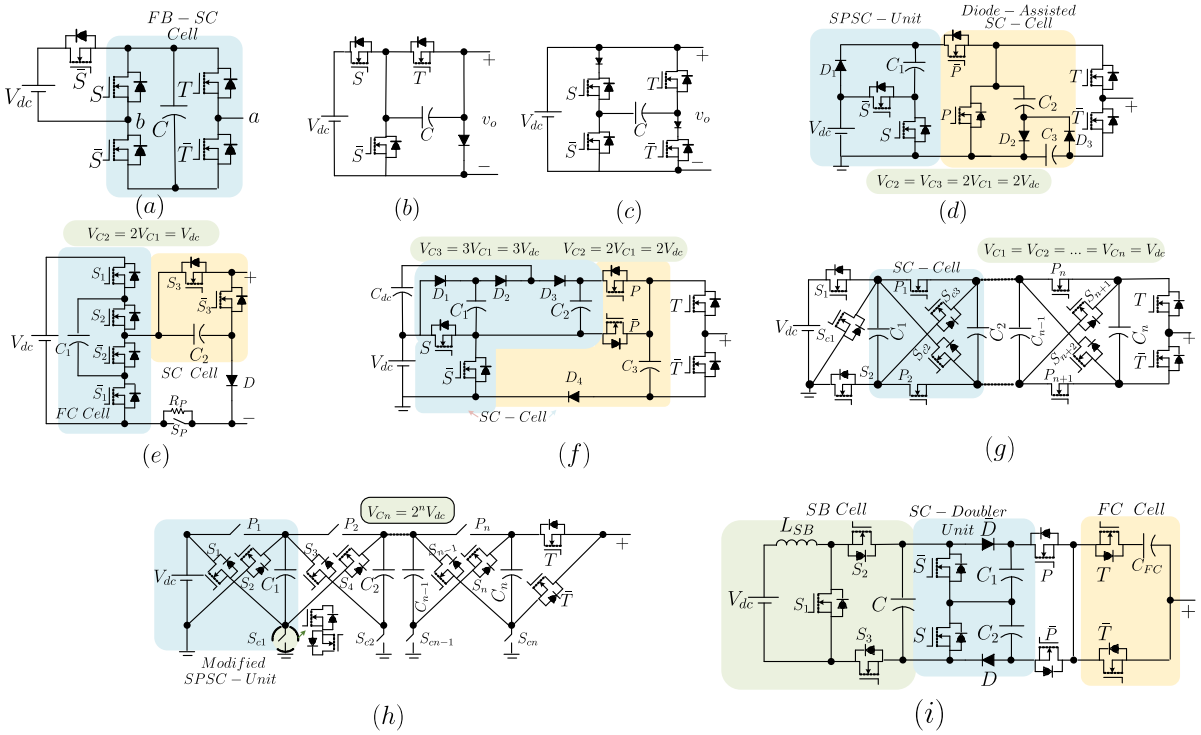


Figure 1.9: Different CGSC-Based TL MLIs presented in (a) [33], (b) and (c) [35], (d) [36], (e) [39], (f) [40], (g) [41], (h) [42], and (i) [43].

C_2, and C_3 are charged to V_{dc}, $2V_{dc}$, and $3V_{dc}$, respectively, to synthesize all the 7L inverter output voltage with a triple voltage gain. Although the number of required power switches is only six, it requires 4 additional power diodes. In this case, the charging path of C_3 is through the series connection of the input dc-source and capacitor, C_2. Similar to the presented 5L-CGSC-based inverters in [44–47], this charging operation is possible during the zero and the top positive output voltage levels, $+3V_{dc}$, generations. Moreover, the dc-link capacitor, C_{dc} is charged and discharged by the load current direction in positive and negative half cycle of the output voltage. Therefore, these long discharging cycles may demand a larger capacitance for both C_{dc}, and C_3 to alleviate the voltage ripple across the capacitors. Having taken the advantages of this reduced switch-count CGSC-based inverter, [48] has developed a 9L mid-point-clamped inverter with nine power switches, as well. In this case, the front-end SC-based part of [40] is combined with the idea used in [49], while a four times voltage conversion gain is achieved. As a counterpart, another 7L-CGSC-based inverter with triple-voltage conversion gain, eight switches, and four power diodes is proposed in [50], which is based on series connection of the front-end SPSC Unit-I and the SC-voltage doubler unit. Although the number of switching devices in this topology is larger than [40], i.e., eight versus six, its number of

required capacitors is three, while the maximum balanced voltage across them is $2V_{dc}$, which leads to the reduced voltage stress and TSV indexes of the converter.

Concerning Fig. 1.9(g) and (h), two other generalized CGSC-based MLIs have been proposed in [41, 42], respectively. Herein, the proposed topology in [41] is based on cross-connected switches, where the voltage across all the involved capacitors are equal to the input dc-source in spite of having a voltage boosting feature. Therefore, this topology is performed based on symmetrical voltage balancing operation of the capacitors. To asymmetrically charge the voltage of the capacitors with a generalized CGSC-based MLIs, [42] has proposed another topology shown in Fig. 1.9(h). This asymmetric topology helps to generate $(2^{n+1}-1)$-level of the output voltage with $6n$-number of required power switches, where n implies the number of required capacitors. Herein, the binary charging operation of the capacitors leads to generate larger number of output voltage levels with larger value of the voltage conversion gain and a reduced number of switching devices. Although the concept is interesting, asymmetrical charging operation of the capacitors in CGSC-based MLIs may be deleterious since the number of redundant switching states (RSSs) to generate the same levels of the output voltage is reduced, while the voltage ripple performance of the capacitors might be adverse.

TL-based MLIs with the CG concept can also possess either static or dynamic voltage boosting feature. In the static case, the SC technique is usually used leading to a discontinuous input current with a large value of the capacitive inrush current [33]-[50]. As for the dynamic voltage boosting case, an inductor is utilized as the SB module, and therefore, the input inrush current problem can be significantly alleviated, whilst the converter can convert a boosted 3L [51, 52] or 5L [53] output voltage waveform to the output within a single-stage energy conversion configuration. Fig. 1.9(i) show an CGSB-based TL-based MLIs presented in [43] with the capability of 9L output voltage generation. Herein, the role of the SB cell is to give a dynamic voltage boosting operation to the capacitor, C, with a fixed boost dc duty-cycle of d, while both the SC-voltage doubler unit and FC cells can generate additional output voltage levels as discussed earlier.

Regarding this, CG-based TL-inverters are chosen as the major focus of this research to further improve their circuit characteristics in terms of enhancement in the number of output voltage levels, extension in the output voltage conversion gain with either static or dynamic voltage boosting operation, reduced voltage and current stress on devices and overall power density/efficiency improvement.

1.1.4 Challenges Over the SC-based MLIs

The charging operation of the capacitors in the pure SC-based basic units causes a sort of challenges/limitations for almost all the discussed SC-MLIs. Large pulsating current during charging operation increases the current stress profile of the switches involved in the charging path that deteriorates the overall efficiency of the converter. In addition, significant capacitor voltage ripple not only aggravates the pulsating current issue, but also causes distortions in the output ac-voltage. These issues might be more severe when multiple SC-based basic units are cascaded to each other to realize higher voltage conversion gain in the SC-MLIs since the top positive/negative output voltage levels are made by discharging operation of all the capacitors in series. To minimize switch count, majority of the existing SC-MLIs are lacking redundant switching states (RSSs) that could be useful for reducing the longest discharging time (LDT) of the capacitor voltage via hybrid PWM. Hence, optimization of these converters to achieve high power conversion with an improved overall efficiency is an imperative task.

To elaborate this capacitor voltage ripple and pulsating charging current issues, a simplified equivalent circuit considering parasitic ON-state impedance of this capacitive charging loop, Z_{ch}, for any SC-based basic unit is shown in Fig. 1.10(a). Considering different voltage levels for C_1, and C_2 during the switching operation and assuming V_1, and V_2 as the capacitors initial stored voltages while $C_1 \gg C_2$, a power loss caused by this hard charging operation occurs as given in (1.1) [54, 55]:

$$P_{loss} = \frac{1}{4} C_2 (V_1 - V_2)^2 f_{sw} = \frac{1}{4} C_2 \Delta V^2 f_{sw}. \tag{1.1}$$

where, f_{sw} is the PWM switching frequency of the switch S, which represents the role of charging path switches in the SC-based circuits. This type of power loss refers as the ripple loss of capacitors in the SC-MLIs and is dissipated in the parasitic impedance of the SC charging path. This ripple loss is not dependent on the value of this parasitic impedance, and instead, it hings on the initial voltage difference of the capacitors, which comes at the cost of the charge transfer between the capacitors. Hence, the ripple loss of capacitors is proportional to the charge drawn by the load and inversely proportional to the capacitor values [54]. Moreover, the change of charge in the capacitor is proportional to the duration of the charge/discharge and, thus, is inversely proportional to the switching frequency as [54]:

$$\Delta V \propto \frac{1}{f_{sw}}, \frac{1}{C_{eq}} \tag{1.2}$$

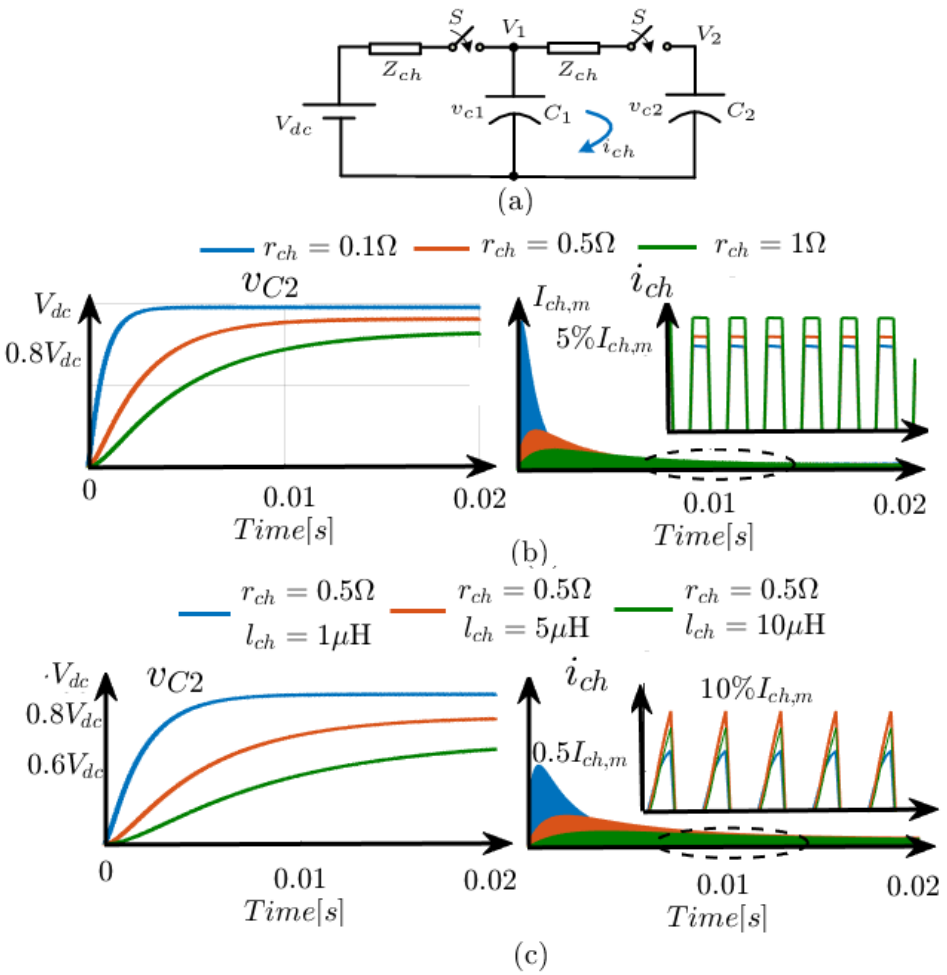


Figure 1.10: (a) A typical capacitive charging path circuit for SC-based converters, (b) the voltage of the capacitor and the charging current of the loop for a pure SC-based converter, and (c) the voltage of the capacitor and the charging current of the loop for the SC-based converter with QSC operation [28].

where, C_{eq} is the equivalent capacitance of the charging path. Hence, with respect to (1.1) and (1.2), we can say, P_{loss} is inversely proportional to f_{sw}, and C_{eq}. This is the reason why to reach higher portion of the output power, larger capacitance of the capacitors is needed. Also, it can be discerned that why the performance of SC-MLIs in high frequency applications is much better than their counterpart in 50 Hz application [28].

As for a pure SC-based basic circuit, the parasitic inductance of the path caused by the layout design of the converter is negligible. Therefore, only an equivalent charging resistance, r_{ch}, related to the parasitic ON-state resistance of the charging path switch(es) and ESR of the capacitor(s) is predominant. Depending on the values of r_{ch}, and f_{sw}, a very large discontinuous charging current, i_{ch}, is seen when the switch S is ON, which not only is deleterious for the lifetime of the switches and the capacitors but also can propagate EMI concern with a false turned-ON operation for even those switches that

are not involved in this SC charging path. Herein, a complete charging process within a so-called fast switching limit (FSL) occurs as long as f_{sw} is to be larger than the critical frequency of this pure SC-based circuit, e.g., $f_{sw} > \frac{1}{2\pi r_{ch} C_{eq}}$. Else, the charging operation of the SC-based converter would not be completed and it works within a slow switching limit (SSL) performance, which is not desired and can even cause larger value of the charging current spike/inrush current [54]. Having considered the FSL region and a constant 50% high frequency duty cycle for switch S, the effects of different usual values of r_{ch} on the voltage stress across C_2 and on i_{ch} can be seen in Fig. 1.10(b). As can be realized, the smaller value of r_{ch} cannot reduce the P_{loss} mentioned in (1.1) since the total power loss in each switching cycle remains the same. In contrast, it can only shorten the capacitor voltage settling time with a larger peak value of i_{ch} ($I_{ch,m}$). It must be noted that this problem in actual case study of SC-MLIs is more significant since the duty cycle of charging path switches is not constant and it follows a sinusoidal trend.

A solution for this concern is to optimize the SC-based converters from hard charging to soft charging [54–56] or quasi-soft charging (QSC) operation. As for the SC-based dc-dc converters, where the duty cycle of high frequency switches is constant, inserting a very small value of the charging inductor, l_{ch}, in series with the charging loop of the SC converter is useful in realizing fully soft charging operation. The importance of different values of l_{ch} on both the capacitor voltage and i_{ch} can be observed in Fig. 1.10(c). Although it can considerably reduce $I_{ch,m}$, it may affect the dynamic response of the capacitor voltage and even in case of larger value of l_{ch}, it can cause a voltage drop problem across the capacitor. As for a proper FSL operation, the condition of $f_{sw} > \frac{1}{2\pi\sqrt{l_{ch} C_{eq}}}$ must be fulfilled [54]. Although this concept might be propitious for the SC-based dc-dc converters [55], achieving a fully soft charging operation in SC-MLIs is still challenging owing to the variable ac duty cycle of charging path switches. In this case, the equivalent RLC circuit for the charging loop of most of the SC-MLIs operates within a over-damped oscillation region since the ratio of $\frac{r_{ch}}{2}\sqrt{\frac{C_{eq}}{l_{ch}}}$ is always greater than one in practice.

Although in most of the cases, adding this small parasitic inductance in the charging path of switches is workable to mitigate the current stress, it cannot still address the LDT problem of the capacitors in many SC-MLIs case studies. In this regard, the type of modulation strategy and the importance of having the RSSs are important. As opposed to the other well-known types of MLIs like modular multilevel converters (MMCs) or ANPC/FC-based MLIs, the switches of the SC-MLIs must be driven using the well-known level-shifted-sinusoidal pulse width modulation (LS-SPWM) technique. This comes at the cost of imperative parallel charging operation of SCs during the output voltage

level generation. The LDT of the capacitors in LS-SPWM technique can be controlled by decreasing the maximum value of the modulation index, M. In this regard, it is more preferable to have a structure which is able to charge/discharge the C_{FC} in every switching cycle. As given in the 5L-ABNPC-based structure presented in [25] [see Fig. 1.8], the maximum value of the charging current is reduced using the following expression:

$$I_{ch,m} \approx \frac{M}{1-M}\frac{1+\delta}{1+2\delta}I_m. \tag{1.3}$$

where, I_m is the maximum value of the load/output current, and δ is a constant ratio as $\frac{C_{FC}}{C_1}$.

Although this approach is helpful to realize a highly efficient converter in higher ratio of the output power, it limits the modulation index. An alternative solution is to add $1/6^{th}$ of the third harmonic order in the reference signal of LS-SPWM [57] for three-phase system. Using this technique, the LDT is reduced, while only the fundamental harmonic content can be seen in the line output current/inverter output voltage.

1.2 An Overview of Major Closed-Loop Control Techniques for Single-Phase Grid-Tied TL-Inverters

Advanced power control strategies for single-phase converters imitate the concept of decoupled active and reactive power control of three-phase converters, which is realized in the synchronous reference frame. In this way, the ac current is decoupled into active and reactive power components, I_d and I_q, respectively. These current components are then regulated in order to eliminate the error between the reference and measured values of the active and reactive powers. In most cases, the active power current component, I_d, is regulated through a dc-link voltage control aiming at balancing the active power flow in the system. By comparing the reference and measured currents, the current controller should generate the proper switching states for the converter to eliminate the current error and produce the desired ac current waveform. The performance of the converter mostly depends on the quality of the current control strategy.

In general, different single-phase closed-loop control strategies can be categorized into four main divisions as the direct current control (DCC), voltage-oriented control (VOC), Proportional-Resonant (PR) control and direct power control (DPC). The goal of all these

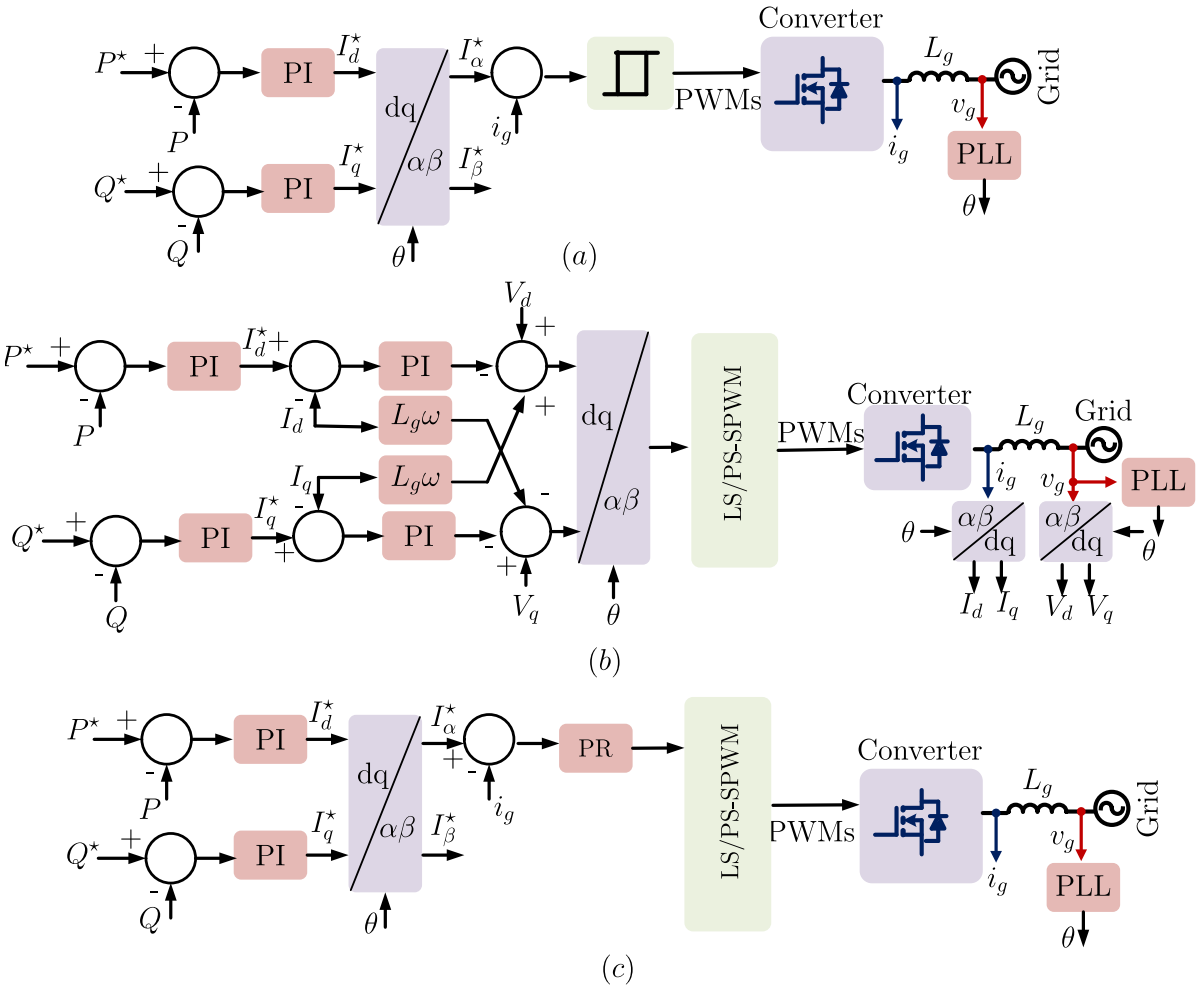


Figure 1.11: Simplified block-diagram of (a) HCC, (b) VOC and (c) PR-based control of single-phase grid-tied converters [58].

closed-loop control techniques is to inject a fully-controlled current (power) to the grid under various dynamic condition of the input dc source, demanded active/reactive power by the grid and even under the presence of grid voltage disturbance. DCC-based strategies aim to directly control the injected current of the TL inverter while making all the possible output voltage levels. Dead-beat controller (DBC) [59], model predictive control (MPC) [60], peak current controller (PCC) [61], sliding mode control (SMC) [62], and the hysteresis current control (HCC) [63] are the major branches of DCC-based strategies. Herein, the converter can be operated either with the fixed switching frequency (with PWM modulator e.g., level-shifted (LS) or Phase-Shifted (PS)-PWM strategies) or with a variable switching frequency (Without the modulator). Finite-control-set MPC (FCS-MPC), finite-control set-SMC (FCS-SMC) [64], the PCC technique, and the HCC strategy all are working based on the variable switching frequency, whereas, DBC, continuous-

control set-MPC (CCS-MPC) [65], and CCS-SMC [66] are designed based on an optimal closed-loop duty cycle calculation and with a fixed value of the switching frequency operation. In this case, DBC method, MPC and SMC approaches highly depend on the system parameters, while HCCsolution can show some robustness against the uncertain conditions of the system parameters.

A role example of HCC procedure applied to the single-phase grid-tied system has been illustrated in Fig. 1.11(a). The HCC is one of the easiest control strategies, in which, the ac current is controlled to stay within the limits of an upper and lower bands around the sinusoidal reference current. For this purpose, the hysteresis controller is used which is simple and provides a high dynamics. The output of the hysteresis controller is the converter switching states, so in HCC there is no PWM modulator block, which simplifies the structure and improves the dynamics. Despite the advantages of simplicity, robustness, good stability, automatic current limiting, and high dynamic response, the basic HCC suffers from major drawbacks such as, widely varying switching frequency and large current ripples. Indeed, the switching frequency depends on the hysteresis bandwidth, the sampling frequency, and system and load parameters and varies over a wide range. As a consequence, significant low-order harmonics are present in the ac current and it is important to carefully design the filter as well as the converter power stage. Besides, the high gain of the hysteresis controller may cause some control difficulties or power quality problems, especially when the filter inductance and/or the sampling frequency are small. It is worth mentioning that some advanced HCC structures have been proposed which use an adaptive band for the controller and could obtain a fixed switching frequency [63]. This is at the expense of deteriorated performance characteristics, such as increased current harmonic distortions, degraded dynamics and lower stability margins.

The voltage-oriented control or VOC is also a well-known method of indirect active and reactive current control and is based on the current vector orientation with respect to the line voltage vector. The VOC is realized in the direct-quadrature (dq) synchronous reference frame, where the error between the direct (I_d) and quadrature (I_q) components of the ac current and their reference values are fed to the proportional-integrator (PI) controllers. Then, the controllers generate the reference voltage for the converter. This voltage is applied to the converter using a PWM modulator. Compared with the HCC, the converter switching frequency is fixed and by using advanced modulation techniques, the switching losses, harmonic currents and total harmonic distortion (THD) can be minimized. Also, thanks to the internal current control loops, high dynamics and static performance is guaranteed. One main drawback associated to the VOC is that the perfor-

mance is highly dependent on the applied current control strategy and the connected ac network conditions. Fig. 1.11(b) shows the general platform of the VOC technique. As one can be seen, in the VOC strategy, electrical signals are all transformed to the synchronous reference frame, where quantities are dc and, as a consequence the zero steady-state error is ensured by using a conventional PI controller. This transformation needs at least two orthogonal signals. As a consequence, a fictitious phase must be generated. To create a two-phase system from a single-phase signal, different techniques can be employed, such as the transport delay, Hilbert transformation, all-pass filter (APF), and SOGI methods [67, 68]. In this case, a lot of synchronization techniques, for both single-phase and three-phase applications, are available in the literature. Thanks to their simplicity, robustness, and effectiveness, the phase locked loops (PLLs) are the most accepted ones.

Generally speaking, a PLL is a closed loop feedback control system, which synchronizes its output signal in phase, as well as in frequency, with the fundamental component of the grid voltage. Among various techniques, currently, the synchronous reference frame PLL (SRF-PLL) is more employed. Accordingly, single-phase PLLs are mainly divided into the transport delay-based, Hilbert transformation-based, all-pass filter-based, and SOGI PLL [67, 68]. In spite of a simple structure, the transport delay-based PLL provides a good synchronization capability in the case of ideal sinusoidal voltages. However, in presence of harmonic components, its performance is highly degraded. The Hilbert transformation-based PLL as well as the all-pass filter-based PLL provides some kind of filtering and consequently presents a better harmonics rejection performance. The inverse Park PLL and the SOGI PLL which uses the SOGI block for the fictitious phase generation [68] are two advanced single-phase PLLs with promising features including ease of implementation, robustness against disturbances, and frequency adaptive performance. Despite the wide acceptance and use of these two PLLs, the tuning of their parameters is not straightforward and is a trade-off between the bandwidth and the robustness and usually depends on the intended application.

The same concept is also applied to the converters through the proportional-resonant (PR) controllers as shown in Fig. 1.11(c), where there is no internal current control loop and the system is highly dependent on tuning the PR parameters [69].

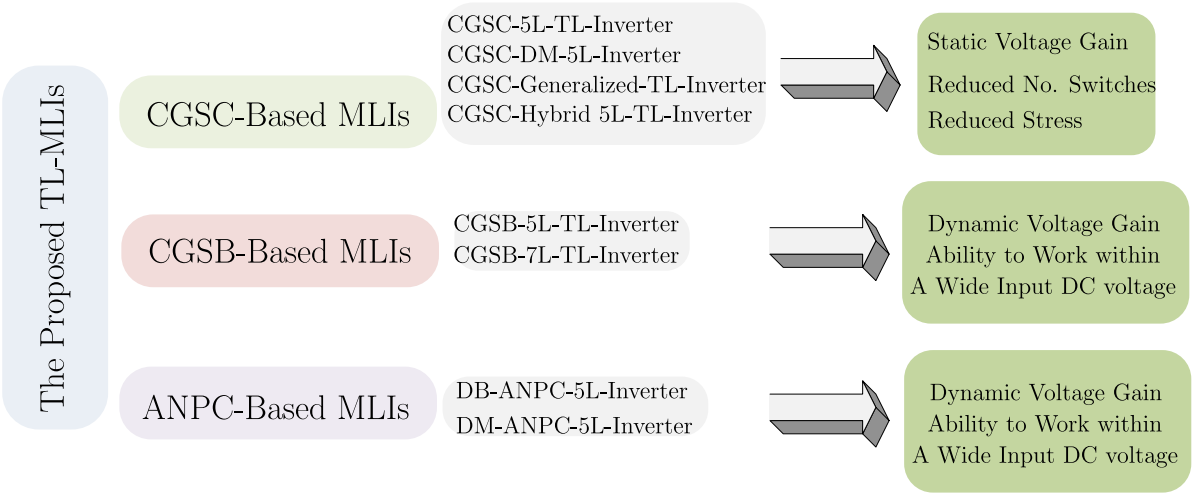


Figure 1.12: Overall Outlook of the Thesis Contribution.

1.3 An Outlook of the Thesis Contribution

Considering the above-mentioned literature review and regarding the grid-tied PV application, the aim of this research is to propose several new MLIs feeding through a single dc-source with CGSC/SB-based or mid-point-clamped design. The motivations behind the proposed topologies are as follows:

- Enhancing the overall efficiency of the entire system when a low and wide varying input dc voltage is available.
- Improving the injected power quality of the grid using the concept of MLIs with lower THD.
- Increasing the power density of the system by the concept of MLIs with a reduced output filter size and stress on devices.
- Reduction of the leakage current in grid-tied PV applications.
- Introducing new family of MLIs with a single-stage integrated dynamic voltage conversion gain.

To this end, in Chapter 2, six different CGSC-based MLIs are presented, in which they possess a static voltage conversion gain. Fig. 1.11 illustrates the general outlook of the proposed topologies. Each of them offers some specific merits in terms of number of inverter output voltage levels, generalization capability, working principles under a wide range of dc voltage source variations, reduced stress on devices and etc over the

conventional types of CGSC-based MLIs. Hence, their performance from different aspects is investigated in details. Following this, three topologies from the family of CGSB-based MLIs are presented in Chapter 3. The working principles of these structures is different in comparison to the CGSC-based MLIs as they can provide a dynamic voltage conversion gain within a single-stage power conversion design. Conversely, in order to introduce some competitive mid point-clamped-based MLIs, a family of ANPC-based 5L inverters with a dual-mode (DM) circuit design and static voltage gain, is presented in Chapter 4. Alternatively, another ANPC-based 5L inverter with a dynamic voltage conversion gain and a single-stage SB-integrated technique is introduced subsequently in this chapter. To confirm the circuit feasibility of all the proposed topologies and to support the discussions, extensive simulation and experimental results under the grid-connected condition are presented.

CHAPTER 2

COMMON-GROUND SWITCHED-CAPACITOR-BASED MLIS

2.1 CGSC-Based 5L Inverters

2.1.1 First Topology

The overall configuration of this proposed CGSC-5L inverter has been depicted in Fig. 2.1(a) [70]. Here, seven power switches, a single power diode, two capacitors alongside an inductor as the filter are utilized. Using the integrated SC-cell, the proposed topology is able to boost the output voltage of the PV arrays as the input dc source within a single stage. In this case, the capacitor C_2 acts as a virtual dc-link like what has been using in the conventional approaches. Regarding this circuit architecture, the negative terminal of the input dc source is directly connected to the null of the grid, which makes a CG feature for the proposed topology. Here, four of the involved power switches are normal power MOSFET/IGBT with anti-parallel diode, while Switch S_3 is a MOSFET/IGBT without antiparallel diode. Also, the Switch S_5 is bi-directional type with the capability of blocking voltage in both directions.

In order to show different current flowing paths of the proposed topology, Fig. 2.1(b)-(f) can be considered. Here, the red and blue lines indicate the active grid current and the charging current paths for the capacitors, respectively. Considering Fig. Fig. 2.1(b), the zero-level of the output voltage is made through the ON state switch S_3, while by discharging of C_1 through S_1, the diode in the SC cell will be in reverse-biased. By taking a fixed voltage of V_{dc} as the input voltage provided by the PV panels, the capacitor C_2 can

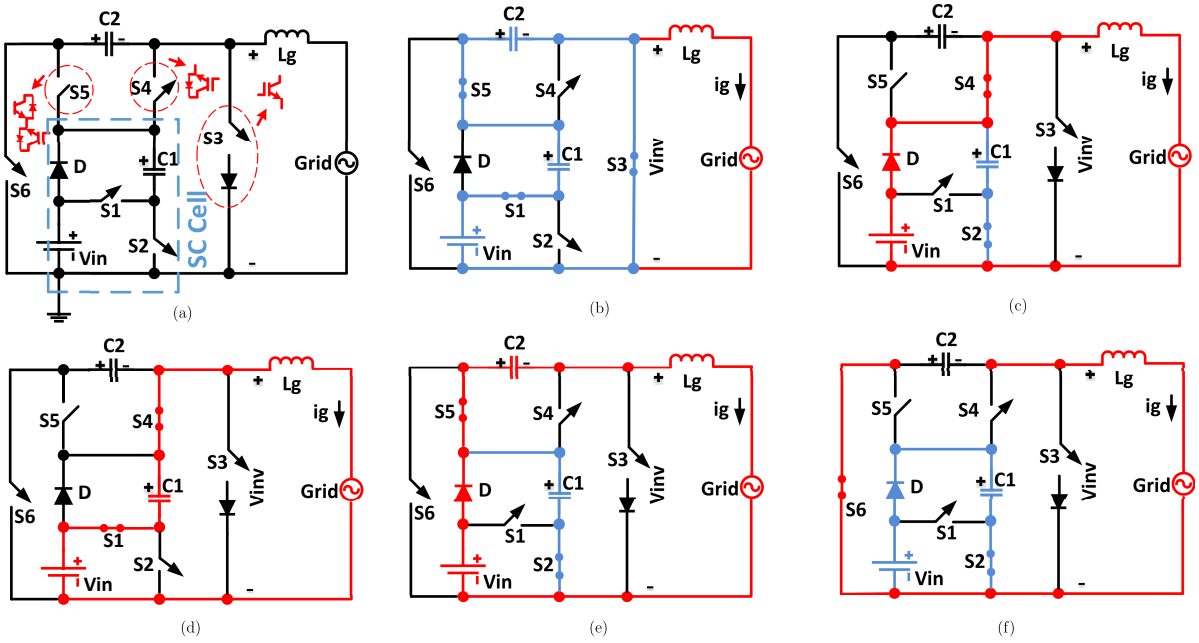


Figure 2.1: The proposed five-level SC-based TL-inverter (a) the main circuit configuration (b) the current flowing path of the zero level (c) the current flowing path of the first positive output voltage level (d) the current flowing path of the top positive output voltage level (e) the current flowing path of the first negative output voltage level (f) the current flowing path of the top negative output voltage level [70]

be charged to $2V_{dc}$ through S_5 and S_3. In this case, once the voltage across C_2 exceeds the summation of the voltage of the PV arrays and the voltage across C_1, the series diode of S_3 will be in forward-biased and therefore the grid current can pass from the red path line. In turn, once the voltage of C_2 is to be less than $2V_{dc}$, the grid current with any of direction will flow through the blue charging flow path.

Considering the same direction of the grid current and the local grid voltage, the first level of the output voltage, $+V_{dc}$ can be made by the parallel switch of the SC cell, S_2 and also the switch S_4 as shown in Fig. 2.1(c). Here, the integrated power diode is in the forward-biased mode and therefore C_2 is disconnected from the grid, whereas irrespective of the grid current direction, C_1 is charged by the dc supply. Afterwards, in order to generate the top-level of the output voltage in the positive half-cycle of the grid voltage, Fig. 2.1(d) should be taken into account. In this case, S_4 is again turned ON, while through the series switch of the SC-cell, S_1, the power diode of the SC-cell is in the reverse-biased; therefore, the voltage across the charged capacitor C_1 is added to the dc supply voltage and in turn the level of $+2V_{dc}$ is generated. Herein, C_2 is again disconnected from the grid, while depending on the direction of the injected current to the grid (active or reactive power support mode), C_1 can be discharged or charged.

During the negative sequence of the grid voltage, the importance of the pre-charged

capacitor C_2 is highlighted. Here, to make the first negative-level of the output voltage $-V_{dc}$, the switch S_5 must be ON as indicated in Fig. 2.1(e), whereas through the parallel switch in the SC cell, C_1 can be charged. It is clear that in the active power mode, the C_2 will be charged by the dc supply and within the reactive power mode it will be discharged. Taking Fig. 2.1(f) into consideration, the top negative level of the output voltage $-2V_{dc}$ can be generated with a direct contribution of the S_6 and C_2. Here, depending on the grid current direction, C_2 can be charged and discharged, whereas through the parallel switch S_2 in the SC-cell, C_1 can be charged by the supply once again. Regarding the above-mentioned description, the voltage across the C_1 and C_1 remains balanced at V_{dc} and $2V_dc$, respectively. Here, in addition to generating the five distinct levels of the output voltage by the aim of only seven power switches, the proposed topology offers a valuable voltage boosting feature also. Such advantage makes sense for a PV with string inverter as it reduces the number of PV panels in string. To practically design the proposed converter, electrolyte capacitors are needed. Regarding the above-mentioned analysis, the maximum voltage stress (MVS) of the SC cell switches is equal to V_{dc}, whereas this value for the switches S_3, S_4, and S_5 is $2V_{dc}$. Here, the switch S_6 is the MVS holder equals to $4V_{dc}$. Details of the control, design, comparative study and the relevant experimental results of this work can be found in [70].

2.1.2 Second Topology

The circuit schematic of this proposed topology and its different current flowing paths are illustrated in Fig. 2.2(a)-(f) [71, 72]. Similar to the first proposed topology, a CG feature is achieved whilst the output voltage of the inverter is measured with respect to the negative terminal of the input dc source. In relation to Fig. 2.2(a), to make the zero-level of the proposed inverter output voltage during the positive half cycle, three power switches named as S_P, S_2 and S_3 must be ON. Hence, regarding the paralleled ON state switch in the SC cell, S_P, the capacitor C_1 is charged to the input dc voltage V_{dc} through the forward-biased SC cell power diode D_{SC} in every direction of the grid current, while C_2 is disconnected from the grid. Following this, the first positive level of the output voltage $+V_dc$, can be made just by turning the state of two power switches S_1 and S_2 in compare to the described zero level of the output voltage in the positive half cycle. As shown in Fig. 2.2(b), the power switch S_P must be again ON to keep on the charging operation of C_1, while V_{dc} can be transferred to the inverter output through the turned ON switches S_1 and S_3. Here, C_2 is again excluded from the grid current flowing path since its upcoming charged voltage makes the integrated power diode D

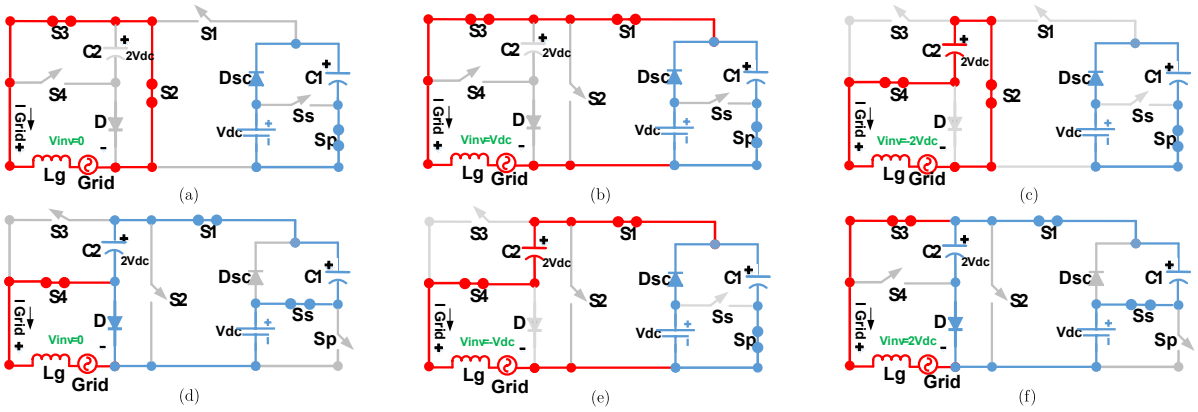


Figure 2.2: The current flowing paths of the proposed inverter at (a) the zero-level of the output voltage in the positive half-cycle (b) the first positive level of the output voltage (c) the top positive level of the output voltage (d) the zero-level of the output voltage in the negative half-cycle of (e) the first negative level of the output voltage, and (f) the top negative level of the output voltage [71, 72].

reverse-biased.

In order to create the top positive level of the output voltage, $+2V_{dc}$, Fig. 2.2(c) should be considered. In this case, the series power switch of the SC cell, S_S must be ON; hence, C_1 is discharged (or charged) if the injected grid current polarity is to be positive (or negative). Therefore through the ON state contribution of S_1 and S_3, the sum of the input voltage value and the charged voltage across the C_1 is converted to the output and the voltage level of $2V_{dc}$ is thereby created. Here, since the clamped voltage across the power diode D is positive; it operates in the forward-biased condition. Thus, depending on the injected grid current polarity, the C_2 can be charged to the output voltage of the SC cell, $2V_{dc}$.

Regarding Fig. 2.2(d) and during the operation of the proposed inverter in the negative half-cycle, the zero level of the output voltage can again be generated with a different current flowing path. Here, through the ON state power switch S_S in the SC cell, the output voltage of the SC cell will be equal to $2V_{dc}$. Hence, depending on the grid current direction, C_1 can be charged or discharged. Having taken the charged voltage of C_2, $2V_{dc}$ and considering the aim of S_1, the power diode D is in the state of being forward-biased again; so, the zero level of the inverter output voltage can be generated once again through the contribution of D and S_4, while in respect of the grid current direction, C_2 can be charged (or discharged) to $2V_{dc}$.

Having taken Fig. 2.2(e) into account, the first negative level of the output voltage, $-V_{dc}$ can be built by the contribution of C_2 and the input dc voltage source value. Considering the charged voltage value of C_2 in the previous stages $2V_{dc}$, the power diode D will be in reverse bias; so by the aim of S_P, the output voltage of the SC cell will be

equal to V_{dc}. Therefore, through the turned ON switches S_1 and S_4, the voltage level of $-V_{dc}$ is converted to the output, while irrespective of the grid current direction, C_1 is charged to V_{dc} once again.

Finally, to make the top negative level of the proposed inverters output voltage, $-2V_{dc}$, Fig. 19 (f) must be taken into account. As is clear from the depicted current flowing path, although C_1 can be charged to V_{dc} in every instance of the grid current polarity through the ON state power switch S_P, the SC cell will be disconnected from the grid by the turned OFF power switch S_1. Hence, in this case, the output power is directly supplied by the sole contribution of C_2 alongside the aim of the ON state power switches S_2 and S_4.

From the above descriptions, it is clear that the charging/discharging operation of the C_2 in the whole operation in the negative half cycle depends on the grid current direction. It can also be concluded that through the series-parallel switching conversion of the switches, both the capacitors are self-balanced on V_{dc} and $2V_{dc}$ at the end of one full cycle of the grid-frequency. As is also evident, the maximum value of the inverter output voltage is $2V_{dc}$ which reflects the double-voltage boosting feature of the proposed topology. Accordingly, to meet the peak voltage value of the grid, a much lower value of the input voltage (at least 160 V for a 311 V-based maximum voltage of the grid) is required. Also, considering the states of the switches, it is apparent that two of the four involved switches, S_3 and S_4 are only ON in the positive and negative half-cycle of the grid frequency, respectively. Hence, they are switched on the basis of the grid‚Äôs frequency while the other four involved switches are working through a high switching frequency modulation. Details of the circuit design, comparative study and the relevant control and experimental results have been discussed in [71, 72].

2.2 CGSC-Based Generalized TL-MLIs

Similar to two previous topologies, the basic structure of the proposed CGSC-TL inverter in the third topology is able to generate 5L of the output voltage with eight unidirectional power switches and two DC-link capacitors. This structure is aimed to present a novel circuit configuration with capability of quasi-soft charging (QSC) operation for the capacitors and to explain the generalization feature in reaching larger number of output voltage levels. By appropriate switching conversion of the switches, the voltages across both the capacitors remains balanced at the input dc voltage value without any need of external voltage sensors (As opposed to the previous topologies), while the proposed

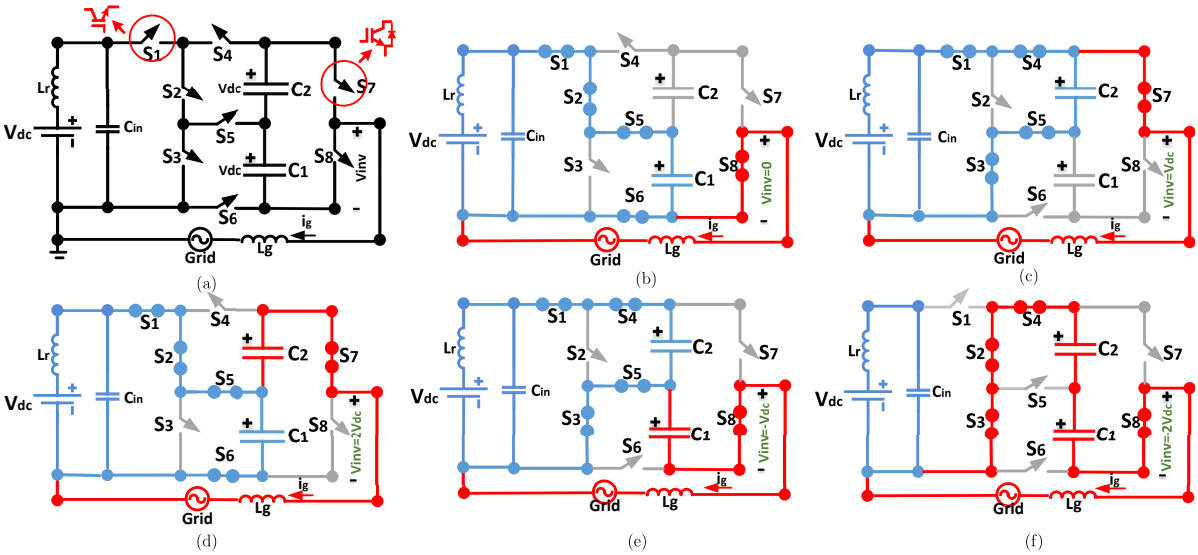


Figure 2.3: The proposed 5L-CGSC-TL inverter (Generalized Topology) (a) the main circuit schematic and the current flowing path at (b) the zero-level, (c) the first positive-level, (d) the top positive level, (e) the first negative-level, (f) the top negative-level of the output voltage [73].

inverter can give a double voltage boosting feature in the output for its basic 5L structure. Herein, the QSC cell including a small inductor, L_r associated with an input capacitor is employed in the input side of the proposed CGSC5L-TL inverter to suppress the current stress and keep the charging current of the capacitors in a permissible range.

Based on this circuit configuration and by adding another capacitor with a single unidirectional and a bidirectional power switches as an added SC network, a new 7L-CGSC-TL inverter is derived. The proposed 7L-CGSC-TL inverter possesses three-time voltage boosting feature with self-voltage balancing of the capacitors, while the input current waveform is free from any huge inrush current owing to the incorporated QSC cell in the input. Following the proposed concept, a generalized $2n+5$-level inverter with n-number of added SC networks is introduced, which possesses all the aforementioned features.

The circuit diagram of the proposed 5L-CGSC-TL inverter and the corresponding switches realization is depicted in Fig. 2.3(a). The proposed topology with a fixed dc source value, V_{dc} is connected to the grid via a simple L-type filter ,L_g whilst it is comprised of eight unidirectional power switches, and two DC- link capacitors C_1 and C_2. Here, the power switch S_1 can be an RB-IGBT without having the internal anti-parallel diode. Also, a QSC cell with a small resonant inductor L_r and an input capacitor C_{in} is used to attenuate the charging current of the capacitors C_1 and C_2. As can be realized, the negative terminal of the input dc source is tied to the neutral point of the grid, which constitutes the CG feature of the proposed topology. To generate all the distinctive output

voltage levels, five different current flowing paths are provided as shown in Fig. 2.3(b)-(f). Here, the red and blue lines respectively denote the grid current path and the capacitors charging loop.

From the above-mentioned circuit descriptions, the following remarks can be concluded as:

- The proposed CGSC5L-TL inverter can generate all the desired output voltage levels within a self-voltage balancing nature of the involved capacitors and can also provide a double voltage boosting feature.

- The maximum voltage stress across five power switches as S_1, S_2, S_3,S_4,and S_5 is kept fixed within the input dc voltage value V_{dc}, while the MVS for the three remaining switches S_6, S_7 and S_8 is $2V_{dc}$. Here, irrespective of the provided voltage boosting feature, the related voltage stress of both the involved capacitors is within the input dc source, as well.

- The QSC capability and the balanced voltage of all the integrated DC-link capacitors at the available input dc voltage value lead to improved performance of the proposed CGSC5L-TL inverter from both the reliability and power density view point. This can be achieved by the lower current stress and operating temperature profile of the involved power switches owing to the incorporated QSC cell as the input filter. This feature is propitious since the size and weight of the required heat sink per each semiconductor device can be further reduced. Moreover, the life span of the electrolyte capacitors is extended when their rated voltage value and their operating voltage can be close to each other. In addition, owing to the lower nominal voltage range of the involved capacitors, their footprint design can be more compact.

By integrating an additional SC network comprising of a unidirectional and a bidirectional power switches with the aim of another DC-link capacitor C_3 into the basic design of the proposed CGSC5L-TL inverter, the number of output voltage levels can be extended to seven. Here, the converter maintains its CG concept likewise. Fig. 2.4(a) shows the overall circuit configuration of the proposed CGSC7L-TL inverter. Herein, again the same QSC cell for capacitive inrush current attenuation has been employed in the input side of the converter. Similar to the previous case, the steady state voltage of all the involved capacitors are equal to the input dc voltage value, while the proposed CGSC7L-TL inverter can make a triple voltage boosting feature at the output using

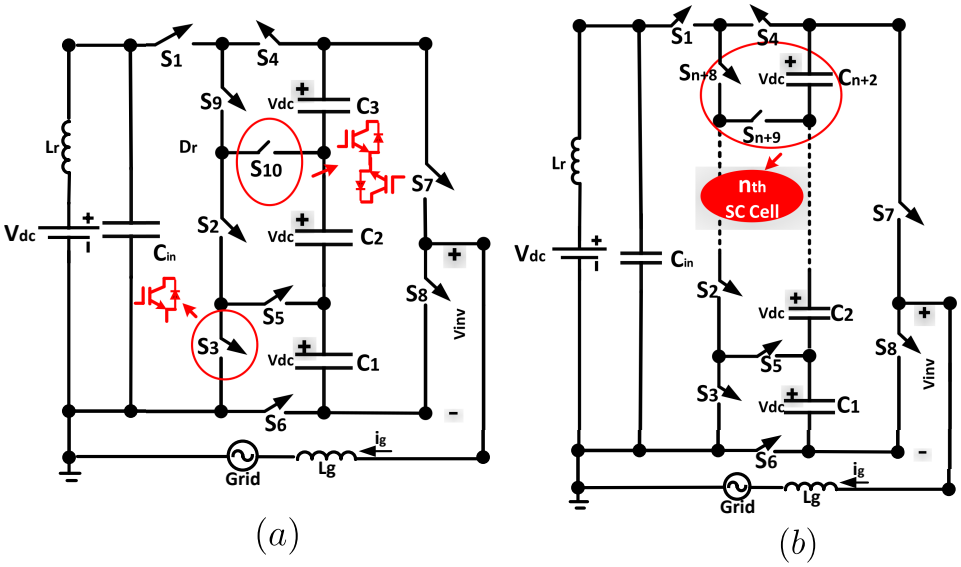


Figure 2.4: (a) The proposed CGSC7L-TL inverter (b) the proposed generalized CGSC-TL inverter [73].

the voltages of capacitor C_1, C_2 and C_3. To generate all the output voltage levels, seven operating states are possible.

Similar to the proposed 7L-CGSC-TL inverter, a generalized structure can be derived as shown in Fig. 2.4(b), which requires n number of added SC network. Herein, the same QSC cell is incorporated in the input dc-side to alleviate the charging current of the involved capacitors. The working principle of the generalized CGSC-TL inverter is also the same as given for the proposed 5L and 7L-CGSC-TL inverters. Therefore, all the DC-link capacitors are self-balanced at the input dc voltage value by the switching conversion of the switches within a fundamental grid frequency period and without requiring any voltage sensors or sophisticated control platform. Also, the switch S_1 is always ON except during the top negative output voltage level generation. Regarding the generalization capability of the proposed topology, the number of added SC networks can be functionalized to reach a required higher number of output voltage levels and the desired static voltage boosting gain. Here, depending on the available input dc voltage for a proper grid-tied application, the unnecessary modules of the added SC networks that are modular with each other can be bypassed.

Therefore, the MVS rating of all the involved power switches can be always remained in a permissible value. From this analysis, the total number of required power switches, the overall number of required DC-link capacitors (rather than the input capacitor for QSC operation), the maximum number of inverter output voltage levels, and the maximum value of the inverter output voltage representing the overall static voltage

gain can be formulated as follows, respectively:

$$\begin{aligned} N_{Switch} &= 3n + 8. \\ N_{Cap} &= n + 2. \\ N_{Level} &= 2n + 5. \\ V_{inv,max} &= (n + 2)V_{dc}. \end{aligned} \tag{2.1}$$

Considering a value of 200 V and 150 V as for the dc source of the proposed 5L and 7L-CGSC-TL inverters, respectively, the overall steady state simulation results are given in Fig. 2.5(a) and (d). As can be observed, all the desired output voltage levels in both the 5L and 7L cases are generated, while the injected grid current with the peak of 5 A could follow the behavior of the assigned sinusoidal reference current. Here, a dead beat controller has been selected for the closed-loop control strategy. In these cases, the peak voltage of the proposed 5L and 7L-CGSC-TL inverters is 400 V and 450 V, respectively, which can reflect the two and three-time voltage boosting ability of the proposed structures. Moreover, the balanced voltage of both the capacitors of the proposed 5L-CGSC-TL inverter is 200 V, while this value for the three involved capacitors of the proposed 7L-CGSC-TL inverter is 150 V. Here, the ripple voltage of all the involved capacitors are within the 10% allowable value of their respective balanced voltage. Considering the importance of the input QSC cell, the input and capacitors currents of both the proposed 5L and 7L-CGSC-TL inverters are shown in Fig. 2.5(b) and (e), respectively. As can be observed, there is no huge inrush current in these waveforms, while the peak of input dc source current stress is within about two and three times of peak of i_g for the case of 5L and 7L-CGSC-TL inverter, respectively. Such type of the input current waveform is suitable for any front-end dc-dc converters to accomplish the maximum power point tracking procedure for a PV-based grid-tied TL inverter.

Considering the quality of i_g, a Fast Fourier Transformation (FFT) analysis in MATLAB/SIMULINK has been conducted as shown in Fig. 2.5(c) and (f), which gives a THD result of 2.13% and 1.42% for the proposed 5L and 7L-CGSC-TL inverters injected grid current, respectively. The fixed switching operation of the proposed controller can also be reconfirmed here where the harmonics cluster are taking place around the switching frequency value (20 kHz). Therefore, they can easily be filtered out through the used simple L-type filter.

Details of the control, design, comparative study and other relevant experimental results of this work can be found in [73].

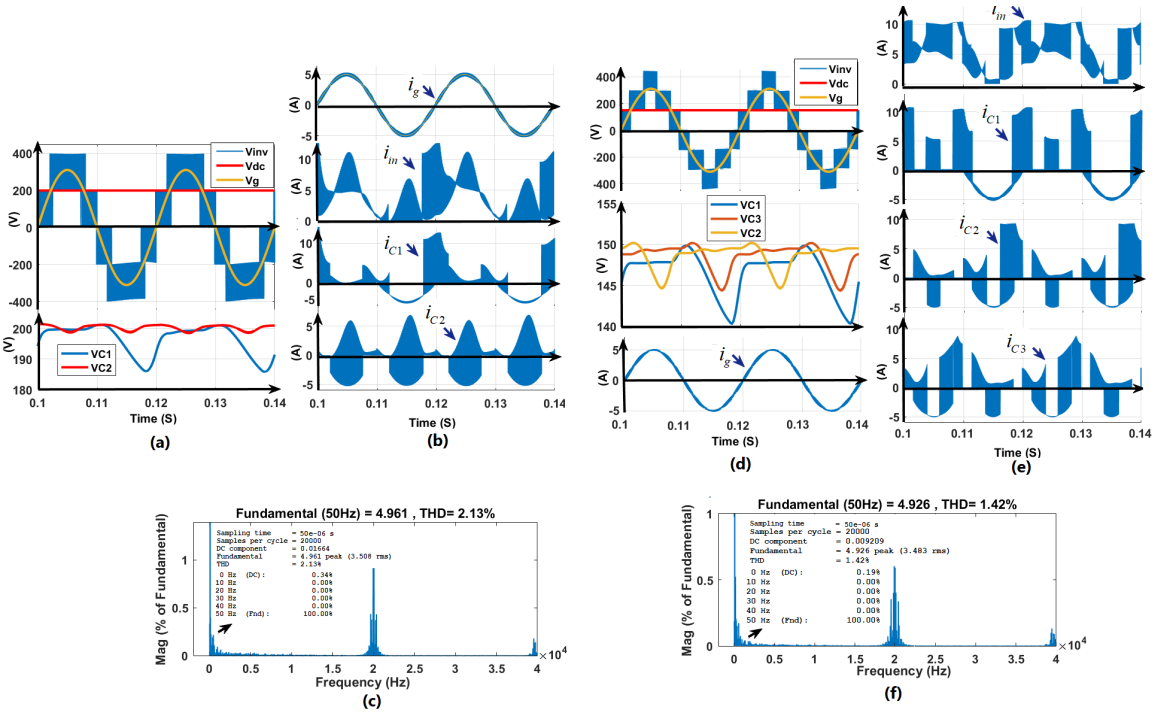


Figure 2.5: Simulation results showing: (a) 5L-inverter output with the grid and dc source voltages alongside the capacitors voltages (b) the injected grid-current with the input dc source and the capacitors currents of the proposed 5L-CGSC-TL inverter (c) the injected grid current spectrum for the proposed 5L-CGSC-TL inverter (d) 7L-inverter output with the grid and dc source voltages alongside the capacitors voltages, (e) the input dc source current and the capacitors currents of the proposed 7L-CGSC-TL inverter, (f) the injected grid current spectrum for the proposed 7L-CGSC-TL inverter [73].

2.3 DM-CGSC-Based 5L Inverter

As described earlier TL grid-connected photovoltaic PV inverters with a CG circuit architecture exhibit some excellent features in removing the leakage current concern and improving the overall efficiency. However, the ability to cope with a wide range of input voltage changes whilst maintaining the output voltage in a single power conversion stage is a key technological challenge. Considering this, the work at hand proposes a novel dual-mode switched-capacitor five-level (DMSC5L)-TL inverter with a CG feature connected to the grid. The proposed topology is comprised of a single dc source and power diode, three capacitors, four unidirectional and three bi-directional power switches. Based on the series-parallel switching conversion of the involved switches, the proposed DMSC5L-TL inverter can generate five distinctive output voltage levels during both the boost and buck modes of the operation with a self-voltage balancing operation for the involved capacitors. A simple dead-beat continuous current controller and modulation technique is also used to handle both the active and reactive power exchange within a fixed switching frequency operation.

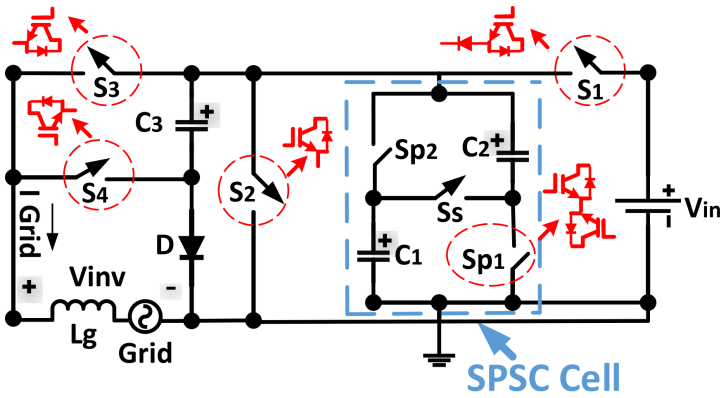


Figure 2.6: The proposed DMSC5L-TL inverter topology [74].

The overall configuration of the proposed DMSC5L grid-connected TL inverter with different switches realization has been depicted in Fig. 2.6. As it is clear, the proposed topology offers a CG feature and contains a SPSC cell with two bi-directional paralleled power switches S_{P1} and S_{P2}, a single series unidirectional power switch, S_S, and two dc-link capacitors, C_1 and C_2. Such an SPSC cell is of essential for the DM operation of the proposed topology under the overall condition of the input dc-source (buck or boost mode). Apart from this cell, the proposed topology needs four other power switches, a single power diode and another dc-link capacitor. Here, three power switches named as S_2, S_3 and S_4 are unidirectional from both the current flowing direction and voltage stress viewpoints, while the type of power switch is the reverse-blocking (RB) one with a unidirectional operation in current flowing direction and bidirectional operation as the MVS aspect. Here also, the C_3 acts as a virtual dc-link like what is used in the other existing TL inverters with a CG concept. Considering a constant input voltage as V_{dc} and regarding the switching conversion of the proposed topology which will be discussed in the following, the balanced voltage across the involved capacitors in each of the boost and buck modes can be summarized as follows, respectively:

$$\begin{aligned} V_{C_1} &= V_{C_2} = V_{dc} \\ V_{C_3} &= 2V_{dc}. \end{aligned} \tag{2.2}$$

$$\begin{aligned} V_{C_1} &= V_{C_2} = 0.5V_{dc} \\ V_{C_3} &= V_{dc}. \end{aligned} \tag{2.3}$$

Once the input voltage of the inverter is lower than the peak amplitude of the grid, e.g., in case of accessing a lower voltage PV string panel, the proposed inverter must ride through the boost mode operation. Considering V_{dc} as a fixed value of the input dc source voltage that can be a string PV panel with a MPPT mechanism, the proposed

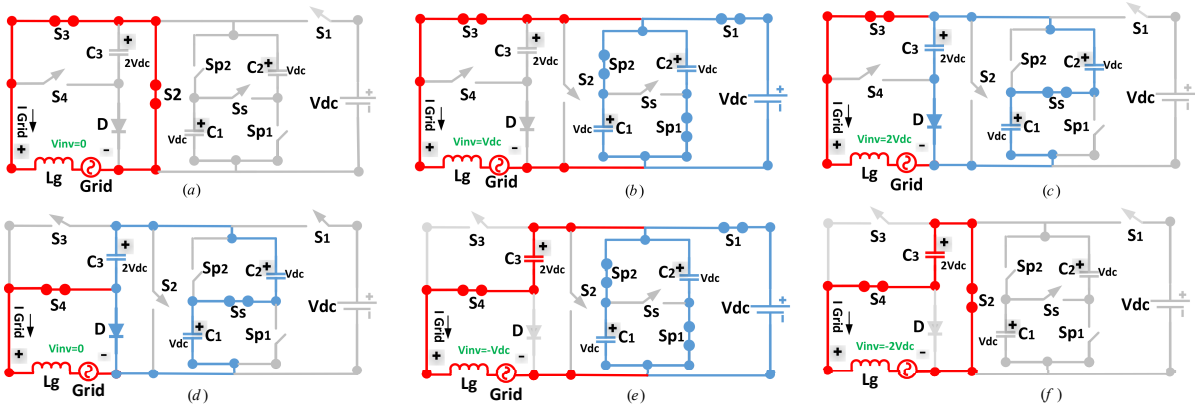


Figure 2.7: Different current flowing paths of the proposed DMSC5L-TL grid-connected inverter in boost mode operation (a) at the zero level of the output voltage in the positive half cycle (b) at the first positive level of the output voltage (c) at the top positive level of the output voltage (d) at the zero level of the output voltage in negative half cycle (e) at the first negative level of the output voltage (f) at the top negative level of the output voltage. [74].

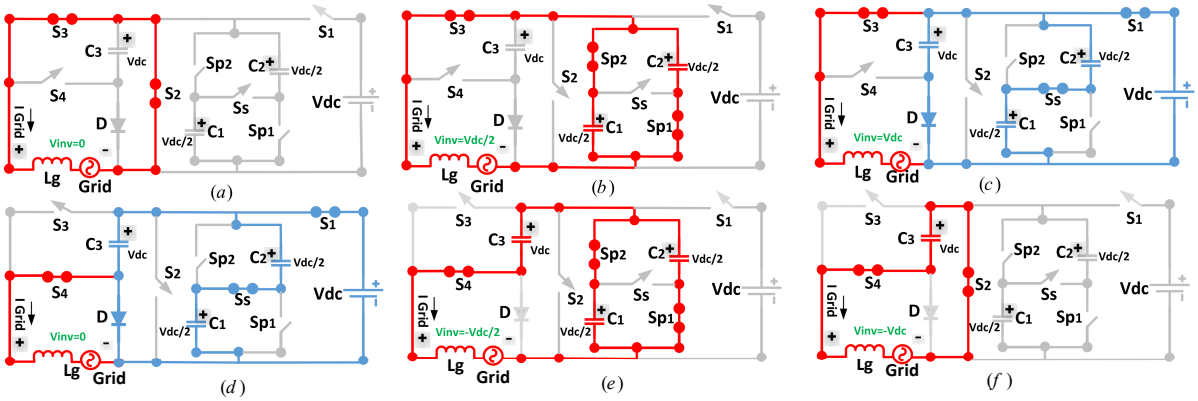


Figure 2.8: Different current flowing paths of the proposed DMSC5L-TL grid-connected inverter in buck mode operation (a) at the zero level of the output voltage in the positive half cycle (b) at the first positive level of the output voltage (c) at the top positive level of the output voltage (d) at the zero level of the output voltage in negative half cycle (e) at the first negative level of the output voltage (f) at the top negative level of the output voltage [74].

DMSC5L-TL inverter can generate $\pm V_{dc}$, $\pm 2V_{dc}$, and the zero-level of the output voltage. Fig. 2.7(a)-(f) illustrate different current flowing paths of the proposed topology within the mentioned five output voltage levels generation. Here, the red and blue lines imply the grid current flowing path and the charging loop of the involved capacitors, respectively.

When the dc-link voltage or the input voltage is sufficient to produce the grid amplitude requirement, the proposed topology can turn its operation towards the buck mode condition, whilst it is likewise able to generate all the five output voltage levels properly with V_{dc} as the peak value. Similar to the boost mode operation, six different current flowing paths as shown in Fig. 2.8(a)-(f) are available to generate five distinctive output voltage levels. Considering the grid peak voltage equals to 320V, and the input dc voltage of 200V and 400V as for the boost and buck operation modes, respectively, a comparative efficiency curve showing the output power between the results provided by

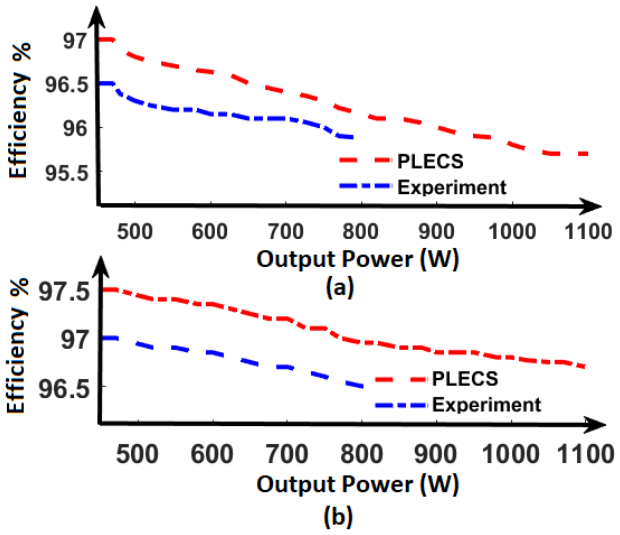


Figure 2.9: Efficiency versus output active power curve of the proposed DMSC5L-TL inverter (a) for the boost mode of operation (b) for the buck mode of operation [74].

the PLECS versus the results obtained from experimental measurements is illustrated in Fig. 2.9. Herein, a generation of CoolMOS^{TM}-C6 power transistors from Infineon Tech have also been utilized in the experiment owing to their reliable performance for handling the pulsating current of the SC-based circuits. The experimental efficiency of the proposed DMSC5L-TL inverter in both operation modes have been measured using a Voltech PM3000A Universal Power Analyzer. As can be seen, the results are close to each other, and as expected the buck operation mode of the proposed topology possesses higher efficiency due to the reduced current stress profile of the switches. Further details of the circuit design, comparative study and the relevant control and experimental results have been discussed in [74].

2.4 CGSC-Based 9L Inverter

The fifth topology is a 9L-CGSC-based TL-inverter focusing on HF micro-grid application [75]. Viable and reliable performance of high-frequency ac (HFac) power distribution systems have already been proven in aerospace and military applications for the latest decades. However, the concept of HFac systems applicable in newly developed microgrids with the integration of RE sources is relatively new, where single-phase HF buses covering a range of 400-Hz to 1-kHz are used to integrate RE resources with the loads and the grid [76–78].

Utilization of the HFac microgrid contributes to some notable advantages such as

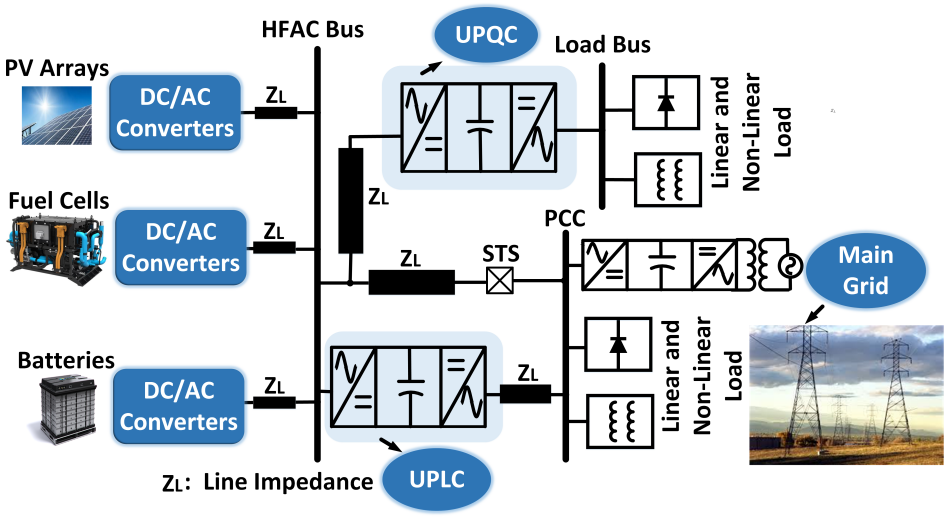


Figure 2.10: Typical configuration of a power electronics-based HFac microgrid [75].

easier filtering of the harmonics clusters, incorporating transformers and other passive components with reduced weight and size, improving the luminous efficiency of the fluorescent lighting by mitigating flickers, and possible inclusion of HF induction motors for compressors and high pressure pumps and turbines [69–71]. Fig. 2.10 shows a configuration of an HFac microgrid, which integrates a unified power quality conditioner (UPQC), universal active power line conditioner (UPLC), and static transfer switch (STS) units. To involve RE sources like fuel cells and PV arrays in such type of microgrids, the role of power electronics converters is of importance, as depicted in Fig. 2.10, where the outputs may need to be connected in series and in parallel to increase their power handling capacity [79, 80]. However, synchronizing the phase and amplitude of different inverter output voltages usually requires a complicated procedure [81]. Moreover, the output voltage of these inverters needs an interface line impedance, Z_L, be able to connect to the HFac grid buses. The usual preference for such type of Z_L is to design them small to make the whole conversion system more compact. Hence, the fundamental frequency components of these HF inverters output voltage have to be large enough to meet the peak voltage magnitude of the HFac microgrids [78].

To this end, MLIs have emerged as a promising alternative to conventional two-level resonant inverters in HFac microgrids. This is mainly due to the high quality of the injected currents, large power capacity, efficient performance and less complexity [82, 83].

Considering the above, recent research on CGSC-based MLIs shows that the ratio between the number of inverter output voltage levels over the number of incorporated switching devices ($\frac{N_{Level}}{N_{Switch}}$) is still larger than one. This fact indicates that some topological

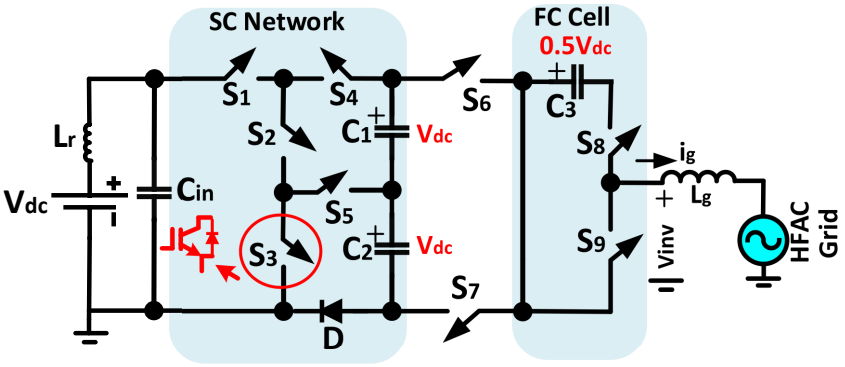


Figure 2.11: Proposed 9L9S-CGSC-TL inverter [75].

improvements are still needed to make them more compact and efficient. Also, the maximum number of output voltage levels generated by most of the existing CGSC-based MLIs are limited to five and seven. Having the ability of higher number of output voltage levels can make the CGSC-TL inverters more attractive, since a further reduction in the size of the output filter can be possible.

The aim of this work is to cover this specific research gap by introducing a novel nine-level nine-switch (9L9S)-CGSC-based TL inverter suitable for HFac applications. The proposed topology offers a unity ratio for $\frac{N_{Level}}{N_{Switch}}$ and it can provide a double voltage boosting feature within a single power processing stage. Comparing with the double-stage step-up configurations, the proposed topology is inductorless. Hence, its overall weight, volume, and efficiency can be much improved. Thanks to addition of an LC input filter, the input current drawn by the dc source does not have any large inrush spikes, while the maximum current stresses of the involved switches is within an acceptable range. The proposed topology can generate all the 9L inverter output voltage with maximum TSV of five in perunit scale. Concerning these features, it could be designed within a compact area for an 1.2-kW fabricated prototype.

The circuit configuration of the proposed 9L9S-CGSC-TL inverter is illustrated in Fig. 2.11. As can be seen, apart from nine unidirectional power switches, the proposed topology needs three self-balanced dc-link capacitors named as C_1, C_2, and C_3, an extra power diode, D, and an LC input filter with two passive components, L_r and C_{in}. Only a single-input dc source is employed, while its ground is tied to the neutral point of the HFac grid. Hence, a CG concept is provided for the proposed topology and, in case of utilizing RE-based dc resources like PV panels, the ground leakage current concern is obviated.

In this case, five front-end power switches named as S_1, S_2, S_3, S_4, and S_5 and a single power diode, D, are used in the charging loop of C_1 and C_2, which defines an

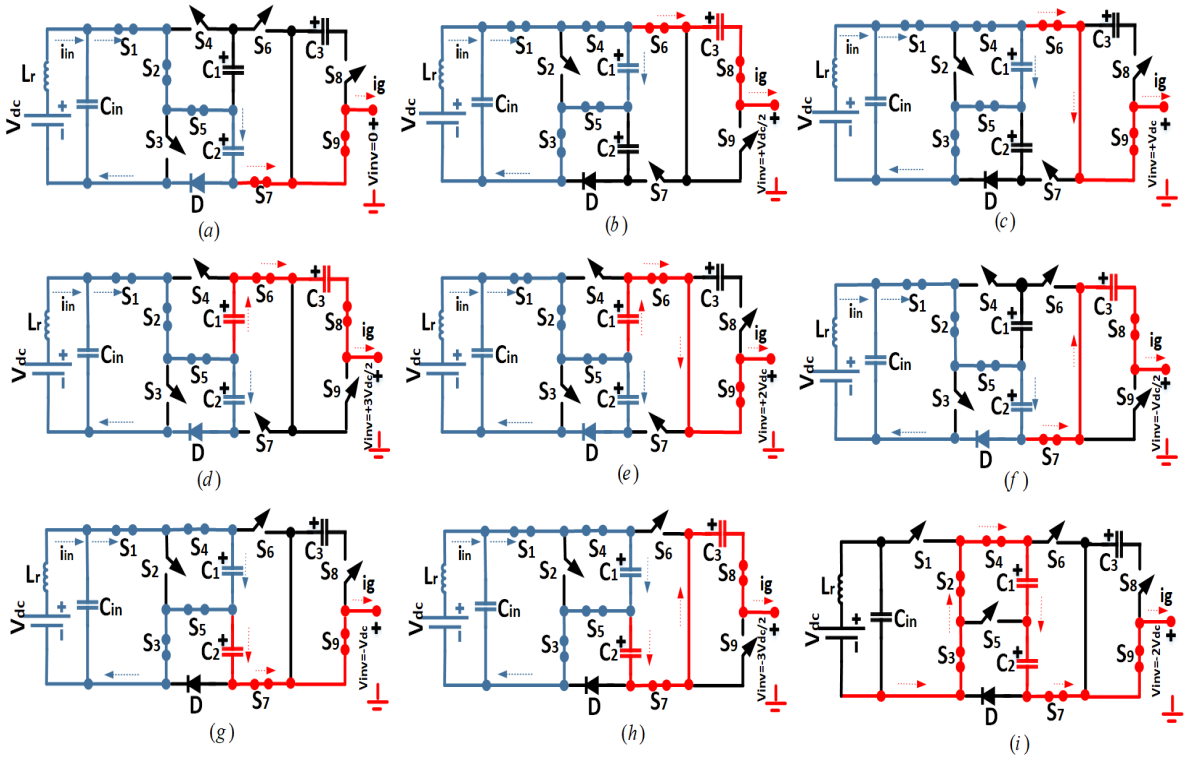


Figure 2.12: Different current flowing paths of the proposed 9L9S-CGSC-TL inverter. (a) Zero-level of the output voltage in both half-cycle, (b) $v_{inv} = \frac{V_{dc}}{2}$, (c) $v_{inv} = V_{dc}$, (d) $v_{inv} = \frac{3V_{dc}}{2}$, (e)$v_{inv} = 2V_{dc}$, (f) $v_{inv} = \frac{-V_{dc}}{2}$, (g) $v_{inv} = -V_{dc}$, (h) $v_{inv} = \frac{-3V_{dc}}{2}$, and (i) $v_{inv} = -2V_{dc}$ [75].

SC network for the proposed topology. Thanks to a series-parallel switching conversion for such an SC network, the voltages across both capacitors C_1 and C_2 are balanced at the input dc voltage value, V_{dc}. The role of L_r in the LC input filter is to smooth the input current waveform to avoid having a large pulsating charging current. Also, the aim of C_{in} in the input LC filter is to prevent a large value of $\frac{dv}{dt}$ caused by the series connection of L_r and S_1 [24]. To generate all the 9L output voltage waveform, along with the switches S_6 and S_7 that act as polarity changer switches, a FC cell including switches S_8 and S_9 and a series capacitor C_3, is also required. The voltage across C_3 is balanced at half value of the input dc source, $0.5V_{dc}$, through the load/grid current. Hence, as opposed to C_1 and C_2 in the SC network, the charging/discharging operation of C_3 is fully soft.

In this circuit architecture, the maximum value of the inverter output voltage will be $2V_{dc}$, which reflects a double voltage boosting feature. Herein, each level of the inverter output voltage possesses a voltage step of $0.5V_{dc}$. Hence, nine different switching states are provided, as shown in Fig. 2.12. In this figure, the blue and red traces represent the SC network charging flow path and the load/grid current following path, respectively.

From these current flowing paths per output voltage level illustration, the following remarks can be stated:

1 Considering a unity power factor condition of the injected grid current, i_g, C_3 is charged by the grid current during the first ($0.5V_{dc}$) and third ($1.5V_{dc}$) positive output voltage levels generation. In turn, it would be discharged by the opposite direction of the injected grid current in the negative half-cycle, i.e., the first negative ($-0.5V_{dc}$) and third negative output voltage levels ($-1.5V_{dc}$). To prove the balanced voltage condition of C_3 at $0.5V_{dc}$, the Kirchhoff's voltage law (KVL) in the presence of L_g, and the grid voltage, v_g, can be applied for any of the first or third positive/negative output voltage levels of the proposed inverter. Regarding Fig. 2.12(b) and (f), the expressions of such KVL for the first positive and negative output voltage levels are:

$$\frac{di_g^+}{dt} = \frac{V_{C3} - V_{dc} + v_g}{L_g} \tag{2.4}$$

$$\frac{di_g^-}{dt} = \frac{v_g - V_{C3}}{L_g} \tag{2.5}$$

where V_{C3} is the instantaneous voltage across C_3, and i_g^+, and i_g^-, are the grid current passing through C_3 in the positive and negative half-cycle, respectively. Hence, regarding the current-second-balance theory for the capacitors, and considering the reverse current direction of i_g in the negative half cycle, the following relationship can be written:

$$\frac{di_g^+}{dt} - \frac{di_g^-}{dt} = 0 \tag{2.6}$$

Considering the above, it can be revealed that V_{C3} would be equal to $0.5V_{dc}$ at the end of a full grid fundamental cycle.

2 The MVS of the involved switches is equal to the peak of inverter output voltage, $2V_{dc}$, where this voltage level should be tolerated by two line frequency-based switches, S_6 and S_7. All the switches of the SC network should withstand the input dc voltage, V_{dc}, as the MVS, while the MVS of the two remaining switches (S_8 and S_9) in the FC side is only half the input dc voltage, $0.5V_{dc}$. Therefore, the maximum value of the TSV for the switches is $10V_{dc}$, which is equal to five in a per unit scale.

3 The maximum current stress value of five involved switches in the SC-network is equal to the charging current of the dc-link capacitors. From this perspective, two line-frequency switches, S_6 and S_7, and two FC cell-involved switches experience the injected grid current as their respective current stress profile.

4 As mentioned earlier, due to the incorporated LC input filter with a small value of L_r, the input current is free from large pulsating current caused by the charging operation of the involved capacitors in the SC-network. Regarding this and considering the parasitic on state resistance of the path, $R_{ch,eq}$, and the equivalent capacitance, C_{eq}, the charging current passing through the SC-network switches, $i_{c,ch}(t)$, is given by:

$$i_{c,ch}(t) = \frac{C_{eq}}{2}(\delta_1 \rho_1 e^{\delta_1 t} + \delta_2 \rho_2 e^{\delta_2 t}) \tag{2.7}$$

$$\delta_{1,2} = \frac{R_{ch,eq}}{2L_r} \pm \sqrt{\left(\frac{R_{ch,eq}}{2L_r}\right)^2 - \frac{2}{L_r C_{eq}}}. \tag{2.8}$$

$$\rho_{1,2} = \frac{\delta_{1,2}}{\delta_1 - \delta_2}\Delta V_{1,2}. \tag{2.9}$$

where $\Delta V_{1,2}$ is the allowable voltage drop across the capacitors C_1 and C_2. The maximum charging current of the involved switches in the SC network can be obtained as follows:

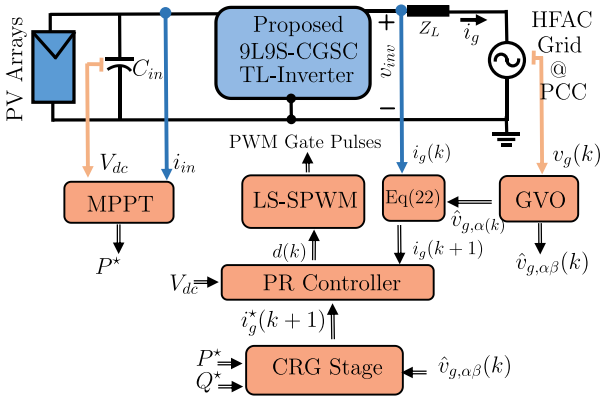
$$i_{ch,max} = \frac{C_{eq}\Delta V_{1,2}}{2}(\frac{\delta_1 \delta_2}{\delta_1 - \delta_2})(e^{\delta_1 t_r} + e^{\delta_2 t_r}) \tag{2.10}$$

$$t_r = \frac{1}{\delta_1 - \delta_2} \ln \frac{\delta_1}{\delta_2}. \tag{2.11}$$

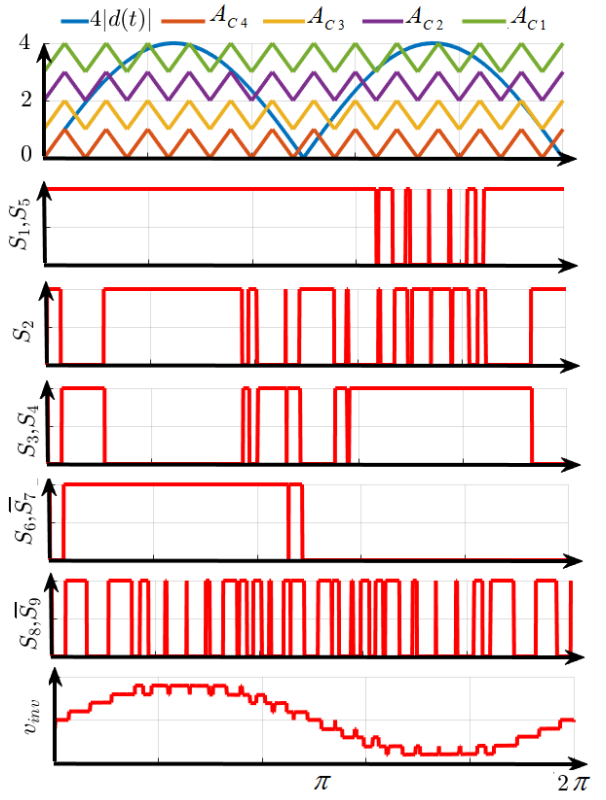
where, t_r is the rise time when $i_{c,ch}(t)$ reaches its maximum peak value. Since $\Delta V_{1,2}$ and the operating line frequency of the system have an inverse relationship with each other, from (3.7), it is revealed that increasing the fundamental-based frequency will lead to a reasonable reduction in the overall maximum current stress profile of the SC-network components [75].

2.4.1 Modulation and Control Scheme

As it has been explained, the involved capacitors of the proposed 9L9S-CGSC-TL inverter are self-balanced. Hence, considering a simple first-order L-type filter, L_g, which reflects its impedance as Z_L, the only controllable variable under the grid-connected condition is the injected grid current, i_g. There have been various control schemes to govern the proposed system to inject a desired controlled current to the HFac grid. In this work, a simple PR controller associated with a LS-SPWM has been used. The overall closed-loop control diagram is depicted in Fig. 2.13(a). Herein, apart from a MPPT Unit for capturing the maximum power of the PV arrays as the input dc source, the overall control mechanism is divided into three parts, i.e., current reference generation (CRG)



(a)



(b)

Figure 2.13: (a) Closed-loop control configuration, and (b) modulated waveforms and PWM gate switching pulses of the proposed 9L9S-CGSC-TL inverter [75].

stage, PR controller, and LS-SPWM technique, in which their details are discussed next.

Considering a PV array injecting its maximum active power, $P^\star$, to the grid, and regarding the intended preassumed value of the reference reactive power, $Q^\star$, the CRG stage of the proposed control mechanism needs the phase and amplitude information of the grid to tune the required value of the reference current, $i_g^\star$. Such information can

be either found by a phase-locked loop block or through a grid voltage observer (GVO) technique. In this work, the latter one is used, since GVO can remove the high frequency ripple component of the injected grid current. This observer requires only the measured voltage of the HFac grid at the PCC, v_g, and its output can effectively cancel out the effect of any distortion caused by HF noises in the grid voltage measurement process.

To digitally implement the PR controller with a reduced-order state GVO, a zero-order hold (ZOH) approximation is used to transfer the system model from the continuous-to the discrete-time domain. Hence, assuming $v_{g\alpha}(k) = v_g(k)$ as the measured grid voltage at sampling instant, k, the GVO vector can be expressed as $\hat{v}_g(k) = [\hat{v}_{g\alpha}(k)\,\hat{v}_{g\beta}(k)]^T$ in the stationary $\alpha\beta$ frame. Therefore, by assuming a sinusoidal grid voltage and applying a time derivative to it, the discrete-time model for $v_g(k)$ after invoking the ZOH discretization is expressed by:

$$v_g(k+1) = \Phi v_g(k) \tag{2.12}$$

$$y(k) = C v_g(k) \tag{2.13}$$

where $v_g(k+1)$ is the grid voltage vector at the next sampling instant, k+1, and $y(k)$ is the desired output of the GVO. In (2.12) and (2.13), Φ and C are:

$$\Phi = \begin{bmatrix} \cos(T_s\omega_g) & -\sin(T_s\omega_g) \\ \sin(T_s\omega_g) & \cos(T_s\omega_g) \end{bmatrix}, C = \begin{bmatrix} 1 & 0 \end{bmatrix} \tag{2.14}$$

where T_s and ω_g are the sampling frequency of the controller and the angular term at the grid fundamental frequency, respectively. Since (2.12) and (2.13) can meet the observability condition for such a linear system, a GVO can be derived as follows:

$$\hat{v}_g(k+1) = \Phi\hat{v}_g(k) - L(v_{g\alpha}(k) - \hat{v}_{g\alpha}(k)) \tag{2.15}$$

where $L = [\lambda_1\ \lambda_2]^T$ is a matrix to adjust the bandwidth of the observer to reject HF noises. Hence, the observer characteristic equation in the z domain is given by:

$$\det(zI - (\Phi + LC)) = z^2 + \sigma_1 z + \sigma_2 \tag{2.16}$$

The desired poles of σ_1 and σ_2 can be obtained using:

$$\begin{aligned} \sigma_1 &= -2e^{-\zeta\omega_n T_s}\cos(\omega_n T_s\sqrt{1-\zeta^2}) \\ \sigma_2 &= e^{-\zeta\omega_n T_s} \end{aligned} \tag{2.17}$$

where ζ is the damping factor and ω_n is the neutral frequency term. Considering (2.17)-(2.18) with the help of the pole placement approach, two components of L are found as

Table 2.1: Working principle of the implemented LS-SPWM with the ON switching states of the proposed 9L9S-CGSC-TL inverter governed by a PR controller [75].

$d(k)$ Polarity	LS-SPWM Condition	ON State Switches	v_{inv}
Positive	$\|4d(t)\| \geq A_{C1}$	S_1, S_2, S_5, S_6, S_9	$2V_{dc}$
	$A_{C2} \leq \|4d(t)\| < A_{C1}$	S_1, S_2, S_5, S_6, S_8	$1.5V_{dc}$
	$A_{C3} \leq \|4d(t)\| < A_{C2}$	$S_1, S_4, S_3, S_5, S_6, S_9$	V_{dc}
	$A_{C4} \leq \|4d(t)\| < A_{C3}$	$S_1, S_4, S_3, S_5, S_6, S_8$	$0.5V_{dc}$
Negative	$\|4d(t)\| \geq A_{C1}$	S_2, S_3, S_4, S_7, S_9	$-2V_{dc}$
	$A_{C2} \leq \|4d(t)\| < A_{C1}$	$S_1, S_4, S_3, S_5, S_7, S_8$	$-1.5V_{dc}$
	$A_{C3} \leq \|4d(t)\| < A_{C2}$	$S_1, S_4, S_3, S_5, S_7, S_9$	$-V_{dc}$
	$A_{C4} \leq \|4d(t)\| < A_{C3}$	S_1, S_2, S_5, S_7, S_8	$-0.5V_{dc}$
-	$\|4d(t)\| < A_{C4}$	S_1, S_2, S_5, S_7, S_9	0

follows:

$$\begin{aligned} \lambda_1 &= \frac{\sigma_1 \cos(T_s\omega_g) + 2\cos^2(T_s\omega_g) + \sigma_2 - 1}{\sin(T_s\omega_g)} \\ \lambda_2 &= \lambda_1 + 2\cos(T_s\omega_g) \end{aligned} \tag{2.18}$$

With respect to (2.15) and (2.18), the estimated grid voltage vector at the next sampling instant, k+1, can be obtained. As a result, the reference current value governing the proposed 9L9S-CGSC-TL grid-connected inverter can be expressed as follows:

$$i_g^\star(k+1) = \frac{2P^\star}{V_m^2}\hat{v}_{g\alpha}(k+1) - \frac{2Q^\star}{V_m^2}\hat{v}_{g\beta}(k+1) \tag{2.19}$$

where V_m^2 is the square value of the grid peak voltage, which can be obtained as:

$$V_m^2 = (\hat{v}_{g\alpha}(k+1))^2 + (\hat{v}_{g\beta}(k+1))^2. \tag{2.20}$$

The aim of this PR controller is to track a sinusoidal current reference, $i_g^\star(k+1)$, as per (2.19), by reducing the tracking error, $e(k) = i_g(k) - i_g^\star(k)$. It is important to emphasize that in this case, the grid voltage acts as a disturbance at the fundamental frequency. A simple way to design a PR controller is to firstly design a PI controller by tuning K_p and K_i. Afterwards, this can be translated into a PR controller by replacing the integral part as follows:

$$\frac{1}{S} \Rightarrow \frac{2S}{S^2 + \omega_g^2} \tag{2.21}$$

Finally, the PR controller can be expressed in the discrete-time domain by:

$$C_{PR}(z) = \frac{d(k)}{e(k)} = \frac{a_0 z^2 + a_1 z + a_2}{z^2 - 2\cos(\omega_g T_s) z + 1} \tag{2.22}$$

where,

$$\begin{aligned} a_0 &= K_p \\ a_1 &= \frac{2K_i}{\omega_g}\sin(\omega_g T_s) - 2K_p\cos(\omega_g T_s) \\ a_2 &= K_p - \frac{2K_i}{\omega_g}\sin(\omega_g T_s) \end{aligned} \tag{2.23}$$

Considering the proposed grid-tied inverter with the L-type filter as a first-order plant, proper values for a_0, a_1, and a_2 are obtained through the respective Bode frequency response, aiming an acceptable tracking performance and also a good noise rejection capability. The output of such a PR controller gives the desired value of the modulation index, $d(k)$, while reducing the instant error. Considering this, the instantaneous value of the proposed inverter output voltage, $v_{inv}(k)$, can be obtained as:

$$v_{inv}(k) = 2d(k)V_{dc} \tag{2.24}$$

where $d(k) \in [-\mathbb{1}, \mathbb{1}]$. To compensate the delay during the computation, the estimated value of $i_g(k+1)$ can be projected ahead by the following discrete-time dynamic equation:

$$i_g(k+1) = \left(1 - \frac{r_g}{L_g}T_s\right) i_g(k) + \frac{T_s}{L_g}(v_{inv}(k) - \hat{v}_{g\alpha}(k)) \tag{2.25}$$

where r_g is the internal parasitic resistance of the L-type filter with an effective inductance value of L_g. To generate all the required gate switching pulses of the proposed 9L9S-CGSC-TL inverter, $4d(t)$, should be sent to the LS-SPWM stage, as shown in Fig. 2.13(a). At this stage, four in phase LS carriers named as A_{C1}, A_{C2}, A_{C3}, and A_{C4}, are needed to compare with $4d(t)$. Herein, to generate all the PWM pulses of the proposed inverter with a fixed switching frequency operation, the frequency of the LS carriers must be accorded with the sampling time used in the PR and GVO processes. The PWM pulses of all the involved switches of the proposed inverter are illustrated in Fig. 2.13(b). Considering Fig. 2.13(b) and regarding the current flowing path analysis conducted in Fig. 2.12, the principle of the implemented LS-SPWM with the list of ON switching states of the involved switches per each output voltage level have been tabulated in Table 2.1. Here, to avoid using the additional carriers, an absolute function of $4d(t)$ has been considered.

2.4.2 Design Guidelines

To determine a correct capacitance value for the involved capacitors, their LDT interval, (α, β), the passing current through them, $i_{C_i}(t)$, and their maximum voltage drop within the LTD have to be identified using the following equation:

$$\Delta V_{C_i} = \frac{1}{C_i}\int_{\alpha}^{\beta} i_{Ci}(t)d(t). \forall i \in \{1,2,3\}. \tag{2.26}$$

Concerning different current flowing paths of the proposed topology shown in Fig. 2.12, it is deduced that the LDT interval for C_1 is within the switching sequence of the third positive ($+1.5V_{dc}$) and the top positive ($+2V_{dc}$) output voltage levels, while as for the C_2 it occurs during the second negative ($-V_{dc}$), the third negative ($-1.5V_{dc}$), and the top negative ($-2V_{dc}$) output voltage levels generation. On the other hand, considering a unity PF condition of the injected grid current, which is the worst case in the capacitance determination, the LDT for C_3 can be considered during the first and the third positive output voltage level generation. Hence, taking such LDTs along with the implemented LS-SPWM principles into account, the current function passing through the capacitors in one quarter of full fundamental cycle can be expressed as follows:

$$i_{C_1}(t) = i_g(t),\ \forall t \in\ [t_z, \frac{T}{4}) \tag{2.27}$$

$$i_{C_2}(t) = \begin{cases} (2-d(t))i_g(t),\ \forall t \in\ [\frac{T}{2}+t_y, \frac{T}{2}+t_z) \\ i_g(t),\ \forall t \in\ [\frac{T}{2}+t_z, \frac{3T}{2}) \end{cases} \tag{2.28}$$

$$i_{C_3}(t) = \begin{cases} 4d(t)i_g(t),\ \forall t \in\ [0, t_x) \\ (4-2d(t))i_g(t),\ \forall t \in\ [t_z, \frac{T}{4}) \end{cases} \tag{2.29}$$

where, considering, D_m as the maximum value of $d(t)$ at the steady-state condition, the voltage levels transition time of t_x, t_y, and t_z is equal to $\frac{1}{\omega_g}\sin^{-1}\left(\frac{0.25}{D_m}\right)$, $\frac{1}{\omega_g}\sin^{-1}\left(\frac{0.5}{D_m}\right)$, and $\frac{1}{\omega_g}\sin^{-1}\left(\frac{0.75}{D_m}\right)$, respectively.

Regarding (2.27)-(2.29), and taking a sinusoidal function for both $d(t)$ and $i_g(t)$ into account, the required capacitance of the involved capacitors can be obtained as follows:

$$\begin{aligned} C_1 &= \frac{2I_m}{\omega_g \Delta V_{C1}}\cos\left(\sin^{-1}\left(\frac{0.75}{D_m}\right)\right) \\ C_2 &\approx \frac{2I_m}{\omega_g \Delta V_{C2}}\cos\left(\sin^{-1}\left(\frac{0.75}{D_m}\right)\right) + \frac{I_m}{8\omega_g \Delta V_{C2}} \\ C_3 &\approx \frac{I_m(8+D_m)}{\omega_g \Delta V_{C3}}\cos\left(\sin^{-1}\left(\frac{0.75}{D_m}\right)\right) - \frac{D_m I_m \pi}{\omega_g \Delta V_{C3}} \end{aligned} \tag{2.30}$$

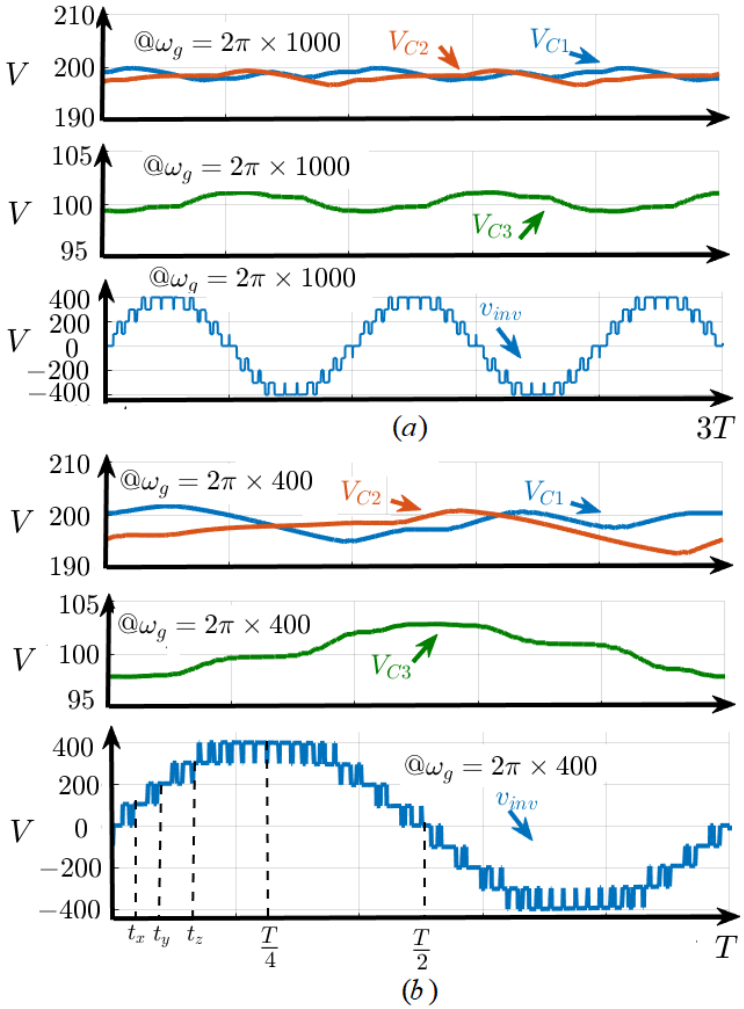


Figure 2.14: Voltage ripple across the capacitors with the 9L output voltage of the inverter at (a) 1-kHz, and (b) 400-Hz fundamental frequency and 20-kHz switching frequency [75]

where, I_m is the maximum value of the injected grid current. Regarding (2.30), it can be realized that the required capacitance for the SC network capacitors is smaller than the C_3 in the FC cell, while owing to the longer LDT interval, C_2 possesses larger capacitance than C_1. Considering a peak of 8 A injected grid current as for a 1.2-kW injected power at 400 Hz fundamental frequency, and regarding 200 V as the input dc voltage value, the capacitance of C_1, C_2, and C_3 are chosen as 220 μF, 330 μF, and 480 μF, respectively. Having taken these assumptions into account, the typical waveforms of the voltage ripple across the capacitors with the resultant 9L output voltage of the proposed inverter have been illustrated in Fig. 2.14. In this case, to better reflect the importance of the fundamental frequency on the voltage ripple values of the involved capacitors, the results are illustrated for two cases. e.g., 400-Hz and 1-kHz fundamental frequency. As can be

Table 2.2: A comparison between the proposed 9L9S-CGSC-TL inverter and other existing 9L-based inverter counterparts.

Type of Converter	No. of Components				Max No. of ON-Switches	Output Voltage Gain	No. of DC Sources	Leakage Current	TSV (pu)/ MVS	Reported Rated Efficiency
	S	D	C	L						
Pure SC-Based [84]	12	2	4	1	6	Double	Double	High	$8/2V_{dc}$	83%@500Hz/60W
Pure SC-Based [85]	9	2	3	1	4	Double	Single	High	$5.75/2V_{dc}$	94.2%@1kHz/200W
Hybrid SC/FC-Based [86]	8	2	3	1	4	Double	Single	High	$6/2V_{dc}$	96.4%@50Hz/500W
ABNPC-Based [29]	12	-	4	1	7	Unity	Single	Low	$12/V_{dc}$	NA@50Hz/100W
Hybrid SC/FC-Based [87]	8	1	3	1	4	Double	Single	High	$5/2V_{dc}$	96.5%@50Hz/330W
Pure SC-Based [88]	10	2	3	1	5	Double	Single	High	$4.5/V_{dc}$	97.12%@50Hz/850W
Pure SC-Based [89]	10	1	3	1	5	Double	Single	High	$6/2V_{dc}$	96%@50Hz/600W
Pure SC-Based [48]	10	3	4	1	5	Quadruple	Single	Low	$5.5/3V_{dc}$	95.2%@50Hz/1kW
Pure SC-Based [90]	11	-	3	1	5	Double	Single	High	$5.5/V_{dc}$	NA@50Hz/300W
Pure SC-Based [91]	12	-	4	1	4	Quadruple	Single	High	$6/4V_{dc}$	96%@50Hz/50W
Pure SC-Based [92]	8	3	4	1	4	Quadruple	Single	High	$5.75/4V_{dc}$	93%@50Hz/500W
Pure SC-Based [93]	8	2	4	1	4	Unity	Quadruple	Low	$5.5/4V_{dc}$	96%@50Hz/1kW
Pure SC-Based [94]	10	4	3	1	5	Double	Single	High	$5.75/2V_{dc}$	97%@50Hz/270W
Boost SC-Based [95]	12	2	5	3	6	Double	Single	Low	$6/2V_{dc}$	95.6%@50Hz/500W
CGSC-Based [73]	14	-	5	2	7	Quadruple	Single	Zero	$7.5/4V_{dc}$	98.3%@50Hz/600W
Proposed 9L9S-CGSC inverter	9	1	4	2	6	Double	Single	Zero	$5/2V_{dc}$	97.5%@400Hz/1.2kW

realized, the voltage ripple values of all the integrated capacitors at 400-Hz fundamental frequency is under 5% of their nominal rated voltage. It can also be observed that by increasing the value of the fundamental frequency, such capacitors voltage ripples can be further reduced.

2.4.3 Comparative Study

In order to compare the circuit features and effectiveness of the proposed 9L9S-CGSC-TL inverter with some of the other recently proposed 9L-based inverter counterparts, a comparative discussion is conducted in this section. The comparative items include the number of switching devices, required passive components (considering the input capacitor and an output L-type filter for PV application), maximum number of on-state power switches, output voltage gain, number of required dc voltage sources, the state of leakage current attenuation, the per unit value of the TSV with the maximum value of the MVS across the switches, and the overall reported rated efficiency. The results of this comparative study are shown in Table 2.2.

As can be seen, among all the 9L-based compared inverters, only the proposed topology and the one proposed in [73] have an inherent CG feature, which leads to alleviate the leakage current concern for a PV-based grid-tied TL inverter. However, the number of switching devices used in [73] is much higher than the proposed topology.

From this perspective, the 9L ABNPC-based topology proposed in [86], and the one introduced in [93], are also able to mitigate the leakage current through the mid-point clamping technique rather than the CG concept. However, their structure provides a

Table 2.3: Parameters used for the experimental prototype [75]

Element	Type and Description
Power Switches	IPDD60R080G7- 650 29@25C
Power Diode	IDDD20G65C6- 65051
Microprocessor	DSP-TMS320F28379D
Switching Frequency	20
C_1, C_2, and C_3	0.33mF & 0.33mF&0.48mF
Gate Drivers	UCC21520DW
Isolated dc/dc Converters	DCP020515DU/1K
Current Sensor	AMC 1200
Voltage Sensor	ISO224B

unity voltage gain, and the one proposed in [93] even needs multiple dc-link input voltages. On the other hand, among all the mentioned topologies, only the hybrid SC/FC-based structure presented in [85], the fully SC-based topology with quadruple voltage boosting gain proposed in [92], and the hybrid and fully SC-based inverters presented in [87] and [93] offer the same number of output voltage levels with one switch less than the proposed one. Nonetheless, none of them can be a suitable choice for PV-based applications, since the concern of leakage current still remains. Additionally, they need extra diodes compared to the proposed 9L9S-CGSC-based inverter, while their overall TSV and the MVS across the switches are larger than the proposed one. In this case, the 9L SC-based inverter proposed in [93] can only offer a unity output voltage gain, as well. Hence, it needs an enhanced dc-link voltage to meet the peak amplitude of the grid. Excluding the structure proposed in [87], the per-unit TSV value of all the eight-switch based 9L inverters presented in [86], [92], and [93], are higher than the proposed one. Conversely, the 9L inverter proposed in [87] suffers from large discontinuous inrush current in the SC side. This is an additional setback rather than inducing the leakage current concern due to its variable CMV. The CG-based circuit feature, which guarantees almost zero leakage current propagation issue, the unity ratio of $\frac{N_{Level}}{N_{Switch}}$ with smaller TSV/MVS, self-voltage balancing of the involved capacitors with smaller balanced voltage value, and a double-voltage boosting characteristic within a single-power processing stage, make the proposed topology an attractive option for HFac grid integration feeding through RE sources.

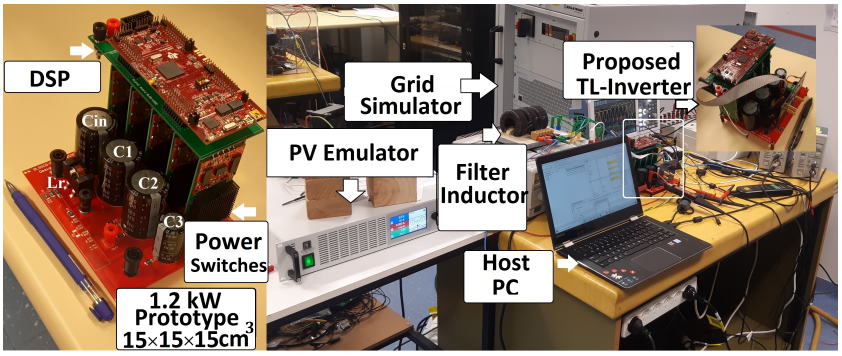


Figure 2.15: Picture of the 1.2-kW prototype with the measurement setup [75].

2.4.4 Open-Loop Experimental Results

Experimental validation of the proposed 9L9S-CGSC-TL inverter have been carried out by developing/fabricating a 1.2-kW laboratory prototype. The main components used in the prototype are shown in Table 3.3, and a picture of the built prototype ($15 \times 15 \times 15 cm^3$) with the HF grid-integration setup is illustrated in Fig. 2.15. Herein, an Elektro-Automatik PV emulator (model EA-PSI-9750-12) is used as an adjustable dc laboratory power supply to electrically feed the proposed inverter. The HF grid-voltage is also generated by a four-quadrant grid-simulator REGATRON TC30.528.43-ACS, where the grid peak voltage and the grid frequency are adjusted to be 311 V and 400-Hz, respectively. An LC input filter with $L_r = 33\ \mu H$, $C_{in} = 0.47$ mF is incorporated to offer a smooth input current waveform for the PV emulator. The experimental performance of the proposed 9L9S-CGSC-TL inverter is verified through both open-and closed-loop grid integration results presented in the following subsections. Owing to the fabricated prototype with a compact PCB design, current stress analysis of the proposed topology is developed by the simulation, where the loss breakdown results with overall efficiency evaluation are conducted using the PLECS software.

For the open-loop performance, a series connection of an adjustable RL-load is used. Herein, instead of using the closed-loop modulation index obtained from the explained PR controller, a simple sinusoidal reference waveform associated with the described LS-SPWM mechanism is employed to obtain the PWM signals. Fig. 2.16(a) shows the input current i_{in}, the 9L-inverter output voltage, and the load current i_{out} waveforms. Here, the input voltage is set at 200 V and the peak value of the modulation index is set at 0.85, which leads to 400 V as the peak value of the inverter output voltage. The frequency of v_{inv} is 400-Hz and the load resistance and inductance are 30 and 10mH, respectively. As can be seen, the peak value of load current is around 7.5A, which leads

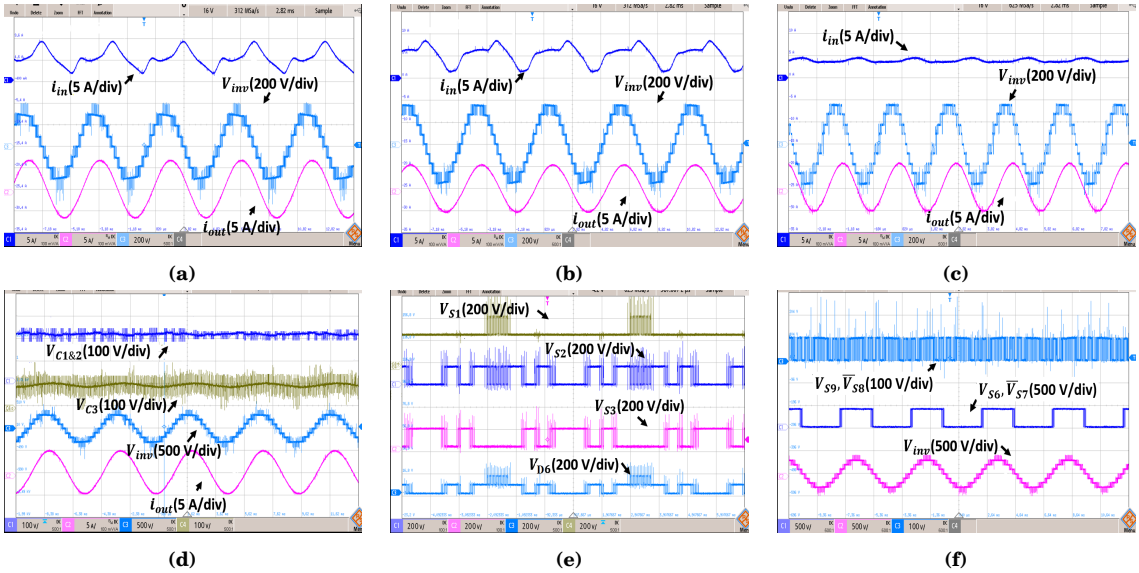


Figure 2.16: Experimental waveforms of the proposed 9L9S-CGSC-TL inverter in open-loop condition. (a) The peak value of the modulation index equals to 0.85 and V_{dc} = 200 V for 400-Hz load; (b) the peak value of the modulation index equals to 1 and V_{dc} = 180 V for 400-Hz load; (c) the peak value of the modulation index equals to 1 and V_{dc} = 190 V for 1-kHz load; (d) the voltages across the capacitors; (e) and (f) MVSs across the switches [75].

to around 1.1-kW output power. Regarding the incorporated LC input filter, the input current waveform possesses a smooth trend without having a significant inrush current. The same test with the input dc voltage of 180 V and the full modulation index value has also been conducted. The related results of the proposed topology can be observed in Fig. 2.16(b), where the peak value of v_{inv} in the fundamental frequency is 360 V, leading to a double voltage boosting feature achieved with a single-power processing stage.

To show the capability of the proposed 9L9S-CGSC-TL inverter to operate at higher range of output frequency, a 1 kHz fundamental frequency is selected, while the input dc voltage value is set at 190 V with full modulation index. The switching frequency of the implemented LS-SPWM is the same as the previous case (20-kHz). The experimental results of this case study are shown in Fig. 2.16(c). As can be seen, by increasing the value of the fundamental frequency, the i_{in} waveform is smoother without having any large ripple. Based on the measured experimental data, the THD of the load current in all the above-cases was less than 1.5%. Next, the balanced voltage of the involved capacitors in the 400 Hz fundamental frequency, the 9L output voltage waveform of the proposed inverter as well as the load current are shown in Fig. 2.16(d). Here, the input dc voltage is set at 200 V. As is expected, both the capacitors voltages of the SC network are balanced at 200 V, while C_3 from the FC-side is balanced at 100 V without requiring any additional voltage balancing procedure. In this case, the MVS waveforms of all the switches and the incorporated diode are also shown in Fig. 2.16(e) and (f). As can be seen,

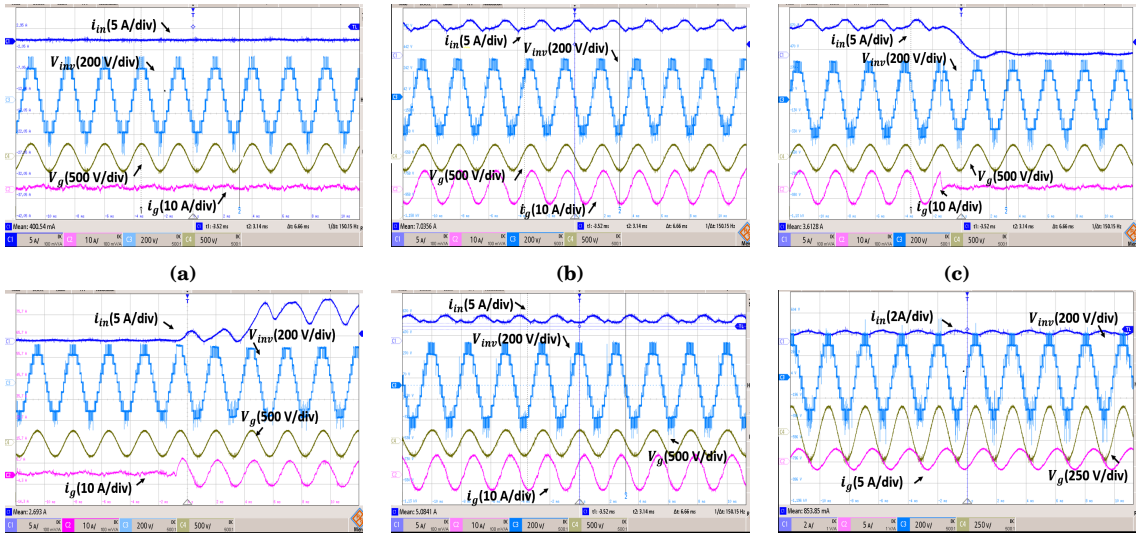


Figure 2.17: Experimental waveforms of the proposed inverter in the closed-loop grid-tied condition. (a) With zero current injection; (b) 1.2-kW full power injection; (c) dynamic condition from 1.2-kW injected power to zero power; (d) dynamic condition from zero injected power to 1.2-kW active power; (e) 1.2-kVA reactive power support mode; and (f) 0.5-kVA reactive power support mode [62].

all the switching devices of the SC network should tolerate 200 V (the input dc voltage value), whilst only the switches S_6, and S_7 must bear the MVS, 400 V. In this regard, the MVS of both switches in the FC-side is 100 V.

2.4.5 Closed-Loop Experimental Results

As for the closed-loop control implementation under 400-Hz grid-connected condition, a simple L-type filter with the values $L_g = 1.8$ mH and $r_g = 0.33$ is utilized. The input voltage value is set at 200 V, while the peak of the grid voltage is 311 V. Regarding the control strategy, both the GVO and PR controller are digitally implemented and synchronized with the LS-PWM stage, i.e., $T_s = 50\mu s$. The GVO is tuned by choosing $\zeta = 0.707$ and $\omega_n = 2\pi \times 400$ rad in order to ensure good HF noise rejection. Hence, considering (3.14) and (3.15), the observer gain is tuned with $\lambda_1 = 0.3362$ and $\lambda_2 = 0.2750$. The PR controller was designed by following the procedure described in [75]. Thus, with respect to (3.20), the PR controller parameters were set with $a_0 = 19.9$, $a_1 = -35.5$, and $a_2 = 15.9$. Fig. 2.17(a)-(f) shows the details of the obtained experimental results under the closed-loop grid-tied condition, where the waveforms of i_{in}, v_{inv}, v_g, and i_g are shown. The experimental results have been captured based on zero current injection, $i_g^\star = 0$ [Fig. 2.17(a)], and 1.2-kW full active power injection, where the peak of injected current is 8 [Fig. 2.17(b)], and the dynamic results from 1.2 kW to zero active power injection and

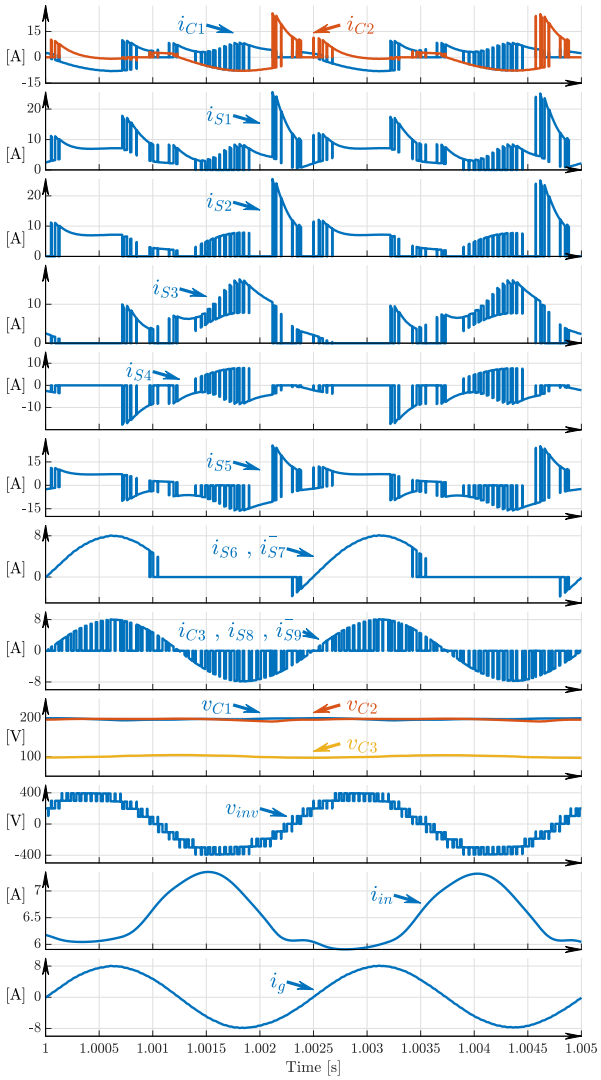


Figure 2.18: Details of the simulation results at 1.2 kW injected power [75].

vice versa [Fig. 2.17(c) and (d)]. Herein, the injected grid current THD at the steady-state full rated power [Fig. 2.17(b)] was around 2.1%. The higher percentage of the measured grid current THD in comparison with the open-loop experimental observations is due to the presence of the unwanted HF noise in the grid current sensor board. Also, the reactive power support results are shown in Fig. 2.17(e) and Fig. 2.17(f). Here, the converter injects 1.2-kVA and 0.5-kVA with a lagging power factor to the grid in both the cases. The closed-loop performance of the proposed topology generating all the 9L in the output voltage and injecting a quality sinusoidal grid current with a fast dynamic response can be confirmed through these results. Herein, the measured efficiency of the proposed 9L9S-CGSC-TL inverter at full rated active power was 97.5%, where the input power obtained from the PV emulator was 1.24-kW, and the losses associated with the

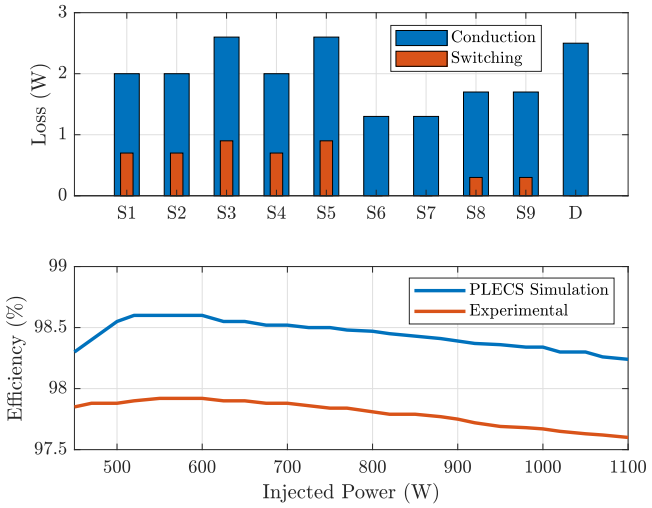


Figure 2.19: Loss and efficiency analysis [75].

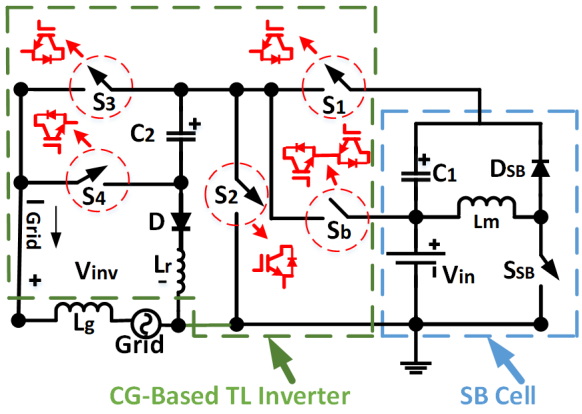


Figure 2.20: The proposed CGSB5L-TL inverter topology [96].

L-type filter were about 10 W.

2.4.6 PLECS Simulation Results

In order to further analyze the performance of the proposed 9L9S-CGSC-TL inverter from the current stress profile of the involved switches and capacitors viewpoint, a simulation result at the rated power of 1.2-kW and under the described closed-loop grid-tied condition is presented in this subsection. The simulation parameters are the same as given in Table 2.3, while the input dc source voltage is set at 200 V. In this case, a 400 Hz grid is considered with 311 V peak of the voltage, while the peak of reference current for the PR controller is 8 A. Fig. 2.18 shows the details of this simulation test

within two fundamental grid cycles. As can be seen, the simulation results have a good agreement with the theory and the experimental observations, while thanks to the incorporated LC input filter, the current passing through the SC-network capacitors does not possess any large inrush spikes. As expected, only five front-end power switches in the SC network should pass this alleviated charging current of the capacitors, whereas the peak of current stress for them is around 20 A for the rated 1.2-kW injected power. Herein, the capacitor C_3 can only see the chopped waveform of the injected grid current. Hence, four remaining power switches have to conduct 8 A of the injected current as their respective current stress. The balanced voltage of the involved capacitors and the smooth waveform of the input current without having any large inrush spikes can also be reconfirmed in Fig. 2.18.

Considering the current stress profile of the involved semiconductor devices, and regarding their internal parasitic resistance, a loss analysis at the rated 1.2-kW injected power using the PLECS has been conducted as shown in Fig. 2.19. Considering 20-kHz switching frequency, and the low value of the MVS across the switches, the switching losses of the converter are negligible. Moreover, thanks to the higher current stress profile, the SC network switches and the power diode dissipate larger values of the conduction loss than other switches. A comparative efficiency curve between the results extracted from PLECS and the data obtained from the measurement over a wide range of output power is shown in Fig. 2.19. In this case, a Voltech PM3000A Universal Power Analyzer is used to measure the overall efficiency of the proposed converter in practice.

2.5 CG-Based 5L Inverter: A hybrid SC and SB topology

So far, all the proposed topologies were based on the SC-technique, where, the inrush current problem and higher current stress profile of the switches were the major shortcomings of the proposed topologies. In following, a new CG-based TL inverters is proposed, the concern of large discontinuous current stress in both the input and switches current profile is mitigated using a hybrid approach, i.e., integration of the SC and SB technique.

The overall circuit configuration of the proposed CGSB5L-TL inverter topology with its relevant power switches realization is shown in Fig. 2.20 [96]. As can be observed, the proposed topology offers a CG feature, where the negative terminal of the input dc-source source, V_{in}, and the grid neutral point have been directly connected. A simple

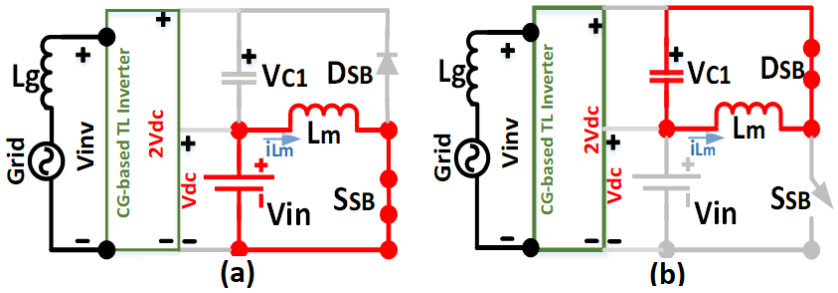


Figure 2.21: Equivalent circuit of the proposed CGSB5L-TL inverter when (a) S_{SB} is ON, and (b) S_{SB} is OFF [96].

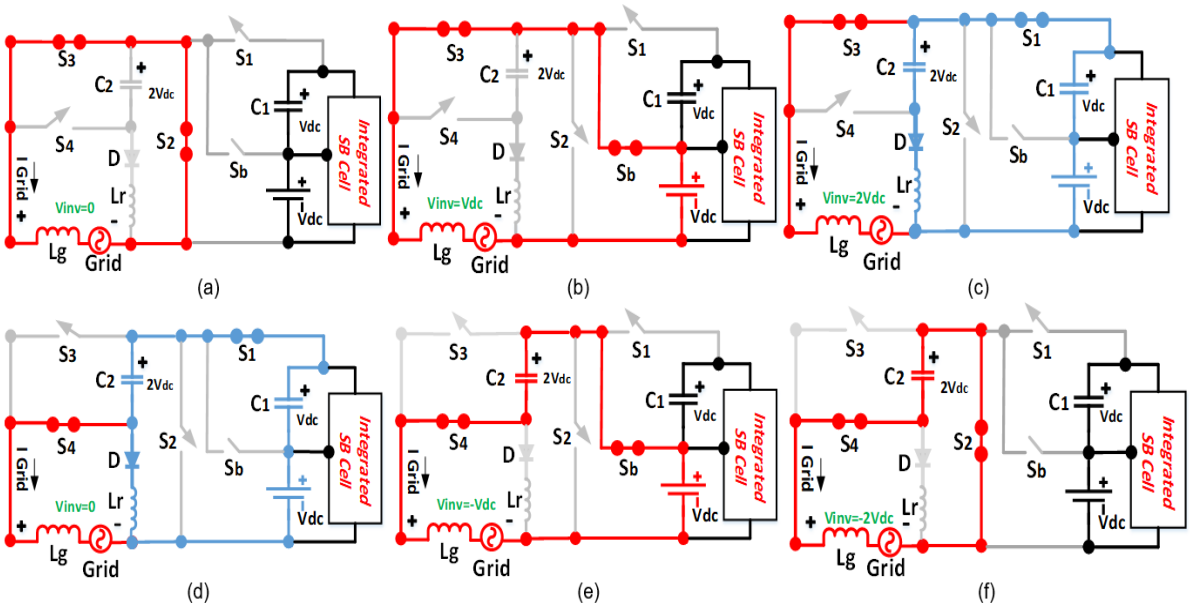


Figure 2.22: Current flowing paths of the proposed SBCG5L-TL inverter showing the (a) zero-level of the output voltage in the positive half-cycle (b) first positive level of the output voltage (c) top positive level of the output voltage (d) zero-level of the output voltage in the negative half-cycle (e) first negative level of the output voltage, and (f) top negative level of the output voltage [96].

L-type filter, L_g, is also used to connect the proposed CGSB5L-TL inverter to the grid. Here, all the power switches, excluding the power switch S_b, are unidirectional. Also, L_m and L_r denote the SB cell's inductor and the resonant inductor, respectively, and their role is explored in the following subsections. Similar to other existing CG-based 5L-TL inverters, two capacitors, C_1 and C_2 are used in the proposed topology, where C_2 acts as the virtual-dc link. The working principle of the integrated SB cell, and the circuit description of the proposed topology with its QSC capability are next discussed.

The operating procedure of the proposed integrated SB cell can be realized by Fig. 2.21(a) and (b). Considering Fig. 2.21(a), once the switch S_{SB} is ON, the current through the inductor,i_{Lm}, is constantly increased, while the diode, D_{SB}, is reverse biased. Hence, considering V_{dc} as a fixed dc voltage value of the input dc source and v_{Lm} as the

instant voltage across L_m, the following relation can be expressed:

$$V_{dc} = v_{Lm} \xrightarrow{S_{SB}:ON} \text{Charging of } L_m \tag{2.31}$$

Consequently, whenever S_{SB} is OFF, the diode D_{SB} will be forward-biased as shown in Fig. 2.21(b). In that case, L_m has a negative slope and the capacitor C_1 is charged as follows:

$$v_{Lm} = V_{C1} \xrightarrow{S_{SB}:OFF} \text{Charging of } C_1 \tag{2.32}$$

where, V_{C1} is the steady state voltage of C_1. Therefore, considering the same ON and OFF switching time interval of S_{SB} in (2.4) and (2.5) over a full cycle of switching frequency, and regarding the volt-second balance principle across L_m, V_{C1} would be equal to V_{dc}.

Hence, similar to the conventional series-parallel SC circuit, the proposed integrated SB cell has an inherent voltage boosting feature that can provide two different voltage levels at its output, in which one is related to the direct contribution of the input dc-source, V_{dc}, and the other one is as for series connection of the input dc-source and C_1 voltage ($V_{dc} + V_{C1}$).

The advantages of the proposed integrated SB cell over its series-parallel SC cell counterpart are as follows:

- The proposed integrated SB cell has employed only one power switch as opposed to two used series-parallel power switches of the conventional SC cell, and two-switch-based SB modules used in [67, 97].

- The charging/discharging operation of the involved capacitor is soft since an inductor is involved in the charging current path of the capacitor. Thanks to this, the huge start-up inrush current of the input dc source can also be alleviated. Therefore, unlike the conventional series-parallel SC cell, the current stress and operating thermal profiles of the involved semiconductor devices is quite smooth.

Considering the operating principle of the proposed integrated SB cell, different current flowing paths of the proposed CGSB5L-TL inverter during the generation of different output voltage levels are illustrated in Fig. 2.22(a)-(f). Here, the red and blue lines represent the grid current flowing path and the capacitive charging loop, respectively.

Considering Fig. 2.22(a), in order to make the zero-level of the output voltage during the positive half cycle operation, only two power switches (S_2 and S_3) must be ON. Herein, the internal capacitor of the integrated SB cell can be charged with ON/OFF

switching conversion of S_{SB}; however, C_2 is disconnected from both the dc source and the grid. Then, to make the first positive level of the output voltage, V_{dc}, S_b and S_3 must be ON as depicted in Fig. 2.22(b), whereas similar to the previous stage and because of the upcoming steady state voltage of C_2, the diode D would be reverse biased. Therefore, C_2 is again disconnected from the dc source and the grid. Here, irrespective of what the grid current direction might be, C_1 can be charged to V_{dc} again through the described working principle of the proposed integrated SB cell.

Regarding Fig. 2.22(c), the top positive level of the proposed TL-inverter output voltage ($2V_{dc}$) is generated whenever S_1 and S_3 are ON. As can be found out by the blue lines in Fig. 2.22(c), the diode D is forward-biased at this stage. Thus, by neglecting the voltage drop across L_r and considering the same direction of the injected grid current and the grid voltage, C_2 is charged to the voltage summation of the input dc source and C_1. Here, an QSC path is provided for charging operation of C_2 in which its details will be discussed in the next subsection. Also, unlike the previous stages, the charging operation of C_1 in the integrated SB cell depends on the grid current direction and the power factor (PF) demanded by the grid.

The zero level of output voltage in the negative half cycle of the grid voltage can be again generated through a different current flowing path as depicted in Fig. 2.22(d). Herein, similar to the top positive level of the output voltage, the same QSC path is again provided for C_2 through the ON state switching condition of S_1 and the forward-biased condition of the power diode D, while with the ON state contribution of S_4, the zero level of the output voltage can be transferred to the output. In this case, the charging/discharging operation of C_1 depends on the grid current direction, as well.

Taking Fig. 2.22(e) into account, the first negative level of the output voltage, $-V_{dc}$, is generated by the charged voltage of C_2 and also by the input dc source. Consequently, both switches S_b and S_4 must be ON. It is clear from the grid current flowing path that the charging/discharging operation of C_2 is related to the demanded grid PF, whereas, similar to the first positive level of the output voltage, C_1 can be again charged to V_{dc} through the ON/OFF switching conversion of the integrated SB cell.
Finally, considering Fig. 2.22(f), the top negative level of the output voltage, $-2V_{dc}$, is generated by the sole contribution of C_2 with the ON switching states of S_b and S_4. Here, like the zero positive level of the output voltage, the proposed integrated SB cell is disconnected from the grid current flowing path, while C_2 can be charged/discharged based on the grid current direction.

From the above-mentioned circuit descriptions, the following remarks can be stated:

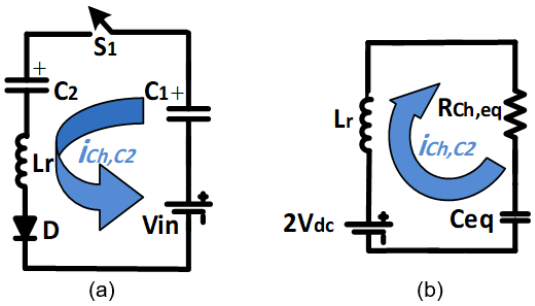


Figure 2.23: Description of the QSC operation (a) main QSC path of the proposed topology (b) equivalent RLC circuit of QSC path [96].

- Like the integrated SB cell capacitor, C_2 can be inherently balanced at $2V_{dc}$ during a full operation over the grid cycle without any need of voltage sensors or balancing procedure.

- The voltage stress across the involved power switches can be summarized as follows:

$$\begin{aligned} V_{Sb,max} &= V_{dc} \\ V_{Si,max} &= 2V_{dc}. \end{aligned} \tag{2.33}$$

  where $i = B, 1, 2, 3, 4$.
  Regarding this, the maximum total standing voltage (MTSV) of the switches for the proposed CGSB5L-TL inverter is $11V_{dc}$.

- Taking the current flowing path analysis into account, the switches S_3 and S_4 are only being ON in the positive and negative half cycles, respectively. Therefore, they are switched based on the grid frequency with almost zero switching power loss, whereas the remaining switches must be commutated through high frequency PWM stages.

As described earlier, the charging loop of C_2 during the top positive and the zero negative output voltage levels generation includes the input dc source, the capacitor C_1, the power switch S_1, the power diode D, the capacitor C_2, and the resonant inductor L_r. This charging loop can give a QSC feature to the proposed topology as shown in Fig. 2.23(a). The equivalent circuit of this charging loop is depicted in Fig. 2.23(b), where C_{eq} and $R_{Ch,eq}$ represent the equivalent capacitance and resistance of the QSC path, respectively. Here, the ON state voltage drop of the power diode D has been neglected. Also, the summation voltage of the input dc source and C_1 in the integrated SB cell ($2V_{dc}$) is considered to provide the balanced voltage of C_2. From Fig. 2.23(b), it is clear that

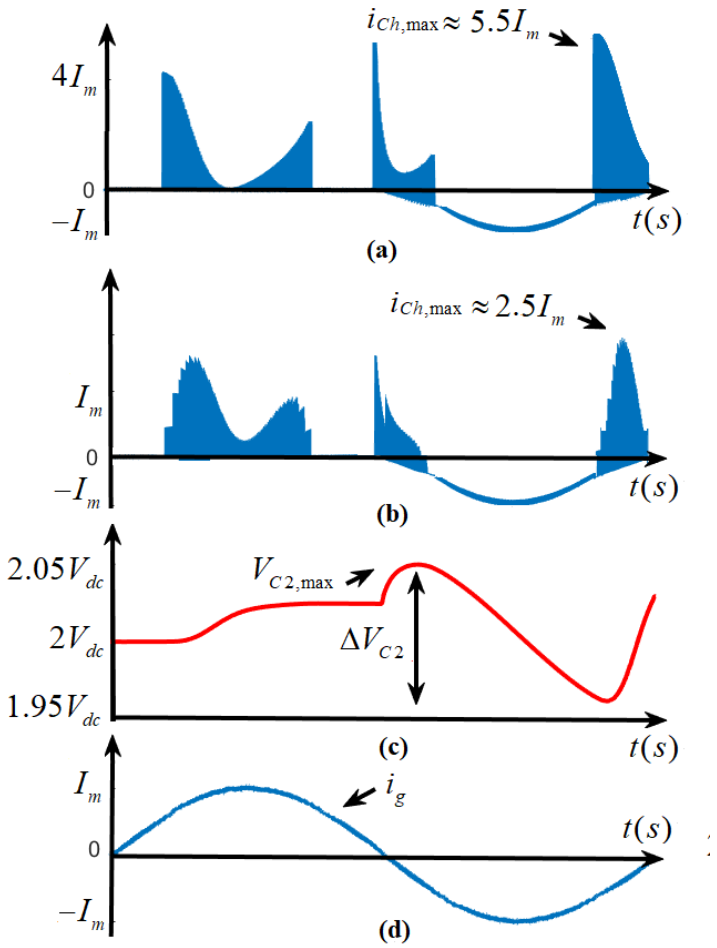


Figure 2.24: Typical waveforms of (a) current passing through C_2 without QSC path, (b) current passing through C_2 with QSC path ($L_r = 22\mu H$), (c), the voltage across C_2 with QSC path (d) the injected grid current with QSC path.

the equivalent RLC series circuit can provide a QSC path for C_2 as long as the under-damped condition of the RLC circuits is fulfilled. Therefore, the following constraint can be expressed:

$$R_{ch,eq} < \sqrt{\frac{4L_r}{C_{eq}}} \tag{2.34}$$

where, all the parasitic ON state resistance of the involved semiconductor devices and the equivalent series resistance (ESR) of the involved capacitors should be included in $R_{Ch,eq}$. Therefore, considering this QSC path, the instantaneous voltage value across C_2 and its required charging current $i_{Ch,C2}(t)$ are obtained:

$$V_{C2}(t) = 2V_{dc} - \frac{\beta}{\omega_r} e^{-\alpha t}(\alpha \sin \omega_r t + \omega_r \cos \omega_r t) \tag{2.35}$$

$$i_{Ch,C2}(t) = \frac{\beta}{\omega_r L_r} e^{-\alpha t} \sin \omega_r t \tag{2.36}$$

where, β, α , and ω_r denote the voltage factor coefficient of C_2, the neper frequency of the QSC path, and the damped quasi-resonant frequency, respectively. The relations of these coefficients can be also expressed as follows:

$$\begin{cases} \beta = 2V_{dc} - V_{C2,max} + \Delta V_{C2} \\ \alpha = \frac{R_{Ch,eq}}{2L_r} \\ \omega_r = \sqrt{\frac{1}{C_{eq}L_r} - \alpha^2}. \end{cases} \tag{2.37}$$

Here, ΔV_{C2} and $V_{C2,max}$ are the maximum allowable voltage ripple and also the maximum voltage value of C_2 during the variation, respectively. It is clear that once $i_{Ch,C2}(t)$ becomes zero, $V_{C2,max}(t)$ reaches its maximum value. Now having taken the importance of such a described QSC path into account and considering (2.10), a standard and feasible value for L_r can be selected. Fig. 2.24(a) and (b), show the typical waveforms of the current passing through C_2 with and without this small resonant inductor of the QSC path, respectively. The waveforms related to the voltage across C_2 along with the injected grid current of the proposed inverter, $i_g(t)$, within a fundamental grid period are illustrated in Fig. 2.24(c) and (d), respectively. Here, the maximum amplitude of $i_g(t)$ is considered I_m. As is clear from Fig. 2.24, the maximum charging current of C_2, $i_{Ch,max}$, becomes more than five times of I_m if no QSC path is provided, while it will be close to $2I_m$ in the presence of the QSC path.

By keeping fixed the integrated SB cell, and extending the series connection of three identical modules of the proposed CG-based TL inverter, a novel single-source single-stage three-phase switched-boost inverter with an inherent CG feature per phase can be attained as shown in Fig. 2.25. The three-phase extension of the proposed CGSB5L-TL inverter can still generate all the five distinctive output voltage levels per phase, while the phase to phase number of output voltage levels can be extended to nine. As clear from Fig. 2.25, the total number of power switches in the three-phase platform of the proposed CGSB5L-TL inverter is 19, while the structure needs only a single boost inductor, four power diodes and four dc-link capacitors. The three-phase working principle of the proposed topology is exactly similar to what presented as for the single phase variant. Here, the integrated SB cell power switch continues its ON/OFF commutation per each switching frequency, while the remaining switches have to be modulated with a sinusoidal PWM stage. The three-phase extension of the proposed CGSB5L-TL inverter is a clear improvement over the existing CG-based TL inverters since they cannot be extended to operate as a three-phase converter with a single dc source. Moreover, owing

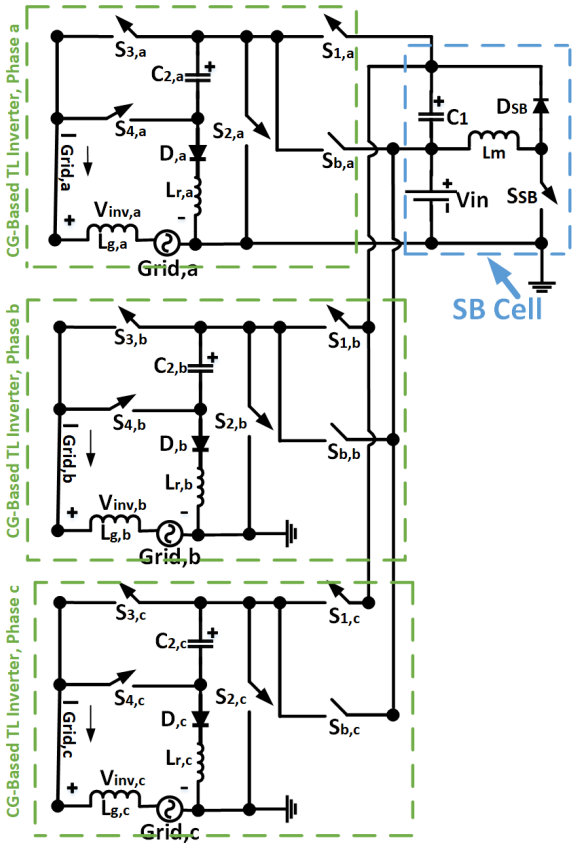


Figure 2.25: Three-phase extension of the proposed CGSB5L-TL inverter [96].

to the incorporated inductor in the SB cell, the input current waveform is free from any pulsating discontinuous waveform. Therefore, the range of application where the proposed CGSB5L-TL inverter can be used is broader than existing CG-based TL-inverters.

2.5.1 CCS-MPC Strategy Applied to the Proposed CGSB5L-TL inverter

Since the involved capacitors of the proposed SBCG5L-TL inverter are inherently balanced during the whole operation, an efficient CCS-MPC technique with a single control objective is used in this work to control the injected grid current. Fig. 2.26 shows the overall control diagram of the proposed PV grid-tied application, where apart from the proposed MPC block, MPPT with a PLL unit are also required to obtain an appropriate value of a sinusoidal current reference $i_{ref}(t)$, which is synchronized with the grid voltage. Here, p_{max}, q_{ref}, ω, and φ, denote the maximum active power available from the PV

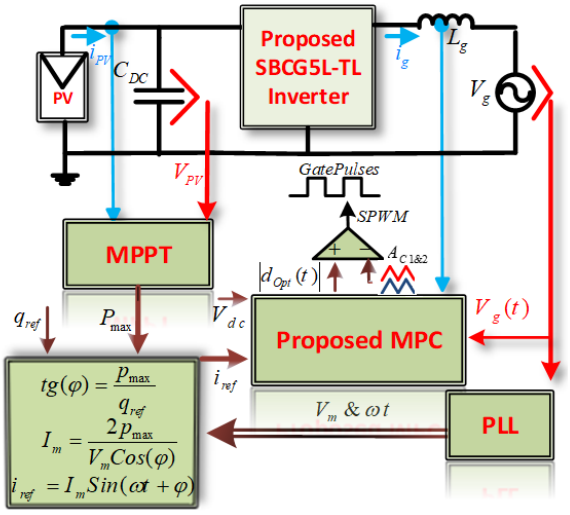


Figure 2.26: Overall control diagram of the proposed CGSB5L-TL inverter with a grid-connected system.

Table 2.4: ON Switching States of the Proposed SBCG5L-TL Inverter Governed by the Proposed CCS-MPC Method.

$d_{SS}(t)$ Polarity	SPWM Condition	ON State Switches	v_{inv}
Positive	$\lvert d_{SS}(t)\rvert \geq A_{C1}$	S_1, S_3	$2V_{dc}$
	$A_{C2} \leq \lvert d_{SS}(t)\rvert < A_{C1}$	S_b, S_3	V_{dc}
	$\lvert d_{SS}(t)\rvert < A_{C2}$	S_2, S_3	0
Negative	$\lvert d_{SS}(t)\rvert \geq A_{C1}$	S_2, S_4	$-2V_{dc}$
	$A_{C1} \leq \lvert d_{SS}(t)\rvert < A_{C2}$	S_b, S_4	$-V_{dc}$
	$\lvert d_{SS}(t)\rvert < A_{C2}$	S_1, S_4	0

panel through the MPPT unit, the required value of the reactive power needed as for LVRT operation, the grid angular frequency term, and the required phase difference for the reactive power injection, respectively. Regarding Fig. 2.26, it is assumed that the grid voltage has the following form: .

$$v_g(t) = V_m \sin(\omega t) \tag{2.38}$$

Thus, the required current reference can be expressed as follows:

$$i_{ref}(t) = I_m \sin(\omega t + \varphi) \tag{2.39}$$

These two reference parameters can be derived in terms of p_{max} and q_{ref} as depicted in Fig. 2.26.

The proposed MPC technique is formulated to obtain an optimal modulating signal, $d_{\mathrm{Opt}}(t)$, to govern the single-phase grid-connected system; hence, it belongs to the CCS-family of the MPCs. Consequently, the modulation stage has to be directly taken into

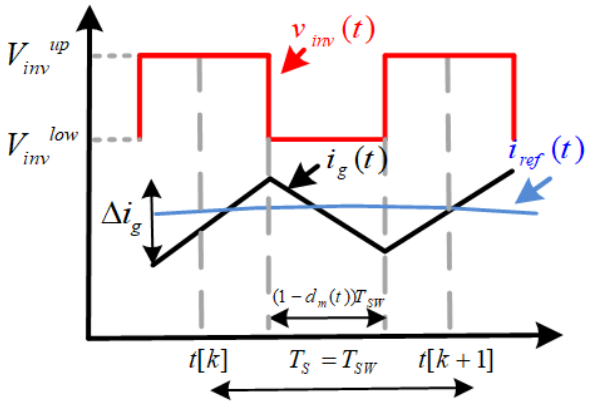


Figure 2.27: The proposed CCS-MPC description with a fixed switching frequency.

account by the proposed MPC. This allows the converter to operate with a fixed switching frequency, in contrast to its FCS-MPC counterpart. Here, a simple SPWM strategy with an absolute function of $d_{\mathrm{Opt}}(t)$ over the grid frequency and two level-shifted high frequency triangular carrier waveforms (A_{C1} and A_{C2}) are used in the modulation stage process. Triggering the gate of three high frequency power switches, S_1, S_2, and S_b, needs such a controlled modulator signal to be incorporated into the modulation. Moreover, the PWM signal of the remaining high frequency power switch from the integrated SB module, S_{SB}, needs a constant 50% duty cycle. Regarding the working principle of the proposed SBCG5L-TL inverter, two power switches, S_3 and S_4 have to be commutated within a grid fundamental frequency in the positive and negative half-cycle of the grid voltage, respectively. Through this way, all the five distinctive output voltage levels of the proposed SBCG5L-TL-inverter are generated. Since the aim of the proposed CCS-MPC technique is to track $i_{ref}(t)$ with a fixed switching frequency operation, the sampling time of the proposed CCS-MPC technique must be synchronized with the frequency of both carrier waveforms used in the SPWM process i.e., f_{sw}=1/T_{sw}. Triggering the gate of the switches in the three-phase application of the proposed topology follows the same rules, where the duty cycle of the switch S_{SB} is independent from the rest of the switches. Here, by changing the phase of $i_{ref}(t)$ and the grid voltage, a specific $d_{\mathrm{Opt}}(t)$ is obtained per each phase that must be integrated into the same LS-SPWM stage to generate the desired PWM signals.

In order to formulate the proposed CCS-MPC and to obtain $d_{\mathrm{Opt}}(t)$ per each phase, the following continuous-time dynamic model can be obtained:

$$\frac{di_g(t)}{dt} = \frac{v_{inv}(t) - v_g(t)}{L_g}. \tag{2.40}$$

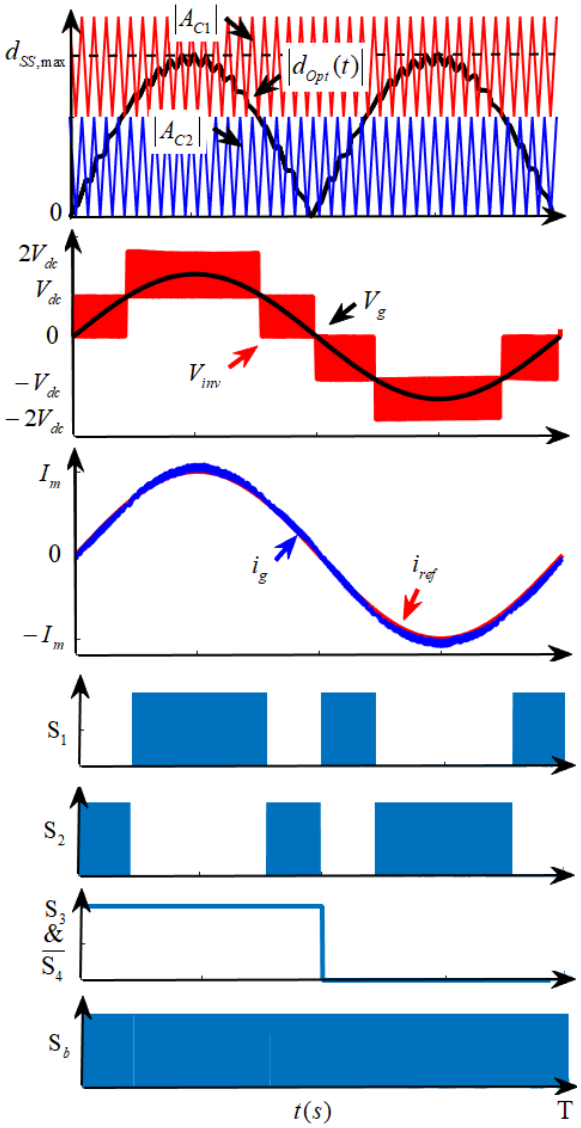


Figure 2.28: Typical modulation waveforms of the proposed CCS-MPC strategy with the final gate switching pulses.

where, $v_{inv}(t)$ and $v_g(t)$, denote the instantaneous value of the inverter and grid voltage per phase, respectively. Here, the internal resistance of the inverter output filter has been neglected to simplify the analysis. As for the proposed SBCG5L-TL inverter, it is evident that during each switching/sampling period, T_{sw}, $v_{inv}(t)$ can possess two adjacent values (v_{inv}^{up} , v_{inv}^{low}) related to the upper and lower inverter output voltage level at each switching instant. The dynamic relationship between $v_{inv}(t)$, $i_{ref}(t)$, and $i_g(t)$ over each sampling/switching time interval has been illustrated in Fig. 2.27, where $d_{\mathrm{m}}(t)$ is the switching duty cycle, in which its optimal value will result in $d_{\mathrm{Opt}}(t)$. Considering $i_g(k)$ as the measured grid current at the instant of k, a prediction for the grid current at the

end of each sampling period (instant of $k+1$) can be computed as:

$$i_g(k+1) = i_g(k) + f_{inc}(k)d_m(k)T_{sw} + f_{dec}(k)(1-d_m(k))T_{sw}. \tag{2.41}$$

where, $f_{inc}(k)$ and $f_{dec}(k)$ are the increasing and decreasing slope of $i_g(k)$ within a switching period, T_{sw}, which can be obtained from (2.40) as follows:

$$f_{inc}(k) = \frac{v_{inv}^{up} - v_g(k)}{L_g} \tag{2.42}$$

$$f_{dec}(k) = \frac{v_{inv}^{low} - v_g(k)}{L_g} \tag{2.43}$$

Now, to obtain the optimal modulated value of $d_m(k)$, $d_{\text{Opt}}(k)$, based on the continuous-time-dynamic model in (2.40), the proposed CCS-MPC technique minimizes the following quadratic cost function:

$$J_{MPC}(t) = (i_{ref}(k+1) - i_g(k+1))^2 + \sigma(d_{SS}(k) - d_m(k))^2 \tag{2.44}$$

where, $i_{ref}(k+1)$ is the projected current reference at the instant of $(k+1)$, which can also be computed by a Lagrange extrapolation. Here, a steady state duty cycle, $d_{SS}(k)$, has also been considered in (2.44), which is required to keep the injected grid current in a desired steady state value as described in. Thus, using (2.39) and (2.40) and considering $2V_{dc}d_{SS}(t)$ as the steady state value of $v_{inv}(t)$, the following relation can be written:

$$\frac{di_{ref}(t)}{dt} = \frac{2V_{dc}d_{SS}(t) - v_g(t)}{L_g}. \tag{2.45}$$

By taking (2.39) and (2.45) into account, the value of $d_{SS}(k)$ during a steady-state can be expressed as follows:

$$d_{SS}(t) = \frac{\omega L_g I_m \cos(\omega t + \varphi) + v_g(t)}{2V_{dc}}. \tag{2.46}$$

It is important to emphasize that the weighting factor, σ, in the cost function (2.44), is used to adjust the closed-loop bandwidth of the controller. Here, if a very small value of σ is selected; then, the first term of (2.44) will become predominant. This results in an aggressive controller that will offer a poor closed-loop performance. On the other hand, if a large value of σ is selected, the second term of (2.44) becomes predominant, which leads to $d_{\text{Opt}}(k) = d_{SS}(k)$. This will result in a slow closed-loop dynamic response. Now, considering (2.38)-(2.46), the following derivative has to be solved to obtain an explicit solution of the optimal duty cycle, $d_{\text{Opt}}(k)$, i.e.:

$$\frac{\mathrm{d}J_{MPC}(t)}{\mathrm{d}d_m(t)} = 0. \tag{2.47}$$

Table 2.5: A Comparison Between the Proposed Topology and Existing TL Grid-Connected Converters

Type of Converter	No. of Components				Max No. of ON-Switches	Minimum V_{in}/ Boosting Feature	No. of Levels	Leakage Current	LVRT/ QSC Ability	Capacitors Charge Balancing	Reported Rated Efficiency
	S	D	C	L							
H5 [12]	5	-	2	2	3	320V/NO	3	Low	Yes/-	Not needed	98.5%@0.5kW
HERIC [13]	6	2	2	2	2	320V/NO	3	Low	NO/-	Not needed	97%@1kW
OH5 [10]	6	-	2	2	3	320V/NO	3	Low	Yes/-	Not needed	97.2%@1kW
H6 [16, 17]	6	2	2	2	3	320V/NO	3	Low	Yes/-	Not needed	97.4%@1kW
Variant H8-5L [20]	8	1	3	1	5	320V/NO	5	Very Low	Yes/NO	Inherent	96.5%@0.5kW
ANPC [98]	6	2	2	1	3	640V/NO	5	Very Low	Yes/-	Needed	NA@1kW
ABNPC [25]	8	-	3	1	3	320V/NO	5	Very Low	Yes/NO	Inherent	97.8%@1.2kW
CG-Type [33]	5	-	2	2	3	320V/NO	3	Zero	Yes/NO	Inherent	95.5%@500W
CGType [35] Type I & II	4	1	3	1	2	320V/NO	3	Zero	Yes/NO	Inherent	99.1%@800W
Type III	4	-	3	1	2	320V/NO	3	Zero	Yes/NO	Inherent	96%@800W
CG-Type [34]	4	2	4	2	2	320V/NO	3	Zero	Yes/NO	Inherent	95.2%@500W
CG-SC-based [99]	7	-	3	1	4	320/NO	5	Zero	Yes/NO	Inherent	97.5%@500W
CG-FC-based [100]	6	-	3	1	3	320V/NO	5	Zero	Yes/Yes	Needed	97%@1kW
CG-FC-based [39]	6	1	3	1	3	320V/NO	5	Zero	Yes/NO	Needed	95.8%@1.2kW
CG-FC-based [38]	6	1	3	1	3	160V/Yes	3	Zero	Yes/NO	Inherent	98.1%@500W
CG-SC-based [37]	6	2	3	1	3	160V/Yes	3	Zero	Yes/NO	Inherent	98.1%@500W
CG-SC-based [70]	7	2	3	1	3	160V/Yes	5	Zero	Yes/NO	Inherent	98.1%@600W
CG-SC-based [71]	6	2	3	1	3	160V/Yes	5	Zero	Yes/NO	Inherent	98.1%@600W
T-Type-SB-based [101]	10	-	2	2	3	160V/Yes	5	Low	Yes/Yes	Inherent	NA@200W
Proposed SBCG5L	7	2	3	2	3	160V/Yes	5	Zero	Yes/Yes	Inherent	97%@750W

Consequently, the optimal value of the duty cycle in the discrete-time-domain, $d_{\mathrm{Opt}}(k)$, is expressed as follows:

$$\begin{cases} d_{\mathrm{Opt}}(k) = \vartheta(k) + \sigma\delta(k) \\ \vartheta(k) = \frac{L_g(i_{ref}(k+1) - i_g(k)) + (v_g(k) - v_{inv}^{low})T_{sw}}{(v_{inv}^{up} - v_{inv}^{low})T_{sw}} \\ \delta(k) = \left(\frac{L_g}{(v_{inv}^{up} - v_{inv}^{low})T_{sw}}\right)^2 d_{SS}(k). \end{cases} \tag{2.48}$$

Having taken (2.48) into account, $d_{\mathrm{Opt}}(k)$ possesses a sinusoidal behavior over a fundamental grid frequency in the continuous-time-domain and it varies between -1 to 1. Considering the operating principle of the proposed SBCG5L-TL inverter, the details of the SPWM procedure with the ON switching states of the involved switches can be realized in Table I. Regarding this Table, the typical waveforms of $d_{\mathrm{Opt}}(t)$ with the associated carrier waveforms, the grid voltage, 5L output voltage of the proposed TL-inverter, the injected grid/reference current and all the gate switching pulses of switches over a fundamental grid cycle, T, are illustrated in Fig. 2.28.

2.5.2 Comparative Study

In order to evaluate the performance of the proposed SBCG5L-TL inverter over some other recently rehearsed TL-inverter structures, a comprehensive comparative study is conducted in this section. Table 2.5 shows details of such a comparative study. Here, the comparative items include the number of required active and passive elements (including

Table 2.6: A Comparison Between Three-Phase Extension of Different Converters.

Respective Converters	No. of Components					Max No. of ON-Switches	Minimum V_{in}/ Boosting Feature/ No. of Stage	No. of Levels Per Phase	CG Concept	No. of DC Sources
	S	G	D	C	L					
ABNPC [25]	18	18	6	9	3	9	320/NO/-	5	NO	1
ANPC [98]	18	18	6	9	3	9	640/NO/-	5	NO	1
CGSC-Based [71]	18	18	6	6	3	9	160/YES/Single	5	YES	3
Current Source Converter [102]	7	7	9	4	4	3	160/YES/Double	2	NO	1
Current Source Converter [103]	8	8	8	5	5	3	320/NO/-	2	NO	1
Current Source Converter [104]	7	7	7	5	4	3	320/NO/-	2	NO	1
T-Type-SB-Based [101]	30	30	-	3	3	15	160/YES/Single	5	NO	3
Proposed SBCG5L (Fig. 2.25)	19	16	4	4	4	9	160/YES/Single	5	YES	1

the pre-assumed filter components and also the decoupling dc-link capacitor for the PV grid-tied applications), the maximum number of ON-state power switches per switching state, the dc input requirement of a standard grid with a peak voltage of 311 V, the number of output voltage levels, the value of leakage current (the terms of "low" and "very low" denote as for a value of the reported leakage current that is less than 120 mA and 10 mA, respectively), the LVRT/QSC capability, the capacitors charged balancing requirement, and finally the overall reported efficiency at the rated power.

As can be seen, similar to the proposed topology, the ANPC and ABNPC-TL inverters of [98] and [25], the CG-FC-based TL topologies of [39, 100], and the CG-SC-based TL inverters presented in [99] and [70, 71] are able to generate a 5L output voltage waveform. Therefore, a much lower value of output L-type filter with an appropriate value of power quality enhancement can be provided. However, none of the structures presented in [25, 98], and [39, 100] has the voltage boosting ability with a CG-based feature. Hence, the presence of leakage current is still expected, while at least a dc-link voltage of 320 V is needed for grid-tied applications. Moreover, although the number of switching devices in the proposed SBCG5L-TL inverter and the presented 5L CG-SC-based topologies of [99] and [70, 71] are somehow the same, their maximum number of ON state power switches is higher than the proposed one without having any QSC capability. Therefore, the value of conduction losses for them is prone to be higher than the proposed topology. By contrast, in spite of having the same boosting feature with the same number of maximum ON state power switches, the 5L CG-SC-based topology in [70] possesses higher overall MTSV ($12V_{dc}$) with a high current stress profile of the power switches caused by hard charging operation of the capacitors. Favorably, the MTSV of the proposed topology is $11V_{dc}$ and it offers a suitable QSC capability for both the involved capacitors. Herein, the recently developed CG-SC-based topology in [71] requires the least number of switching devices (only six) with two-times voltage boosting feature for a 5L TL-inverter. Nevertheless, it suffers from hard charging operation of the capacitors as opposed to the

proposed topology. Moreover, three power switches in the presented SC-CG-based 5L inverter in [71] are placed in the capacitive charging loop, while only the power switch S_1 is in the charging loop of C_2 as for the proposed SBCG5L-TL inverter. Thanks to the provided QSC path in the proposed topology, its current stresses also can be suppressed as opposed to the structure presented in [71]. Also, [71] cannot be extended to operate in a three-phase configuration unless three identical cascaded units of its basic single-phase design have been incorporated. Therefore, it needs 18 power switches/gate drivers, six capacitors, and six power diodes for its possible three-phase extension. The structure proposed in [101] although has offered a single-stage voltage boosting feature with a soft charging capability for a 5L inverter, it requires ten power switches without the CG feature. The SB-based cell used in [101] also requires one additional power switches rather that the diode used in the proposed SBCG5L-TL inverter.

Since one of the main merits of the proposed SBCG5L-TL inverter is its three-phase extension capability with a modular design per phase, a brief comparative study between some topologies which might be extended to three-phase configuration has also been conducted in Table 2.6. As it is clear, the three-phase extension of the proposed topology requires 19 power switches, 16 gate drivers (considering the single gate driver required per each bi-directional power switch), four capacitors, and four power diodes. Here, the number of required gate drivers is indicated by G in Table 2.6. Although the current-source TL inverters proposed in [102–104] require the least number of power switches/gate drivers, they can only generate two-identical output voltage level. Therefore, the quality of the injected grid current waveform cannot be comparable with a multilevel-based inverter like the proposed topology. Lacking the ability of suppressing the leakage current is a major shortcoming of all these current-source-based inverters as well, which imposes the use of galvanic transformer for their possible grid-connected application. In addition, all of them need additional series power diodes rather than standard power switches. Such issues can again reflect additional thermal dissipation concern.

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2.5.3 Verification Results

The feasibility and correctness of the proposed SBCG5L grid-tied TL inverter with the contribution of the proposed CCS-MPC strategy is verified by some laboratory measurement results in this section. As shown in Fig. 2.29, the built prototype has been fabricated based on four SiC-CREE modules, i.e., C2M0080120, for the single-phase

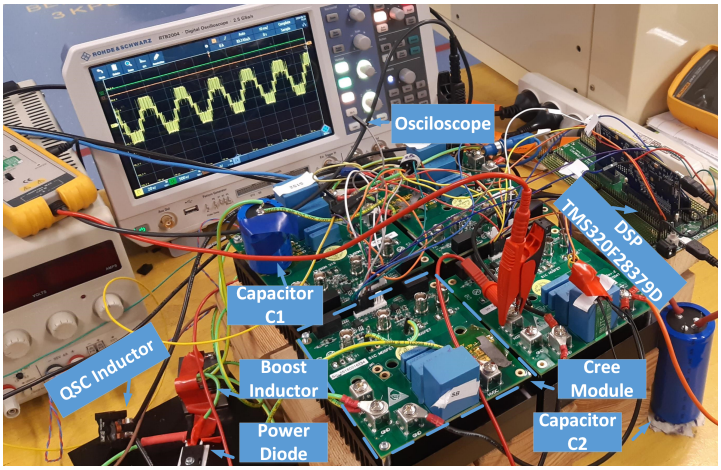


Figure 2.29: A picture of the built prototype.

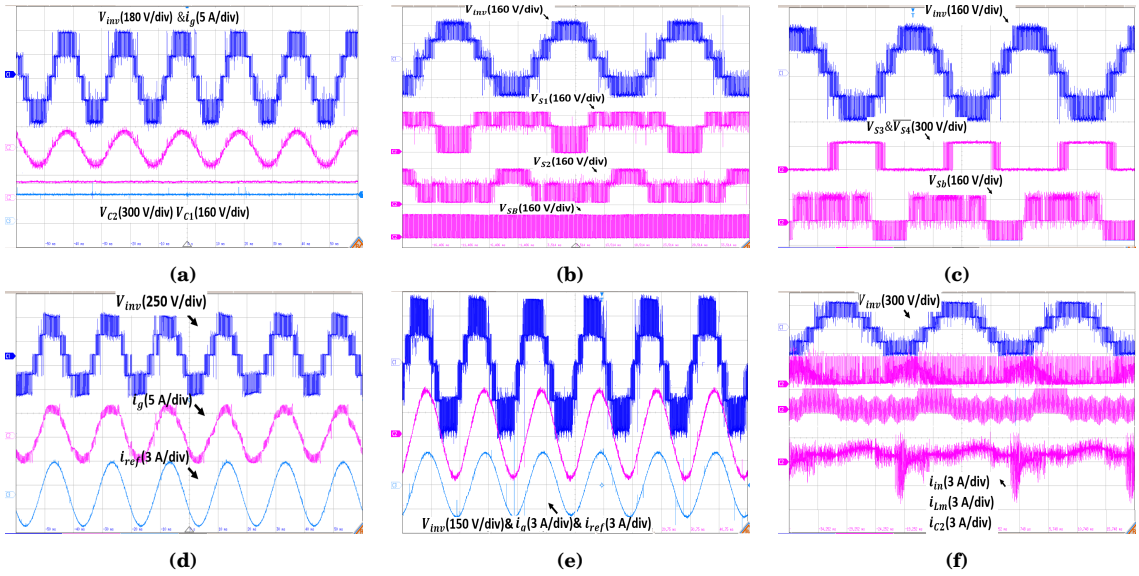


Figure 2.30: Measured waveforms of the inverter showing: (a) the inverter output voltage (180V/div), the injected grid current (5A/div), and the involved capacitors voltage (300V/div) and (160V/div) (b) the inverter output voltage (160V/div) and the MVS waveforms of S_1, S_2 and S_{SB} (160V/div), (c) the inverter output voltage (160V/div) and the MVS waveforms of S_3 and S_4 (300V/div) and S_b (160V/div) (d) the inverter output voltage (250V/div), the injected grid current (5A/div) , and the reference current (3A/div) at the unity PF condition (e) the inverter output voltage (150V/div), the injected grid current (3A/div) , and the reference current (3A/div) at lagging PF condition (f) the inverter output voltage (300V/div), the input current, the SB cell inductor current, and the current passing through C_2 (3A/div).

configuration of the proposed SBCG5L-TL inverter. The inductors value used as the L_m and L_g are 150uH and 2.3mH, respectively, while the capacitors values are 470uF and 1mF. Since the analysis of the MPPT procedure is beyond the scope of this paper, a PV simulator as an adjustable input dc source has been used in throughout the verification.

Considering these observations and regarding a peak of 4A for $i_{ref}(t)$ at the unity PF condition with 160 V as for the input voltage, the measured results of the 5L inverter

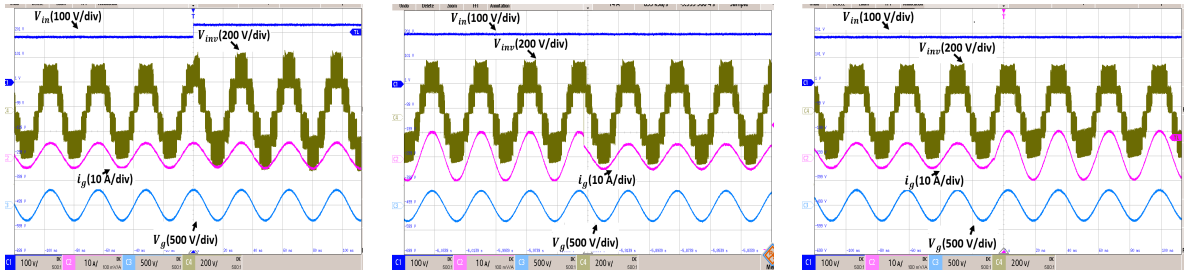
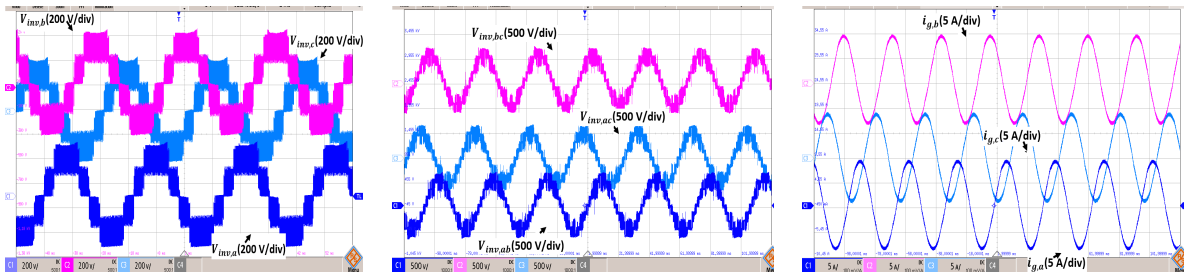


Figure 2.31: Measured waveforms of the inverter showing from top to bottom: input dc voltage (200V/div& 160V/div), inverter output voltage (100V/div), injected grid current (10A/div), and grid voltage (500V/div) (a) step-up change in the dc input voltage (from 180V to 240V); (b) step-down in the current reference (from 10A to 5A at unity PF); and (c) step-uo in the current reference (from 5A to 10A at non-unity PF).

output voltage, the injected grid current and also the balanced voltages across the involved capacitors are provided in Fig. 2.30(a). Following this, the measured results of 5L inverter output voltage alongside the MVS waveforms of all the involved power switches are shown in Fig. 2.30(b) and (c). As can be confirmed from these results, all the desired 5L output voltage waveform with 320V peak value could be generated whilst C_1 and C_2 are balanced at 160V and 320V, respectively. The measured results of the proposed CCS-MPC closed loop strategy applied to the proposed SBCG5L-TL inverter can also be observed in Fig. 2.30(d) and (e), while a peak of 5A with unity and lagging PF has been considered for $i_{ref}(t)$. Here, a value of $\sigma = 1$ has been selected for $d_{\text{Opt}}(t)$ to accordingly cover both terms in the proposed CCS-MPC cost function. Therefore, a good trade-off between the dynamic response and steady-state performance of the proposed CCS-MPC can be achieved. The appropriate injected grid current waveform with the desired 5L output voltage of the proposed inverter in both the unity and lagging PF condition (reactive power support mode) can be ascertained by these results. To show the smooth condition of the input current, the SB inductor cell current and also the current passing through C_2, Fig. 2.30(f) can be also considered. It can be seen that the maximum charging current of C_2 and the maximum peak value of input current could be limited to around 6A through the incorporated QSC path provided in the charging loop of C_2.

To further attest the robust dynamic capability of the proposed SBCG5L-TL inverter with the applied CCS-MPC strategy, some real time simulation results (measured in an oscilloscope) obtained by an OPAL-RT platform with the incorporated eHS module have been captured as shown in Fig. 2.31(a)-(c). Such dynamic tests include the step-change in the value of the input voltage (from 180V to 240V) and also the upward and downward step changes in the value of $i_{ref}(t)$ at the unity PF condition (from 5A to 10A in both



(a) (b) (c)

Figure 2.32: Three-phase measured waveforms of the proposed SBCG5L-TLinverter showing: (a) the phase to ground 5L inverter output voltage (200V/div); (b) the 9L phase to phase voltages (500V/div); (c) the injected grid current per each phase (5A/div) at unity PF.

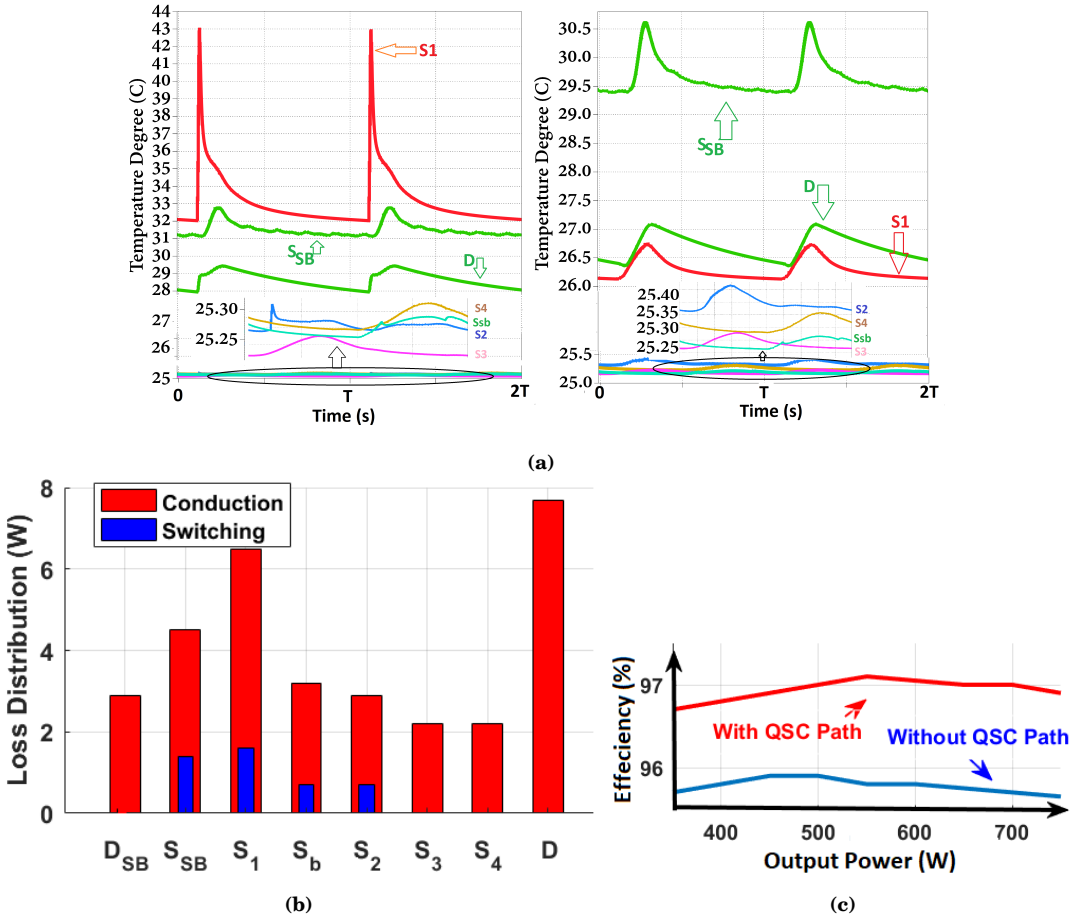


Figure 2.33: PLECS thermal/loss analysis @ 1kW operating power and 20kHz fixed switching frequency (a) steady state operating junction temperature of the semiconductors without the presence of the QSC path (left hand side) and with the presence of QSC path (right hand side) (b) conduction and switching losses distributions among the semiconductor devices, and (c) the efficiency curve versus the output power.

directions) when the converter has been connected to the grid via the aforementioned L-type filter. As for the reference current step change results, the input dc voltage is set on 180 V. As can be observed, the injected grid current waveform offers a steady

performance in delivering the power to the grid and also all the desired 5L output voltages of the proposed inverter can be generated under these dynamic tests.

To further evaluate the three-phase performance of the proposed SBCG5L-TL inverter, the same CCS-MPC has been used, while the phase of the grid voltage and the reference current have been changed per each phase to make a balanced three-phase system. Hence, a phase shifted value for $d_{\mathrm{Opt}}(t)$ is obtained per each phase, which has to be involved into the presented level-shifted SPWM process. Herein, only a single dc source with a value of 180V has been used, and the duty cycle of the switch S_{SB} is fixed at 50 percent. The 5L waveform per each phase output voltage of the proposed inverter along with the 9L phase-to-phase voltages and the steady balanced waveforms of the three-phase injected grid current waveforms can be seen in Fig. 2.32(a) to (c), respectively.

Finally, in order to verify the effectiveness of the QSC path provided in the charging loop of C_2, the thermal and loss distribution analysis at 1 kW operating power have been carried out through PLECS software. Herein, the internal parasitic resistance of all the incorporated semiconductor devices compiled in data sheet is considered. Fig. 2.33(a), show such an average thermal profile of all the involved semiconductors with and without the presence of QSC path during the operation within two fundamental cycles of the grid, whereas the switching and conduction losses distribution are illustrated in Fig. 2.33(b). In this case study, a constant ambient temperature of 25C with uniform temperature distribution across the heatsink has been considered. As is expected, without the use of L_r in the provided QSC path of the proposed SBCG5L-TL inverter, S_1, S_{SB}, and D experience the highest junction temperature, which causes a higher conduction losses consequences. Therefore, QSC capability of the proposed structure is helpful to attain higher overall efficiency in TL grid-tied applications as can be observed in Fig. 2.33(c).

CHAPTER 3

COMMON-GROUND SWITCHED-BOOST-BASED MLIS

So far, all the proposed topologies were based on the SC-technique, where, the inrush current problem and large current stress profile of the switches are the major shortcomings of the proposed topologies. In following, three new CG-based TL inverters are proposed, where they can overcome the concern of the large discontinuous current stress in both the input and switches current profile through an SB-integrated technique. Unlike all the proposed structures so far, these topologies offer a dynamic voltage-boosting feature. Hence, the need for the front-end boost-integrated dc-dc converter is obviated in case of having a low value of the available dc source. This interesting feature can also be helpful to adopt the MPPT procedure integrated within the single-stage design as the input dc voltage can be wide varying whilst injecting a constant power to the grid.

3.1 CGSB-Based 5L Inverter: First topology

Similar to other TL-based MLIs presented, this topology has a CG feature as well, while since all the output voltage levels are generated by the contribution of the capacitors only, it can cancel out the effect of dc-offset issue. An inductor in the integrated SB module is used to boost the voltage across two involved capacitors of the dual T-type (D2T) cell. Therefore, a desirable ac voltage magnitude for the grid-connected application can be achieved over a wide range of input voltage changes. Current stress is also kept within a permissible input current range by the soft-charging operation of the involved capacitors through the inductor. A corresponding dead-beat continuous-current-control with a si-

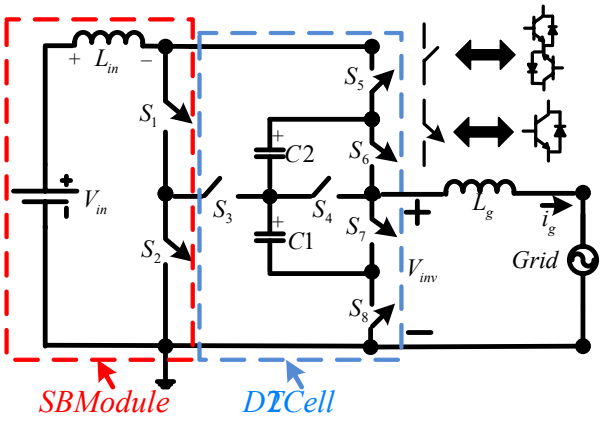


Figure 3.1: The overall structure of the proposed SBD2T5L-TL inverter [105]

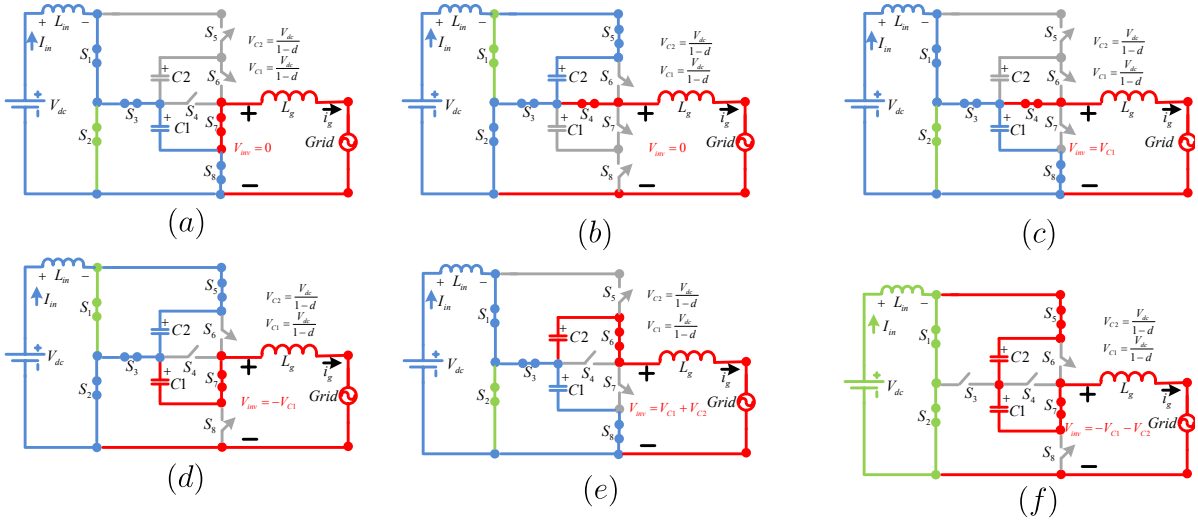


Figure 3.2: Different current flowing paths of the proposed SBD2T5L-TL inverter (a) the first redundant state at the zero level of the output voltage (b) the second redundant state at the zero level of the output voltage (c) at the first positive level of the output voltage (d) at the top positive level of the output voltage (e) at the first negative level of the output voltage, and (f) at the top negative level of the output voltage [105].

nusoidal PWM modulator is implemented for controlling the real and reactive powers. The overall circuit configuration of the proposed topology is depicted in Fig. 3.1[105]. A single inductor, two unidirectional power switches S_1 and S_2, and a single input dc voltage source, which can represent the PV string panels, are included in the integrated SB module, while four unidirectional (S_5, S_6, S_7, and S_8 and two bidirectional power switches, S_3 and S_4 with two additional dc-link capacitors C_1 and C_2 form the D2T cell.

Here, the integrated SB module acts as the conventional boost-converters and therefore, with a proper switching conversion over a full cycle of the grid frequency, a boosted voltage across both the dc-link capacitors of the D2T cell within a single stage energy conversion platform can be achieved. Using these capacitors voltage, five different out-

put voltage levels can also be made. As the grid-connected application is subject, the proposed topology is also tied to the grid via a single L-type filter. Regarding the CG connection between the null of the grid and the negative terminal of the input dc source, the concern of leakage current injection is also removed. The switching states of the proposed SBD2T5L-TL inverter are analyzed as illustrated in Fig. 3.2. Here, the charging loop of the capacitors is shown by the blue lines, whereas, the grid current flowing path is indicated by the red lines. Also, the green lines indicates the input inductor, L_{in}, charging flowing path. Regarding these noted notions, the circuit description of the proposed topology is discussed as follows:

In respect to Fig. 3.2(a), the zero level of the output voltage can be made by turning ON contribution of S_1, S_7, and S_8, while S_2 and S_3 have a complementary ON/OFF operation and they are in the charging path of L_{in} and C_1, respectively. Here, once S_2 is ON, the input current i_{in} is linearly increased to charge the L_{in}; therefore, considering V_{dc} as the input dc source, the following relation can be expressed:

$$v_{L_{in}} = V_{dc}. \tag{3.1}$$

where, v_{Lin} is the instantaneous voltage across the L_{in}.

Also, whenever S_3 is ON, the input current is reduced and C_1 is charged as follows:

$$V_{C1} = V_{dc} + v_{L_{in}}. \tag{3.2}$$

where, V_{C1} is the steady state voltage across C_1. Hence, considering d as the supposed duty cycle ratio of the involved complementary switches over the switching frequency, V_{C1} can be taken by:

$$V_{C1} = \frac{V_{dc}}{1-d}. \tag{3.3}$$

It can be deduced that through such a mentioned current flowing path, C_2 is disconnected from the grid and the input dc source. Concerning this switching conversion, the injected grid current with unity PF direction is passed through the anti-parallel internal power diode of S_7 and the power switch S_8, whereas as for the non-unity PF demanded by the grid, the power switch S_7 and the anti-parallel diode of S_8 are conducting.

A redundant zero state is also possible as shown in Fig. 3.2(b). Here, S_2, S_3, and S_4 must be ON, while S_1 and S_5 have a complementary operation with each other. It is clear that once S_1 is ON, the L_{in} gets charged through the input dc source and whenever S_5 is to be ON, the charged voltage of L_{in} and the input dc voltage are pumped to C_2 and therefore it is charged by:

$$V_{C2} = V_{dc} + v_{L_{in}}. \tag{3.4}$$

where, V_{C2} is the steady state voltage across C_2. Hence, with respect to (3.1) and (3.4) and with a similar principle as given for V_{C1}, V_{C2} can be obtained as:

$$V_{C2} = \frac{V_{dc}}{1-d}. \tag{3.5}$$

Here, as opposed to the previous redundant state for the zero-level of the output voltage shown in Fig. 3.2(a), C_1 is disconnected from the grid and the dc input. Also, the grid current flowing path for non-unity PF belongs to the conduction path of S_3, and S_4 associated with the power switch S_2.

As shown in Fig. 3.2(c), the first positive output voltage level is created by the aim of the pre-charged voltage value of C_1 and the ON state contribution of S_1, S_4, and S_8, whereas similar to the first redundant state as for the zero-level of the output voltage, S_2 and S_3 must be switched with a complementary switching scheme. So, with hindsight to (3.2) and (3.3), C_1 can still be charged to its steady state voltage as expressed in (3.3), while C_2 is again disconnected from the grid and the dc input supply. Here, similar to the charging path provided by the second redundant state for the zero-level of the output voltage, the reverse grid current caused by a non-unity PF condition is passed through S_3, S_4 and S_2, while C_1 can be charged from both the input dc source and the grid at the same time.

As shown in Fig. 3.2(d), this output voltage level is made by the contribution of both the involved capacitors and the ON state aim of S_1, S_6, and S_8. Here, to keep on the charging process of C_1 similar to the previous stage, S_2 and S_3 still must be ON/OFF with a complementary principle. Hence, regarding (3.4) and (3.5), the maximum value of the inverter output voltage $V_{inv,max}$ is made as:

$$V_{inv,max} = V_{C1} + V_{C2} = \frac{2V_{dc}}{1-d}. \tag{3.6}$$

Regarding the red and blue lines of the current flowing path shown in Fig. 3.2(d), it is evident that the direction of the injected grid current i_g is of importance for the charging/discharging operation of C_2. It is also apparent that in case of non-unity PF condition, the grid current flowing path is formed through the anti-parallel internal power diode of S_6, the capacitor C_2, and the power switches S_2 and S_3.

In order to generate the first negative level of the output voltage, Fig. 3.2(e) must be considered. As is clear, three power switches as S_2, S_3, and S_7 must be ON, while similar to the second redundant state of the zero-level output voltage (Fig. 3.2(b)), S_1

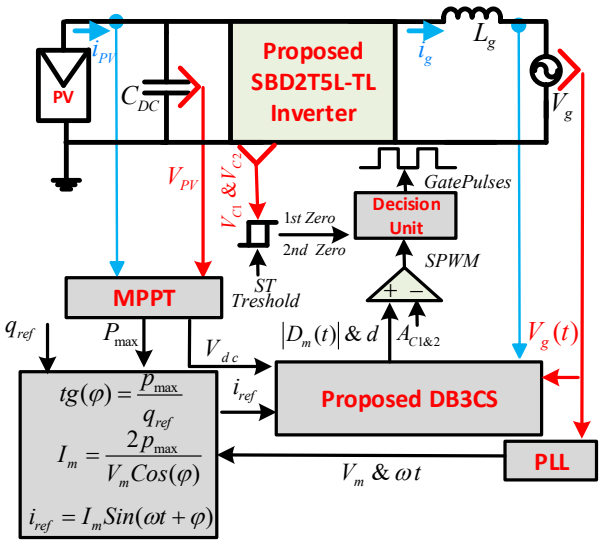
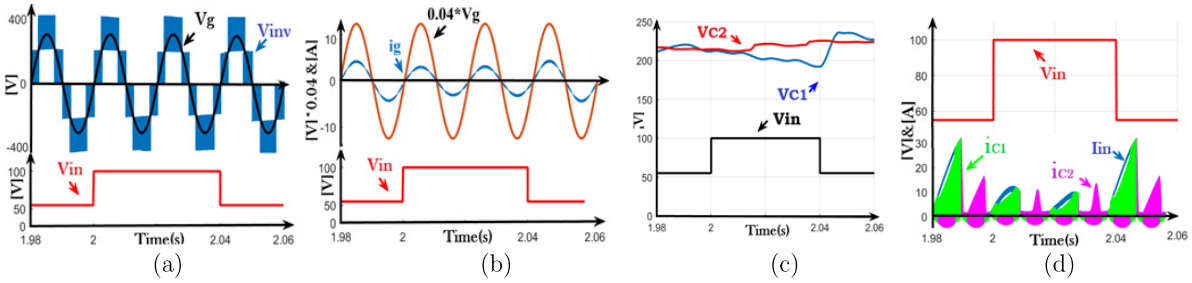


Figure 3.3: The overall control block diagram of the proposed grid-connected SBD2T5L-TL inverter [105].



(a) (b) (c) (d)

Figure 3.4: Simulation results once a upward and downward step change (from 50 V to 100 V and vice versa) is applied in the input voltage: (a) 5L inverter,Äôs output voltage with the grid/input voltage (b) the injected grid current with the grid voltage and the input voltage (c) the voltage across C_1 and C_2 with the input voltage, and (d) the input current along with the capacitors passing current and the input voltage [105].

and S_5 have a complementary operation with each other. Hence, the output voltage of the inverter is generated by the contribution of C_1, whereas C_2 is charged to its steady state value. Here, in case of unity PF, C_1 is charged, while it would be discharged when a non-unity PF operation is demanded.

The overall modulation/control platform of the proposed SBD2T5L-TL inverter is on the basis of a new DB3CS principle as depicted in Fig. 3.3. Here, the capacitors voltage balancing issue is another aim. Hence, to sufficiently integrate both the redundant states provided by the zero-level of the output voltage, a Schmitt Triger (ST) block with a decision maker unit has also been used in the overall control diagram. The controlled is a based dead-beat current controller as described earlier. Regarding the boosting property of the proposed SBD2T5L-TL inverter and considering (3.6), $V_{inv,max}$ can be remained fixed by changing the instant value of d. This approach can address the MPPT operation of the input PV main string panels with a constant MPP voltage, where the maximum

input power of the PV emulator can be remained fixed through the power balanced theory by adjusting the appropriate value of the SB module duty cycle.

Considering such observations, a step change in the value of the input voltage, i.e., from 50 V to 100 V in both directions is applied, while the peak of the reference current is considered to be 5 A. So, to keep fixed $V_{inv,max}$ at 400 V, the value of d has to be dynamically changed from 0.75 to 0.5 in both the upward and downward directions. Fig. 3.4(a)-(d) shows the detailed simulation results of this dynamic test, while all the 5L inverter output voltage could be generated with a 5 A peak value of the injected current to the grid. The balanced voltage of both the involved capacitors can also be seen in Fig. 3.4(c), while the currents through the input dc source and the involved capacitors are shown in Fig. 3.4(d). It can be confirmed that owing to the employed SB module, the input current possesses a limited range of inrush current during the charging operation of the involved capacitors. Here, when the input voltage is 50 V ($d = 0.75$), the maximum value of the input current, which corresponds to the maximum charging current of C_1 is around 30 A, while the maximum value of the injected grid current is 5 A. By contrast, once the input voltage goes up to 100 V ($d = 0.5$), the maximum value of the input current is around 10 A, while because of the applied power balanced theory, the peak of injected grid current is around 3.5 A. Therefore, based on the maximum input voltage and input current capacity of the PV emulator, a fixed value of 400 V is selected for $V_{inv,max}$ in throughout the measurement process. Here, a 10% allowable ripple voltage has been considered for the balanced voltage of the dc-link capacitors; so regarding, the fixed value of $V_{inv,max}$ at 400 V, a value of 220 V has been chosen for V_{ST}.

In order to evaluate the superiority of the proposed CG-based SBD2T5L-TL inverter over its other TL-inverter counterparts, a comparative study from different aspects is presented in this section. The comparative items are the number of active and passive involved components (with considering the pre-assumed output filter, and the input decoupling capacitor for PV applications), maximum number of ON state power switches at each switching instant, which can somehow represent the conduction losses of the switches, the ability as for boosting feature with minimum required value of the input dc voltage utilization for a standard grid-connected application, maximum number of the inverter output voltage levels, the capacitors soft charging operation capability, the reported value of the leakage current, the reactive power support ability, and the reported measured efficiency at the rated power. Here, the value of the leakage current is considered low and very low if it is less than 120 mA and 10 mA, respectively. The overall results of such a comparative study is summarized in Table 3.1. As can be seen,

Table 3.1: A Comparison Between the Proposed Topology and Existing TL Grid-Connected Converters.

Type of Converter	No. of Components				Max No. of ON-Switches	Minimum V_{in}/ Boosting Feature	No. of Levels	Leakage Current	Reactive/ Power Support	Soft Charging Capability	Reported Rated Efficiency
	S	D	C	L							
H5 [12]	5	-	2	2	3	320V/NO	3	Low	Yes	Not needed	98.5%@0.5kW
HERIC [13]	6	2	2	2	2	320V/NO	3	Low	NO	Not needed	97%@1kW
OH5 [10]	6	-	2	2	3	320V/NO	3	Low	Yes	Not needed	97.2%@1kW
H6 [16, 17]	6	2	2	2	3	320V/NO	3	Low	Yes	Not needed	97.4%@1kW
Variant H8-5L [20]	8	1	3	1	5	320V/NO	5	Very Low	Yes	NO	96.5%@0.5kW
ANPC [98]	6	2	2	1	3	640V/NO	5	Very Low	Yes	NO	NA@1kW
ABNPC [25]	8	-	3	1	3	320V/NO	5	Very Low	Yes	NO	97.8%@1.2kW
CG-Type [33]	5	-	2	2	3	320V/NO	3	Zero	Yes	NO	95.5%@500W
CGType [35] Type I & II	4	1	3	1	2	320V/NO	3	Zero	Yes	NO	99.1%@800W
CGType [35] Type III	4	-	3	1	2	320V/NO	3	Zero	Yes	NO	96%@800W
CG-Type [34]	4	2	4	2	2	320V/NO	3	Zero	Yes	NO	95.2%@500W
CG-SC-based [99]	7	-	3	1	4	320/NO	5	Zero	Yes/NO	Inherent	97.5%@500W
CG-FC-based [100]	6	-	3	1	3	320V/NO	5	Zero	Yes	NO	97%@1kW
CG-FC-based [39]	6	1	3	1	3	320V/NO	5	Zero	Yes	No	95.8%@1.2kW
CG-SC-based [37]	6	2	3	1	3	160V/Yes	3	Zero	Yes	No	98.1%@500W
Proposed SBD2T5L	10	-	3	2	4	Dynamic/Yes	5	Zero	Yes	Yes	98.1%@1kW

the proposed topology, the Variant 5LH8-TL inverter presented in [20], the ANPC and ABNPC structures of [98] and [25], and the CG-FC- based topologies of [100] and [39] are only able to generate 5L of the output voltage levels. However, the main difference of such a mentioned 5L-TL inverter structures is the minimum dc input voltage utilization to meet the amplitude of a standard grid (with 311 V as the peak) requirement. In light of this, only a 50 V input dc source is enough to make the eight-time voltage boosting feature as for the proposed structure. Herein, none of the topologies mentioned in [20], [98] and [25] possesses the CG feature; so, still the concern of leakage current elimination is left. By contrast, although the number of switching devices of the proposed SBD2T5L-TL inverter is slightly higher than other 5L-CG-based TL-inverter counterparts, it has a valuable dynamic voltage boosting feature with an inherent soft charging nature of the involved capacitors. It is also notable that all the positive and negative output voltage levels of the proposed topology are made by the dc-link capacitors as discussed earlier, while other 5L-CG-SC-based-TL inverters are using the aim of both the input dc source and the virtual dc-link voltage of the capacitors. Regarding this remark and as opposed to them, the dc-bias injection concern can be properly mitigated by the aim of the proposed topology. Other Details of the circuit design, and the relevant control and experimental results have been discussed in [105].

3.2 CGSB-Based 5L Inverter: Second topology

The overall circuit configuration of the proposed CGSB5L-TL inverter (second proposed topology with a dynamic voltage conversion gain) connected through a simple L-type filter, L_g, to the grid is illustrated in Fig. 3.5 [106]. As can be inspected, the proposed

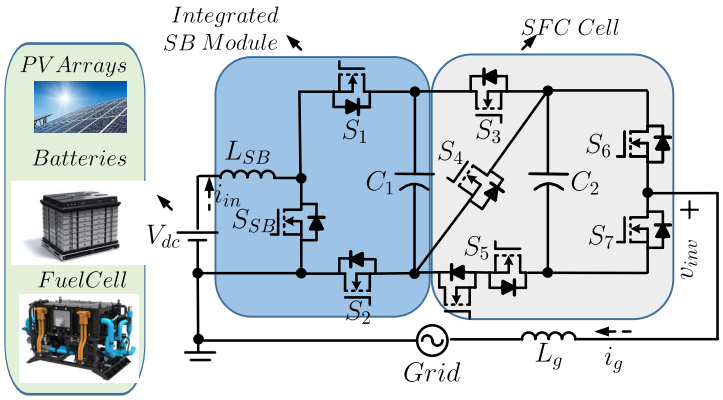


Figure 3.5: Proposed CGSB5L-TL inverter.

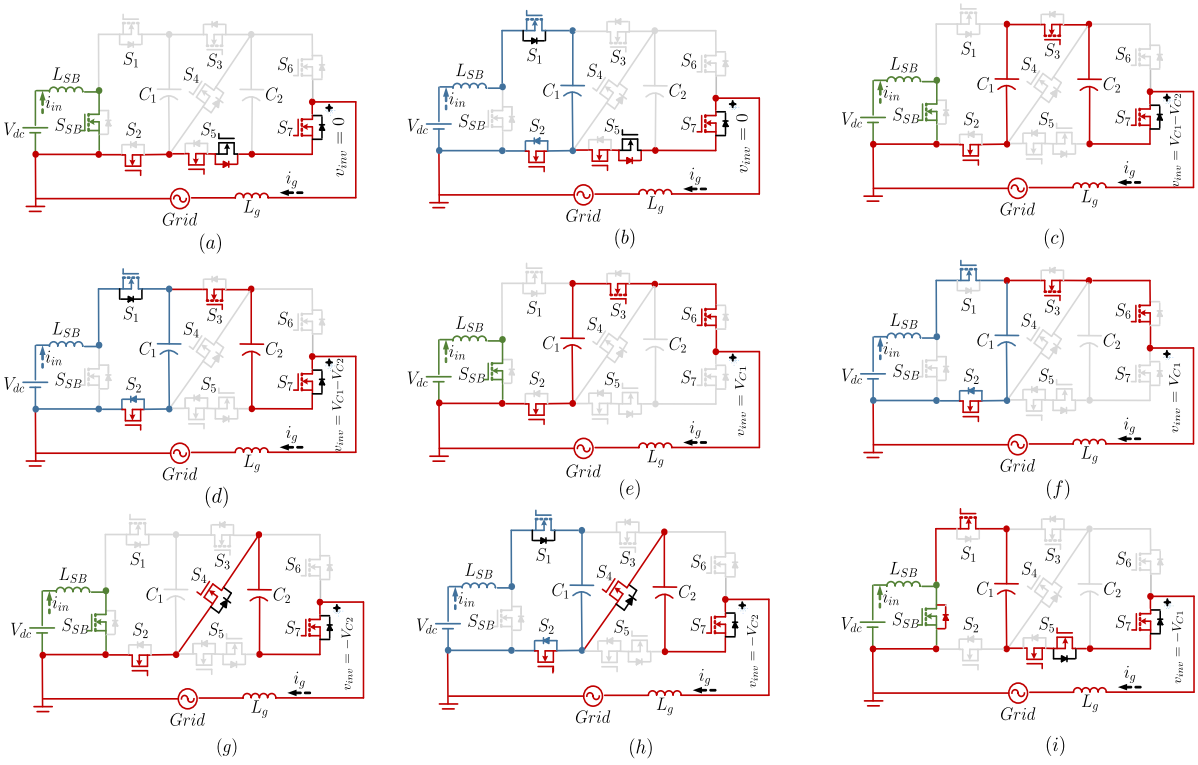


Figure 3.6: Different current flowing paths of the proposed CGSB5L-TL inverter at the (a) zero-level of the output voltage in both half-cycle in Sub-Mode I (b) zero-level of the output voltage in both half-cycle in Sub-Mode II (c) $v_{inv} = V_{C_1} - V_{C_2}$ in Sub-Mode I, (d) $v_{inv} = V_{C_1} - V_{C_2}$ in Sub-Mode II, (e) $v_{inv} = V_{C_1}$ in Sub-Mode I, (f) $v_{inv} = V_{C_1}$ in Sub-Mode II, (g) $v_{inv} = -V_{C_2}$ in Sub-Mode I, (h) $v_{inv} = -V_{C_2}$ in Sub-Mode II, and (i) $v_{inv} = -V_{C_1}$ in Sub-Mode.

topology offers a CG feature through a direct connection between the negative terminal of the input dc source, V_{dc}, and the neutral point of the grid. Herein, excluding the bidirectional switch S_5, all the remaining involved power switches are unidirectional. As can also be observed, the proposed CGSB5L-TL inverter is comprised of an integrated SB module and a switched-flying-capacitor (SFC) cell. The integrated SB module requires a single boost inductor, L_{SB}, three power switches and a single capacitor, C_1, whereas

the incorporated SFC cell needs a flying capacitor, C_2, four unidirectional and one bidirectional switches. Here, through a proper switching conversion of the switches integrated in the SB module, the voltage across C_1 can be balanced at a required boosted voltage value with respect to the input dc voltage, V_{dc}. Also, with the help of the grid/load current and such a boosted voltage across C_1, the voltage across C_2 can be balanced at the half value of the boosted voltage across C_1 without the need of additional voltage sensors and/or control. Hence, considering V_{C1}, and V_{C2}, as the steady state voltages across C_1, and C_2, respectively, the proposed topology is able to generate five distinctive output voltage levels as ($\pm V_{C1}$, $\pm V_{C2}$, and zero) within a single-stage power conversion operation over each fundamental grid period.

Fig. 3.6(a)-(i) show different switching states and current flowing paths representation of the proposed topology to generate a 5L output voltage. Excluding the top negative output voltage level, $v_{inv} = -V_{C1}$, the operating principle of the proposed SBCG5L-TL inverter is based on two sub-modes per each output voltage level, in which the first sub-mode (Sub-Mode I) is related to the charging operation of L_{SB} represented in green color, and the second one (Sub-Mode II) is concerned with the charging operation of C_1 highlighted in blue color. Herein, the grid current flowing paths are described in red color. As shown in Fig. 3.6, the operation in the Sub-Mode I is realized by turning ON S_{SB}, while Sub-Mode II is established through two ON-state power switches S_1 and S_2. Considering the ideal condition of all the involved switches and the passive elements, and taking both the Sub-Mode I and Sub-Mode II into account, a fixed dc duty cycle, d, has to be considered for the integrated SB module over each switching frequency. Hence, regarding a volt-sec balance principle applied to L_{SB}, the steady state voltage across C_1 can be written as:

$$V_{C1} = \frac{V_{dc}}{1-d}. \tag{3.7}$$

Moreover, considering the switching operation of the proposed inverter during both the first positive and the first negative output voltage levels and regarding a KVL, the steady-state voltage of C_2 can be determined by the following expressions:

$$\frac{di_g^+}{dt} = \frac{V_{C2} - V_{C1} + v_g}{L_g} \tag{3.8}$$

$$\frac{di_g^-}{dt} = \frac{v_g - V_{C2}}{L_g} \tag{3.9}$$

where i_g^+, and i_g^-, are the grid current passing through C_2 in the positive and negative half-cycle, respectively; whereas v_g is the instantaneous value of the grid voltage. Hence,

regarding the charge-sec balance theory for the capacitors, and considering the reverse current direction of i_g in the negative half cycle, the following relationship can be written:

$$\frac{di_g^+}{dt} - \frac{di_g^-}{dt} = 0. \tag{3.10}$$

where i_g^+, and i_g^-, are the grid current passing through C_2 in the positive and negative half-cycle, respectively; whereas v_g is the instantaneous value of the grid voltage. Hence, regarding the charge-sec balance theory for the capacitors, and considering the reverse current direction of i_g in the negative half cycle, the following relationship can be written:

$$\frac{di_g^+}{dt} - \frac{di_g^-}{dt} = 0. \tag{3.11}$$

Considering (3.9)-(3.11), it can be revealed that V_{C2} is equal to $0.5V_{C1}$ at the end

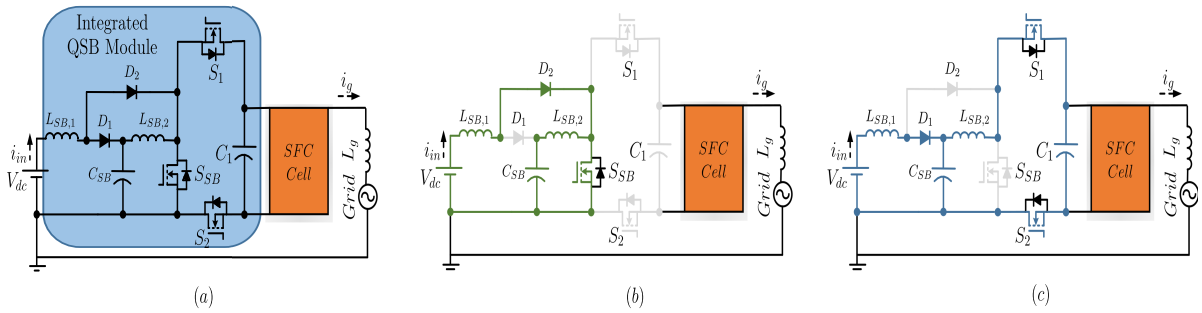


Figure 3.7: Proposed QSBCG5L-TL inverter, (a) main circuit configuration, (b) operation in Sub-Mode I, (c) operation in Sub-Mode II [106].

of a full grid fundamental period, T. Regarding the working principle of the proposed CGSB5L-TL inverter shown in Fig. 3.6, the following remarks can be drawn:

1) The proposed CGSB5L-TL inverter can generate all distinctive 5L in the output voltage with an adjustable boosted peak value of $\frac{V_{dc}}{1-d}$. Hence, with a wide range of input voltage changes, the peak value of the inverter output voltage can be kept fixed whilst having all the distinctive 5L staircase waveform.

2) Both the involved capacitors of the proposed CGSB5L-TL inverter are self-balanced over a full grid fundamental period without the need of any active voltage balancing procedure.

3) Due to the incorporated boost inductor in the integrated SB-module, the current stress profile of all the switches that are involved in the charging path of C_1 is limited to a permissible input current range. Here, all the involved switches of the SFC cell only experience the stress of the injected grid current since the charging/discharging operation of C_2 is fully soft with the help of the grid current.

4) All the positive and negative output voltage levels are generated by the contribution of the capacitors voltages only. Hence, the dc-offset problem associated with most of the available CG-based TL-inverters is not an issue for this proposal.

5) The MVS across the switches, which corresponds to the maximum OFF-state drain-source voltage value of the switches is equal to:

$$\begin{aligned} V_{S_i} &= \frac{V_{dc}}{1-d}, \forall i \in \{1,2,3,4,SB\} \\ V_{S_j} &= \frac{V_{dc}}{2(1-d)}, \forall j \in \{5,6,7\} \end{aligned} \tag{3.12}$$

3.2.1 Proposed QSBCG5L-TL Inverter

The integrated SB cell of the proposed TL-based grid-tied inverter can be replaced with an extra inductor, a dc-link capacitor and two additional power diodes. Hence, the performance of the proposed topology can be further enhanced by offering a quadratic voltage boosting feature without any additional power switch. Such a passive DCL network is named as an integrated quadratic switched-boost (QSB) cell and can accordingly change the overall circuit design of the proposed topology to be as an QSBCG5L-TL inverter as shown in Fig. 3.7 (a). The working principle of the proposed QSBCG5L-TL inverter, related to having two Sub-Modes per each output voltage level (except the top negative level), is the same as given for the proposed CGSB5L-TL inverter. Herein, once the switch S_{SB} is ON, the switching operation works in the Sub-Mode I as can be realized in Fig. 3.7 (b). Therefore, through forward biasing the power diode D_2, the following relation over a switching duty cycle of dT_s is expressed.

$$\begin{aligned} V_{L_{SB,1}} &= V_{dc} \\ V_{L_{SB,2}} &= V_{C_{SB}} \end{aligned} \tag{3.13}$$

where, $V_{L_{SB,1}}$, $V_{L_{SB,2}}$, and $V_{C_{SB}}$ are the steady-state voltage across $L_{SB,1}$, $L_{SB,2}$ and, C_{SB} respectively. Alternatively, as shown in Fig. 3.7(c), whenever the power switch S_{SB} is OFF, the power diode D_1 is in forward bias. Hence, the operation in the Sub-Mode II is started and within a duty cycle of $(1-d)T_s$ over each switching time interval, T_s, the following relation can be stated:

$$\begin{aligned} V_{L_{SB,1}} &= V_{dc} - V_{C_{SB}} \\ V_{L_{SB,2}} &= V_{C_{SB}} - V_{C_1} \end{aligned} \tag{3.14}$$

Therefore, by applying the volt-sec balance principle across both the involved inductors in the integrated QSB cell, and taking (3.13)-(3.14) into account, the steady-state

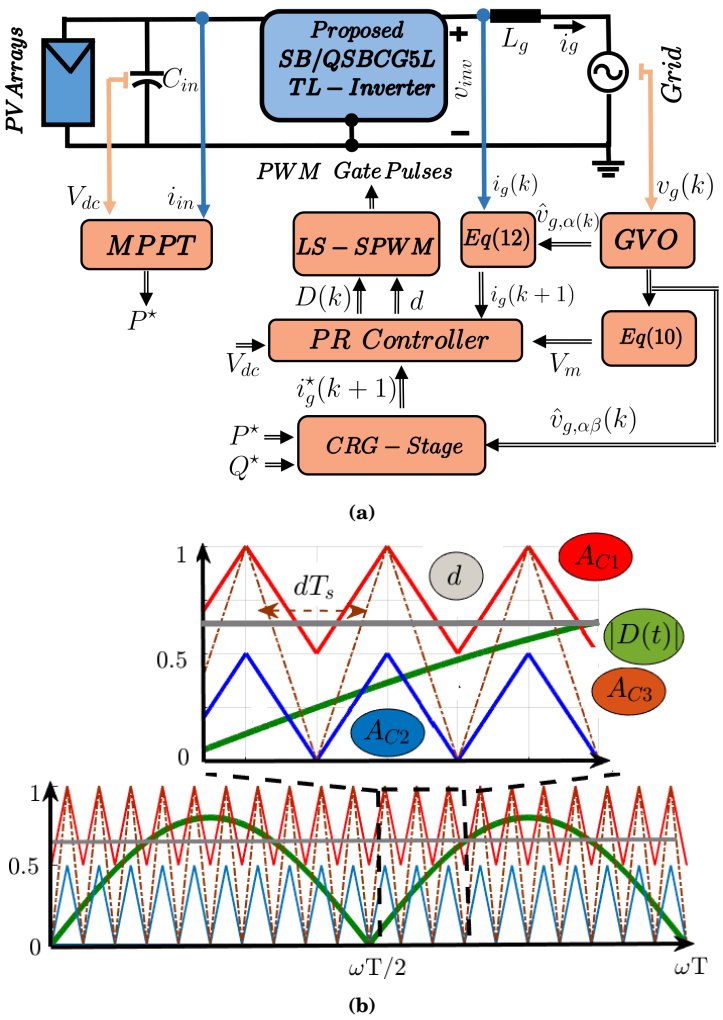


Figure 3.8: (a) Closed-loop control configuration of the proposed CGSB5L-TL inverter, and (b) maximum boost LS-SPWM scheme [106].

boosted voltage across the involved capacitors can be obtained as follows:

$$\begin{aligned} V_{C_{SB}} &= \frac{V_{dc}}{1-d} \\ V_{C1} = 2V_{C2} &= \frac{V_{C_{SB}}}{1-d} = \frac{V_{dc}}{(1-d)^2} \end{aligned} \tag{3.15}$$

As can be realized, since the peak of the inverter output voltage is equal to the voltage across C_1, the proposed topology presents a quadratic dynamic voltage conversion gain. All the other mentioned highlights related to the proposed CGSB5L-TL inverter are also hold for the proposed QSBCG5L-TL inverter.

Table 3.2: ON switching states of the proposed CGSB5L-TL inverter modulated with a LS-SPWM technique.

$D(t)$ Sign	LS-SPWM Condition	ON State Switches	v_{inv}
P	$\|D(t)\| \geq A_{C1}$, d$\geq A_{C3}$	S_{SB},S_2,S_3,S_6	V_{C1}
	$\|D(t)\| \geq A_{C1}$, d $\leq A_{C3}$	S_1,S_2,S_3,S_6	V_{C1}
	$A_{C2} \leq \|D(t)\| < A_{C1}, d \geq A_{C3}$	S_{SB},S_2,S_3,S_7	$0.5V_{C1}$
	$A_{C2} \leq \|D(t)\| < A_{C1}, d \leq A_{C3}$	S_1,S_2,S_3,S_7	$0.5V_{C1}$
N	$\|D(t)\| \geq A_{C1}$, d$\geq A_{C3}$	S_{SB},S_1,S_5,S_7	$-V_{C1}$
	$A_{C2} \leq \|D(t)\| < A_{C1}, d \geq A_{C3}$	S_{SB},S_2,S_4,S_7	$-0.5V_{C1}$
	$A_{C2} \leq \|D(t)\| < A_{C1}, d \leq A_{C3}$	S_1,S_2,S_4,S_7	$-0.5V_{C1}$
-	$\|D(t)\| \leq A_{C2}, d \geq A_{C3}$	S_{SB},S_2,S_5,S_7	0
	$\|D(t)\| \leq A_{C2}, d \leq A_{C3}$	S_1,S_2,S_5,S_7	0

3.2.2 Modulation and Control Strategy of the Proposed CGSB-5L inverter: Second Topology

As was previously discussed, all the integrated capacitors in both the proposed CGSB5L-TL inverter and its quadratic derived version are self-balanced by the described switching operation in different output voltage levels. Therefore, the only controllable variable in grid-connected condition of the proposed TL-based inverter is the injected grid current, i_g. There are several types of control strategies to govern the grid-connected inverters in the literature. In this work, a PR controller has been selected due to its simplicity and appropriate dynamic performance. The overall closed-loop control procedure of the proposed grid-tied system has been depicted in Fig. 3.8(a), where the system needs a MPPT unit to extract the maximum available power of a PV panel string, $P^\star$. Similar to the proposed 9L9S-CGSC-TL inverter, to find the proper phase and amplitude of the grid voltage, any types of well-known phase-locked loop methods or GVO technique can be employed.

The aim of PR controller is to track this sinusoidal current. The output of such a PR controller gives the desired value of the controlled signal, $D(k)$, while reducing the instant error. Considering this, the instantaneous value of the proposed inverter output voltage, $v_{inv}(k)$, can be obtained as:

$$v_{inv}(k) = \frac{V_{dc}}{1-d} D(k) \tag{3.16}$$

where $D(k) \in [-\mathbb{1}, \mathbb{1}]$.

To generate all the required gate switching pulses of the proposed TL-based inverter,

$D(t)$, and d are then sent to the LS-SPWM stage. This comes from the fact that each of the involved switches in the proposed CGSB5L-TL needs an individual PWM signal and due to the CG-based configuration of the proposed topology, these PWMs cannot be complementary provided. The working principle of this LS-SPWM technique has been illustrated in Fig. 3.8(b), while the details of ON switching states have been tabulated in Table 3.2. Here, the terms P and N represent the positive and negative polarity of $D(t)$, respectively. Additionally, three in phase LS carriers named A_{C1}, A_{C2}, and A_{C3}, are needed to compare with absolute value of $D(t)$ and d. In this case, A_{C1}, A_{C2} are used to generate the ac PWM pulses, while A_{C3} is incorporated to generate the required dc PWM pulses of the proposed system. Herein, to generate all the PWM pulses of the proposed inverter with a fixed switching frequency operation, the frequency of these LS carriers must be accorded with the sampling time used in the PR and GVO processes. Regarding the switching conversion of the proposed inverter in different output voltage levels shown in Fig. 3.6, the maximum fundamental component term of the proposed inverter output voltage is obtained as follows:

$$v_{inv,\max} = \frac{V_{dc}(0.5d + 0.5)}{1 - d} \tag{3.17}$$

The above-mentioned relationship comes from the fact that, during the top negative output voltage level generation [see Fig. 3.6(i)], the switch S_{SB} must be always ON. Considering Fig. 3.8(b), this constraint can only be possible whenever d is greater than 0.5. Therefore, regarding (3.17), the practical constraint of d to generate all the 5L inverter output voltage while injecting power to the grid is expressed by:

$$d \geq \frac{2(V_m - V_{dc})}{V_{dc} + 2V_m}. \tag{3.18}$$

3.2.3 Design Guidelines

The design guidelines of the required passive elements in the proposed CGSB5L-TL inverter are presented in the following subsections. Herein, a unity PF is considered for the injected grid current since it reflects the worst scenario for the passive elements design considerations [107].

The required value of L_{SB} in the integrated SB module directly depends on the input current, i_{in}, and its associated permissible ripple at different values of the integrated SB module duty cycle [61]. Similar to any other single-phase 50-Hz grid-tied TL-inverters, i_{in} presents a low frequency component (100-Hz) and a high switching frequency ripple. The low frequency component in i_{in} can also be related to 100-Hz ripple component

of the steady state ripple voltage across C_1. Therefore, taking (3.7) into account and considering I_m, as the peak value of the injected grid current, the following expressions for the low-frequency ripple of V_{C_1} and i_{in} at a steady-state condition can be obtained:

$$\Delta V_{LF,C1} = \frac{I_m}{3\pi^2 \omega C_1} \tag{3.19}$$

$$\Delta i_{LF,in} = \frac{I_m(1-d)}{12\pi^3 \omega^2 C_1 L_{SB}} \tag{3.20}$$

where, ω is the angular frequency term at the grid fundamental cycle. On the other hand, the high frequency ripple component of the V_{C_1} and i_{in} at the steady-state condition can also be developed as follows, respectively:

$$\Delta V_{HF,C1} = \frac{d(1-d)i_{in}}{2C_1 f_{sw}} \tag{3.21}$$

$$\Delta i_{HF,in} = \frac{dV_{dc}}{L_{SB} f_{sw}} \tag{3.22}$$

where, f_{sw} represents the switching frequency of the proposed inverter. Hence, regarding (3.19)-(3.22), and considering the fact that the summation of low and high frequency contents of the input current and the capacitor voltage have to be less than the twofold of their average value, the minimum required value of L_{SB} and C_1 are then taken as follows:

$$C_{1,min} = \frac{d(1-d)i_{in}}{2\Delta V_{HF,C1} f_{sw}} + \frac{I_m}{3\pi^2 \omega \Delta V_{LF,C1}} \tag{3.23}$$

$$L_{SB,min} = \frac{1}{2i_{in}} \left(\frac{dV_{dc}}{f_{sw}} + \frac{I_m(1-d)}{12\pi^3 \omega^2 C_1} \right) \tag{3.24}$$

It is worth nothing that design of $L_{SB,1}$ and C_1 in the proposed QSBCG5L-TL inverter is the same as given for L_{SB} and C_1 of the proposed CGSB5L-TL inverter since they act as the input inductor and the boosted capacitor of the converter. However, design of $L_{SB,2}$ and C_{SB} is slighty different since they just will see the high switching frequency ripple components of the current passing through $L_{SB,2}$ and the voltage across C_{SB}. Hence, their inductance and capacitance can be chosen smaller than L_{SB} and C_1.

The capacitor C_2 in both the proposed CGSB5L and its derived quadratic version TL inverter is charged/discharged through the grid current path over a grid period. Hence, to determine a feasible capacitance for C_2, its voltage ripple over a half-cycle of the grid frequency, which represents the longest discharging period of C_2 over the grid frequency, can be expressed via:

$$\Delta V_{C_2} = \frac{2}{C_2} \int_0^{\frac{T}{4}} i_{C2}(t) d(t). \tag{3.25}$$

Table 3.3: A comparison between the proposed SBCG5L-TL inverter and its other 5L-CG-Based TL-inverter counterparts.

Type of Converter	No. of Components				Max No. of ON-Switches	Output Voltage Gain (Type)	Presence of dc offset /TSV(pu)	Soft Charging/ Capacitors Self Balancing	Reported Rated Efficiency
	S(G)	D	C	L					
FC-CG-based [100]	6(6)	0	3	1	3	Unity (Static)	Yes/4	Yes/Yes	97%@1kW
SC-CG-based [39]	6(6)	1	3	1	3	Unity (Static)	Yes/4	No/No	95.8%@1.2kW
SC-CG-based [99]	7(7)	0	3	1	3	Unity (Static)	Yes/4.5	Yes/Yes	97.5%@0.5kW
SC-CG-based [73]	8(8)	0	3	1	4	Double (Static)	Yes/6	No/Yes	97.5%@1kW
SC-CG-based [44]	7(7)	2	4	1	3	Double (Static)	Yes/6	No/Yes	96%@0.04kW
SC-CG-based [70]	7(7)	1	3	1	3	Double (Static)	Yes/6	No/Yes	98.1%@0.6kW
SC-CG-based [47]	8(8)	0	4	2	4	Unity (Static)	Yes/6.5	No/Yes	97.1%@NA
SB/SC-CG-based [96]	7(6)	2	3	2	4	Double (Static)	Yes/5	No/Yes	97.1%@700W
SB/SC-CG-based [108]	10(10)	0	2	2	5	Quadruple (Static)	No/5	Yes/Yes	97.1%@600W
SB-CG-based [105]	10(8)	0	3	2	4	$\frac{2}{1-d}$ (Dynamic)	No/6.5	Yes/No	98.2%@1kW
SB-CG-based [53]	14(10)	0	3	2	6	$\frac{2}{1-d}$ (Dynamic)	No/6.5	Yes/Yes	NA
Proposed SB-CG-based	9(8)	0	3	2	4	$\frac{1}{1-d}$ (Dynamic)	No/6.5	Yes/Yes	97.3%@1.5kW

where, $i_{C2}(t)$ is the passing current through C_2. Hence, regarding the current flowing path analysis conducted before, $i_{C2}(t)$ can be related to $i_g(t)$ through the following relations:

$$i_{C2}(t) = \begin{cases} 2D(t)i_g(t) \ \forall t \in \ [0, \frac{\pi}{6\omega}) \\ 2(1-D(t))i_g(t), \forall t \in \ [\frac{\pi}{6\omega}, \frac{\pi}{2\omega}). \end{cases} \tag{3.26}$$

Considering the standard switching transition time among different inverter output voltage levels in positive half cycle at the grid fundamental frequency and regarding (3.25) and (3.26), the minimum required capacitance for C_2 is obtained as:

$$C_{2,min} \approx \frac{2I_m}{3\pi\omega\Delta V_{C2}}. \tag{3.27}$$

3.2.4 Comparative Study

To show the main features and differences of the proposed SBCG5L-TL inverter over some of the recently introduced CG-based 5L-TL inverters, a comparative study has been conducted in this section and summarized in Table 3.3. The comparative items are the number of required active and passive elements including the input dc-link capacitor and the employed output filters, maximum number of ON state power switches at different switching states, the type/value of output voltage gain, the presence of dc-offset in the output voltage of the inverters with the TSV index across the switches in perunit scale, soft charging and capacitors self-balancing features, and the reported overall efficiency at the rated power. Herein, the terms of S, G, D, C, and L devote the number of required switches, gate drivers, diodes, capacitors and inductors, respectively.

As can be noted from Table 3.3, a few types of SBCG-based TL inverters with a dynamic and adjustable output voltage gain have been proposed so far in the literature. The major portions of the available 5L-CG-based TL inverters belong to the SC or FC-based family with a static output voltage gain. As earlier explained, FC and/or SC-based TL-inverters are only suitable when a large value of the main dc-link voltage is available. Although they require less number of switching devices compared with SB-based TL inverters, another step-up dc-dc stage is needed to deal with a low available dc-link voltage from the PV-arrays. This generally result in an overall lower efficiency compared to a single-stage dc-ac SBCG-based inverters. Additionally, the CGSC-based TL inverters suffer from large discontinuous input inrush current as opposed to the SB-based topologies. This is a main limitation to reach higher range of injected output power. The dc-offset issue can also degrade the inverter output voltage quality, which is the case in CGSC/FC-based TL inverters. Comparing with [105] and [53] that are categorized in the SBCG-based TL inverter family, the proposed topology requires less number of switching devices/gate drivers with the same value of the TSV in perunit scale. Self-voltage balancing of the integrated capacitors and the ability to reach a higher dynamic output voltage gain through the quadratic version of the proposed topology are two important features that can further highlight the potentiality of the proposed topology in comparison with [105] and [53]. The overall cost of the proposed SBCG5L-TL inverter and its quadratic version can be cheaper than the one proposed in [105] and [53] since apart from less number of switching devices, less value of the capacitors with a reduced voltage rating can also be employed.

3.2.5 Verification Results

To further evaluate the performance of the proposed CGSB5L-TL inverter in a grid-connected condition, experimental associated with some simulation results were carried out and summarized in this section. Fig. 3.9 shows the 1.5 kW laboratory-built prototype with the measurement setup, while the main prototype components have been tabulated in Table 3.4. Herein, an Elektro-Automatik PV emulator (model EA-PSI-9750-12) is used as an adjustable dc laboratory power supply to electrically feed the proposed inverter. A 50-Hz grid voltage is also generated by a four-quadrant grid-simulator REGATRON TC30.528.43-ACS, where the grid peak voltage is adjusted to be 311 V throughout the experiments. To connect the proposed inverter to the grid, an L-type filter with values of $L_g = 3.8$ mH and $r_g = 0.33$ is utilized. Regarding the integrated voltage boosting property of the proposed CGSB5L-TL inverter, the input dc voltage is set at 100 V, while the peak

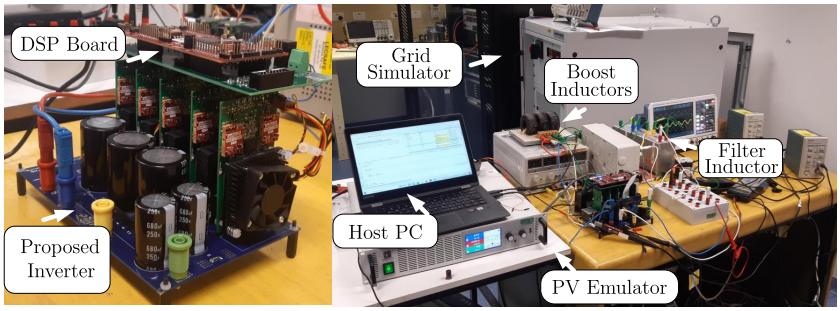


Figure 3.9: Proposed CGSB5L-TL inverter prototype with the measurement setup [106].

Table 3.4: Parameters used for the experimental prototype of the proposed CGSB5L-TL inverter

Element	Type and Description
Power Switches	UJ4C075018K4S
Microprocessor	DSP-TMS320F28379D
Switching Frequency	20
C_1, C_2, and L_{SB}	0.94, 0.68, 0.3H
Gate Drivers	UCC21520DW
Isolated dc/dc Converters	MGJ1D051505MPC
Current Sensor	AMC 1200
Voltage Sensor	ISO224B

of 5L inverter output voltage is supposed to be 400 V with a dc duty cycle of 0.75 as per (3.17).

The nominal voltage of the selected capacitors, C_1 and C_2 is 450 V, and 250 V, respectively whilst a 10% allowable ripple voltage is considered for them. Also, the input boost inductor, L_{SB}, is selected based on its nominal saturated current and the input dc current at the extreme case study. The selection of SiC switches is based on their very low ON state resistance, low value of the drain-source capacitance, and very low value of the required reverse recovery charge i.e., $Q_{rr} = 102nC$. Regarding the SiC power switches used in the prototype, a 20 kHz switching frequency is chosen, which results in $T_s = 50\mu$S sampling time to execute the GVO and the PR controller. Taking Table 3.4 into account, the required gate switching pulses have also been provided using a standard DSP with the model number of TMS320F28379D. A peak of 9.5 A for the grid current reference has also been chosen to inject around 1.5 kW power to the grid.

Considering the above-mentioned notions, an experimental steady-state performance of the proposed inverter is shown in Fig. 3.10(a) and (b). Here, the grid voltage, the injected grid current, the 5L inverter output voltage, and the voltage across C_1 and C_2 are shown, respectively. As can be seen, through the proper balanced voltage of

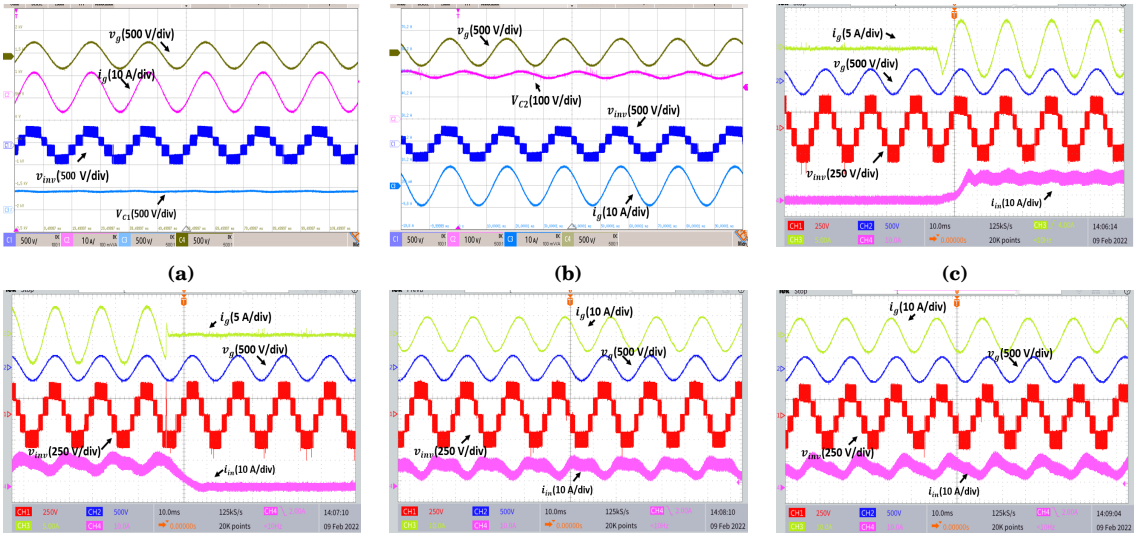


Figure 3.10: Experimental waveforms of the proposed CGSB5L-TL inverter in the closed-loop grid-tied condition showing the grid voltage, the injected grid current, and the 5L inverter output voltage (a) with the presence of the voltage across C_1 at 1.5 kW injected power, (b) with the presence of the voltage across C_2 at 1.5 kW injected power, (c) with the presence of the input current when the injected power is changed from zero to 1.1 kW, (d) with the presence of the input current when the injected power is changed from 1.1 kW to zero, (e) with the presence of the input current and under a lagging reactive power support mode, and (f) with the presence of the input current and under a leading reactive power support mode [106].

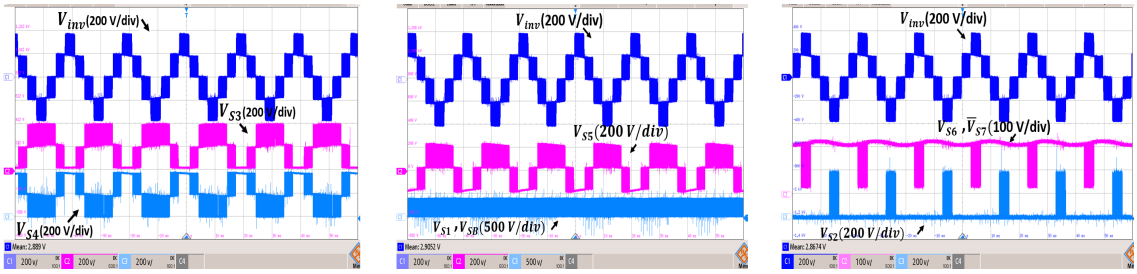
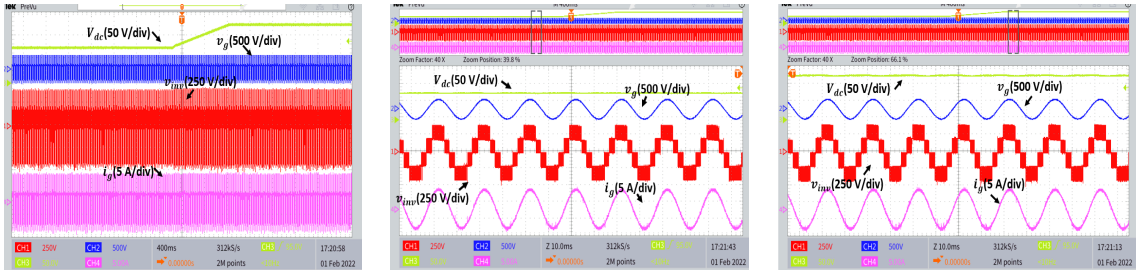


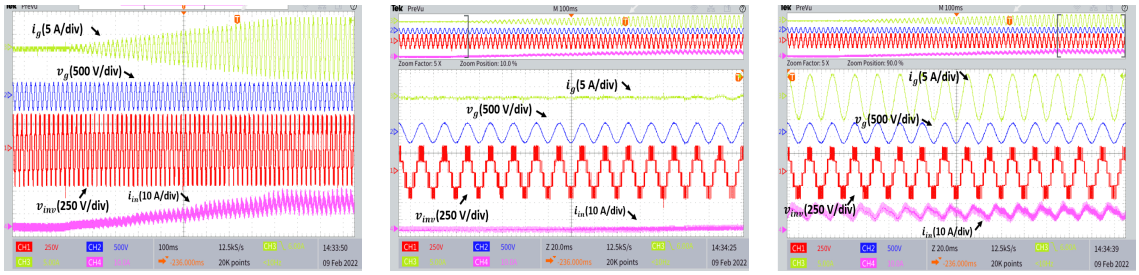
Figure 3.11: Experimental waveforms of the proposed CGSB5L-TL inverter output voltage with (a) MVS across S_3, and S_4, (b) MVS across S_5, S_1, and S_{SB}, and (c) MVS across S_6, S_7, and S_2 [106].

the capacitors, e.g., 400 V, 200 V as for the voltage across C_1 and C_2, respectively, all distinctive 5L in the output voltage are generated. Moreover, as a result of this, a high quality injected current can also be observed. The maximum output voltage of the inverter is 400 V reflecting the integrated voltage boosting feature of the converter. To attest the acceptable dynamic performance of the proposed converter, a step change from zero to around 1.1 kW injected power and vice versa in the reference current is applied as shown in Fig. 3.10(c) and (d). The results contain the continuous input current waveform, as well. As can be seen, the proposed closed-loop grid-connected system with the implemented PR controller presents a fast dynamic response in tracking the assigned



(a) (b) (c)

Figure 3.12: Grid-connected experimental result at 1 kW injected power, (a) under a dynamic test in input dc voltage changing within a ramp trend from 70 V to 130 V, (b) a zoom shot of the result when the input dc voltage is at 70 V, and (c) a zoom shot of the result when the input dc voltage is at 130 V [106].



(a) (b) (c)

Figure 3.13: Grid-connected experimental result at 1.1 kW injected power, (a) under a dynamic test when the peak of the reference current is changed from zero to 7 A, (b) a zoom shot of the result when the peak of the reference current is zero, and (c) a zoom shot of the result when the peak of the reference current is 7 A [106].

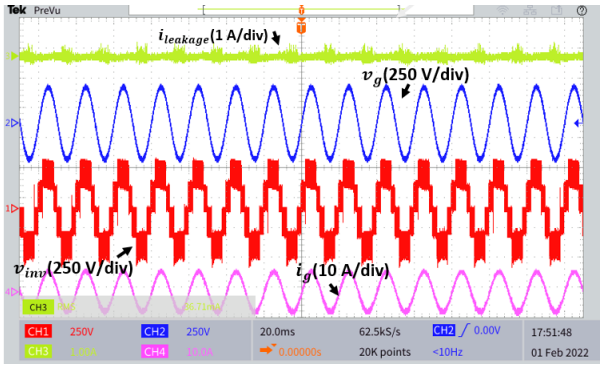


Figure 3.14: Grid-connected experimental result showing the leakage current propagation of the proposed SBCG5L-TL inverter in presence of 1.2 kW injected power [106].

reference current. From these results, it can also be revealed that the input current is free from large discontinuous inrush current as opposed to other available CGSC-based TL inverters with a static voltage gain technique. The reactive power support performance of the proposed system in both the lagging and leading injected grid current conditions have been shown in Fig. 3.10(e) and (f), respectively. In both cases, the converter can inject around 1 kW and 1 kVAR power to the grid.

Having taken the same value of the input dc voltage and the dc duty cycle, the 5L

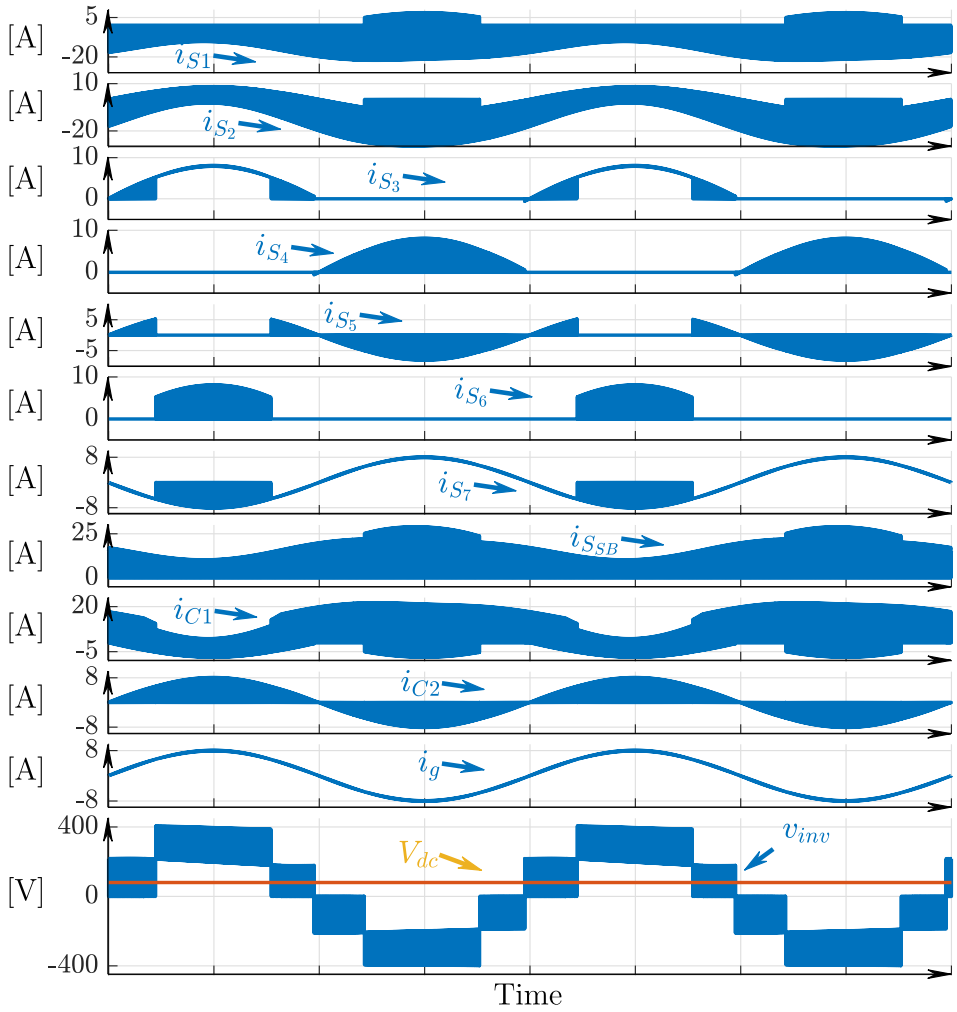


Figure 3.15: Simulation results showing the current stress profile of the integrated switches and capacitors in the proposed SBCG5L-TL inverter under 1.2 kW injected power to the grid [106].

inverter output voltage along with the MVS waveforms of all the integrated switches are illustrated in Fig. 3.2.5, where the results conform the relationships presented in (3.15). Here, the maximum MVS is equal to the maximum inverter boosted voltage,i.e., 400 V, while the switches S_5, S_6, and S_7 have to tolerate a half value of this maximum voltage.

Conversely, to show the dynamic voltage boosting capability of the proposed CGSB5L-TL inverter, the value of the input dc voltage is changed to possess a ramp trend from 70 V to 130 V. Herein, to inject the same amount of power to the grid, which is the case for MPPT purpose, the maximum fundamental value of the inverter output voltage mentioned in (3.33) must be fixed at V_m. Hence, a peak of 6 A is selected for the CRG stage of the closed-loop control system, which results in around 1 kW injected power. To keep fixed the maximum value of the inverter output voltage at 400 V, the dc duty

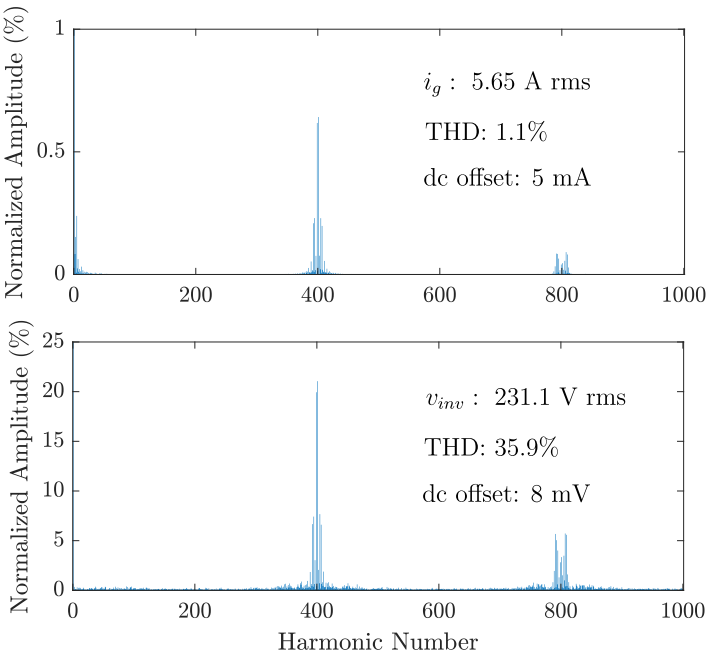


Figure 3.16: FFT analysis of the grid current and the inverter output voltage at 1.2 kW injected power [106].

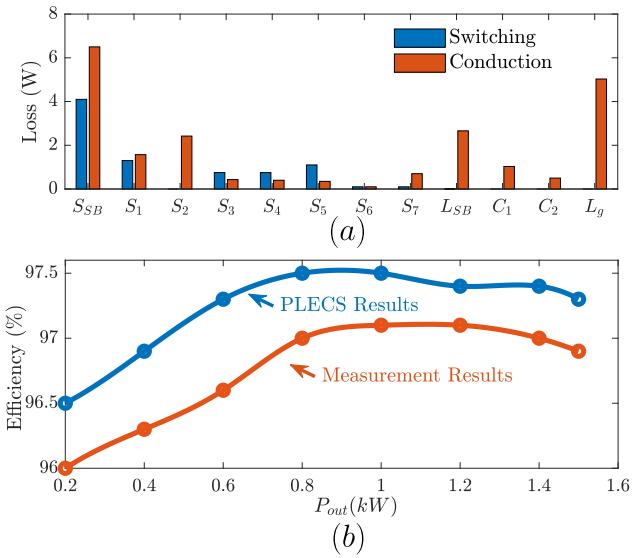


Figure 3.17: (a) Loss analysis of the proposed CGSB5L-TL inverter at the rated power, and (b) efficiency results extracted by the PLECS and measurement [106].

cycle, d, must be dynamically changed from 0.82 to 0.67. The experimental results of this dynamic test are shown in Fig. 3.12(a)-(c), while there is no change in the peak value of the injected grid current. Even though having a large variation in the input dc voltage value, all the 5L output voltage waveform with a high quality are generated and the peak output voltage of the inverter is not affected by this variation.

Alternatively, Fig. 3.13(a)-(c) show the relevant experimental results of the proposed

CGSB5L-TL inverter when the peak of reference current waveform is changed with a 1 second from zero to 7 A. In this case, the input dc voltage value is set at 100 V, while the dc duty cycle, d is fixed at 0.75. The leakage current suppression capability of the proposed CGSB5L-TL inverter is also verified experimentally at 1.2 kW injected power as shown in Fig. 3.14, while the maximum rms value of the $i_{leakage}$ is less than 30 mA.

Since the fabricated prototype is designed with a compact printed circuit board as depicted in Fig. 3.9, the current stress profiles of all the integrated switches as well as capacitors are investigated through the PLECS simulation software. The result of this simulation has been shown in Fig. 3.15, while 1.2 kW power with the input dc voltage equal to 80 V is injected to the grid. In this case, the value of the dc duty cycle is set at 0.8 to achieve 400 V for the peak voltage of the proposed CGSB5L-TL inverter. As can be confirmed, due to incorporating the SB technique associated with FC concept for C_1 and C_2, respectively, the current passing through the involved switches does not contain any large discontinuous inrush spikes. Here, only the switches integrating in the SB module experience the highest current stress related to the voltage boosting property of the proposed topology, whereas the rest of the switches are passing a chopped waveform of the injected grid current. The FFT analysis of the 5L inverter output voltage and the injected grid current at the same rated power have also been shown in Fig. 3.16. As can be seen the THD of the output voltage and the injected grid current is 35.9% and 1.1%, respectively, at 20 kHz switching frequency, while there is no significant dc-offset in the captured waveforms.

Finally, with respect to the information compiled in the data sheet of the power switches, and the circuit specification of the proposed topology at the rated power, i.e., P_{out} = 1.5 kW, a loss analysis has been developed in the PLECS and its details are shown in Fig. 3.17(a). Here, the input dc voltage is set at 80 V, while the peak of the inverter output voltage is kept at 400 V. The losses associated to the passive elements are considered based on their internal equivalent series resistance, ESR, and the rms value of the injected grid current. Regarding this, a comparative efficiency curve between the results extracted from the PLECS and the data captured by the experiment is conducted and shown in Fig. 3.17(b). As for the measurement results, a Voltech PM3000A Universal Power Analyzer is used, while the peak efficiency of the proposed CGSB5L-TL inverter was above 96.5% over a wide range of injected output power.

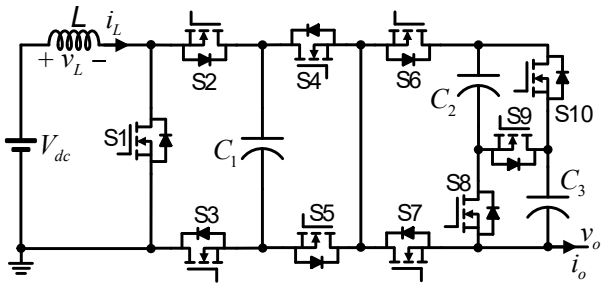


Figure 3.18: The proposed CGSB7L-TL inverter [109].

3.3 Proposed CGSB7L-TL Inverter with Single-Stage Dynamic Gain

In following the above-mentioned proposed CGSB5L-TL inverters with a dynamic voltage boosting feature, a new CGSB7L-TL inverter is proposed in this section. The number of output voltage levels for this proposed topology is enhanced to seven, whilst attaining a flexible output voltage conversion gain, which is an important factor for dealing with low and wide varying input dc source in grid-tied PV applications.

The overall structure of the proposed CGSB7L-TL inverter is illustrated in Fig. 3.18. As can be seen, the proposed topology is comprised of 10 unidirectional power switches, three capacitors, and one input inductor. The ground of the input dc source and the load/grid is tied to each other, which results in a CG-based configuration for the overall structure. Herein, the front-end inductor, L, the capacitor C_1 and three power switches S_1, S_2 and S_3 act as a boost-integrated circuit for the proposed topology. Hence, with a proper high switching conversion over each sampling/switching time, a boosted voltage equal to $V_{dc}/(1-d)$ is converted across C_1. In this case, d is a fixed duty cycle for the switch, S_1, and V_{dc} is the input dc voltage provided by any types of RE resources like PV string panels.

To generate all the desired 7L output voltage of the inverter, two switches from this front-end boost-integrated circuit, S_2 and S_3, as well as all the remaining power switches from the rest of the circuit must also be driven by a sinusoidal PWM duty cycle. Details of working principles of the proposed topology, while generating different output voltage levels are depicted in Fig. 3.19.

As can be observed, the inverter output voltage levels are made by the stored voltages of the involved capacitors. In this case, the maximum output voltage of the proposed CGSB7L-TL inverter in both half cycles, e.g., the top positive (+3) and top negative (-3) are equal to (3.28), while to create all the middle output voltage levels in both half cycle,

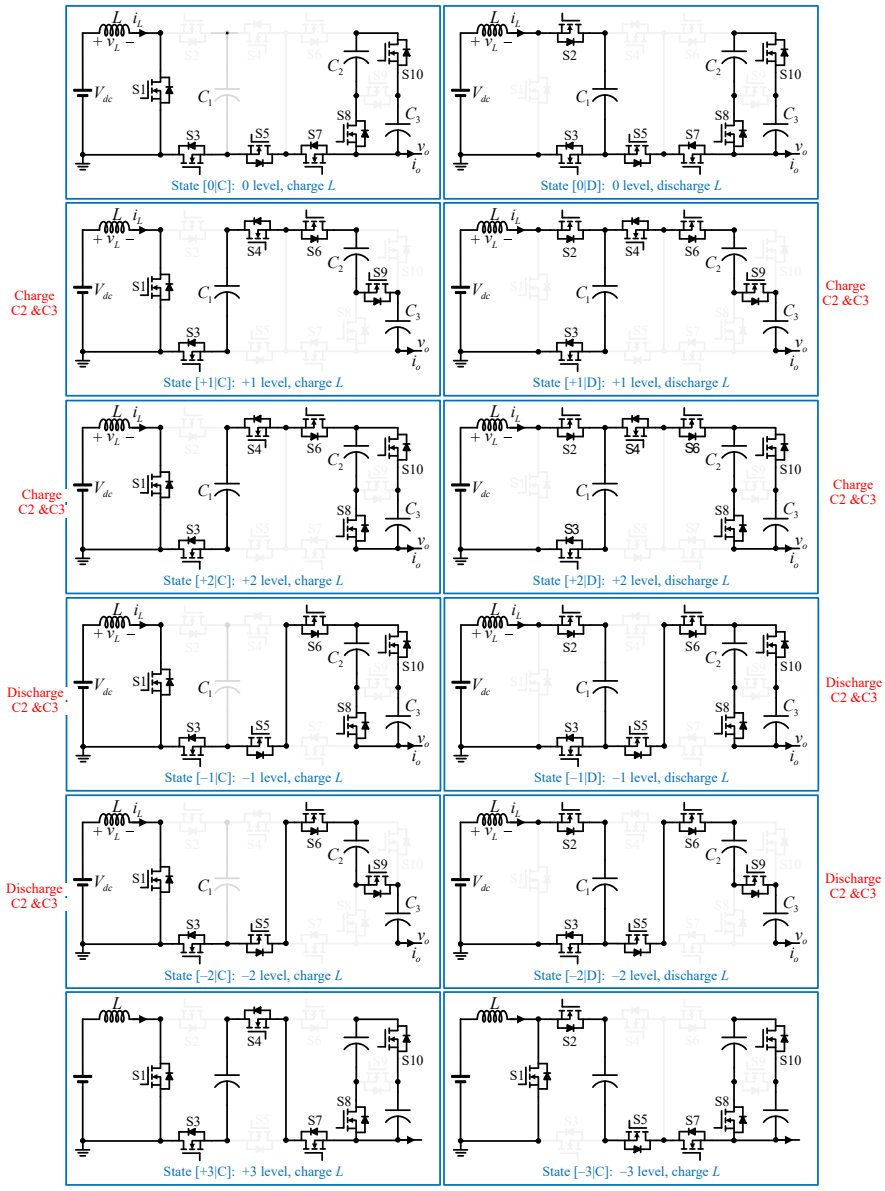


Figure 3.19: Different current flowing paths of the proposed CGSB7L-TL inverter [109].

the voltage across C_2 and C_3 must be balanced at (3.29).

$$V_{max} = V_{C1} = \frac{V_{dc}}{1-d} \tag{3.28}$$

$$V_{C2} = V_{C3} = \frac{V_{dc}}{3(1-d)}. \tag{3.29}$$

Herein, to keep a steady boosted voltage across C_1 during whole the switching operation, except the top positive and negative output voltage levels, two charging and discharging sub-modes are defined during each output voltage level generation as can be seen from Fig. 3.19. Here, in one sub-mode and during a switching time interval of dT_{sw},

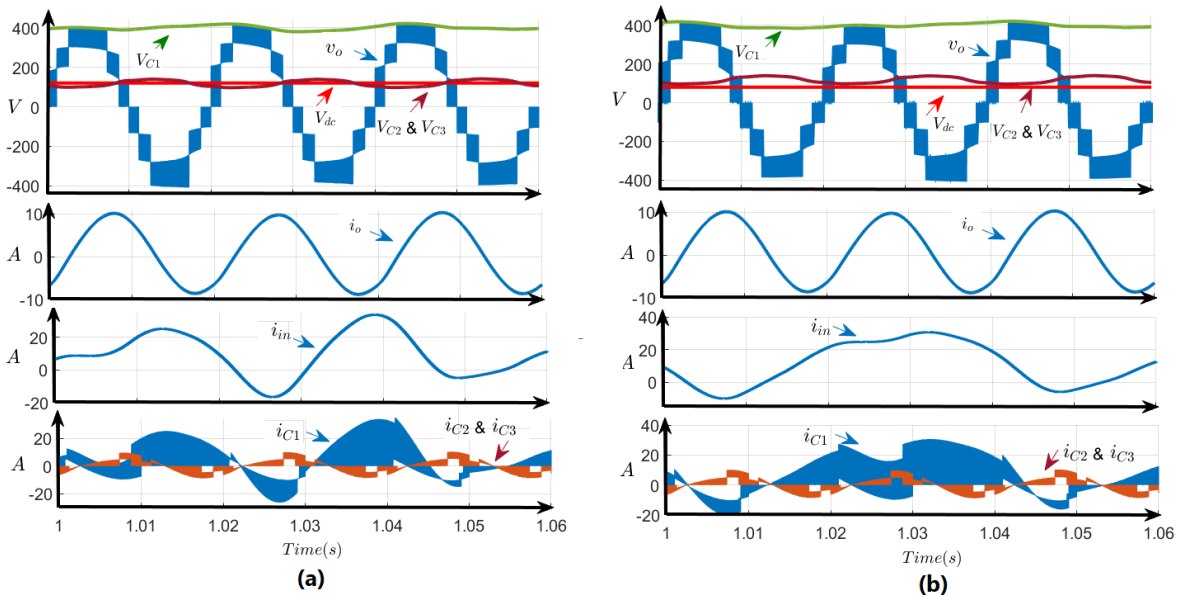


Figure 3.20: Simulation results of the proposed CGSB7L-TL inverter at (a) $D = 0.7$, (b) $D = 0.8$ [109].

the input inductor is charged through the switch S_1. Also, in the remaining dc duty cycle of S_1, the inductor is discharged through the path of input dc source, switches S_2 and S_3, and the capacitor C_1. These two sub-modes cannot be operated in top negative output voltage level as the condition of generating these levels is to keep switch S_1 ON all the time. Therefore, considering M as the peak value of the ac modulation index, the dynamic voltage boosting gain of the converter can be expressed as (3.30) [109]:

$$G = \frac{M}{1-d}. \tag{3.30}$$

From the current flowing paths illustration, it can also be realized that the charging/discharging operation of C_2 and C_3 are made by the load current direction in positive and negative half cycle of the operation. Therefore, both of these capacitors can only see a chopped waveform of the load/grid current as their respective current stress profile. Alternatively, owing to the incorporated boosted inductor in the front-end boost-integrated circuit, the current stress profile of all the switches that are involved in the charging path of C_1 is limited to a permissible input current range. Moreover, the maximum voltage stress across the switches, which corresponds to the maximum OFF-state drain-source

voltage of the switches can also possess an acceptable value as summarizing in (3.31):

$$\begin{aligned} V_{S_i} &= \frac{V_{dc}}{1-d}, \forall i \in \{1,2,3,4,5\} \\ V_{S_7} &= \frac{V_{dc}}{2(1-d)} \\ V_{S_j} &= \frac{V_{dc}}{3(1-d)}, \forall j \in \{6,8,9,10\} \end{aligned} \tag{3.31}$$

In order to show the correct performance of the proposed SBCG7L-TL inverter, two case studies for the dc duty cycle of $d = 0.7$, and $d = 0.8$ have been considered in a standard MATLAB simulation platform as shown in Fig. 3.20(a) and (b), respectively. Herein, a LS-SPWM technique was used to provide the required gate switching pulses. The switching frequency of the modulation is chosen at 100 kHz, and the value of the input inductor is set at 300uH. The capacitance of C_1 is set at 1mF, while C_2 and C_3 are adjusted to be the same as 680uF. In both the cases, a simple R-L load with value of 25 Ohm and 100mH is considered. As for the case of $d = 0.7$, the input dc voltage is set at 120 V, while for the given case of $d = 0.8$, its value is 80 V. The 7L waveform of the inverter output voltage, the capacitors voltages, the input voltage, the input current, and the capacitors current have been shown for both the above-mentioned case studies. As can be observed, all the 7L output voltage waveform within a smooth performance of the converter from the input current view point are generated, while the load current is sinusoidal with a peak of 8 A. The peak of inverter output voltage is 400 V in both the cases, which is in agreement with (3.31). The capacitors voltages of C_2 and C_3 are both balanced at one-third value of the boosted voltage across C_1 which confirm the theoretical observation expressed in (3.29). The input current waveform in both the cases are quite continuous without inducing any inrush spikes in both the cases as well.

CHAPTER 4

MID POINT-CLAMPED-BASED MLIS

Application of mid-point-clamped MLIs have been significantly broadened in recent years due to better performance, reduced common-mode voltage and leakage current, bidirectional power flow capability and simplicity in circuit design. Nonetheless, the dc-link voltage utilisation factor is only 50% (i.e. the peak of the ac output voltage is half of the dc-link voltage), which require additional front-end boost integrated circuit to accommodate low and wide varying input voltage. In this chapter, a single-stage ANPC-5L boost integrated inverter is presented first, which is able to meet the peak amplitude of the grid voltage even when the dc-link voltage is low and wide varying. Compared with the conventional two-stage ANPC-5L or stacked-multicell (SMC) 5L inverters with a front-end bidirectional boost converter, the proposed topology requires the same number of power switches, whilst providing more flexible/dynamic voltage conversion gain with a reduced total standing voltage across the switches. Afterwards, the concept of dual-mode (DM) converter that can retain a good ac voltage quality with a reduced voltage stress on devices over a wide range of the input dc voltage is applied to a new family of ANPC-5L-TL inverter. Hence, they can be operated in either buck or boost mode that caters a wide range of input dc voltage utilization with an improved performance. Each of the proposed DM-ANPC-5L converters requires 10 power switches, while they offer a bidirectional power flow feature with an integrated FC and/or SC concept. Extensive analysis, comparative study, simulation and several experimental results obtained from a laboratory-built prototype operating in the grid-connected condition are presented to validate the performance of the proposed converters.

4.1 Proposed Dual-Boost ANPC-5L Iinverter with Integrated Single-Stage Dynamic Voltage Gain

As earlier stated, among many families of MLIs, those topologies are of interest, which can provide a reliable operation in terms of CMV, leakage current propagation issue, and voltage/current stress profile of the involved semiconductor devices. Integration of the SC concept into the conventional ANPC-MLIs results in introducing ABNPC-based MLIs [25]. They have become a popular solution to reduce the burden of this front-end dc-dc boost converter. Nonetheless, similar to the CGFC/SC-based MLIs, the overall voltage conversion gain of the inverter stage is still static (fixed). This is an additional setback in addition to inducing a large discontinuous input current and a spiky current stress profile for the SC-network switches in both the ABNPC or CGSC-based MLIs [28]. In this context, integration of the SB cells consisting of some switches, diodes, capacitor(s) and inductor(s) that are controlled with a fixed dc duty cycle have also been adopted in mid-point-clamped [110] and CG-based MLIs [96, 108]. However, the problem of static output voltage gain for the inverter stage still remains in place, which calls another power processing stage for whole the system.

Having taken the above-mentioned contributions into account, the aim of this subsection is to present a novel single-stage ANPC-based 5L inverter with an integrated SB concept. The proposed topology requires two boost inductors, four dc-link capacitors, and 10 power switches, and is named as dual-boost (DB)-ANPC-5L inverter in the rest of the article. Owing to the utilization of the inductors with a SB technique, the overall voltage conversion gain of the proposed converter is flexible and two times larger than a standard two-stage system including a dc-dc bidirectional boost converter followed by a back-end ANPC-5L inverter. Moreover, with the same number of required power switches compared to the above-mentioned two-stage converter, the overall TSV index of the proposed DB-ANPC-5L inverter is lower. Further, a bidirectional power flow performance can also be possible making its application more broaden even for EV systems with vehicle-to-grid (V2G) and grid-to-vehicle (G2V) operations. Regarding a symmetric power sharing performance among the switches in both half cycle, the gate switching pulses of the proposed topology can be provided with either PS or LS-PWM techniques. Continuous input current waveform, reduced size of required passive elements and three-phase circuit extension capability with a reduced switch-count design are other important features of the proposed DB-ANPC-5L inverter.

Conventional two-stage grid-connected system feeding through a single input dc

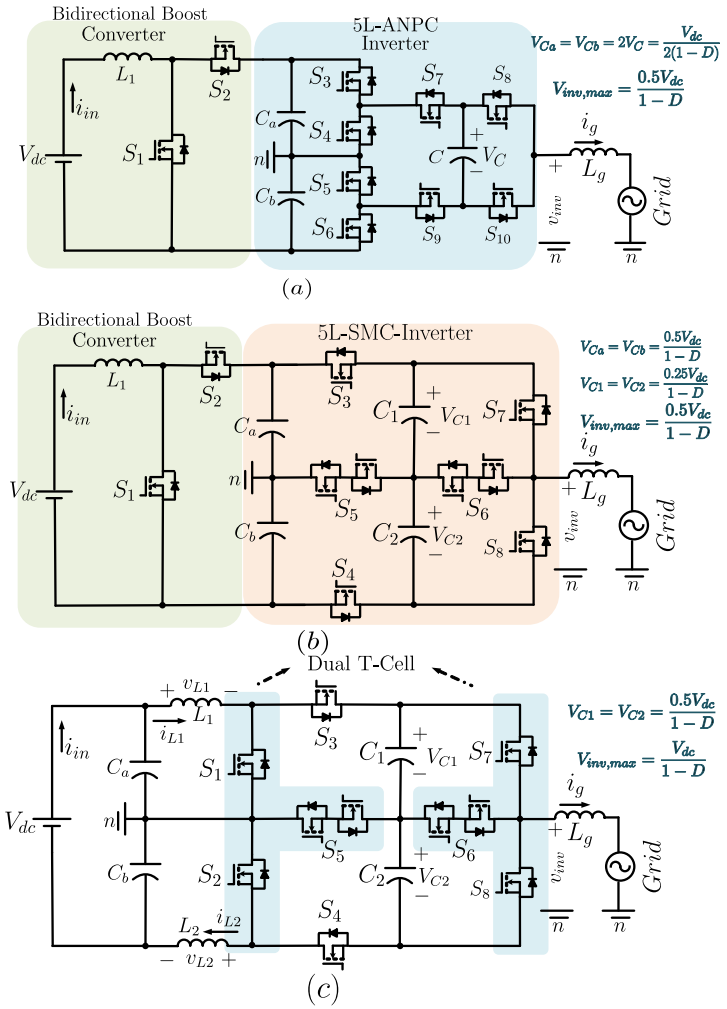


Figure 4.1: Grid-connected system based on (a) conventional two-stage platform with front-end dc-dc boost converter and a back-end ANPC-5L inverter, (b) conventional two-stage platform with front-end dc-dc boost converter and a back-end SMC-5L inverter and (c) the proposed single-stage DB-ANPC-5L inverter [111].

source, V_{dc}, and being constructed based on a front-end dc-dc boost converter followed by an ANPC- or SMC-5L inverters are illustrated in Fig. 4.1(a) and (b), respectively. This circuit architecture is being widely used in both PV and EV applications due to its reduced CMV profile, bidirectional power flow performance, standard design with five half-bridge switch modules available in the market, possibility to be modulated with both PS and LS-PWM techniques, and reduced voltage/current stress profile of its switches. Considering a dc duty cycle of D as for the switches S_1 and S_2, the maximum 5L output voltage of this two-stage system is $\frac{0.5V_{dc}}{1-D}$, while its capacitors voltages are:

$$V_{C_a} = V_{C_b} = 2V_C = \frac{V_{dc}}{2(1-D)}. \tag{4.1}$$

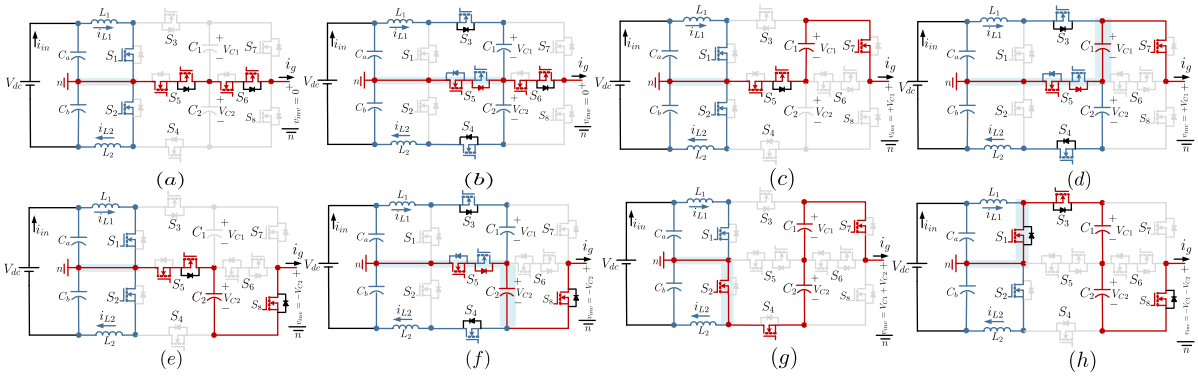


Figure 4.2: Different current flowing paths of the proposed DB-ANPC-5L inverter at (a) $v_{inv} = 0$ and charging operation of the boost inductors, (b) $v_{inv} = 0$ and charging operation of the capacitors, (c) $v_{inv} = +V_{C1}$ and charging operation of the boost inductors, (d) $v_{inv} = +V_{C1}$ and charging operation of the capacitors, (e) $v_{inv} = -V_{C2}$ and charging operation of the boost inductors, (f) $v_{inv} = -V_{C2}$ and charging operation of the capacitors, (g) $v_{inv} = +V_{C1} + V_{C2}$ and charging operation of the boost inductors, and (h) $v_{inv} = -V_{C1} - V_{C2}$ and charging operation of the boost inductors [111].

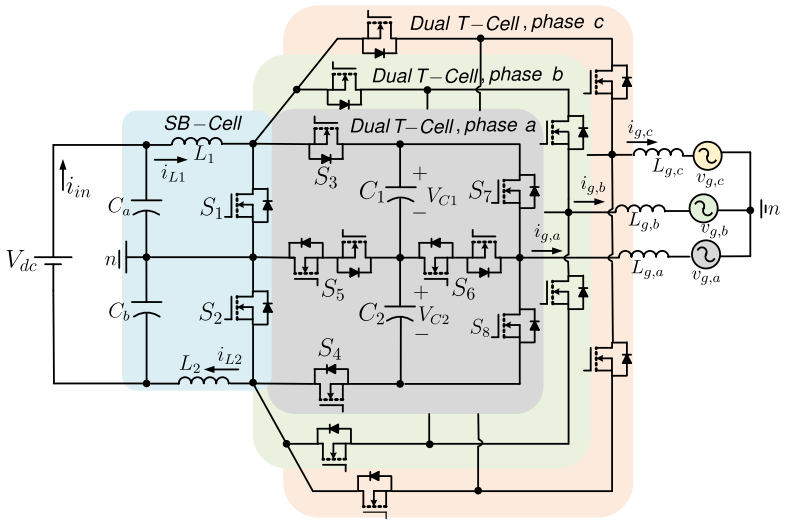


Figure 4.3: Three-phase extension of the proposed DB-ANPC-5L inverter [111].

The leakage current propagation issue in this system is minimal as long as an active voltage balancing for the dc-link capacitors, C_a, and C_b is to be provided. Otherwise, for each of these dc-link capacitors, a dedicated front-end dc-dc boost converter is needed, which can enlarge the overall cost and complexity of the control system.

As opposed to this standard topology, the proposed DB-ANPC-5L inverter requires a single-stage circuit design as shown in Fig. 4.1(c). Herein, the same number of power switches has been employed with a two standard T-Type switching modules and two discrete power switches. Two boost inductors, L_1 and L_2 in the upper and lower sides of the dc-link capacitors are also used. Herein, both the switches S_1 and S_2 are operated within a flexible dc duty cycle of D, which can be adjusted based on the availability

Table 4.1: Voltage stress across the switches for the proposed single-stage DB-ANPC-5L inverter and its two-stage conventional counterparts.

Switches	Proposed Topology	ANPC-5L Fig. 4.1(a)	SMC-5L Fig. 4.1(b)
S_1, S_2	$\frac{0.5V_{dc}}{1-D}$	$\frac{V_{dc}}{1-D}$	$\frac{V_{dc}}{1-D}$
S_3, S_4	$\frac{V_{dc}}{1-D}$	$\frac{0.5V_{dc}}{1-D}$	$\frac{0.5V_{dc}}{1-D}$
S_5, S_6	$\frac{\pm 0.5V_{dc}}{1-D}$	$\frac{0.5V_{dc}}{1-D}$	$\frac{\pm 0.25V_{dc}}{1-D}$
S_7, S_8	$\frac{V_{dc}}{1-D}$	$\frac{0.25V_{dc}}{1-D}$	$\frac{0.5V_{dc}}{1-D}$
S_9, S_{10}	NA	$\frac{0.25V_{dc}}{1-D}$	NA

of the input dc voltage and the peak of the grid voltage. Hence, both switches S_1 and S_2 require the same gate switching pulses. Considering the four-quadrant switching arrangement as for S_5 and S_6, only seven PWM signals are required for the proposed system. Concerning V_{C1} and V_{C_2} as the boosted voltages across C_1 and C_2, respectively, five distinctive output voltage levels e.g. zero, V_{C1}, $-V_{C2}$, $V_{C1}+V_{C2}$, and $-V_{C1}-V_{C2}$ are generated at the output of the proposed inverter. For both the conventional two-stage and the proposed single-stage system, L_g acts as the grid-interfaced filter.

Different current flowing paths of the proposed DB-ANPC-5L inverter per each output voltage level are depicted in Fig. 4.2(a)-(h). Herein, the charging paths of the inductors and capacitors are highlighted with a blue color, while the grid current flowing path is shown in a red color. As can be realized, except the top positive [see Fig. 4.2(g)] and the top negative [see Fig. 4.2(h)] output voltage levels, the remaining output voltage levels are made based on two operating sub-modes per switching time interval. In one of these sub-modes, both the inductors are charged to the voltage across the dc-link capacitors of C_a or C_b through two independent power loops e.g., C_a, L_1, S_1 and C_b, L_2, S_2. Consequently, in the other operating sub-mode, the capacitors C_1 and C_2 are being charged to the voltage across L_1, and L_2 and the voltage across C_a and C_b through two others independent power loops e.g., C_a, L_1, S_3, S_5, C_1, and C_b, L_2, S_4, S_5, C_2. As is clear from Fig. 4.2(a) to (f), during the output voltage generation in zero and the first positive/negative levels, these power loops act as two integrated boost circuits (dual boost circuits). To succeed the desired zero and the first positive/negative output voltage levels, the four-quadrant switch S_5 is always ON, while the pair switches of S_1/S_2, and S_3/S_4 are switching within a complementary dc duty cycle fashion in respect to D. Therefore, having taken these sub-modes switching operations as dual boost circuits over each switching frequency, the following relationship for the involved capacitors voltages can

be expressed as:

$$V_{C_1} = V_{C_2} = \frac{0.5V_{dc}}{1-D}$$
$$V_{C_a} = V_{C_b} = 0.5V_{dc}. \tag{4.2}$$

Conversely, considering Fig. 4.2(g) and (h), the charging operation of the capacitors C_1 and C_2 is not possible during the top positive and the top negative output voltage levels generation since switches S_1 and S_2 must be always ON to provide the grid current flowing path. It is clear from Fig. 4.2(g) and (h) that both switches S_3, and S_4 require an ac duty cycle during these time intervals of the operation, as well. Herein, in order to symmetrically keep the charging operation of both inductors, both switches S_1, and S_2 still are being switched under the dc duty cycle D. It is also worth mentioning that similar to any T-Type network, the role of switches S_6,S_7, and S_8 is for polarity inverting purpose. Hence, all these switches are driven based on the line switching frequency.

Considering the value of the inverter output voltage in the top positive/negative levels, which are made by the summation of the voltages across C_1, and C_2, the maximum voltage of the proposed DB-ANPC-5L inverter is equal to $\frac{V_{dc}}{1-D}$. Apparently, this value is two times larger than its counterpart two-stage topology shown in Fig. 4.1(a). The voltage stress across different switches of the proposed single-stage DB-ANPC-5L inverter and its two-stage ANPC/SMC-5L inverter-based counterparts [Fig. 4.1(a) and (b)] have been tabulated in Table 4.1. Regarding this circuitry analysis, the following points are highlighted as:

1) Considering the maximum value of the 5L inverter output voltage and regarding Table I, the TSV index of the proposed converter in per unit scale is seven, while for its two-stage counterpart with a front-end dc-dc boost converter plus a back-end standard ANPC-5L inverter, this value is 10. Reduced value of the TSV index in the proposed DB-ANPC-5L inverter can reflect the fact that the overall manufacturing cost of the proposed system is smaller whist due to the reduced $\frac{dv}{dt}$ across the switches, less EMI noises are propagated during the operation.

2) Comparing with the conventional two-stage system, the dc-link capacitors of the proposed DB-ANPC-5L inverter should tolerate less value of the nominal voltage, i.e., only half value of the main dc-link voltage, which helps to incorporate small film or electrolyte capacitors for C_a and C_b. Also, both C_1 and C_2 must be able to only tolerate the half peak output voltage value of the inverter. This can significantly reduce the overall withstand voltage across the capacitors and can help entire the system to possess an acceptable overall power density.

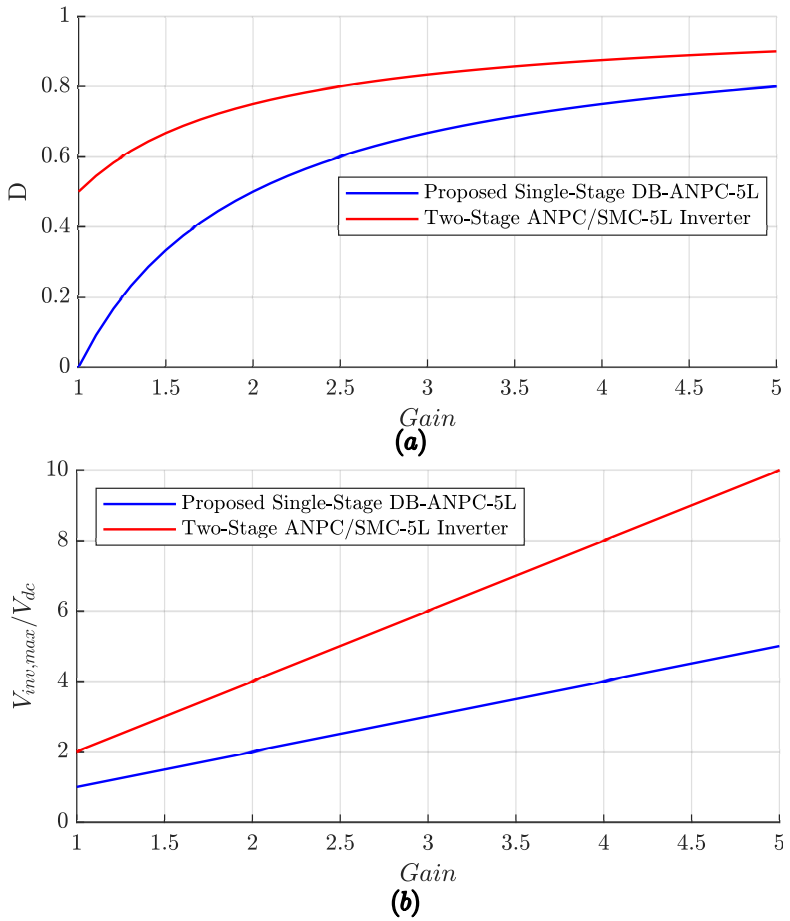


Figure 4.4: A comparative study of the working region between the proposed DB-ANPC-5L inverter and the conventional two-stage ANPC/SMC-5L-based converters, (a) dc duty cycle, D versus the overall voltage conversion gain, (b) the ratio between $V_{inv,max}/V_{dc}$ and the overall voltage conversion gain [111].

3) In the conventional two-stage ANPC and/or SMC-5L converters, the top positive/negative inverter output voltage levels are generated by discharging each of the dc-link capacitors. Hence, this causes a half dc-link voltage utilization in the ac output. Conversely, these output voltage levels are created by the aim of series connection of the boost capacitors, C_1 and C_2, leading to full dc-link voltage utilization in the output with less value of the required dc duty cycle, D, and enhancement in the voltage conversion gain. The comparative curves of the variations of D and $V_{inv,max}/V_{dc}$ versus the overall voltage conversion gain are illustrated in Fig. 4.4(a) and (b), respectively.

4) The proposed DB-ANPC-5L inverter can be extended to a three-phase design as shown in Fig. 4.3. Considering the dc-link capacitors and the boost inductors with switches S_1 and S_2 as the SB-cell, the rest of the circuit configured based on dual T-cell can be stacked to realize the three-phase multilevel operation for entire the

Table 4.2: ON switching states of the proposed DB-ANPC-5L inverter modulated with a PS-PWM technique.

$d(t)$ Sign	PS-PWM Condition	ON State Switches	v_{inv}
P	$\|d(t)\| \geq A_a, A_b$, D$\geq A_b$	S_1, S_2, S_4, S_7	$V_{C1}+V_{C2}$
	$A_a \leq \|d(t)\| < A_b, D \geq A_b$	S_1, S_2, S_5, S_7	V_{C1}
	$A_b \leq \|d(t)\| < A_a, D \geq A_b$	S_1, S_2, S_5, S_7	V_{C1}
	$A_a \leq \|d(t)\| < A_b, D < A_b$	S_3, S_4, S_5, S_7	V_{C1}
	$A_b \leq \|d(t)\| < A_a, D < A_b$	S_3, S_4, S_5, S_7	V_{C1}
N	$\|d(t)\| \geq A_a, A_b$, D$\geq A_b$	S_1, S_2, S_3, S_8	$-(V_{C1}+V_{C2})$
	$A_a \leq \|d(t)\| < A_b, D \geq A_b$	S_1, S_2, S_5, S_8	$-V_{C2}$
	$A_b \leq \|d(t)\| < A_a, D \geq A_b$	S_1, S_2, S_5, S_8	$-V_{C2}$
	$A_a \leq \|d(t)\| < A_b, D < A_b$	S_3, S_4, S_5, S_8	$-V_{C2}$
	$A_b \leq \|d(t)\| < A_a, D < A_b$	S_3, S_4, S_5, S_8	$-V_{C2}$
-	$\|d(t)\| \leq A_a, A_b D \geq A_b$	S_1, S_2, S_5, S_6	0
	$\|d(t)\| \leq A_a, A_b D < A_b$	S_3, S_4, S_5, S_6	0

system. This comes from the fact that both the SB-cell switches need only the boost dc duty cycle, while a combination of the dc and ac duty cycles that are different per phase are required for the rest of dual T-cell in each phase.

5) As opposed to the SC-based mid-point-clamped MLIs, the input current, i_{in}, is free from large discontinuous inrush spikes and it only possesses the double-line frequency in the single-phase grid-connected operation. Such a continuous waveform profile can facilitate the incorporation of APD and single-stage MPPT in the control design of the system.

6) Due to incorporation of the inductors in the SB-cell stage, only four switches S_1, S_2, S_3, S_4 of the proposed DB-ANPC-5L inverter experience a current stress equal to the charging current of the boost capacitors C_1 and C_2. The remaining switches experience the intended peak value of the injected grid current, i_g. This helps the proposed converter to possess an acceptable thermal and conduction loss distribution to reach higher range of the injected power with a reliable overall operating temperature.

4.1.1 Modulation and Control Strategy

As earlier stated, to provide the required gate switching pulses for the proposed DB-ANPC-5L inverter, two control references representing the dc and ac duty cycles of the switches are needed. In case of having an input dc source with a wide range of variations

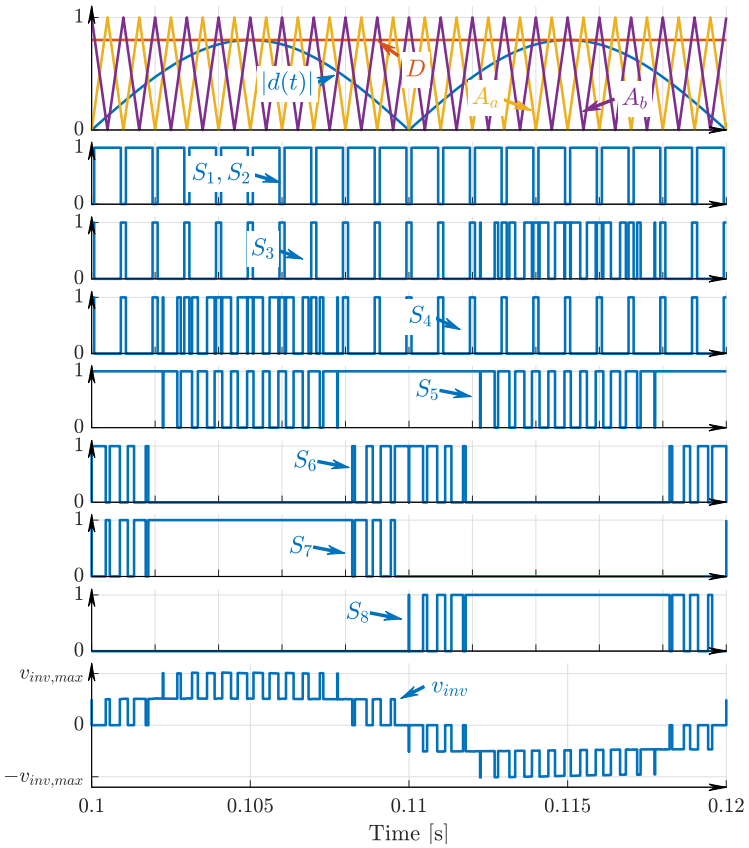


Figure 4.5: Modulation and gate pulses of the proposed DB-ANPC-5L inverter.

like PV string arrays, the dc reference, D, can be provided through the information of the MPPT and APD processes to meet the required amplitude of the grid voltage. On the other hand, since all the involved capacitors of the proposed DB-ANPC-5L are self-balanced based on the described switching platform, the only controllable variable to inject the power to the grid is the injected grid current, i_g. The proposed grid-connected inverter can be governed to track a desired reference current, $i_g^\star$, by handling the ac reference, $d(t)$.

Herein, any kinds of single-objective time-domain or frequency-domain-based controllers can be adopted to reduce the instantaneous error between the i_g and $i_g^\star$. The output of such a designed controller is equal to $d(t)$, which is sent to the modulator stage, i.e., PS-or LS-PWMs. As previously discussed, the proposed topology can be driven based on either the PS-or LS-PWM principles. Due to better output harmonic profile of the PS-PWM, which can reflect two times of effective switching frequency in the output, this type of modulator is used in the article. Details of this PS-PWM technique are tabulated in Table 4.2, while the resultant gate switching pulses of the proposed DB-ANPC-5L inverter is illustrated in Fig. 4.5. Since an absolute function of the ac reference is used in

the modulation, the terms of P and N in Table 4.2 devote the positive and negative half cycle of this controlled ac reference, respectively. Herein, A_a, and A_b are two 180 degrees PS carriers. The required dc duty cycle of the SB-cell switches is generated by comparing the dc reference of D and the high frequency carrier A_b. As it can be seen from Fig. 4.5, switches S_3, and S_4 require a dc duty cycle during the zero and the first positive/negative output voltage levels, which is in complementary fashion in respect to S_1, and S_2. Also, they need both this dc and ac duty cycles during the top positive/negative output voltage levels. It can also be deduced from Table 4.2 that at each level of the output voltage, only half number of the involved switches are ON. This confirms an acceptable overall conduction losses of the proposed DB-ANPC-5L inverter.

Regarding the switching conversion of the proposed inverter in different output voltage levels shown in Fig. 4.2, the maximum fundamental component term of the proposed inverter output voltage is obtained as follows:

$$v_{inv,\phi} = \frac{DV_{dc}}{1-D} \tag{4.3}$$

The above-mentioned relationship comes from the fact that, during the top positive/negative output voltage levels generation [see Fig. 4.2(g) and (h)], both the SB cell switches must be always ON. This constraint can only be possible whenever the maximum value of the ac reference $d(t)$ is to be less than D. Therefore, regarding (4.3), the practical constraint of D to generate all the 5L inverter output voltage while injecting power to the grid is expressed by:

$$D \geq \frac{V_m}{V_{dc}+V_m}. \tag{4.4}$$

4.1.2 Passive Elements Design

The input current of the proposed DB-ANPC-5L inverter in the single-phase design possesses a double-line frequency, 2ω. The role of dc-link capacitors C_a and C_b is to store the ripple component of the input dc source. Hence, the required capacitance for them is expressed as [112]:

$$C_a = C_b = \frac{V_m I_m}{\omega V_{dc} \Delta V_{dc}}. \tag{4.5}$$

where, ω and ΔV_{dc} are the angular term at the grid fundamental frequency and the voltage ripple across the capacitors. Also, I_m devotes the peak value of the injected grid current.

On the other hand, the required value of L_1 and L_2 in the integrated SB-cell directly

depends on the current passing through them, i_{L_1}, and i_{L_2} and their associated permissible ripple at different values of the dc duty cycle. Concerning a balanced neutral point for the dc-link capacitors, the low frequency component in i_{L_1}, and i_{L_2} can be relatively related to the double-line frequency ripple component of the steady state ripple voltages across C_1 and C_2. Therefore, taking (4.2) into account, the following expressions for the low-frequency ripple of V_{C_1} (V_{C_2}) and $i_{L_1}(i_{L_2})$ at a steady-state condition can be obtained [107]:

$$\Delta V_{LF,C_1} = \frac{I_m}{3\pi^2 \omega C_1} \tag{4.6}$$

$$\Delta i_{LF,L_1} = \frac{I_m(1-D)}{12\pi^3 \omega^2 C_1 L_1} \tag{4.7}$$

On the other hand, the high frequency ripple component of the V_{C_1} (V_{C_2}) and i_{L_1} (i_{L_2}) at the steady-state condition can also be developed as follows, respectively [113]:

$$\Delta V_{HF,C_1} = \frac{D(1-D)i_{L_1}}{2C_1 f_{sw}} \tag{4.8}$$

$$\Delta i_{HF,L_1} = \frac{0.5DV_{dc}}{L_1 f_{sw}} \tag{4.9}$$

where, f_{sw} represents the switching frequency of the proposed converter. Hence, regarding (4.6)-(4.9), and considering the fact that the summation of low and high frequency contents of the inductors currents and the boosted capacitor voltages have to be less than the twofold of their average value, the minimum required value of L_1=L_2 and C_1=C_2 are then taken as follows:

$$C_{1,min} = \frac{D(1-D)i_{L_1}}{2\Delta V_{HF,C_1} f_{sw}} + \frac{I_m}{3\pi^2 \omega \Delta V_{LF,C_1}} \tag{4.10}$$

$$L_{1,min} = \frac{1}{2i_{L_1}} \left(\frac{DV_{dc}}{f_{sw}} + \frac{I_m(1-D)}{12\pi^3 \omega^2 C_1} \right) \tag{4.11}$$

4.1.3 Comparative Study

To further compare the main circuit features of the proposed DB-ANPC-5L inveter over the state-of-the-art 5L-SB-based inverters with voltage boosting feature, a comparative study is conducted in this section. The comparative items are the number of required components, i.e., switches (S), diodes (D), capacitors (C), and the inductors (L), the type of output voltage gain, the MVS across the switches and the TSV index in perunit scale, the

Table 4.3: A comparison between the proposed DB-ANPC-5L inverter and the other single-source 5L-SB-based inverters.

Type of Converter	No. of Components				Type of Voltage Gain	MVS (pu) /TSV (pu)	Nature of Input Current	Bidirectional/ Caps Self Balancing	Leakage Current /PS-PWM?	Reported Efficiency
	S	D	C	L						
ANPC-Based [110]	12	0	4	2	Static	1.5/11	Continuous	Yes/Yes	Low/No	97.5%@160W
CG-Based [96]	7	2	2	1	Static	1/6	Semi-Continuous	No/Yes	Zero/No	97.5%@700W
CG-Based [108]	10	0	2	1	Static	0.5/5	Discontinuous	Yes/Yes	Zero/No	97.13%@600W
Cascaded-Based [114]	10	0	2	2	Dynamic	0.5/5	Continuous	Yes/Yes	High/Yes	97.3%@1kW
Split-Source-Based [115]	7	0	2	1	Dynamic	1/6	Continuous	Yes/Yes	High/No	95%@180W
CG-Based [53]	14	0	2	1	Dynamic	1/6	Semi-Continuous	Yes/No	Zero/No	NA
CG-Based [105]	10	0	2	1	Dynamic	1/6	Semi-Continuous	Yes/Yes	Zero/No	98%@1kW
CG-Based [106]	9	0	2	1	Dynamic	1/6.5	Continuous	Yes/Yes	Zero/No	NA
CG-Based [116]	7	0	2	1	Dynamic	1/6	Continuous	Yes/No	Zero/No	94.9%@1kW
Proposed DB-ANPC	10	0	4	2	Dynamic	1/5	Continuous	Yes/Yes	Low/Yes	97.5%@880W

nature of input current waveform, bidirectional and self voltage balancing of the capacitors, leakage current value, possibility of applying PS-PWM for the modulation, and the reported maximum efficiency at the rated power. In this case, the leakage current profile of topologies is considered “Low” if a mid-point-clamped technique is to be employed, while it referes to be “Zero” as long as the circuit configuration is to be CG-based. In other cases rather than the above-mentioned circuit design, the leakage current is expected to be “High”.

As can be noted from Table 4.3, the type of output voltage gain of the selected topologies are either static (fixed), or dynamic (flexible). As earlier discussed, in case of having a static voltage conversion gain, the peak of the inverter output voltage cannot be controlled over a wide variation of the input dc voltage unless adopting another front-end dc-dc boost/buck-boost converter, which results in lower overall efficiency. This can affect the input current nature, as well, i.e., being continuous, discontinuous, or semi-continuous depending on the type of the input boost circuit. Among the topologies with a dynamic voltage conversion gain, only the proposed structure is based on the mid-point-clamped technique with a reduced leakage current propagation issue. Although the proposed topology requires 10 active power switches, its TSV index in perunit scale is only five. Additionally, similar to the most of the reported topologies in Table 4.3, the involved capacitors of the proposed DB-ANPC-5L inverter are self-balanced but as opposed to them, they are balanced at the lower rated voltage. This can significantly reduce their losses as well as their dimension area for the fabrication purpose. Having the ability of applying PS-PWM technique is also a notable merit for the proposed topology since it can increase the output frequency of the inverter leading to higher injected power quality with a reduced value of the interfaced filter. Excluding the cascaded-boost 5L-inverter in [114] and the proposed DB-ANPC-5L inverter, rest of the mentioned topologies need to be modulated under the LS-PWM condition only. Herein, although the CGSB-based

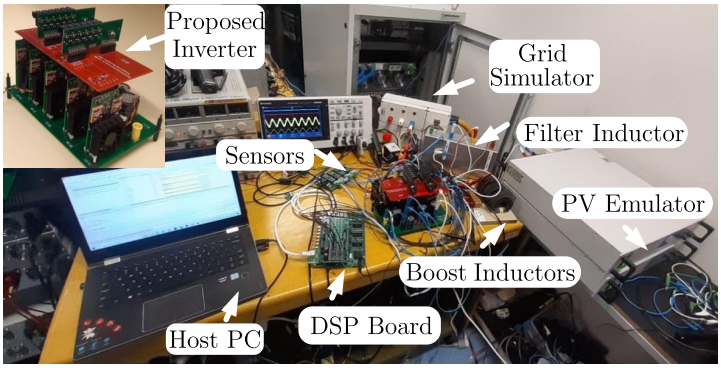
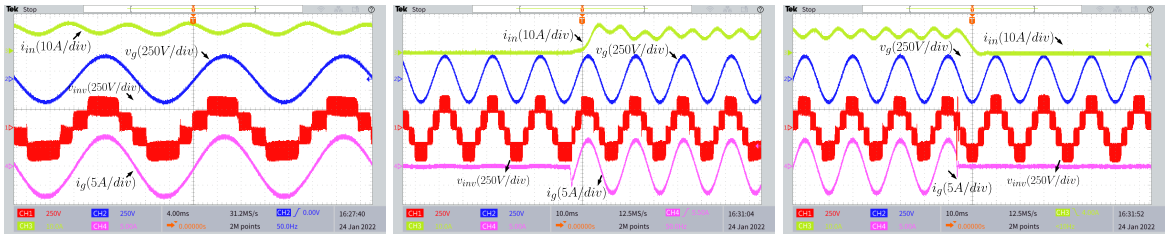
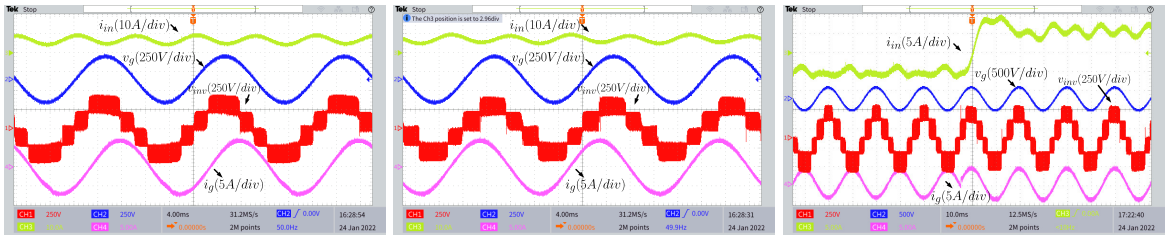


Figure 4.6: Proposed DB-ANPC-5L inverter prototype with the measurement setup [111].



(a) **(b)** **(c)**

Figure 4.7: Experimental results showing from up to bottom: the input current, the grid voltage, the inverter output voltage, and the injected grid current, (a) at 1.3 kW injected power, (b) under a dynamic test from zero to 1 kW power injection, (c) under a dynamic test from 1 kW to zero power injection [111].



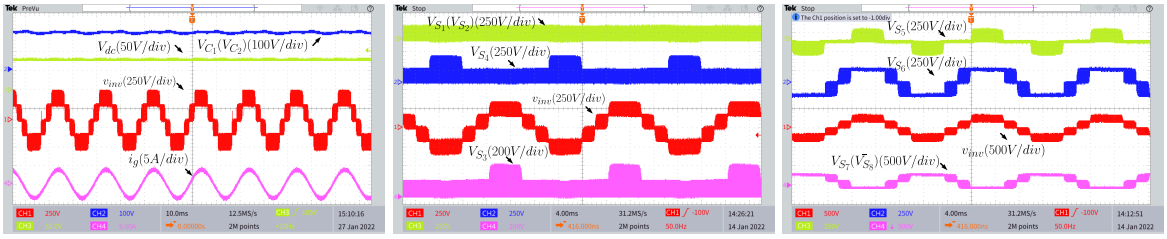
(a) **(b)** **(c)**

Figure 4.8: Experimental results showing (a) lagging power factor ($P^\star$= 800 W, $Q^\star$= -800 VAR) (b) leading power factor ($P^\star$= 800 W, $Q^\star$= 800 VAR) (c) bidirectional operation ($P^\star$= -500 W to $P^\star$= +500 W) [111].

topologies can cancel out the effect of leakage current concern, they suffer from dc offset issue in the output voltage profile of the inverter. This is mainly due to their asymmetry operation in the positive and negative half cycle of the output voltage, while this issue is not the case for the proposed topology with a symmetric operation in both half cycle.

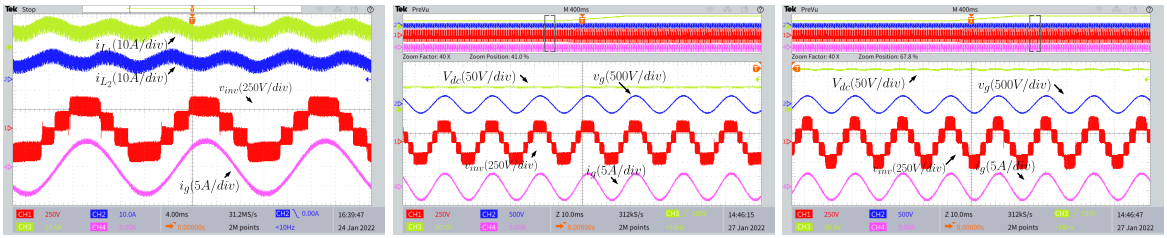
4.1.4 Experimental Results

To confirm the feasibility and correct operation of the proposed DB-ANPC-5L inverter under the transfomerless grid-connected condition, several experimental results are



(a) **(b)** **(c)**

Figure 4.9: Experimental results showing a) the input dc voltage, the capacitors boosted voltages, the inverter output voltage, and the injected grid current, (b) the voltage stress across switches S_1, S_2, S_3, and S_4 in presence of the inverter output voltage, (c) the voltage stress across switches S_5, S_6, S_7, and S_8 in presence of the inverter output voltage [111].



(a) **(b)** **(c)**

Figure 4.10: Experimental results showing a) the inductors currents with inverter output voltage and injected grid current at 1 kW injected power, (b) the steady-state waveforms before applying a ramp change in the input dc voltage from 80 V to 140 V, (c) the steady-state waveforms after applying a ramp change in the input dc voltage from 80 V to 140 V [111].

presented in this section. The laboratory-built prototype with the measurement setup is depicted in Fig. 4.6, while the main parameters used in the experimental tests are the same as summarized in Table 3.2. The passive elements are chosen based on the design guidelines principles, while an Elektro-Automatik PV emulator (model EA-PSI-9750-12) is used as an adjustable dc laboratory power supply to electrically feed the proposed inverter. An 50-Hz electrical utility grid is emulated in Regatron TC30.528.43 ACS to interface and test the proposed converter with the grid. Here, the grid peak voltage is adjusted to be 320 V throughout the experiments. To connect the proposed inverter to the grid, an L-type filter with values of $L_g = 3.8$ mH and $r_g = 0.33$ is utilized. As for the closed-loop control implementation, a PR controller synchronized with a GVO technique is used to govern the converter. Details of digital implementation for such a PR controller and GVO mechanism can be found in [75]. The modulator used in the experiment is based on the described PS-PWM technique, which has been implemented in a DSP to provide the required gate switching pulses of the proposed DB-ANPC-5L inverter.

Regarding the above-mentioned circuit specifications, and taking the flexible voltage boosting property of the proposed inverter into account, a fixed input dc voltage of 100 V is initially considered. Hence, to meet the grid voltage peak amplitude requirement, the

dc duty cycle, D, is set at 75% as per (4.3). Fig. 4.7(a) shows the input current, i_{in}, the grid voltage, v_g, the 5L inverter output voltage, v_{inv} and the injected grid current, i_g, while the peak of the reference current is set at 8 A, which results in 1.3 kW injected power to the grid. As can be seen from this result, the input current is continuous with 100-Hz double-line frequency without inducing any large pulsating inrush spikes, while all the 5L output voltage waveform of the inverter with the peak voltage of 400 V and a quality injected grid current have been accordingly generated. To show the appropriate performance of the controller from the dynamic response view point, the reference active power is changed from zero to 1 kW and vice versa. The respective experimental results of these dynamic tests have been illustrated in Fig. Fig. 4.7(b), and (c), respectively.

Conversely, the reactive power support capability of the proposed DB-ANPC-5L inverter has been verified through Fig. 4.8(a) and (b), whilst the value of $P^\star$ is set at 800 W and the amount of $Q^\star$ is selected at -800 VAR and +800 VAR for the lagging and leading power factor condition, respectively. In both these cases, the proposed inverter has been fed through 100 V input dc voltage, and it shows a correct grid-connected performance under the reactive power support mode. Alternatively, Fig. 4.8(c) confirms the bidirectional power flow operation of the proposed DB-ANPC-5L inverter, while a resistive load is parallelized with the PV emulator to absorb the reverse power imposed from the grid to the dc side. In this case, the value of $P^\star$ is dynamically changed from -500 W to + 500 W, while there is no distortion in the 5L inverter output voltage.

In following, some detailed specifications of the proposed DB-ANPC-5L inverter under the grid-connected condition are shown. To do this, the input dc voltage is set at 80 V, while the peak of the inverter output voltage is 400 V. As can be seen from Fig. 4.9(a), the boosted voltages across the capacitors, i.e., V_{C1} or V_{C2}, are balanced at 200 V, while the peak of the injected grid current is 4 A. The voltage stress across all the power switches in presence of the 5L inverter output voltage have also been illustrated in Fig. 4.9(b) and (c), while their peak can confirm the described relations of Table I. The smooth and spike-free performance of the currents passing through the boost inductors at 1 kW injected power can also be observed in Fig. 4.9(a), while their HF ripple can be controlled through larger values of the either inductors or operating switching frequency.

To further attest the flexible/dynamic voltage boosting capability of the proposed DB-ANPC-5L inverter, the value of the input dc voltage is changed within a ramp trend from 80 V to 140 V. Considering the peak fundamental component of the inverter output voltage as 320 V, to inject a constant power to the grid, the value of D should be dynamically changed from 83% to 75%. The correct performance of the proposed inverter

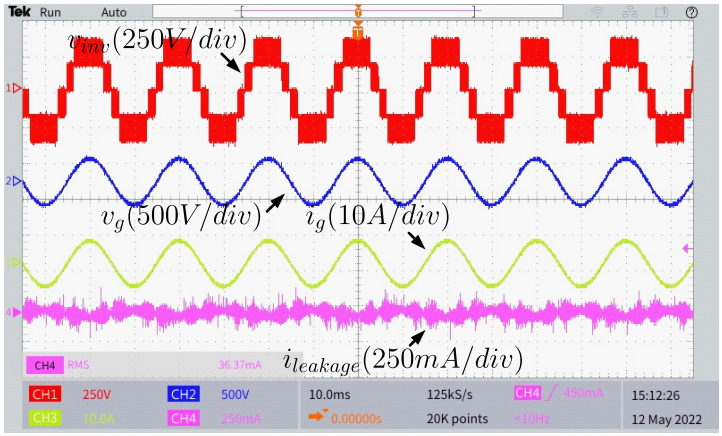


Figure 4.11: Experimental results of the proposed DB-ANPC-5L inverter emphasizing on the leakage current at P_g = 1.5kW [111].

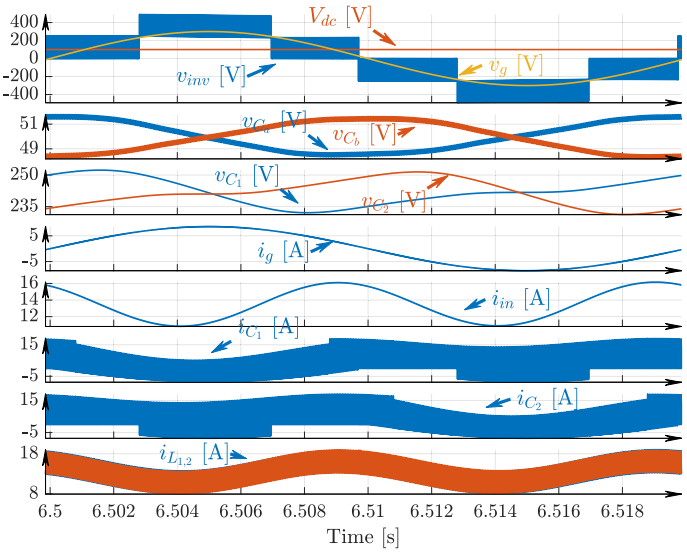


Figure 4.12: Detailed simulation results at 1.5 kW steady state injected power emphasizing on the stress on capacitors and inductors [111].

highlighted at V_{dc} = 80 V (before applying the ramp dynamic test), and V_{dc} = 140 V (after applying the ramp dynamic test) can be confirmed through Fig. 4.10(b), and (c), respectively, whilst a constant 800 W power with a quality current is injected to the grid. Alternatively, similar to the other mid-point-clamped MLIs, the proposed DB-ANPC-5L converter is also able to mitigate the leakage current propagation issue as demonstrated by the experiment in Fig. 4.11. Here, the root mean square (RMS) value of the leakage current is less than 30 mA at the rated 1.5 kW injected power.

The voltage/current stresses over the chosen passive elements have also been shown in Fig. 4.12. Here, the input dc voltage is set at 100 V, while the peak value of the 5L

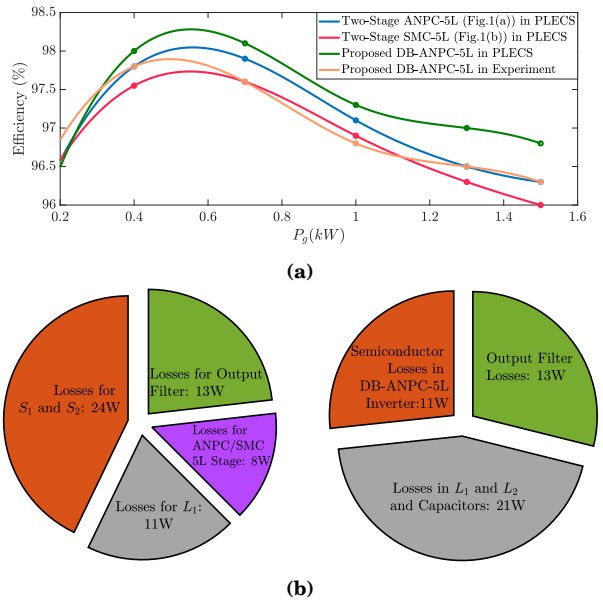


Figure 4.13: (a) A comparative efficiency results of two-stage ANPC, two-stage SMC, and the proposed DB-ANPC-5L converters at $V_{dc} = 150V$, (b) losses distribution comparison between the two-stage ANPC converters and the proposed DB-ANPC-5L inverter at $P_g = 1.5$kW, and $V_{dc} = 150V$ [111].

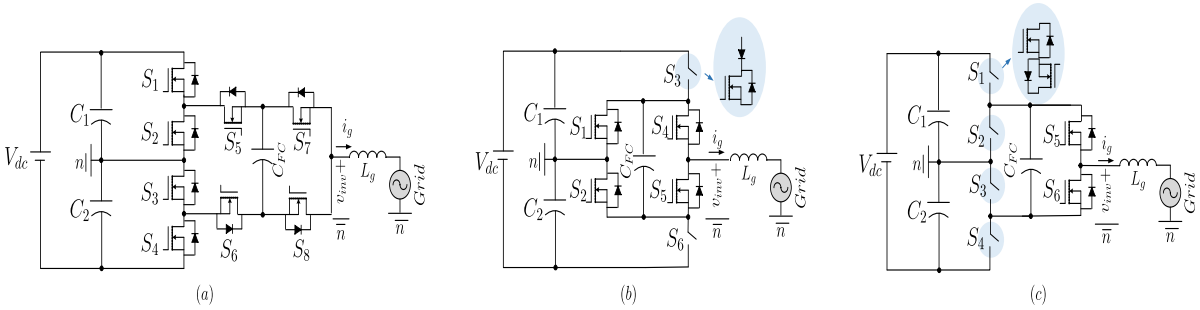


Figure 4.14: ANPC-based 5L inverter structures, (a) conventional topology with half dc-link voltage utilization [117], (b) ABNPC-5L inverter proposed in [25] with full dc-link voltage utilization, (c) the proposed DM-ANPC-5L-Type-I converter [118].

inverter output voltage is considered 500 V to inject 1.5 kW power to the grid. The results are taken by the aim of PLECS software with respect to the exact model of the semiconductor devices mentioned in Table 3.2. The chosen value for the dc-link capacitors, C_a, and C_b, is 75 uF based on (4.5), while the amount of other involved passive elements is the same as given in Table 3.2. As can be seen, the balanced voltage across the dc-link capacitors is 50 V without requiring any active voltage control. As expected, each of the boost capacitors, C_1, and C_2 is balanced at 250 V, i.e., half value of the inverter peak voltage with a less than 5% ripple content. The continuous input current waveform with 100 Hz double-line frequency, and the smooth current stress profile of the boost capacitors and inductors with permissible HF components have also

been shown in Fig. 4.12

Finally, the comparative results of the overall efficiency and the loss distribution of the proposed DB-ANPC-5L inverter over its previously discussed two-stage counterparts, i.e., front-end dc-dc boost converter plus ANPC/SMC-5L converters have been shown in Fig. 4.13(a) and (b), respectively. Here, the input dc voltage for all the cases is set at 150 V to inject the power varying from 400 W to 1.5 kW to the grid. The semiconductor devices for the proposed topology and the inverter stage of the conventional system are chosen the same, i.e., UJ4C075018K4S with 20 kHz switching frequency. Conversely, since both the ANPC and SMC-5L converters suffer from half dc-link voltage utilization, the switches S_1 and S_2 of the front-end dc-dc boost converter in the conventional two-stage system must tolerate the largest MVS equals to 800 V. Hence, the type of SiC switches for them is selected as UF3C120040K4S from the same company but with at least 1200 V breaking voltage. A PR controller is used to govern the converters, whereas the modulation strategy for all the cases is based on the described PS-PWM technique since it can facilitate the utilization of the same output filter design for all the cases. Due to the active voltage balancing requirement of the capacitors in the conventional ANPC and SMC-5L converters, two dc-link capacitors with 470 uF capacitance are chosen for them, while the value of the boost inductor with an ESR of 0.1 for all the cases is the same as given in Table 3.2. Regarding the lack of charge balancing requirement for the dc-link capacitors of the proposed topology, two 75 uF film capacitors are considered as C_a and C_b. The loss analysis of the conventional two-stage ANPC and SMC-5L converters are performed using the PLECS software, while both the PLECS and measured results from the power analyzer are considered as for the proposed topology. As can be seen from Fig. 4.13(a), the proposed topology offers the higher efficiency in comparison to its two-stage counterpart over a wide range of the injected grid power. From the loss distribution results at the rated power shown in Fig. 4.13(b), it can also be confirmed that the major power losses of the conventional system belongs the front-end dc-dc converter stage, i.e., switching and conduction losses in S_1/S_2 and the ESR losses of the input boost inductors.

4.2 A Family of DM-ANPC-5L-TL Inverters

The DM-based circuit configuration for MLIs has recently emerged, where novel circuit architecture and PWM technique can produce 3L [119] or 5L [74, 120] output voltage within two independent operating modes, i.e., buck and boost. Therefore, when the input

dc voltage is sufficient to meet the peak amplitude of the grid voltage, the circuit can be operated in buck mode whilst generating the maximum number of output voltage levels with half dc-link voltage utilization. Alternatively, whenever the input dc voltage is low, i.e., at 50% of the previous case, the DM converter can produce the same number of output voltage levels but in the boost mode of operation with full dc-link voltage utilization.

Currently, there are a few number of topologies presented so far with such an DM-integrated concept. The DM-based VSIs with 3L, and 5L output voltage proposed in [119], [74, 120], are all SC-based in both operating modes. Even though their structures are based on a CG-based circuit design leading to almost zero leakage current for sensitive RE-based applications, their input current profile is discontinuous with a large inrush spikes. Thus, due to the current stress on devices and ripple voltage concern across the capacitors, large electrolyte capacitors are needed, while their applicability for a higher range of output power needs a careful attention [28]. Moreover, due to the SC technique constraint in these structures, only applying the LS-PWM technique is possible in both operating modes. Hence, it makes the apparent frequency of the ac output and the effective switching frequency of the switches equal leading to excessive switching loss and large output filters requirement.

The aim of this subsection is to apply the above-mentioned DM concept to the ANPC-5L converters. Three different DM-ANPC-5L converters are introduced to configure this family of MLIs, in which 10 power switches are used for each of them and due to absence of diode, bidirectional operation, i.e., V2G and G2V, is possible for all. Herein, in the buck mode of operation, the voltage conversion gain of all the proposed DM-ANPC-5L converters is 0.5, while as for the boost operating mode, a unity gain is achieved. As opposed to the other DM-based converters, FC technique is used for the Type-I and Type-II of the proposed DM-ANPC-5L converters during the buck operating mode, while similar to the conventional ABNPC-VSIs, an SC-integrated technique is used for them during the boost operating mode. The Type-III of the proposed topology uses the SC technique in both operating modes, but with reduced stress on FCs.

4.2.1 Proposed DM-ANPC-5L-Type-I Converter

The Type-I of the proposed DM-ANPC-5L converter is illustrated in Fig. 4.14(c), where the converter is connected to the grid via a simple L-type filter L_g. An abstract version of the concept was introduced in [118]; however, its extensive analysis are given in this article. As can be realized from Fig. 4.14(c), the proposed topology needs two more

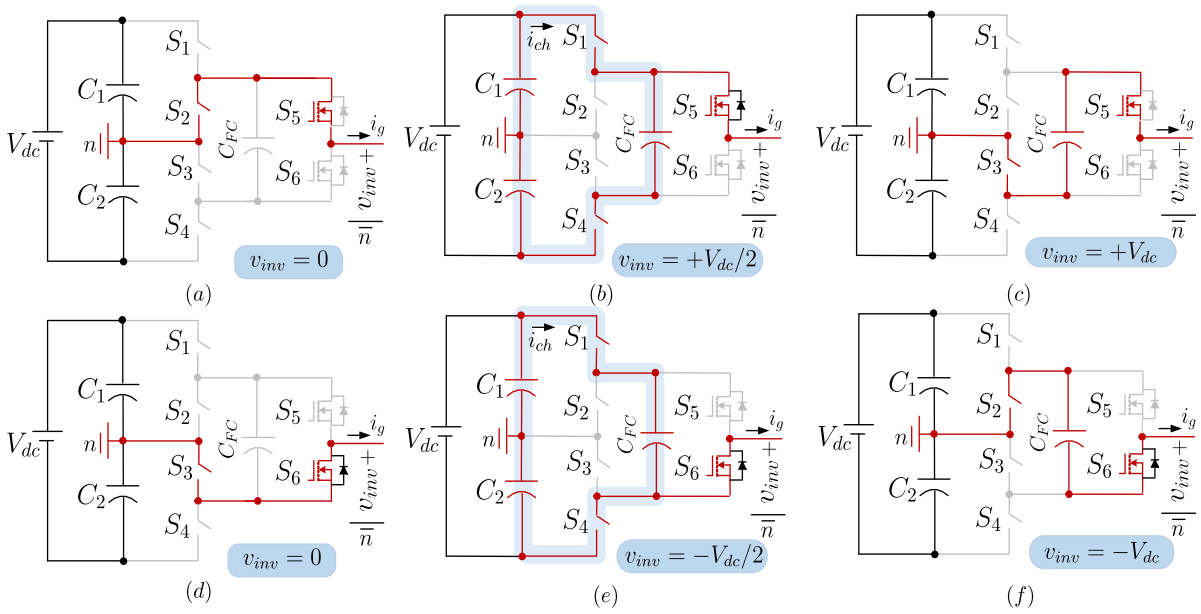


Figure 4.15: Different current flowing paths of the proposed DM-ANPC-5L-Type-I inverter during boost operating mode at (a) $v_{inv} = 0$ in the positive half cycle, (b) $v_{inv} = +V_{dc}/2$, (c) $v_{inv} = +V_{dc}$, (d) $v_{inv} = 0$ in the negative half cycle, (e) $v_{inv} = -V_{dc}/2$, and (f) $v_{inv} = -V_{dc}$.

power switches in comparison to the original ANPC and ABNPC-5L converters shown in Fig. 4.14(a), and (b) to realize all the 5L distinctive output voltage within two independent operating modes. The type of switches S_1-S_4 is four-quadrant, while switches S_5, and S_6 are normal power MOSFET. Hence, six single-channel or three dual-channel gate drivers available in the market e.g., UCC21520DW from Texas Instrument or NCP51560 from Onsemi companies, can be utilized to provide the required gate switching pulses to a certain range of switching frequency.

The related current flowing paths of the proposed DM-ANPC-5L-Type-I converter in boost and buck operating modes are illustrated in Fig. 4.15 and Fig. 4.16, respectively. As can be seen from Fig. 4.15(a)-(f), six switching states are available to realize 5L output voltage in the boost mode of operation. Considering, V_{dc} as the available input dc voltage, the inverter output voltage levels are 0, $\pm V_{dc}/2$, and $\pm V_{dc}$. Similar to ABNPC-5L converters described earlier, a full dc-link voltage utilization is achieved in this mode of operation, while an SC technique during the middle positive/negative output voltage levels as per Fig. 4.15(b) and (e) is needed to balance the voltage across FC, C_{FC} at V_{dc}. Excluding these middle positive/negative switching states, the topology needs only two ON-state switches per remaining output voltage levels at each switching state. It is worth highlighting that except the switches S_1, and S_4 that are in charging flow path of C_{FC}, the current stress profile of all the remaining switches is a function of the injected

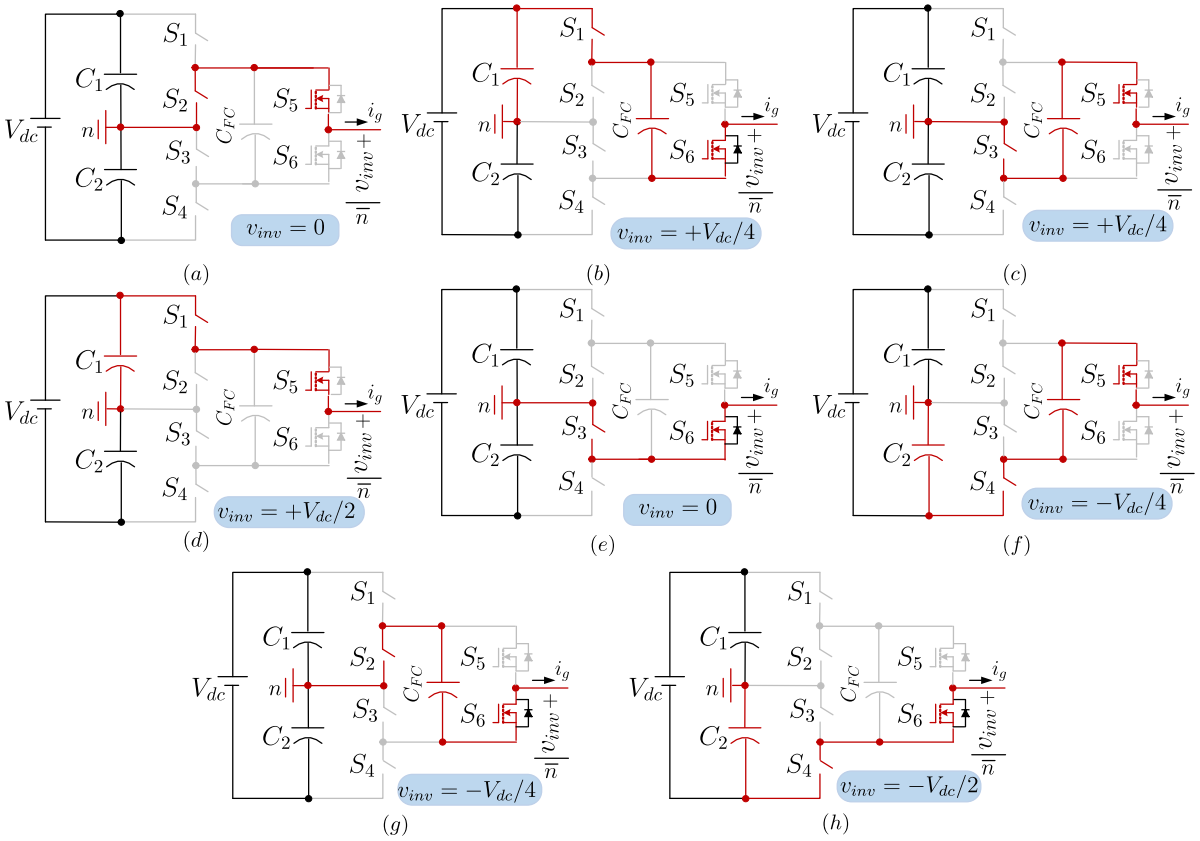


Figure 4.16: Different current flowing paths of the proposed DM-ANPC-5L-Type-I inverter during buck operating mode at (a) $v_{inv} = 0$ in the positive half cycle, (b) $v_{inv} = +V_{dc}/4$ with the first RSS, (c) $v_{inv} = +V_{dc}/4$ with the second RSS, (d) $v_{inv} = +V_{dc}/2$, (e) $v_{inv} = 0$ in the negative half cycle, (f) $v_{inv} = -V_{dc}/4$ with the first RSS, (g) $v_{inv} = -V_{dc}/4$ with the second RSS, (h) $v_{inv} = -V_{dc}/2$.

grid current waveform, i_g, whereas, due to SC technique, the maximum current stress on S_1, and S_4 is related to the FC charging current, i_{ch}.

When it comes to the buck mode of operation, the proposed DM-ANPC-5L converter can operate as a normal ANPC-5L converter with half dc-link voltage utilization. Eight different switching states are considered for this operating mode to synthesize 5L output voltage as 0, $\pm V_{dc}/4$, and $\pm V_{dc}/2$ as illustrated in Fig. 4.16(a)-(h). As can be seen, similar to the original ANPC-5L converters [117], two RSSs are provided as for generating the $\pm V_{dc}/4$ output voltage levels, where they can ease the FC voltage balancing during the operation in one fundamental cycle. The RSSs as for the zero-level of the output voltage are used in positive and negative half cycles. As opposed to the boost mode of operation, the FC voltage is balanced to one-quarter of the dc-link voltage, $V_{dc}/4$ by changing the injected grid current flowing path direction per each RSS. Hence, there is no additional concern pertaining to the current stress profile of the devices. Requiring only two ON-state semiconductors per each output voltage level reduces the conduction

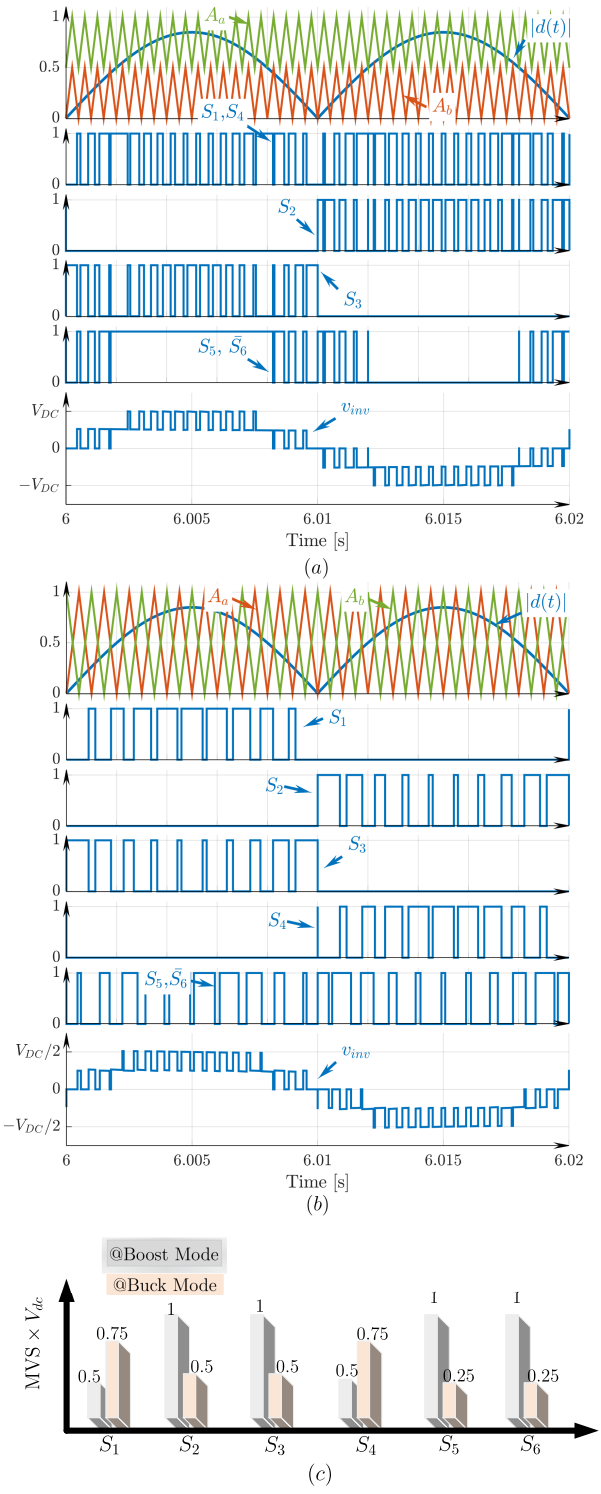
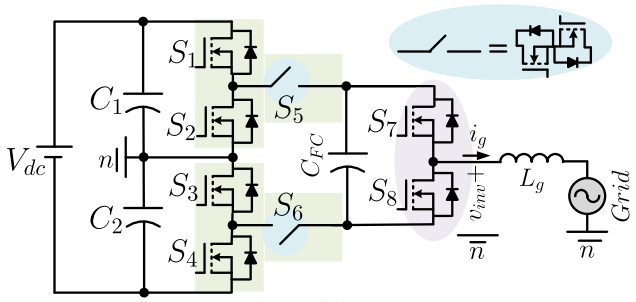


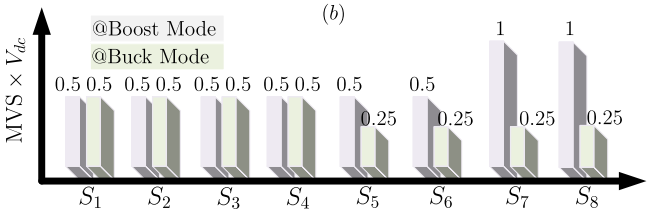
Figure 4.17: Details of the modulation strategy for the proposed DM-ANPC-5L-Type-I converter, (a) with LS-PWM method in the boost mode of operation, (b) with PS-PWM method in the buck mode of operation, (c) the MVS across the switches in both modes.



(a)

Switching States	@Boost Mode ON Switches	C_{FC}	v_{inv}	@Buck Mode ON Switches	C_{FC}	v_{inv}
1	S_2, S_5, S_7 / S_3, S_6, S_8	–	0	S_2, S_5, S_7 / S_3, S_6, S_8	–	0
2	S_1, S_4, S_5, S_6, S_7	▲	$+\frac{V_{DC}}{2}$	S_1, S_5, S_8 / S_3, S_6, S_7	▲ / ▼	$+\frac{V_{DC}}{4}$
3	S_3, S_6, S_7	▼	$+V_{DC}$	S_1, S_5, S_7	–	$V_{DC}/2$
4	S_3, S_4, S_5, S_6, S_8	▲	$-\frac{V_{DC}}{2}$	S_4, S_6, S_7 / S_2, S_5, S_8	▲ / ▼	$-\frac{V_{DC}}{4}$
5	S_2, S_5, S_8	▼	$-V_{DC}$	S_4, S_6, S_8	–	$-V_{DC}/2$

(b)



(c)

Figure 4.18: Proposed DM-ANPC-5L-Type-II converter, (a) the main circuit architecture, (b) the switching and FC status, (c) the MVS across the switches in both modes.

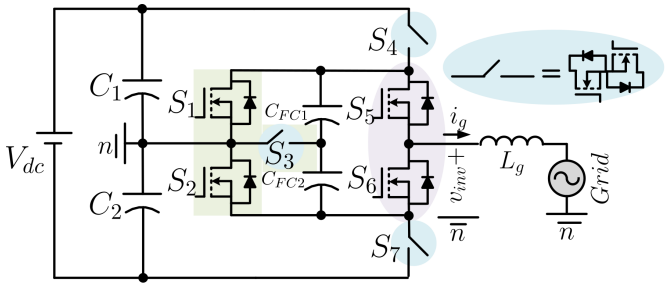
and switching losses in the the proposed DM-ANPC-5L converter for the buck mode of operation. Considering the above discussion, the following relationships can be written to describe the maximum output voltage of the proposed converter and the steady-state voltage across FC in each of the operating modes:

$$V_{inv,max} = \begin{cases} D_m V_{dc} \Rightarrow Boost \\ 0.5 D_m V_{dc}, \Rightarrow Buck \end{cases} \tag{4.12}$$

$$V_{FC} = \begin{cases} V_{dc} \Rightarrow Boost \\ 0.25 V_{dc} \Rightarrow Buck \end{cases} \tag{4.13}$$

where, D_m is the maximum modulation index equals to $\frac{V_m}{V_{dc}}$, in which, V_m is the peak value of the grid voltage.

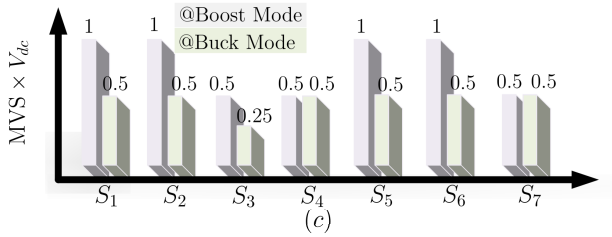
Details of modulation strategy in both modes of operation as well as the MVS across the semiconductors are shown in Fig. 4.17(a)-(c). As can be taken from Fig. 4.17(a) and (b),



(a)

Switching States	@Boost Mode ON Switches	C_{FC1}	C_{FC2}	v_{inv}	@Buck Mode ON Switches	C_{FC1}	C_{FC2}	v_{inv}
1	S_1, S_5 / S_2, S_6	–	–	0	S_1, S_5, S_7 / S_2, S_4, S_6	▲	▲	0
2	S_4, S_5, S_7	▲	▲	$+\frac{V_{DC}}{2}$	S_3, S_5	▼	–	$+\frac{V_{DC}}{4}$
3	S_2, S_5	▼	▼	$+V_{DC}$	S_2, S_4, S_5	▲	▲	$V_{DC}/2$
4	S_4, S_6, S_7	▲	▲	$-\frac{V_{DC}}{2}$	S_3, S_6	–	▼	$-\frac{V_{DC}}{4}$
5	S_1, S_6	▼	▼	$-V_{DC}$	S_1, S_6, S_7	▲	▲	$-V_{DC}/2$

(b)



(c)

Figure 4.19: Proposed DM-ANPC-5L-Type-III converter, (a) the main circuit architecture, (b) the switching and FC status, (c) MVS across the switches in both modes.

the Type-I of the proposed DM-ANPC-5L converter needs a LS-PWM and a phase-shifted PWM (PS-PWM) scheme for its boost and buck mode of operation, respectively. Since there is no RSS for FC voltage balancing in the boost mode, LS-PWM is used, while due to having two RSSs per middle positive/negative output voltage levels, a PS-PWM scheme is workable to balance the FC at its desired voltage. In both the cases, two high frequency carriers, A_a, and A_b are required to configure all the distinctive 5L output voltage. Here, an absolute function of a reference waveform, $|d(t)|$ from the controller is compared with the carriers in both operating modes. Similar to any standard LS-PWM scheme, both the effective and apparent switching frequencies are the same, while in the PS-PWM, the 5L inverter output voltage possesses an apparent switching frequency which is double with respect to the effective switching frequency. One can also be noticed from Fig. 4.17(c) is the larger MVS across switches S_2, S_3, S_5 and S_6 than the two remaining switches in the boost mode, i.e., V_{dc} versus $0.5V_{dc}$. Conversely, only two switches, i.e., S_1 and S_4 need to tolerate $0.75V_{dc}$ as the MVS in the buck mode of operation, while the MVS for

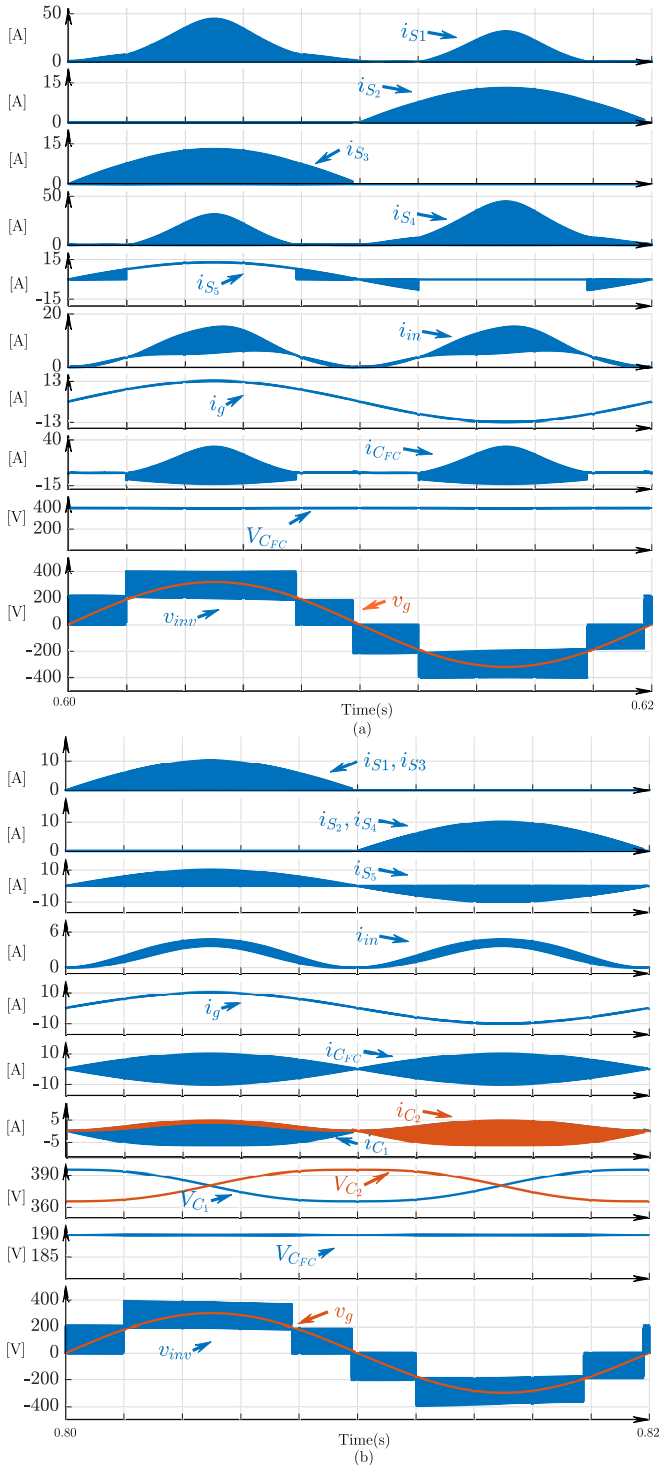


Figure 4.20: Simulation results at 1.5kW steady-state grid-connected condition for the proposed DM-ANPC-5L-Type-I, (a) at the boost operating mode, (b) at the buck operating mode.

all the remaining switches in this mode is $0.5V_{dc}$.

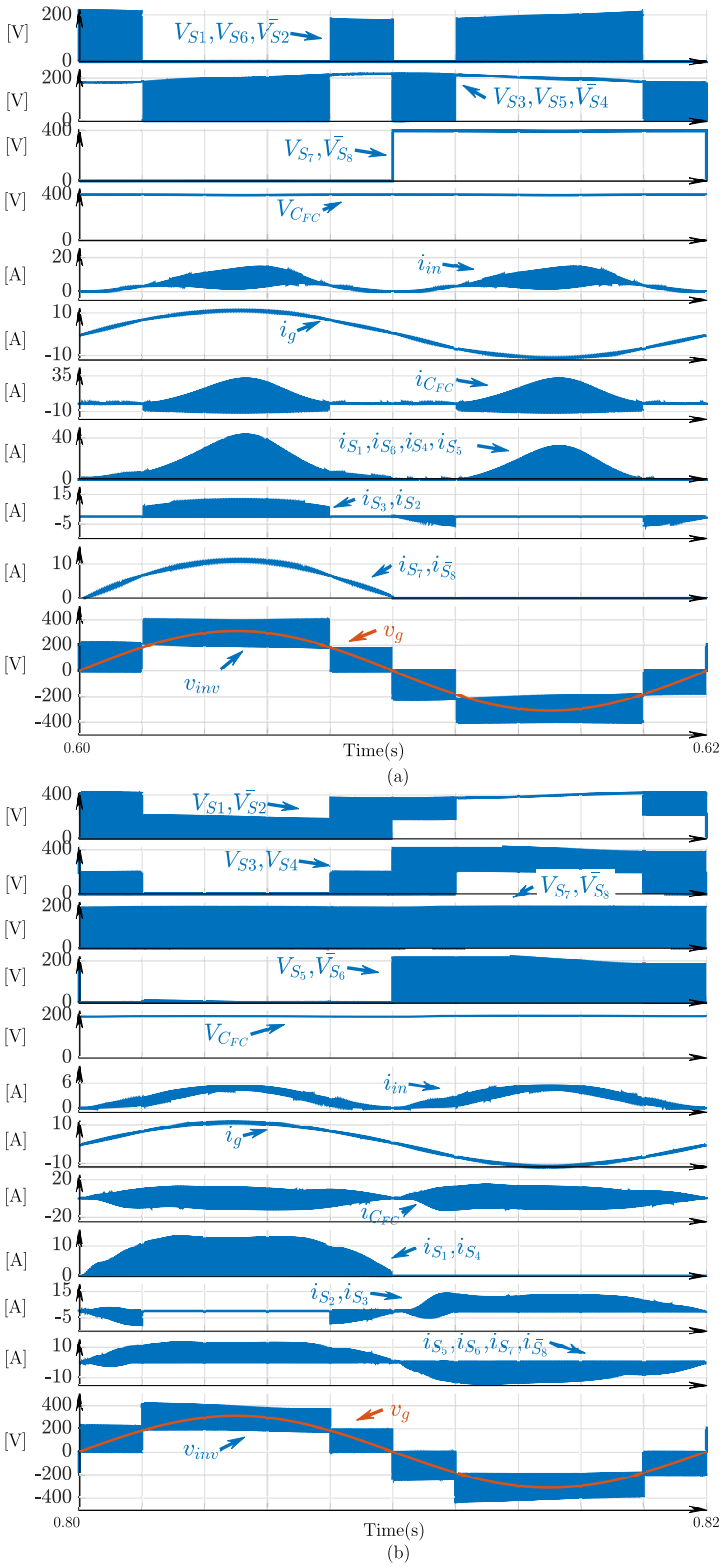


Figure 4.21: Simulation results at 1.5 kW steady-state grid-connected condition for the proposed DM-ANPC-5L-Type-II, (a) at the boost operating mode, (b) at the buck operating mode.

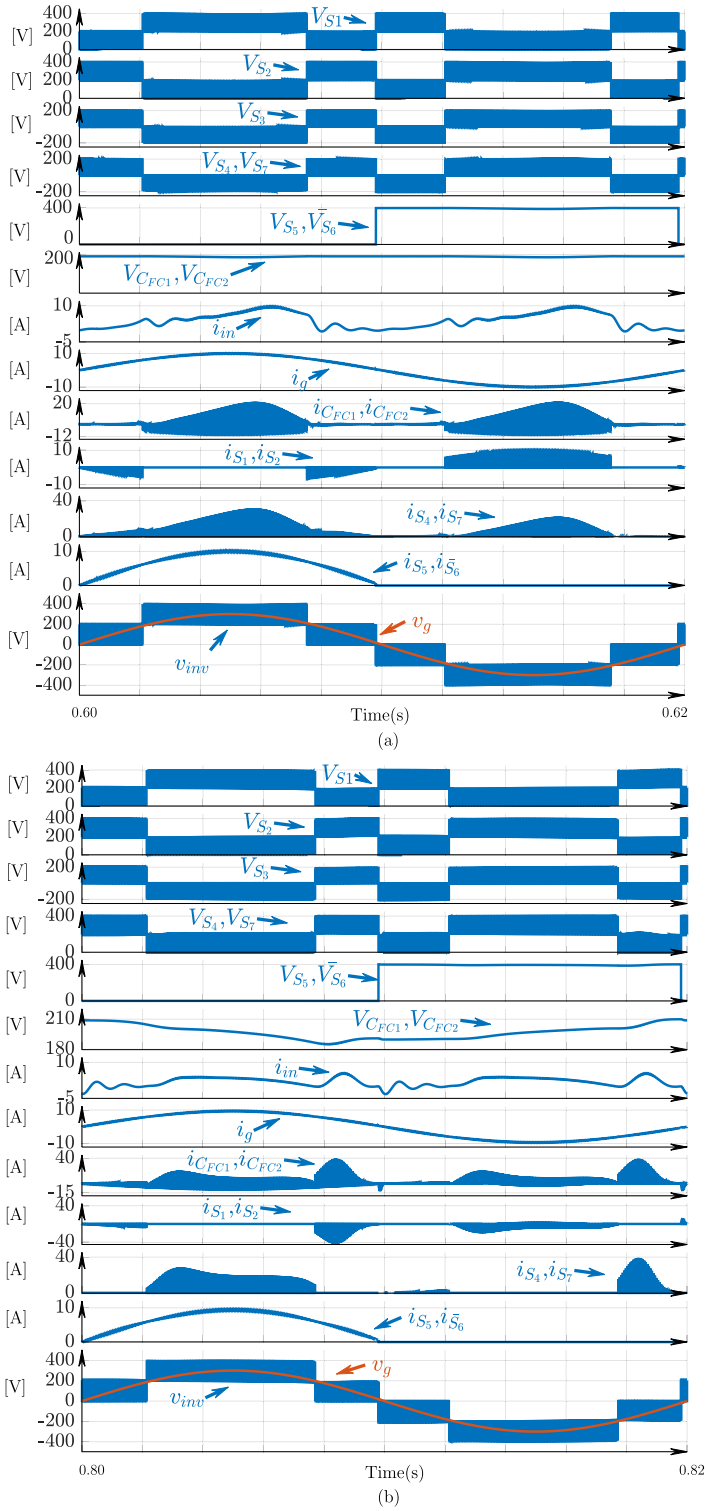


Figure 4.22: Simulation results at 1.5 kW steady-state grid-connected condition for the proposed DM-ANPC-5L-Type-III, (a) at the boost operating mode, (b) at the buck operating mode.

4.2.2 Proposed DM-ANPC-5L-Type-II converter

The second variant of the proposed DM-ANPC-5L grid-connected converter is shown in Fig. 4.18(a), while it has been comprised of two T-types switching arrangements as S_1, S_2, S_5, and S_3, S_4, S_6, and a standard half-bridge leg, i.e., S_7 and S_8. As can be seen, it needs the same number of switching devices as per the Type-I of the proposed DM-ANPC-5L converter and the same principle as for the voltage balancing for the dc-link capacitors, i.e., C_1, C_2, and C_{FC}. Considering a single gate driver as per each of four-quadrant switches, i.e., S_5 and S_6, the structure needs eight single-channel or five dual-channel gate driver circuits.

The switching states and the status of C_{FC} voltage during each of the operating modes are illustrated in Fig. 4.18(b). Similar to the first variant of the proposed DM-ANPC-5L converter, the Type-II of the proposed topology has six switching states in the boost mode of operation, and eight switching states in its buck mode. Hence, an SC technique with a LS-PWM scheme is used in the boost mode of operation, while the voltage across C_{FC} is balanced at the maximum voltage level of the ac output, V_{dc}. Accordingly, as per the buck mode of operation, FC technique with an PS-PWM scheme is used to stabilize the FC voltage at $0.25V_{dc}$, which is half of the maximum inverter voltage level, $0.5V_{dc}$. Hence, the relationships of the maximum value of the converter output voltage and the voltage across C_{FC} are still valid as per (1) and (2). Regarding this, the MVS across the switches during the operation in each mode is summarized in Fig. 4.18(c). As can be seen, switches S_7 and S_8, which are being switched in the positive and negative half cycle of the output voltage in the boost operating mode, respectively, possess the largest MVS equal to V_{dc}, while the MVS for the rest of switches, which are being switched with high switching frequency is 0.5. Similarly, as per the buck mode of operation, four switches, i.e., S_1, S_2, S_3, and S_4 must tolerate an MVS equal to $0.5V_{dc}$, whereas the MVS of the remaining switches is only one-quarter of the input voltage, $0.25V_{dc}$. It is worth highlighting that since the operating principle of this type of the proposed DM-ANPC-5L converter in the boost mode is SC-based, switches S_1, S_5, S_6, and S_4, that are involved in the charging path of C_{FC}, must tolerate the highest current stress equal to the charging current of C_{FC}, while in the buck mode of operation, a function of the injected grid current waveform is passed through all the involved switches due to the integrated FC technique.

4.2.3 Proposed DM-ANPC-5L-Type-III converter

Fig. 4.19(a) shows the details of the third variant of the proposed DM-ANPC-5L converter. As can be realized, the structure is configured using one standard T-type switching configuration with switches S_1, S_2, and S_3, two discrete four-quadrant switches, S_4, and S_7, and one standard half-bridge leg, i.e., S_5, and S_6. Hence, this topology also needs 10 power switches, and seven single-channel or five dual-channel gate driver circuits. As opposed to other previously-discussed converters, this variant of the circuit needs two FCs, i.e., C_{FC1}, and C_{FC2}.

Fig. 4.19(b) shows the details of switching states and FCs voltage status during the boost and buck mode of operation. Similar to other developed DM-ANPC-5L converters, the voltage conversion gain of this variant of the proposed topology is unity in the boost mode of operation, while it is half in the buck mode. Considering Fig. 4.19(b), the FCs voltages are balanced at $0.5V_{dc}$ in the boost operating mode, while this value in the buck mode is $0.25V_{dc}$. As opposed to two initial types of the proposed DM-ANPC-5L converters, the FCs voltage balancing is possible using only SC technique in both operating modes. Hence, only LS-PWM in both modes of operation is applicable for the modulation process purpose. Here, although the voltages across FCs is reduced in the boost operating mode compared to others, the concern of excessive current stress for the switches involved in the charging path of the FCs still remains in place since SC technique is being used for FC voltage balancing operation. The MVS value across the devices in each mode of operation has also been indicated in Fig. 4.19(c). As can be seen, four switches, S_1, S_2, S_5, and S_6 must tolerate the highest MVS, V_{dc}, in the boost mode, while excluding switch S_3 with an MVS equals to $0.25V_{dc}$, all the remaining switches in the buck mode of operation must tolerate $0.5V_{dc}$ as the MVS.

4.2.4 Design Guidelines

The dc-link capacitors, C_1, and C_2 can be designed based on (4.5); however, the capacitor, C_{FC} named as FC need to be carefully designed as for the proposed DM-ANPC-5L converters to provide sufficient power quality for the system. Since, the working principles of the Type-I and Type-II of the proposed converters in both modes is similar, the design guidance is considered for them in this section.

Herein, the design of C_{FC} is slightly different for each mode. This is because of the applied switching technique of the converter, which is based on SC and FC technique, in

the boost and buck mode of operation, respectively. Hence, to drive the needed equations for C_{FC}, the following sinusoidal functions as for the reference control signal, and the injected grid current are considered, respectively:

$$d(t) = D_m \sin \omega t \tag{4.14}$$

$$i_g = I_m \sin \omega t. \tag{4.15}$$

Hence, taking the boost mode of operation with an LS-PWM technique into account for any of Type-I or II of the proposed DM-ANPC-5L converters, it can be realized that the C_{FC} is discharged when maximum value of the inverter output voltage is generated. Therefore, the charge/discharging time interval of C_{FC} over every switching frequency, f_{sw} can be written as:

$$\Delta t_{ch} = \frac{2d(t)-1}{f_{sw}}. \Rightarrow d(t) \geq 0.5 \tag{4.16}$$

Hence, the electric charge variation taking out from C_{FC} during each discharging time interval can be written as:

$$\Delta Q_{FC} = \Delta t_{ch} i_g(t). \tag{4.17}$$

Therefore, considering Δv_{FC} as the ripple voltage across C_{FC}, the required capacitance for C_{FC} is obtained as [121]:

$$C_{FC} = \frac{\Delta Q_{FC}}{\Delta v_{FC}} = \frac{I_m k_{FC}}{f_{sw}}. \tag{4.18}$$

where, k_{FC} is a non-dimensional coefficient as:

$$k_{FC} = (2d(t)-1)\sin \omega t. \tag{4.19}$$

Taking (4.18) and (4.20) into account, the maximum charging current of FC, which can represent the maximum current stress of charging path switches in the boost mode can be obtained as [25]:

$$i_{ch,max} = \frac{D_m}{1-D_m} \times \frac{1+\delta}{1+2\delta} I_m. \tag{4.20}$$

where, δ is equal to $\frac{C_{FC}}{C_1}$. As can be taken from (4.18), as opposed to the CGSC-based MLIs or other pure SC-based converters, $i_{ch,max}$ in the proposed DM-ANPC-5L converters can be controlled to a permissible range by applying a limitation in D_m or choosing larger capacitance for C_{FC}.

On the other hand, the charge/discharging duration of C_{FC} in the buck mode of

Table 4.4: A comparison between the proposed DM-ANPC-5L converters and their other available 5L inverters/converters counterparts.

Type of Converter	No. of Components				Output Voltage Gain	MVS (pu) /TSV (pu)	FC-Balancing Technique	Bidirectional/ MVS on FCs (pu)	Leakage Current /Modulation	Reported Efficiency
	S	D	C	G						
ANPC-based [117]	8	0	3	8	0.5	1/6	FC-based	Yes/0.25	Low/PS	99%@1kW
ANPC-Based [98]	6	2	3	6	0.5	1.5/7	FC-based	No/0.25	Low/PS	NA%@1kW
ANPC-Based[123]	7	2	3	7	0.5	1.5/6.5	FC-based	No/0.25	Low/PS	NA%@1kW
ABNPC-Based [25]	6	2	3	6	1	1/5	SC-based	No/1	Low/LS	97.8%@1.5kW
ABNPC-Based [121]	8	0	3	8	1	1/5	SC-based	Yes/1	Low/LS	98.3%@3kW
ABNPC-Based [124]	10	0	3	10	1	1/7	SC-based	Yes/0.5	Low/LS	NA%@50W
ABNPC-Based [125]	10	2	3	10	1	0.5/5	SC-based	No/0.5	Low/LS	96%@1kW
ABNPC-Based [126]	10	0	4	9	1	1.5/7	SC-based	Yes/0.5	Low/LS	NA%@160W
CG-Based [116]	9	1	3	7	1(2)	1(2)/5.5	SC-based	No/1(2)	Zero/LS	96%@600W
CG-Based [120]	9	1	2	8	1(2)	1(2)/6	SC-based	No/1(2)	Zero/LS	98.5%@1kW
Proposed DM-ANPC-Type-I	10	0	3	6	0.5(1)	0.75(1)/5(6)	FC(SC)-based	Yes/0.25(1)	Low/PS(LS)	98.3%@2.2kW
Proposed DM-ANPC-Type-II	10	0	3	8	0.5(1)	0.5(1)/5(6)	FC(SC)-based	Yes/0.25(1)	Low/PS(LS)	98.2%@1.5kW
Proposed DM-ANPC-Type-III	10	0	4	7	0.5(1)	0.5(1)/5.5(6.5)	SC-based	Yes/0.25(0.5)	Low/LS	97.3%@1.5kW

operation is similar to any conventional type of FC or ANPC-based converter since it comes from the PS-PWM principle as:

$$\Delta t_{ch} = \frac{1 - d(t)}{2 f_{sw}}. \tag{4.21}$$

Hence, the required minimum capacitance for C_{FC} is much smaller than the boost mode as [122]:

$$C_{FC,min} = \frac{I_m}{2 \Delta v_{FC} f_{sw}}. \tag{4.22}$$

Therefore, the larger value of C_{FC} extracted from the boost mode of operation in (4.18), is considered for the proposed DM-ANPC-5L converter since it can cover the worst case scenario.

4.2.5 Comparative Study

The circuit characteristics of the proposed DM-ANPC-5L converters are compared with several recently proposed ANPC/ABNPC or DM-based 5L converters/inverters in this section. As tabulated in Table 4.4, the comparative items are the number of required components, i.e., switches (S), diodes (D), capacitors (C), gate drivers (G), output voltage gain, the MVS and TSV on devices in the per-unit scale, the type of FC voltage balancing, i.e., pure SC-or FC-based, the bidirectional power flow and leakage current attenuation capabilities, the per-unit value of the MVS across FCs, the type of modulation, and finally the reported overall efficiency at the rated power. Herein, the value of the leakage current is considered "low" if the topologies are based on a mid-point clamping technique, i.e., ANPC or ABNPC-based converters, while it is assumed to be "zero" if a CG-based structure is adopted. Moreover, a single-channel gate driver is considered for each normal

MOSFET/IGBT or four-quadrant switch in all the discussed topologies in order to count the number of required gate drivers. Since the type of all the proposed converters are ANPC/ABNPC-based, most of the compared topologies are selected from this category of MLIs, while two recently proposed CGSC-based 5L inverters in [116, 120] are selected owing to their DM-based capability. The importance of modulation technique, i.e., LS or PS-PWM is as for addressing the size of output filters since PS-PWM technique can possess larger apparent output frequency with a minimized switching loss on devices.

As can be realized from Table 4.4, the notable advantages of all the proposed topologies compared with ANPC or ABNPC-5L converters are the bidirectional power flow performance, flexible output voltage gain, different types of the modulation per each mode of operation, and reduced value of the MVS and TSV across devices. The main differences among three different proposed DM-ANPC-5L converters are the number of required gate drivers, MVS/TSV indexes, the number of FCs and the voltage stress across them, and the type of FC voltage balancing technique. Here, although both the CG-based 5L inverters proposed in [116, 120] possess larger voltage conversion gain even in the buck mode of operation, their excessive charging current of the involved capacitors due to pure SC-based technique in both modes causes a large current stress passing through the devices. Moreover, none of them offers a bidirectional power flow performance to further broaden their range of possible applications. Conversely, although during the boost mode of operation, both the first and second variants of the proposed DM-ANPC-5L converters are SC-based, the current stress profile of the switches is limited with a proper selection of the maximum modulation index value. The reported efficiency of the Type-I of the proposed topology is based on the captured data in practice, while a PLECS software is used to extract this data as for the Type-II and-III of the proposed converters.

4.2.6 Single-Phase Simulation Results

The steady-state performance of the first variant of the proposed DM-ANPC-5L grid-connected converter in both modes of operation is shown in Fig. 4.20(a) and (b). The specification of this simulation is accorded with the data the same compiled in Table 3.3. The main aim of this simulation is to verify the current stress profile of the switches and the nature of the input current in both modes of operation since other related dynamic tests over this type of the proposed topology are later shown by the experiments. The input dc voltage for the boost and buck mode of operation is set at 400 V and 760 V, respectively. The peak of reference current is also set at 13 A and 10 A for the boost and buck mode of operation leading to around 2 and 1.5 kW injected power, respectively. As

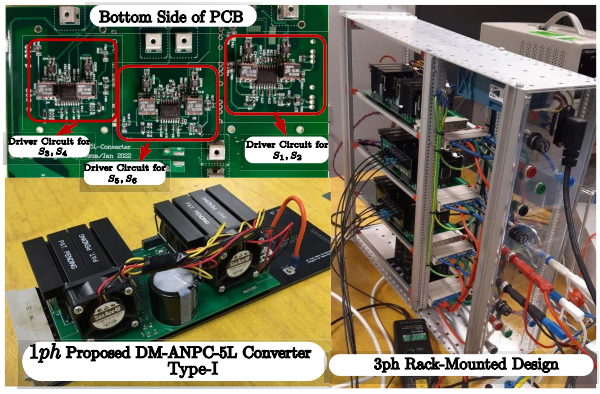


Figure 4.23: Experimental prototype of the proposed DM-ANPC-5L-Type-I converter.

already discussed, the boost mode of operation is based on the SC technique; hence, the maximum value of the modulation index, D_m, is limited to 0.9 in order to alleviate the current stress profile of the switches. As can be seen from Fig. 4.20(a), the FC charging path switches, S_1, and S_4, experience the highest current stress, while the input current is free from large discontinuous inrush spikes. The smooth performance of the proposed converter from the current stress view point on devices in the buck mode of operation can also be confirmed in Fig. 4.20(b), while the average voltage across the dc-link capacitors is half value of the input dc voltage, and the voltage across C_{FC} is at 190 V. Due to FC voltage balancing technique in the buck mode of operation, the peak of the input current is around 5 A at 1.5 kW injected power.

Consequently, a same detailed simulation is performed to prove the correctness of the second and third variants of the proposed DM-ANPC-5L converters [Fig. 4.18(a) and Fig. 4.19(a).]. Herein, the input dc voltage is set at 400 V and 800 V as for the boost and buck mode of operation for both topologies, respectively, while an 1.5 kW is considered for their rated power. In all the verification results, the peak of the grid voltage is set at 320 V. In both the simulation and experimental results, a PR controller is used in order to govern the proposed converters to inject a controlled current to the grid. Moreover, as for synchronization of the proposed converters with the grid, a simple GVO technique with an adjustable bandwidth is employed to detect the phase and amplitude of the grid voltage.The simulation results are shown in Fig. Fig. 4.21(a)-(b) and Fig. 4.22(a)-(b), where the voltage and current stress on devices as well as the 5L output voltage waveform of any of the proposed converters with the capacitors voltages in both modes of operation are depicted. Similar to the first variant of the proposed DM-ANPC-5L converter, the capacitors charging path switches for the second and third variants must tolerate the highest current stress. From Fig. 4.21(b), it can be seen that due to the FC

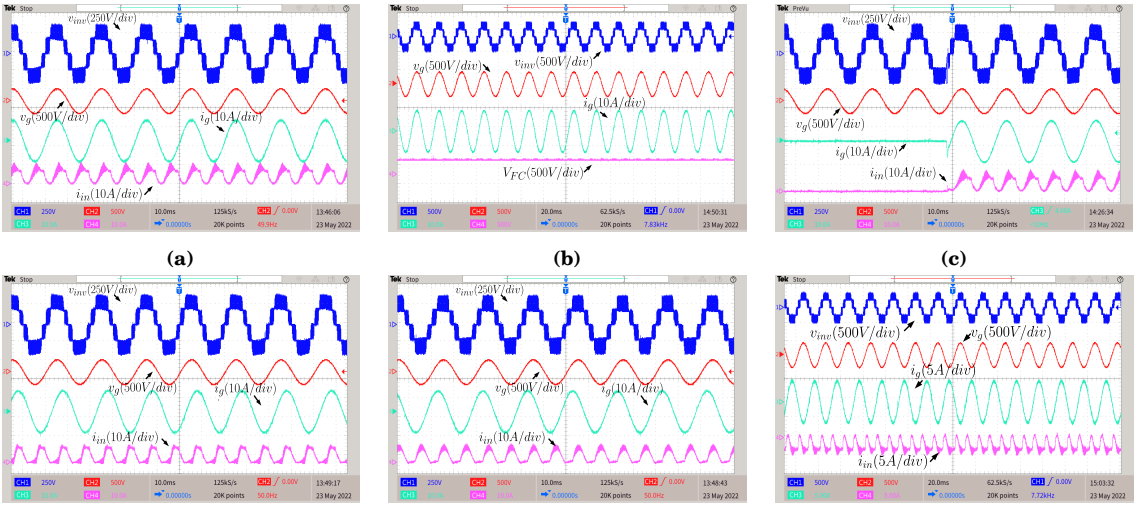


Figure 4.24: Experimental results of the proposed DM-ANPC-5L-Type-I converter in the single-phase grid-connected condition and during the boost mode of operation, (a) at the rated injected power, (b) at the rated injected power and with the presence of the voltage across C_{FC}, (c) with a step-change in injected power from zero to the rated power, (d) at the lagging reactive power support mode, (e) at the leading reactive power support mode (f) in the the reverse bidirectional mode.

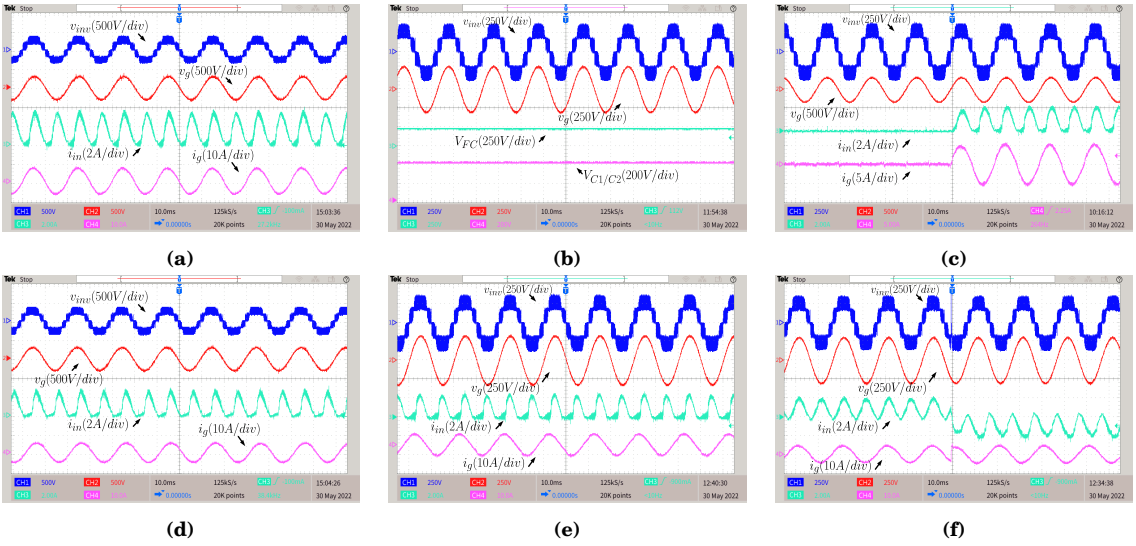
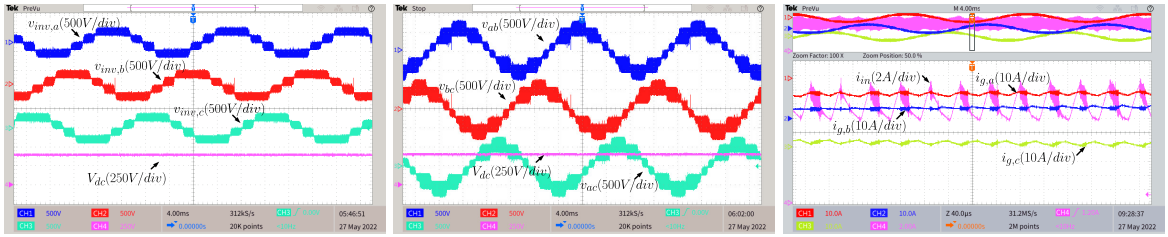


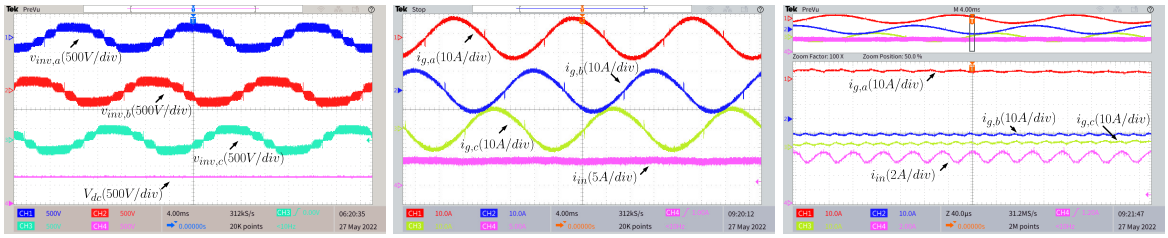
Figure 4.25: Experimental results of the proposed DM-ANPC-5L-Type-I converter in the single-phase grid-connected condition and during the buck mode of operation, (a) at the rated injected power, (b) at the rated injected power and with the presence of the voltage across dc-link capacitors and C_{FC}, (c) with a step-change in injected power from zero to 1 kW, (d) at the lagging reactive power support mode, (e) at the leading reactive power support mode (f) V2G and G2V dynamic test.

voltage balancing technique in the buck mode, the input and the switches current in the second variant of the proposed DM-ANPC-5L converter do not possess any large inrush spike. Conversely, owing to utilization of the SC technique in both operating modes, the involved switches in the charging path of FCs in the third variant of the



(a) **(b)** **(c)**

Figure 4.26: Experimental results for three-phase design of the proposed DM-ANPC-5L-Type-I converter during the boost mode of operation at P_g=5.7 kW, (a) 5L phase-voltage, (b) line-voltage, and (c) A zoomed shot of the injected grid current for each phase and the input current.



(a) **(b)** **(c)**

Figure 4.27: Experimental results for three-phase design of the proposed DM-ANPC-5L-Type-I converter during the buck mode of operation at P_g=5.3 kW, (a) 5L phase-voltage, (b) phase-current, and (c) A zoomed shot of the injected grid current for each phase and the input current.

proposed topology must tolerate the highest current stress as shown in Fig. 4.22(a)-(b). From the 5L peak output voltage of the proposed converters, the DM capability can also be confirmed, where a unity gain is achieved in the boost mode of operation, while in the buck mode, a half dc-link utilization is obtained. The main difference between the second and third variant of the proposed DM-ANPC-5L converters is the voltage appearing across the FCs. Due to utilization of two FCs in series, the MVS across the capacitors in the third variant of the proposed topology is half in comparison to their counterpart in the second variant. The MVS waveforms across all the devices in each mode of operation can also confirm the correctness of the analysis shown in Fig. 4.18(c) and Fig. 4.19(c).

4.2.7 Single- and Three-Phase Experimental Results

The fabricated SiC-based prototype as for the first variant of the proposed DM-ANPC-5L converter is illustrated in Fig. 4.23. In order to extensively address the performance of the proposed topology for both single-and three-phase applications, a rack-mouthed setup is also developed as shown in Fig. 4.23. The input dc-supply is an PV emulator (EA-PSI-9360-12), while as for the grid, a four-quadrant grid simulator (REGATRON

TC30.528.43-ACS) is used. A DSP (TMS320F28379D) has also been used to implement the respective control and modulation strategy, whereas the switching frequency of the converter is 20 kHz in each operating mode.

Considering 400 V as the input dc voltage, the converter is firstly connected to the grid in the boost mode of operation. Fig. 4.24(a) and (b) show the obtained experimental results related to the 5L output voltage, the grid voltage, the injected grid current, the input current and the voltage across the capacitor, C_{FC} at the steady-state condition and under 2.2 kW injected power to the grid. As can be seen, all the destictive output voltage levels are generated in this mode, while due to applying a limitation in D_m, the input current profile is still smooth without having any large inrush spikes. The dynamic results of the converter under a step change in the injected power, i.e., from zero to full 2.2 kW power, have also been illustrated in Fig. 4.24(c). The performance of the proposed DM-ANPC-5L converter under the lagging, leading, and bi-directional operations can also be seen in Fig. 4.24(d) to (f), respectively. Due to SiC switches used in the prototype with a very small value of ON-state resistance, the measured efficiency of the proposed converter at the full rated power was around 98.3%.

Conversely, to show the correctness of the proposed converter in the buck mode of operation, a dc voltage equals to 760 V is considered. The steady-state experimental results of the proposed converter at 1.3 kW injected power and the balanced voltage across the capacitors under this operating mode can be seen in Fig. 4.25(a) and (b), respectively, while the dynamic results from zero to full power injection are demonstrated in Fig. 4.25(c). As can be seen, similar to the boost mode of operation, all the 5L output voltage have been generated, whereas due to FC voltage balancing technique, the input current profile is smooth and only contains the double-line frequency. The reactive power support results of the proposed DM-ANPC-5L-Type-I converter under the lagging and leading power factors can also be seen in Fig. 4.25(d) and (e), respectively. The last experiment is related to a dynamic test for bidirectional power flow operation, i.e., V2G and G2V. Herein, an electronic load has been connected to the input PV emulator to absorb the reverse power from the grid. As can be seen from Fig. 4.25(f), all the output voltage levels in presence of the grid voltage are created, while the direction of the input current is changed suddenly to support the bidirectional operation. According to the data captured by the power analyzer, the measured efficiency of the proposed converter in the buck mode of operation and at the rated power was around 98.8%. The increased overall efficiency of the proposed converter in this mode is due to less overall current stress profile of the involved switches in comparison to the boost mode of operation with

a SC-integrated technique.

In following, the three-phase experimental results of the proposed DM-ANPC-5L converter, i.e., the phase voltages, the phase currents, the input dc voltage, and the input current, in both modes of operation are shown in Fig. 4.26 and Fig. 4.27. The value of the input dc voltage is similar as what has been used for the previous cases in the single-phase operation, i.e., 400 V and 760 V as for the boost and buck operating mode, respectively. The injected three-phase power for the boost mode is around 5.7 kW, while it is around 5.3 kW in the buck operating mode. As can be seen through the results, the input current in the buck mode of operation shown in Fig. 4.27(b) is free from any low-frequency pulsating content, while the similar case can be seen in the boost mode of operation shown in Fig. 4.27(c) but with some high-frequency spikes due to the incorporated SC technique. The smooth operation of the proposed converter in generating all the desired output voltage levels with a sinusoidal phase current in both modes of operation can clearly be confirmed through these results.

CHAPTER 5

CONCLUSION

Grid-connected TL-inverters are beneficial from the viewpoints of higher overall efficiency, lower overall cost and appropriate power density in comparison to the transformer-based inverters. However, to meet different IEEE standards, some associated challenges caused by removing the galvanic isolation between the TL inverters and the grid must be taken into account. Variable CMV and in turn the ground leakage current concern, step-up voltage boosting ability within a single-stage energy conversion platform and power quality enhancement issue motivated by generating larger number of inverter output voltage levels are three main motivations/research gaps of the available TL-based grid-tied inverters. LVRT ability, reliability, lower number of involved semiconductor devices, and reduced voltage and current stress across the semiconductor devices are other main targets of a proper TL-based grid-connected inverter. With hindsight to the literature review conducted in Chapter 1, it has been revealed that grid-tied TL-inverters can be considered within three main categories as: 1) Freewheeling-based structures that are mostly 3L-based inverters, e. g., H5, OH5. HERIC, PN-NPC, H6, 2) Mid point clamping-based topologies like ANPC, T-Type, and FC-based TL inverters, and 3) CG-based structures. Among various topologies available in literature, only the CG-based TL inverters are able to completely mitigate the concern of ground-leakage current. However, the available types of such converters have some limitations from the current stress of the involved switches, generating the boosted voltage with the static gain and also ability to cope with multilevel output voltage generations. The same observation is drawn for addressing the existing shortcomings of the mid-point-clamped-based TL-inverters, where the output

voltage of the inverter is usually half value of the main dc-link voltage. Although in case of using the SC-integrated technique, this setback has been resolved by emerging some ABNPC-based MLIs structures, still their output voltage gain is static/fixed and in case of having a wide varying dc-source voltage, additional measures must be taken into account.

In this research, several new CG-based grid-connected TL inverter topologies with the capability of at least 5L output voltage generation have been investigated, while each one has its own specific features. The first six of topologies explored in Chapter 2 are based on the static voltage conversion gain with an SC-integrated technique. Hence, although they can reduce the burden of the input dc voltage in providing a much smaller value of the input voltage to meet the minimum requirement of the grid voltage, still another power processing stage is needed in case of dealing with a very low and wide varying available voltage of the PV main string panels. The first, the second proposed CGSC5L-TL inverters and the dual mode CGSC5L-TL inverter presented as forth topology in Chapter 2 are all based on the SC technique. Discontinuous nature of the input current and large pulsating waveform of the current passing through the switches are their major setbacks. Reduced number of required power switches with reasonable voltage stress and having an ability to work in different switching mode are their main important benefits. The first and second CGSC5L-TL inverters have used the virtual dc-link concept to generate negative output voltage levels. Hence, two different capacitors with different nominal voltages are required per each structure. This can increase the risk of dc-offset in the output waveforms of the inverters. The third topology of this context uses a bit more number of switching devices but with the ability of output voltage levels extension and also with reduced capacitance values required per the involved capacitors.
The fourth CGSC5L-TL inverter is a dual-mode structure. Although it is able to generate 5L output voltage in both modes (once the input voltage is high, e. g., 400 V, or once the input voltage is low, e. g., 200 V), it is still based on SC-technique with a static voltage conversion gain. Hence, it needs another front-end dc-dc stage in case of low and wider varying input dc voltage and the concern of large pulsating current stresses of the switches remains in place.

Integration of TL-based MLIs feeding through RE-based sources in HFac grid-tied applications was the prime focus of the fifth topology presented in Chapter 2. Herein, a novel 9L9S-CGSC-based TL inverter has been introduced, which offers some important features like a compact design, double voltage conversion gain within a single-power processing stage, leakage current cancellation ability, and high efficiency through the

integration of both the SC and FC techniques concept. In addition to a unity ratio between the number of output voltage levels and the number of required power switches, the self-voltage balancing operation of the involved capacitors with a smooth input current waveform, is the extra merit of the proposed topology in comparison to most of its state-of-the-art counterparts. Extensive simulation and experimental results obtained from a 1.2-kW laboratory-built grid-tied prototype with a measured efficiency of more than 97.5% over a wide range of the injected power have verified the feasibility and effectiveness of this proposal. The last topology presented in Chapter 2 was a CGSB5L-TL inverter and has somehow addressed the concern of pulsating input current with smaller number of switching devices required. However, its output voltage is limited to five with only static gain of two.

In following, three new configurations of CG-based TL inverters with a dynamic voltage conversion gain have been proposed/investigated in Chapter 3. The first and second topologies in this chapter is a 5L grid-tied inverter with an integrated single-stage voltage boosting feature and a CG-based circuit configuration has been introduced. The proposed topologies are CGSB-based and require ten and nine power switches, a single boost inductor and two capacitors. Utilising the adjustable integrated switched-boost cell duty cycle, a dynamic voltage boosting property within a single power processing stage is achieved, while both involved capacitors are self-balanced. Such a dynamic voltage conversion gain is further enhanced using a quadratic version of the proposed topology. Interestingly, the input current in both cases is free from large discontinuous inrush current. These features make the proposed converter an attractive TL-based inverter for grid-tied applications. Design guidelines of the passive elements, comparative study and the laboratory experimental results at 1.5 kW rated power have confirmed the effectiveness and feasibility of the proposed topology. Following this, a novel 7L-CG-based TL inverter with a single-stage dynamic voltage conversion gain concept has been proposed as the last topology explored in Chapter 3. The proposed topology requires 10 unidirectional power switches with three self-balanced capacitors and an input inductor. Due to the SB-based feature and the ability of soft charging performance for the capacitors, the current stress profile of the switches is within a permissible range without inducing any inrush spikes. The working principle of the proposed topology followed by some simulation was also discussed.

As for the mid-point-clamped based inverters, a new ANPC-5L inverter with an integrated single-stage voltage boosting feature has been presented as the first proposed structure of Chapter 4. The proposed topology can generate 5L output voltage with a

dynamic (flexible) voltage conversion gain. This leads the converter to operate under a wide range of input dc voltage changes whilst maintaining the fundamental value of the inverter output voltage at the desired value. Reduced voltage stress across both the active and passive elements, continuous input current without having any large pulsating inrush current, bidirectional power flow capability, and ability to be modulated with PS-PWM technique are the other notable features of the proposed topology. Details of the circuit description, design guidelines and comparative study have been conducted. Finally, the performance of the proposed DB-ANPC-based 5L inverter under various grid-connected scenarios has been verified through a laboratory-built prototype and several experimental results.

Finally, a new family of dual-mode ANPC-5L grid-connected converters with three different topologies has been presented in Chapter 4. The dual-mode concept helps the converters to be operated under a wide range of the input dc voltage, i.e., buck or boost operating modes. When the input dc voltage is sufficient, the proposed topologies give a half dc-link voltage utilization in their ac output as their buck operating mode. Conversely, when the input dc voltage provided by any RE-based resources is low i.e., 50% of the previous case, all the proposed topologies can generate the same number of output voltage levels with a full dc-link voltage utilization as the boost operating mode. The capability of the proposed topologies in generating 5L ac voltage for a wide range of the dc source voltage is a significant improvement compared to the conventional ANPC-5L converters. Circuit analysis, design guidance, and a comparative study have been developed. Finally, extensive simulation and experimental results are presented to prove the feasibility and correctness of the proposed solution.

Regarding such presented findings, the following works and research can be conducted as for the future roadmap.

1) The research gap still shows that CGSB-based TL inverters with a dynamic voltage conversion gain can be further extended to have the generalization feature in generating larger number of output voltage levels. This can make them more attractive from the reliability and modularity concept point of view.

2) CGSB-based TL grid-connected inverters with a dynamic voltage conversion gain are capable of removing the double-line frequency content from the input current spectrum. Such concept needs an APD-based closed-loop technique and can make the converter more dense and suitable for the integrated MPPT operation within a single

power processing stage.

3) CGSB/SC-based MLIs can be designed based on the new wide band gap devices, e.g., GaN switches. Design consideration of these converters with GaN devices has some challenges even though it offers a high overall efficiency/power density. Hence, fabrication of new printed circuit prototypes with a compact design for the future proposed topologies can be another aim.

4) Further broadening the range of applications for both the battery-integrated or PV grid-connected systems using the proposed topologies can further establish their effectiveness in practice. Hence, some applications like dynamic voltage restorer, active power filter, and so on can be considered for future works on this topic.

5) Application of a fully soft switching technique for CGSC-based MLIs to improve the efficiency and reduce the current stress of the switches is still a challenging task that can be interesting for the future research on this topic.

6) Due to hard charging operation of pure SC-based MLIs, propagation of EMI noises is one of the major challenges during the switching operation of the converters. Mitigating or alleviating these noises needs a careful design consideration as it might cause false turn ON operation for the switches and reliability issue. Hence, a deep study on EMI suppression issue over the SC-based MLIs seems to be an interesting topic for the future development of application-oriented converters.

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