UTS UNIVERSITY OF TECHNOLOGY SYDNEY

Non-Isolated Multi-port DC-DC Converters: Topologies, Control Techniques and Fault-Tolerant Operation

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Doctor of Philosophy

under the supervision of Prof. Dylan Lu and A/Prof. Yam P. Siwakoti

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CERTIFICATE OF ORIGINAL AUTHORSHIP

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This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis. This document has not been submitted for qualifications at any other academic institution. This research is supported by the Australian Government Research Training Program.

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Abstract

This thesis proposed a family of dual-input single-output (DISO) step-up dc-dc converters exhibiting high voltage gain for grid-connected applications. The main advantage of the proposed concept is the common ground between input and output ports with a continuous input current profile at both input ports. Secondly, unlike previously reported solutions with discontinuous conduction (DCM) or pseudo-continuous conduction (PCCM) operation of the inductor, this thesis proposed a time multiplexed hysteretic control scheme (TMHC) to decouple the power-sharing among two input sources by keeping the inductor current in continuous conduction mode (CCM). Decoupling power sharing among the two input sources will remove unwanted transients and disruptions in the output. Lastly, this thesis proposed a fault-tolerant multiport converter where attention is given to the faults at the MOSFET level. This multiport converter can work in five different modes and reconfigure in case of a fault.

List of Publications

Published/Accepted Papers

- **MM Alam**, D.D.-C. Lu, Y.P. Siwakoti, "Small signal analysis of dual input buck converter," International Journal of Smart Grid and Clean Energy, 2020, 9, (1), pp. 8-16
- **Muhammad Alam**, D.D.-C. Lu, Y.P. Siwakoti, "Time-multiplexed hysteretic control for single-inductor dual-input single-output DC-DC power converter," International Journal of Circuit Theory and Applications, April 2022, pp. 1235-1249
- **Muhammad Alam**, D.D.-C. Lu, Y.P. Siwakoti, "A Novel DC/DC Three Port Converter with Fault-Tolerant Ability," 5th International Conference on Power Electronics and their Applications (ICPEA), 2022, pp. 1-7
- **Muhammad Alam**, D.D.-C. Lu, Y.P. Siwakoti, "A Novel Non-Isolated Three-Port Converter for Battery Management Systems," 32nd Australasian Universities Power Engineering Conference, (AUPEC), 2022
- Priyabrata Shaw, **Muhammad Alam**, D.D.-C. Lu, Y.P. Siwakoti, "A New Dual-Input Single-Output Step-up DC-DC Converter for Grid-Connected Photovoltaic Applications," 4th International Conference on Smart Power & Internet Energy Systems, (SPIES), 2022

Papers Under Preparation

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- Priyabrata Shaw, **Muhammad Alam**, D.D.-C. Lu, Y.P. Siwakoti, "Analysis and Design of a New Dual-Input Single-Output Step-up DC-DC Converter for Grid-Connected Photovoltaic Applications," IEEE Transactions of Industrial Applications, TIA, 2022

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Chapter 1

Introduction

1.1 Research Background

Energy generation has always been one of the essential commodities of human civilization. For centuries, human civilization has been burning fossil fuels, such as coal, oil and gas, to generate energy. Nevertheless, with the advent of science, humans realise they are destructively affecting the Earth's atmosphere using fossil fuel-based power generation [1–3]. This century, two-thirds of greenhouse gas emissions are generated mainly from energy-related sources [4–8]. This greenhouse gas emission is the root cause of increased global warming, and decreasing global warming is one of the biggest dilemmas of modern technology today. However, renewable energy systems represent a pathway for attaining a system having characteristics of immediate deployment, safe conversion process and reliable green energy production [9, 10]. This green energy production gives an alternative way to conventional ways and helps reduce global warming. The latest renewable energy systems use multi-port converters interface multiple sources and loads simultaneously.

1.2 Motivation and Research Problem

Renewable energy systems are facing many challenges, including but not limited to size, cost, energy efficiency, and control complexity [11–13]. Firstly, many renewable energy sources and energy storage elements such as PV panels, fuel cell units, batteries and thermoelectric generators produce low voltages. To obtain a practical use of those sources such as integrating them into a microgrid, a high step-up voltage conversion is required. Secondly, the power converters are required to interface with multiple sources and loads from a power system perspective. Most available solutions are based on single-input, single-output (SISO) converters. It is not uncommon to use several SISO converters in a system due to the convenience of their modularity nature. However, when multiple SISO converters are cascaded or stacked, they lower the overall power conversion efficiency and create uneven power-sharing and cross-regulation issues. Thirdly, the protection and remedial actions after a fault occur in the power systems become increasingly complex to handle due to each SISO converter being managed by an individual controller. Multiple-input, multiple-output (MIMO) converters, which possess multiple-port interfaces and a more centralized control approach, become a viable solution, particularly when the renewable energy sources and loads are in proximity. However, as the thesis would unpack in the subsequent chapters, MIMO converters also inherit some of the issues as that of SISO converter implementation. This thesis hence attempts to investigate those issues, namely, high step-up conversion, power-sharing issue and fault-tolerant capability, and to produce feasible solutions to those challenges to advance the knowledge further.

1.3 Objectives

The main goal of this research project is to present the technical limitations of multiport converters and propose a novel solution for these limitations in order to

increase the efficiency of renewable energy systems. The work presented in this research thesis consists of theoretical and hardware-level results. All the mathematical and experimental results are listed in this thesis. The conceptual ideas related to multiport converters were first verified using the LTspice and PLECS circuit simulators, followed by experimentation.. The main objectives of this research are as follows:

- To study and analyze Three Port Converters (TPCs) in terms of cost, size and control complexity.
- To find the optimal solution for increasing the output voltage gain of Three Port Converters (TPCs).
- To find the optimal solution to decouple the power-sharing between the multiport converter.
- To find a fault-tolerant Three Port Converter (TPC) structure to increase the converter's reliability.
- To perform the reliability assessment using existing stochastic procedures.
- To find a fault-tolerant Three Port Converter (TPC) structure having more than one storage element.
- Design scaled laboratory prototypes, perform testing, debugging and record hardware results.

1.4 Organization of the Thesis

In Chapter 2, a brief review of the technical limitations of TPCs has been carried out. In Chapter 3, different TPCs have been studied, and based on their comparison, a novel dual-input single-output (DISO) TPC has been proposed to increase the

output voltage gain of the converter. In Chapter 4, an optimal solution to decouple the power-sharing between the dual-input single-output (DISO) buck converter in continuous conduction mode (CCM) has been proposed. In addition, studies have been carried out in discontinuous conduction mode (DCM) for the same buck converter. Then a comparison using the same parameter between CCM and DCM has been performed. In Chapter 5, a new fault-tolerant topology of TPC is proposed and reliability assessment has been performed using the Markov chain model. Additionally, a novel fault-tolerant converter having more than one energy storage is also proposed in Chapter 6. Finally, a conclusion is drawn, and future work is explained in Chapter 7.

Chapter 2

Literature Review of Multiport DC/DC Converters

2.1 Overview

Multi-input multi-output (MIMO) converters play a crucial role in hybrid renewable power generation systems which typically consist of multiple sources producing power at different voltage levels due to different limitations, i.e., solar irradiation in the case of PV cells and chemical reactions in fuel cells [14]. MIMO converters are the optimal solution for utilising the different types of DC-DC sources to produce power at a fixed DC voltage level in a hybrid power system. One example of using a MIMO converter in a hybrid solar power generation system is the smart home, depicted in Fig. 2.1., which is connected to the grid and uses different renewable energy resources to provide either DC or AC power. In this case, if the system uses single-input single-output (SISO) power converters, it will require a separate power stage for every load, as depicted in Fig. 2.2, in which case there should be a separate control system, which will increase control problems and maximise the cost. Fig. 2.2 shows that communication is required between the different inputs and loads. If the system uses SISO converters, then there is a risk of a communication delay

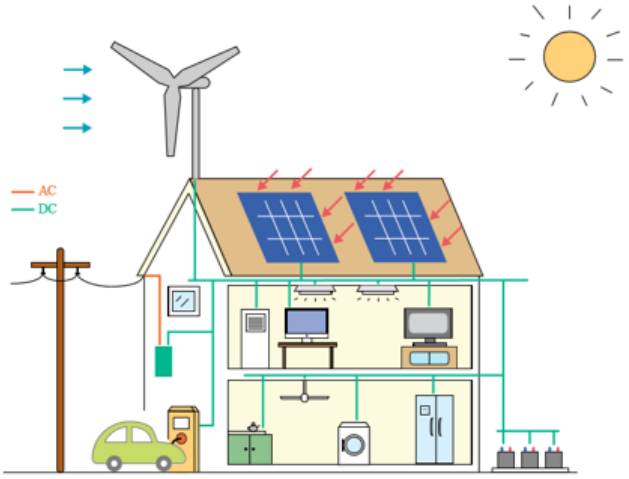


Fig 2.1: Smart home infrastructure [1].

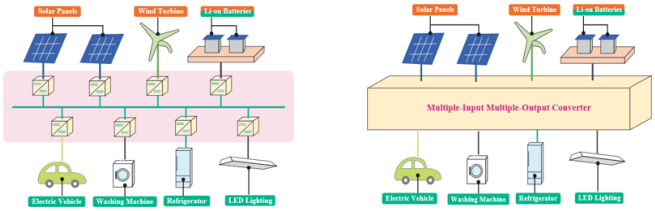


Fig 2.2: Difference between SISO and MIMO converters [1].

between the sources, which can cause operational problems. Therefore, it requires MIMO converter-based topology, which will handle this process quite easily.

The MIMO converter allows users to input from various sources and utilise them at different loads [15], and they also help integrate other converters to generate DC power. MIMO converters play a vital role when it is required to give preference to one source over another (usually, preference is given to renewable resources). These converters can also perform power budgeting between the loads. There are many advantages of using a MIMO converter compared to SISO converters, i.e., fewer components, compact packaging, high power density, and centralised converter control, as shown in Fig. 2.2 [16].

MIMO converters can be used in different applications, including DC nano-grids, electric vehicles, multi-port power supplies, distributed generation systems, and smart homes [16–21]. However, there are a few common problems with MIMO converters, including interfacing multiple inputs and power sharing between them,

low output voltage gain, and switching faults during the converter's operation in different modes.

The scope of this thesis is limited to the research, design, and implementation of non-isolated dual-input single-output (DISO) converters, of which this chapter provides a comprehensive overview. Section II will briefly discuss the DISO topologies used in different electronic applications. Finally, a conclusion will be drawn about the technical limitations related to DISO converters.

2.2 Dual-input single-output (DISO) converters

Conventional DC-DC power converters use discrete power converters to supply variable voltage levels to different loads. With these systems, there is a common control system responsible for managing the unidirectional power flow between the power converters through different communication channels, which increases the number of components and creates a communicational delay that negatively affects the output of the converter [15].

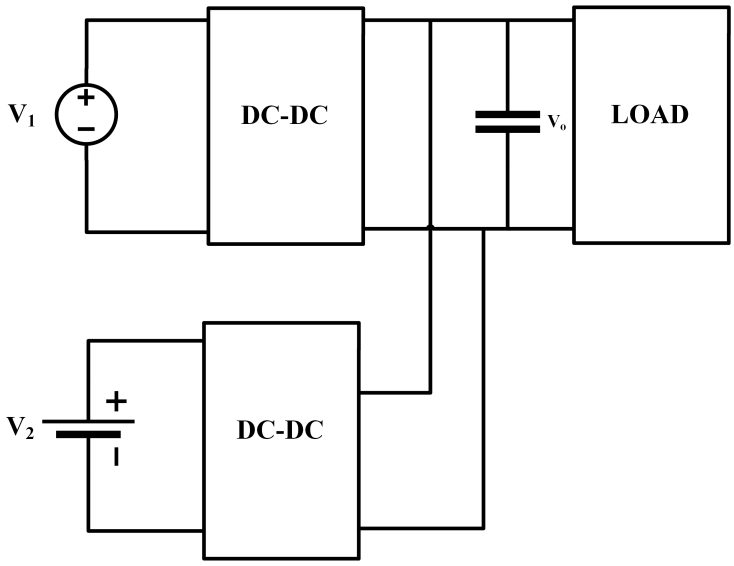


Fig 2.3: Conventional dc-dc converter multi-port structure.

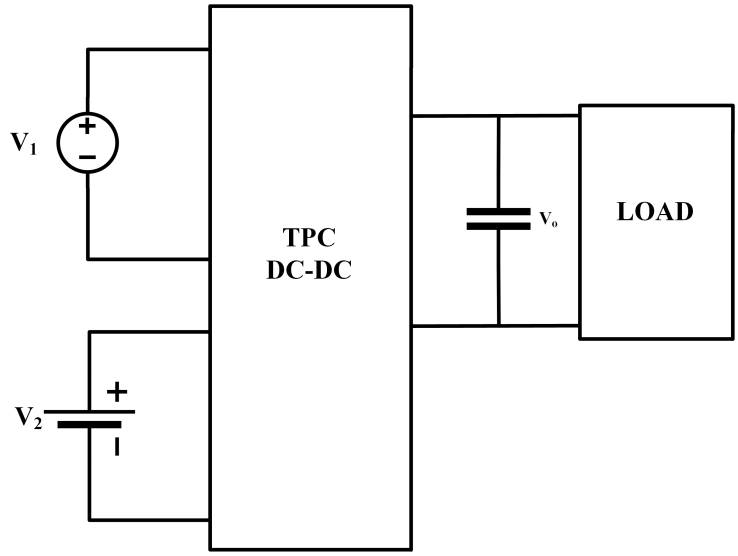


Fig 2.4: Multi-port dc-dc structure.

There are several advantages to using non-isolated DISO converters compared to SISO converters, including low cost, centralised control, and a simple structure. In DISO converters, semiconductor switches and passive elements can reduce the number of components using multiplexing techniques that help to improve the power density in those cases where the power flow relation between the input and output ports is satisfied. Therefore, a non-isolated DISO converter is useful when handling multiple inputs and a single load, using fewer components. There are several studies related to multi-port converters [22–31] covering this specific topic.

A bi-directional, non-isolated DISO converter is proposed in [22], where a battery is added to provide a reliable output when there is partial shading of the PV panels, or there are fuel cell fluctuations due to constantly changing external conditions. The circuit configuration consists of five switches and two inductors, and a DC motor is connected to the converter as an output, as shown in Fig. 2.5.

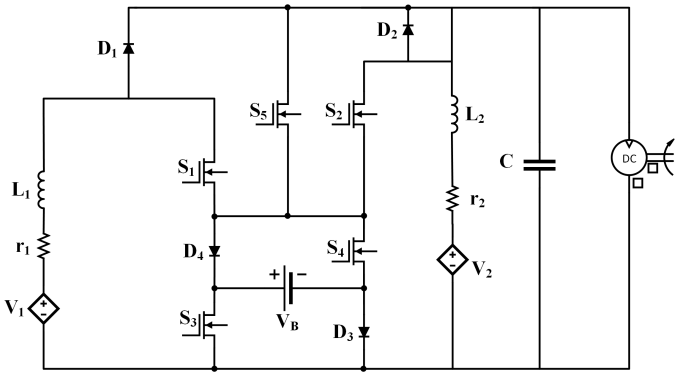


Fig 2.5: A bidirectional non-isolated diso converter [22].

The circuit can work in four different modes. In first mode, S_1, S_2, S_3 and D_3 are active to charge the inductor, as in a SISO DC/DC boost converter. The battery is charging inductors L_1& L_2 while S_4 is performing output voltage regulation in second mode. The input sources provide the required output voltage and charge the battery. The battery is charged with the help of the regenerative braking of the motor. This feature of the proposed converter provides the additional benefit of having a bi-directional power flow.

Another non-isolated DISO converter for PV power generation is proposed in [23] and shown in Fig. 2.6. The main idea is to deliver each input's power through an independent control. This topology decreases the current stress on the metal–oxide–semiconductor field-effect transistors (MOSFETs) by limiting the current rating of each power to its related power stage respectively, thereby producing a higher voltage gain. This circuit can also work in four different modes. The capacitor is charging due to the discharging of inductor L_1, while S_1 and S_2 are turned off simultaneously. The inductor L_2 discharges into the output capacitor. S_1 is turned on and S_2 stays off. The first input will charge L_1, while L_2 is still discharging into the output capacitor. Both S_1 and S_2 are turned on. L_1 is charging due to V_1 while L_2 is charging due to C_1. In the last two modes, the operation will be reversed as compared to the first two modes. An additional diode reconfigures the circuit in case of failure. The proposed topology can be expanded up to N number of inputs.

A non-isolated double-input PWM DC-DC converter and a non-isolated dual-input

H-bridge-Based Buck-boost-Buck-boost converter are assessed in [24] and [26], respectively, and shown in Fig. 2.7 and Fig. 2.8, respectively. In both converters, the power from two different input sources can be supplied to the load simultaneously.

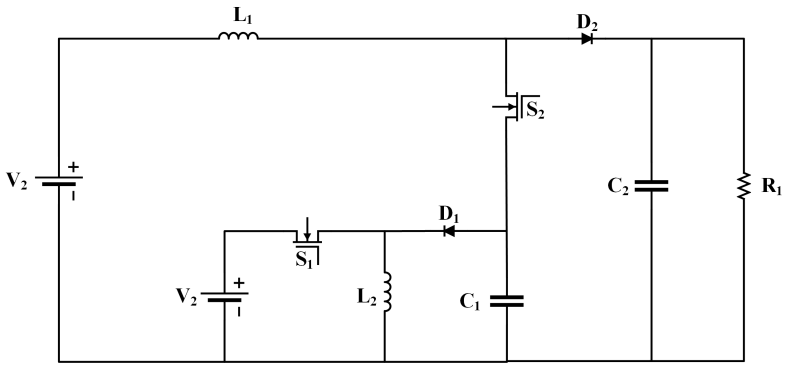


Fig 2.6: A non-isolated diso converter for pv power generation [23].

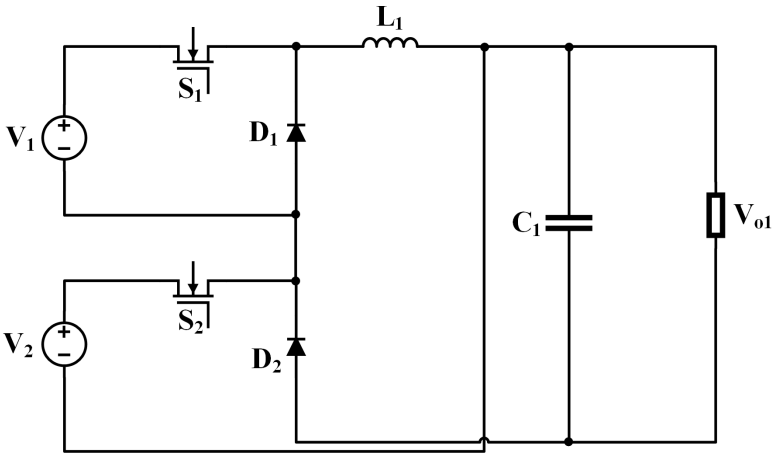


Fig 2.7: A non-isolated double-input pwm dc-dc converter [24].

The topology in [24] contains two MOSFETs and two diodes with a single inductor. The converter can operate in four different modes. The structure of the converter is shown in Fig. 2.7. On the other hand, the topology proposed in [26] has three MOSFETs and three diodes. However, if the main switch S_1 of either of these two topologies fails, it will lead to a complete system shutdown. Another non-isolated dual-input dual-output DC-DC converter is proposed in [25]. As shown in Fig. 2.8, both PV and the battery share a single inductor with three MOSFETs and three diodes. The converter can operate in four different modes depending upon the switching of the four MOSFETs.

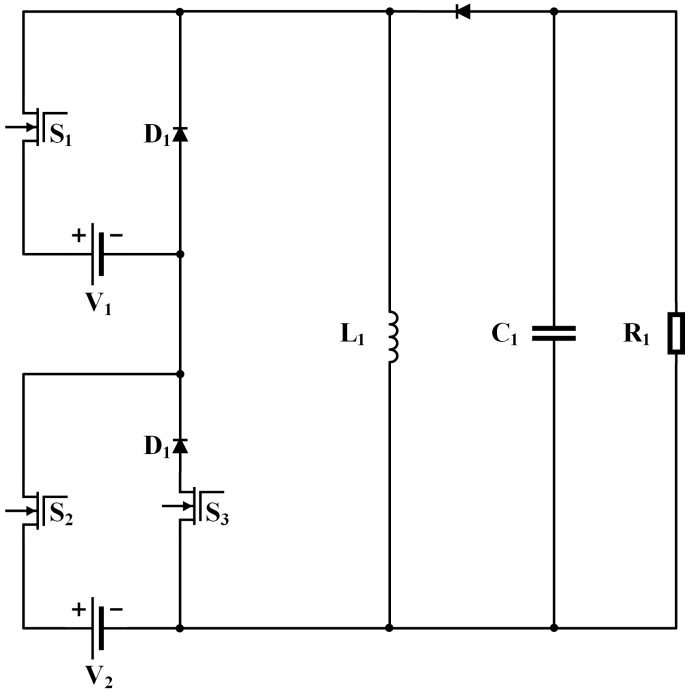


Fig 2.8: A non-isolated dual-input H-bridge-based buck-boost-buck-boost converter [26].

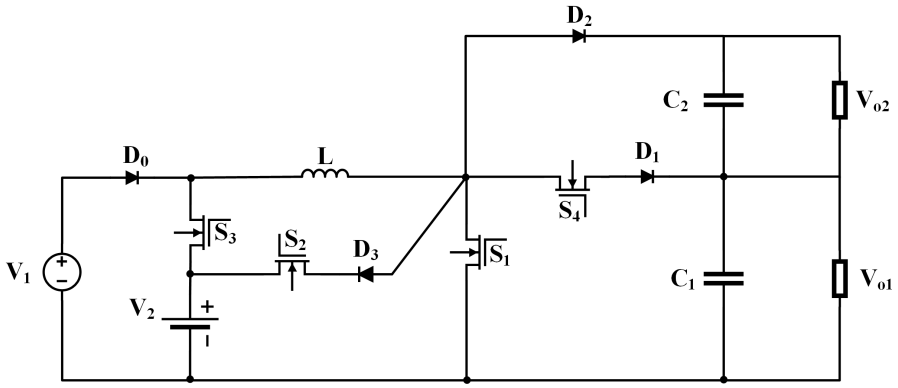


Fig 2.9: A non-isolated dual-input dual-output dc-dc converter for electric vehicle [25].

However, there is no redundant MOSFET for the main switch S_1; if S_1 fails, then the converter can neither charge the battery nor boost the output voltage. Another non-isolated multiple-input DC-DC converter for power diversity and optimization is proposed in [27]. This converter has a fault-tolerant structure, as shown in [27], and if a fault occurs at any of the MOSFETs, the parallel input source can continue supplying the power. Non-isolated multiple-input DC-DC converters are proposed in [28] to enhance local availability to the grid. The proposed structure

contains boost and buck-boost legs and integrates several power sources into a common DC bus, as shown in Fig. 2.11. However, there is no redundant MOSFET for the main switch S_1. If S_1 fails, then the converter can neither charge the battery nor boost the output voltage. Another non-isolated multiple-input dc-dc converter for power diversity and optimization has been proposed in [27]. This converter has a fault-tolerant structure, as shown in Fig. 2.10, and if there is any fault occurs at any of the MOSFETs, the parallel input source can keep supplying the power. Non-isolated Multiple-input dc-dc converters to enhance local availability in grids are proposed in [28]. The proposed structure contains boost and buck-boost legs and integrates several power sources into a common dc bus, as shown in Fig. 2.11.

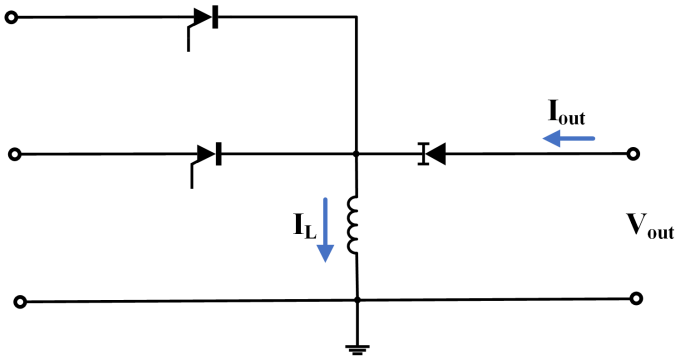


Fig 2.10: A non-isolated multiple-input dc-dc converter for power diversity [27].

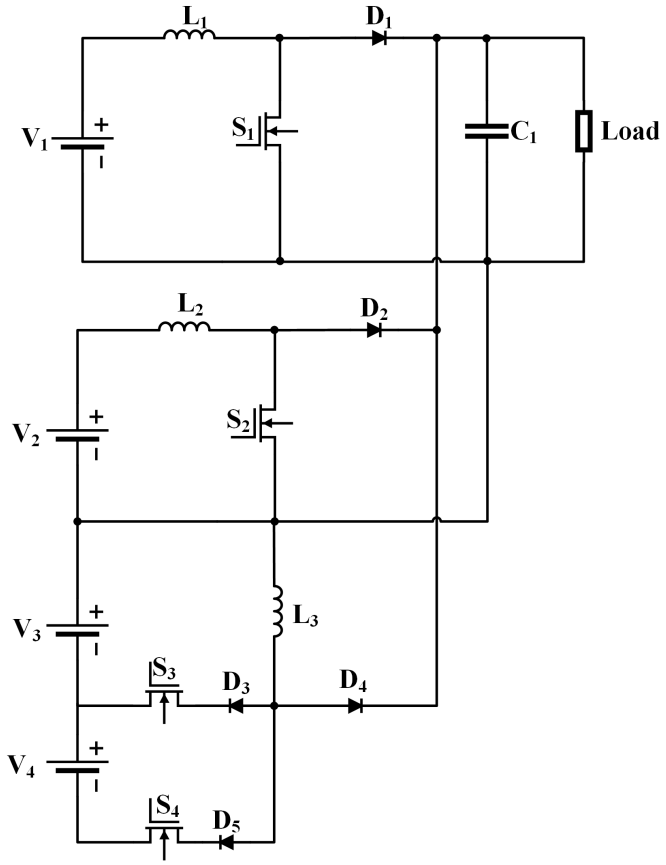


Fig 2.11: A non-isolated multiple-input dc-dc converter for power diversity [28].

The converter has boost input sub-modules for the power sources. However, it uses common module components for all the stages, increasing the reliability of the converter as compared to those previously discussed. In [29], a non-isolated multiple-input single-ended primary inductor (SEPIC) converter is proposed, which has dual inputs with two MOSFETs, three diodes, and three inductors, as shown in Fig. 2.12

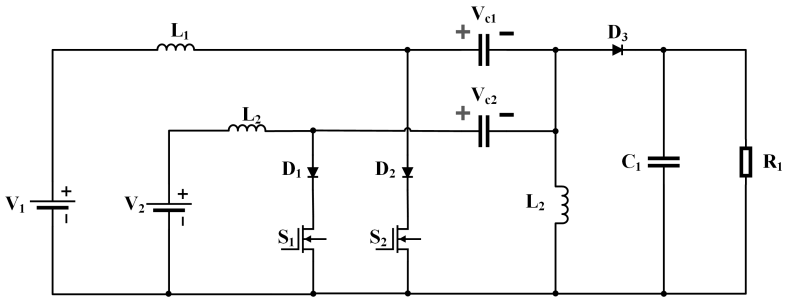


Fig 2.12: A non-isolated multiple-input single-ended primary inductor (SEPIC) converter [29].

In case of failure in any input leg, the parallel leg can keep providing the required output voltage. A non-isolated bipolar output four-port converter, sharing a common reference, is proposed in [30] that has three MOSFETs, three inductors, and six capacitors. This converter has integrated PV and battery to the DC microgrid systems using single power processing stages. A novel non-isolated dual-input converter with high gain and low average peak inverse voltage is proposed in [31].

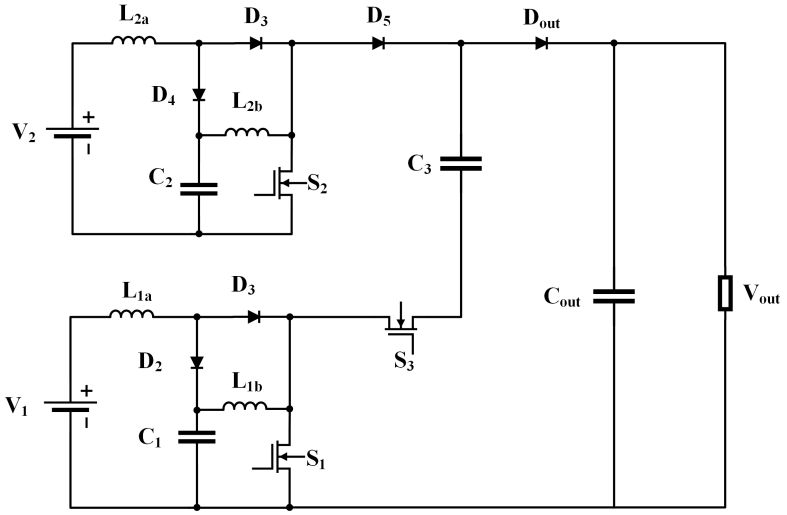


Fig 2.13: A non-isolated dual-input converter with high gain and low average peak inverse voltage [31].

The main benefits of using this converter are the continuous input current and the option of using n number of input sources, as shown in Fig. 2.13. In case of a fault in any leg, the other power source can continue supplying the power. However, the high component count, as well as the higher duty ratio for MOSFETs, are the main shortcomings of this converter. Developing DISO converters is challenging due to multiple design constraints from the literature listed in the form of a Table 2.1. These constraints include the total number of circuit elements, the nature of input currents, the output voltage gain, the possibility of circuit extension to multiport structure and the common ground between input/s and the output/s of the converter.

In [32], a non-isolated DC-DC converter is presented for grid-connected PV power generation systems, as shown in Fig. 2.14. Both the current sources provide con-

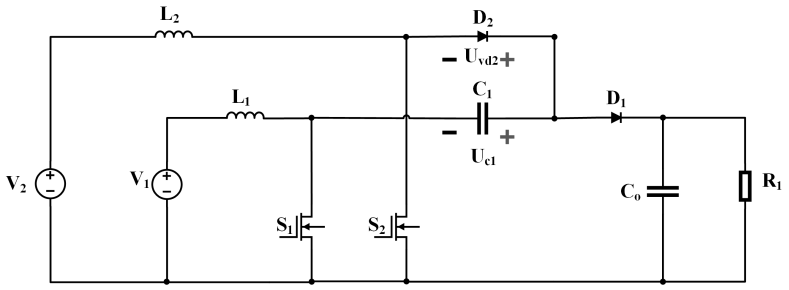


Fig 2.14: A non-isolated dc-dc converter for grid connected system [32].

tinuous input current to the converter. The circuit has a common ground between the inputs and the outputs and number of inputs can be increased. Another DISO step-up converter is proposed in [33] and shown in Fig. 2.15. This is a three-port

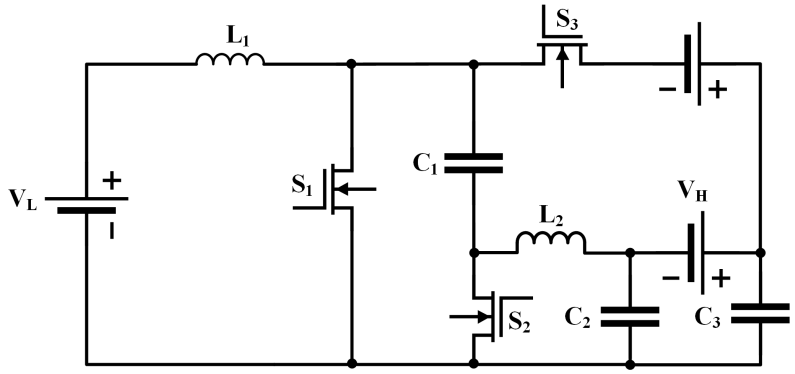


Fig 2.15: A non-isolated DISO step-up converter [33].

converter with a bidirectional feature whereby it can provide power from two different sources and perform step-up or step-down operations. However, the current nature of the first source is pulsating while the second is continuous. The circuit does not have a common ground and is not extendable to a multiport structure. In [34], a novel interleaved double-input three-level boost converter is proposed and shown in Fig. 2.16. The main feature of this converter is low input current ripple due to the interleaved control. Both input sources provide a continuous input current, and more inputs can be added. In [35], a fourth-order dual-input dual-output converter is proposed as shown in Fig. 2.17. This converter does not have a common ground between the inputs and the outputs and is not extendable to other multiport structures. The first input source provides pulsating current. However, the second source has continuous input current nature. A bridge type DISO DC-DC

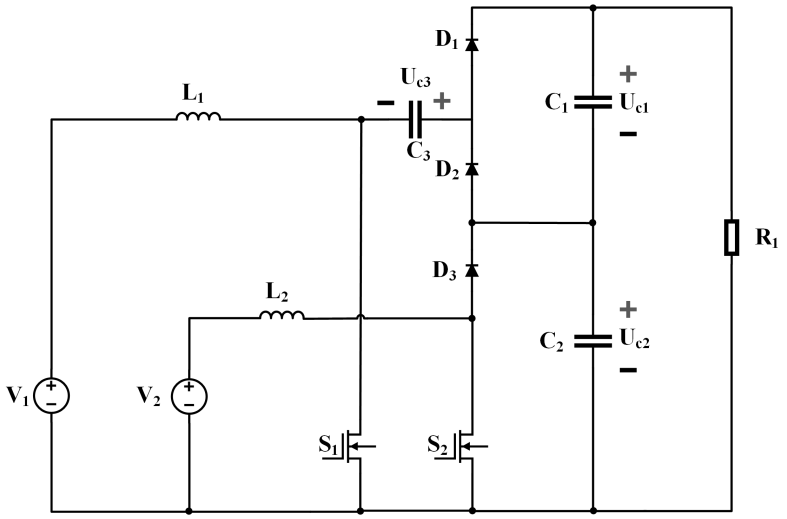


Fig 2.16: A interleaved double-input three-level boost converter [34].

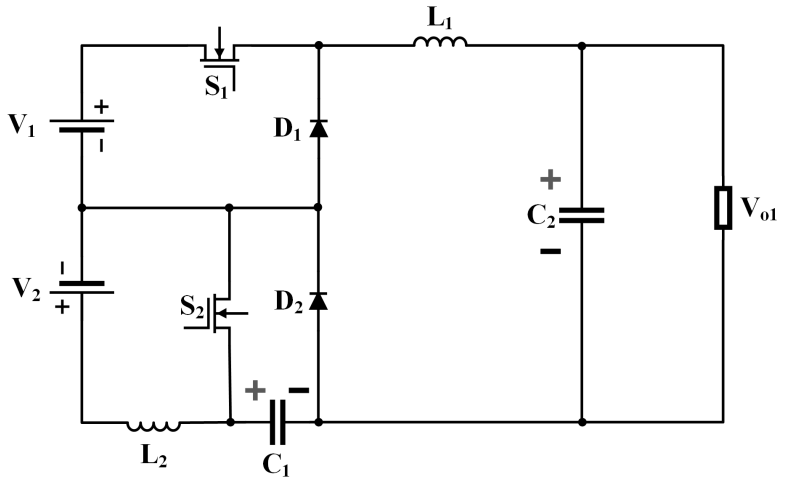


Fig 2.17: A fourth-order dual-input dual-output converter [35].

converter proposed in [36] shown in Fig. 2.18. The main feature of this converter is its ability to perform buck, boost, and buck-boost operations using two different input energy sources. However, this converter does not have a common ground and is not extendable to other multi-port structures and the current into both input sources is pulsating. In [37], another non-isolated dual-input step-up converter with bidirectional power flow from one port to another is presented. The nature of the input current of one source is pulsating while the other is continuous as shown in Fig. 2.19.

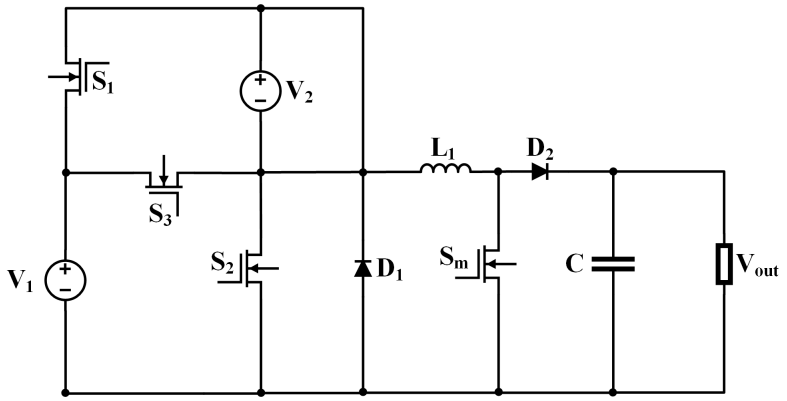


Fig 2.18: A two novel bridge type DISO dc-dc converter [36] .

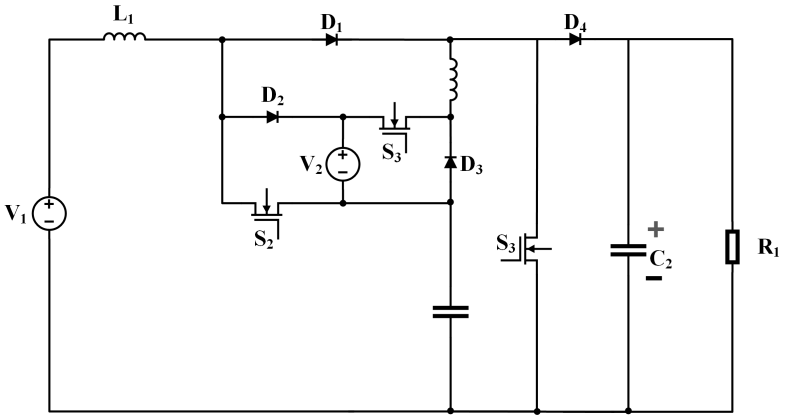


Fig 2.19: A non-isolated dual-input step-up converter [37].

However, the converter is not extendable to other multi-port structures. A dual-input buck SEPIC converter-based DC-DC converter with a two-loop digital control strategy is presented in [38]. The converter has two decoupled control loops,

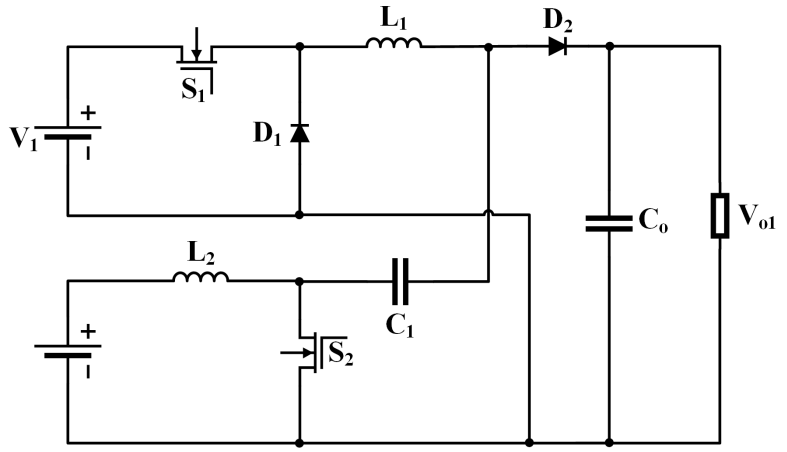


Fig 2.20: A non-isolated dual-input buck SEPIC converter-based dc-dc converter [38].

as shown in Fig. 2.20, the first loop is used for low-voltage sources, while the second is used for voltage regulation. The input current of one of the sources is pulsating, and the other is continuous. The converter has a common ground between the inputs and the output but it is not extendable to other multi-port structures. A dual-input converter drawing power from two different power sources with a common DC bus is proposed in [39] and shown in Fig. 2.21.

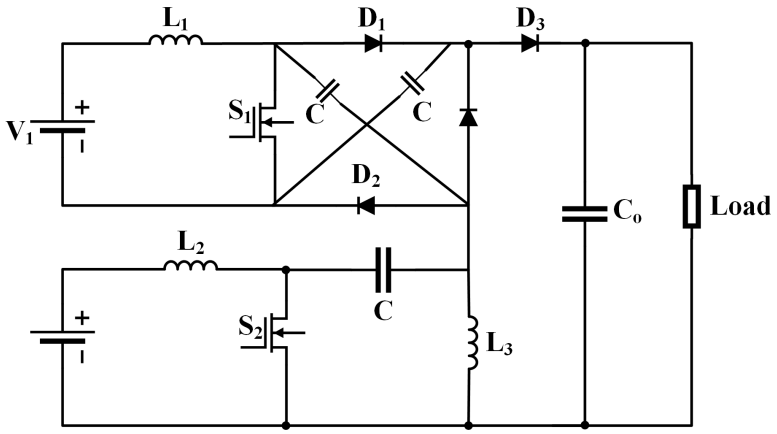


Fig 2.21: A non-isolated dual-input converter with common dc bus [39].

This converter has the additional benefit of using a soft switching technique which increases the converter's efficiency. However, the circuit is not extendable to other multi-port structures.

2.3 Summary

Multi-port converters are widely used in different applications to provide power from different renewable energy resources by sharing components. This sharing of components helps reduce the number of power processing stages and increases the converter's efficiency. However, in addition to efficiency, reliability and performance are also crucial for the multi-port converter. This chapter provided a brief insight into different non-isolated multi-input topologies that have been proposed to increase the output voltage gain and share the power between the multiple inputs

Ref No.	Components	Total number of Devices/ Storage Elements	Source Current Nature	Common Ground	Extendable to Multiport?	Gain & Efficiency
[32]	2 MOSFETs 2 Diodes 2 Inductors 2 Capacitors	4/4	1. Pulsating 2. Continuous	Yes	Yes	$V_{out} = \frac{1}{(1-D_1)}V_{in1} + \frac{1}{(1-D_2)}V_{in2;}$ 93%
[33]	3 MOSFETs 0 Diodes 2 Inductors 3 Capacitors	3/5	1. Pulsating 2. Continuous	No	No	$V_{out} = \frac{1+D_1}{(1-D_1)}V_{in1} + V_{in2}$; 90%
[34]	2 MOSFETs 3 Diodes 2 Inductors 3 Capacitors	5/5	1. Continuous 2. Continuous	Yes	Yes	$V_{out} = \frac{1}{(1-D_1)}V_{in1} + \frac{1}{(1-D_2)}V_{in2}$; 91%
[35]	2 MOSFETs 2 Diodes 2 Inductors 2 Capacitors	4/4	1. Pulsating 2. Continuous	No	No	$V_{out} = D_1V_{in1} + \frac{D_2V_{in2}}{1-D_2}$; 90%
[36]	4 MOSFETs 2 Diodes 1 Inductors 1 Capacitors	5/7	1. Pulsating 2. Pulsating	No	No	$V_{out} = \frac{D_1+D_3}{(1-D_1-D_3)}V_{in1} + \frac{1-D_1}{(1-D_1-D_3)}V_{in2}$; 94%
[37]	3 MOSFETs 4 Diodes 2 Inductors 2 Capacitors	7/4	1. Continuous 2. Pulsating	No	No	$V_{out} = \frac{1}{(1-D_1)^2}V_{in1} + [\frac{(D_1-D_2)+(1-D_1)(D_3-D_2)}{(1-D_1)^2}]V_{in2}$; 90%
[38]	2 MOSFETs 2 Diodes 2 Inductors 2 Capacitors	5/4	1. Pulsating 2. Continuous	Yes	No	$V_{out} = D_1V_{in1} + \frac{D_2V_{in2}}{1-D_2}$;92%
[39]	2 MOSFETs 4 Diodes 3 Inductors 4 Capacitors	6/7	1. Continuous 2. Continuous	No	No	$V_{out} = \frac{V_{g1}(1+d_1-2d_2)+V_{g2}d_2(1-d_1)}{(1-d_1)(1-d_2)}$; 94%
Proposed Converter	2 MOSFETs 2 Diodes 2 Inductors 2 Capacitors	4/4	1. Continuous 2. Continuous	Yes	Yes	$V_{out} = \frac{V_{in1}}{(1-D_1)} + \frac{D_2V_{in2}}{(1-D_1)(1-D_2)}$; 90%

Table 2.1: Comparison Table for non-isolated DISO dc-dc converter topologies.

with increased reliability. Non-isolated converters do not require galvanic isolation, resulting in a transformerless converter structure. This property of non-isolated converters not only reduces the cost but also helps reduce the converter's size. This thesis provides the solution for high voltage gain, power sharing, and fault tolerance of the non-isolated multi-port converter, and a non-isolated dual-input single output (DISO) converter with high voltage gain will be introduced in the next chapter.

Chapter 3

Novel DISO Step-up DC-DC Converters

3.1 Introduction

As mentioned in the previous chapter, non-isolated two-port DC-DC converters are popular due to their transformerless structure. However, when multiple energy sources, whether it is multiple PV panels, hybrid energy sources or a combination of those are used, multiple-input converters are an attractive solution due to their simpler structure and centralized control. Hence, this chapter will discuss different non-isolated dual-input single-output (DISO) converters, their voltage gains and the total number of circuit elements used to construct their respective topologies. This chapter will also propose a novel family of non-isolated DISO converters and provide in-depth analysis and design details of a selected circuit. As non-isolated DISO converters do not require galvanic isolation, these converters can be used in applications where the space and size for the converter are limited.

This chapter is a collaborative work between Priyabrata Shaw, Muhammad Alam, Dylan D-C. Lu and Yam P. Siwakoti. Priyabrata Shaw have conceieved the idea, while Muhammad Alam have performed all the technical and mathematical steps

to carried out the studies. Dylan D-C. Lu and Yam P. Siwakoti were the supervisors and helped with supervising as well as proof reading the manuscript/chapter. Section **??**, a literature review of non-isolated DISO step-up converters is presented in which eight different DISO step-up topologies, along with their voltage gains and structures, are compared, and the results are provided in the form of a table. In the next section, a family of novel DISO converters has been derived using power flow graphs and then a novel DISO step up converter and its analysis and design have been proposed, followed by open-loop experimental results and conclusion.

3.2 Novel Non-Isolated Step-up DC-DC converters

Based on the comparison table and the derivation from power flow graph, this section proposes a family of new dual-input single-output (DISO) step-up DC-DC converters exhibiting high voltage gain for grid-connected photovoltaic (PV) applications. The foremost advantages of the proposed concept is the common ground between input and output ports, a continuous input current profile at both input ports, high gain, fewer components, and the option to extend to other multi-port structures.
This section focuses on the characteristics and commonalities of the Dual-Input Step-up DC-DC converters in this converter family. This converter family (Fig. 3.1) can be derived from its related power flow graphs. Several circuit realisations can be derived from the power flow graphs shown in Fig. 3.2.

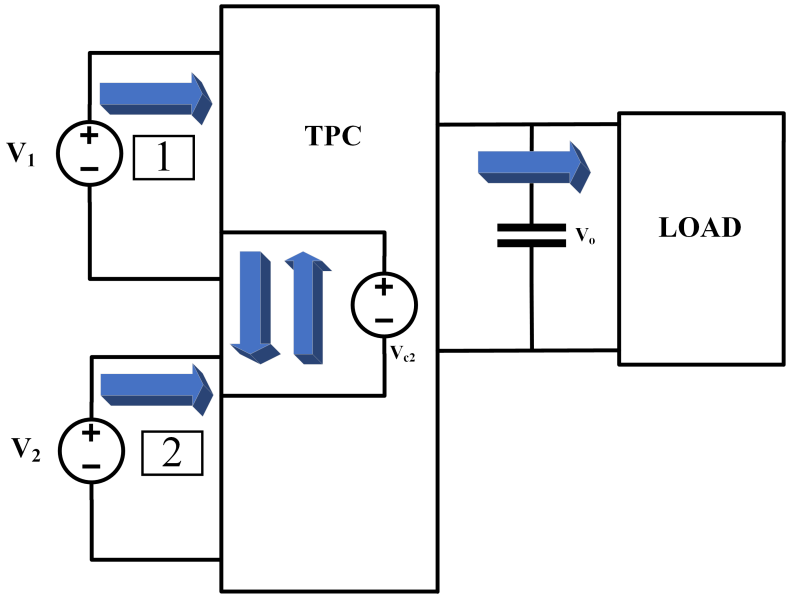


Fig 3.1: Key power flows in the proposed DISO converter family..

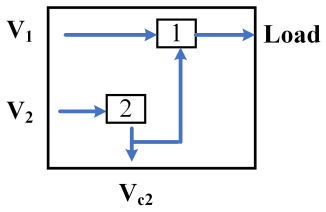


Fig 3.2: Power flow graphs for the proposed DISO converter family.

To demonstrate the feasibility of the proposed converter structure, the section shows the converter derivations using a buck/boost, a boost or a SEPIC converter combined with a boost converter. The base configuration serves as a DISO converter and if a particular type is selected, the associated converter topology is confirmed. These converter topologies are shown in Fig. 3.3 to Fig. 3.5.

3.2.1 DISO Buck-boost Based converter

First, the derivation starts by selecting a simple buck converter as a single port. For instance, if the three ports follow the constraint i.e. $V_2 > V_1 > V_o$. Secondly, in order to form a dual-input converter, the conventional single input has been replaced

with dual-inputs. Thirdly, selecting a bi-directional output port results in a novel bi-directional buck-boost converter as shown in Fig. 3.3.

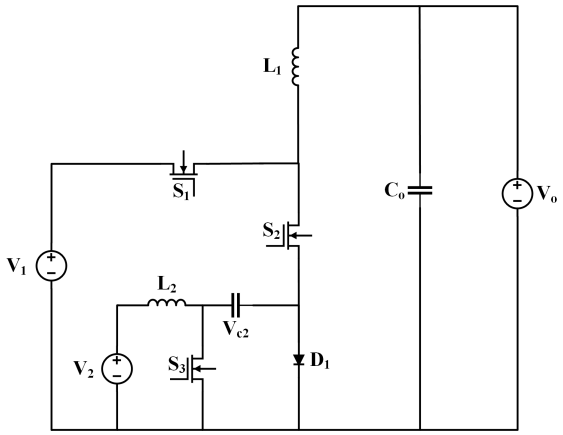


Fig 3.3: DISO Buck-Boost Converter.

3.2.2 DISO Boost Based Converter

First, the derivation starts by selecting a simple boost converter as a single port. For instance, if the three ports follow the constraint i.e. $V_1 < V_2 < V_o$. Secondly, in order to form a dual-input converter, the conventional single input has been replaced to dual-inputs. Thirdly, selecting a bi-directional output port results into a novel bi-directional boost converter as shown in Fig. 3.4.

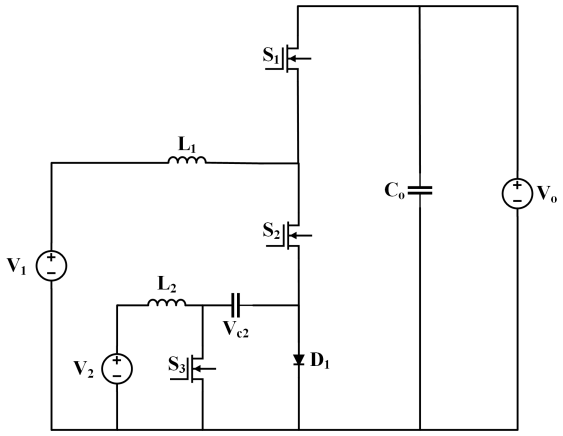


Fig 3.4: DISO Boost Converter.

3.2.3 DISO SEPIC based converter

First, the derivation starts by selecting a simple SEPIC converter as a single port. For instance, if the three ports follow the constraint i.e. $V_1 > V_2 > V_o$. Secondly, in order to form a dual-input converter, the conventional single input of SEPIC converter has been replaced to dual-inputs as shown in Fig. 3.5.

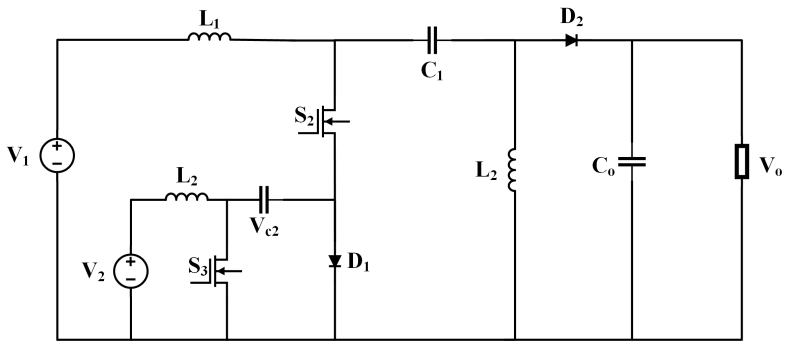


Fig 3.5: DISO SEPIC based Converter.

3.3 Analysis and Design of the proposed step-up DC-DC converter

The circuit structure of the proposed DISO DC-DC converter is shown in Fig. 3.6, and comprises two controllable switches (S_1 and S_2), two diodes (D_1 and D_2), two inductors (L_1 and L_2), and two capacitors (C_1 and C_2). Both the sources (source-1: Vin_1 and source-2: Vin_2) have inductors in series that result in a smooth input current. This topology is intended to be employed in a grid-connected PV system and will operate in continuous conduction mode (CCM) in which this DISO topology has three different switching modes within a switching time period (Ts); (i) mode-1, (ii) mode-2, and (iii) mode-3. The equivalent circuits of these three operating modes are shown in Fig. 3.7, Fig. 3.8 and Fig. 3.9 respectively. In this analysis, the duty ratio for switch S_1 is always considered more than that of switch S_2, which means that source-1 will be capable of supplying than source-2. Hence, mode-1 will be for $d_2T_s$duration, mode-2 will be for $(d_1 - d_2)T_s$ duration, and mode-3 will be

for $(1 - d_1)T_s$ duration, as presented in Fig. 3.10 which displays the ideal steady-state waveforms of the proposed DISO topology with respect to the gate signals of switches S_1 and S_2.

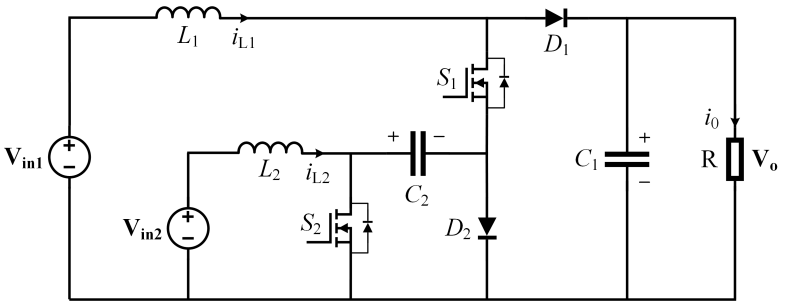


Fig 3.6: Proposed Non-Isolated DISO Boost Converter.

3.3.1 Operating Modes and Steady-state Analysis

1. **Mode 1** $[0 < t < d_2T_s]$: In this mode, both switches S_1 and S_2 are turned ON, thus the diodes D_1 and D_2 become reverse biased. In mode-1, the inductor L_1 is charged by source-1 Vin_1 and capacitor C_2 simultaneously through the switches S_1 and S_2. However during this interval, L_2 is charged by only source-2 (Vin_2) through switch S_2 and capacitor C_1 supplies the load. The equivalent circuit of this operating state is shown in Fig. 3.7.

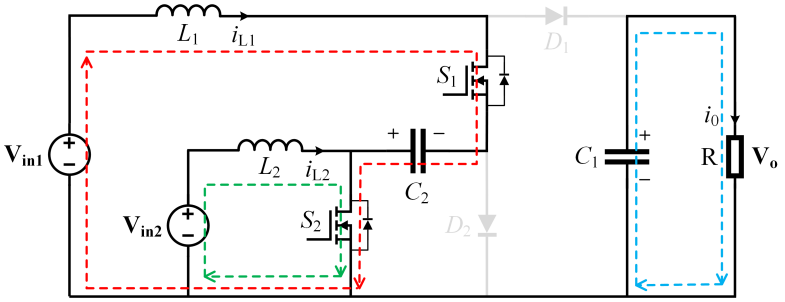


Fig 3.7: Mode 1.

2. **Mode 2** $[d_2T_s < t < (d_1 - d_2)T_s]$: In mode 2, switch S_1 is turned ON, and switch S_2 is turned OFF. This results in the conduction of diode D_2 and D_1 remains in the blocking state. In this interval, the inductor L_1 is charged by only source-1 (Vin_1) through switch S_1 and diode D_2. At this time, the

inductor L_2 discharges to energize C_2 through diode D_2 and the load is still supplied by the capacitor C_1 same as the mode-1 state. The equivalent circuit of the mode-2 operating state is presented in Fig. 3.8 to show the charging and discharging states of inductors and capacitors.

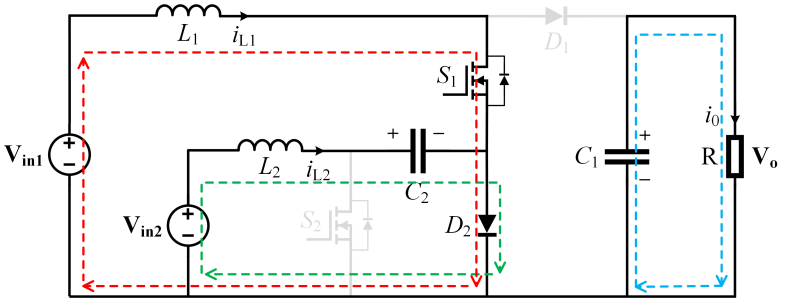


Fig 3.8: Mode 2.

3. **Mode 3** $[(d_1 - d_2)T_s < t < (1 - d_1)T_s]$: In this mode, both switches S_1 and S_2 are turned OFF, and thus, the diodes D_1 and D_2 become forward biased and start conducting. In mode-3, the inductor L_1 is discharged through load and it charges the capacitor C_1 through diode D_1. Similar to the mode-2 interval, the capacitor C_2 is charged by the inductor L_2 through diode D_2. The equivalent circuit diagram of the mode-3 operating state is shown in Fig. 3.9.

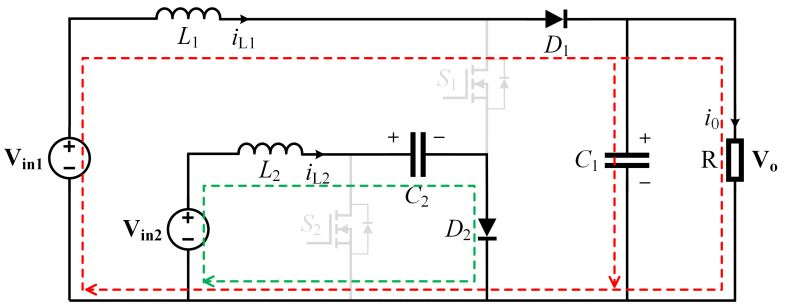


Fig 3.9: Mode 3.

From these three equivalent circuits shown in Fig. 3.7 to Fig. 3.9, the inductor voltages and capacitor currents during each operating mode are listed in Table 3.1 and 3.2, respectively. The steady-state inductor voltage and current waveforms (i_{L_1} and i_{L_2}) with gate signals of the proposed DISO step-up DC-DC converter are shown in Fig. 3.10 for reference together with the voltages across switches and diodes during steady-state operation.

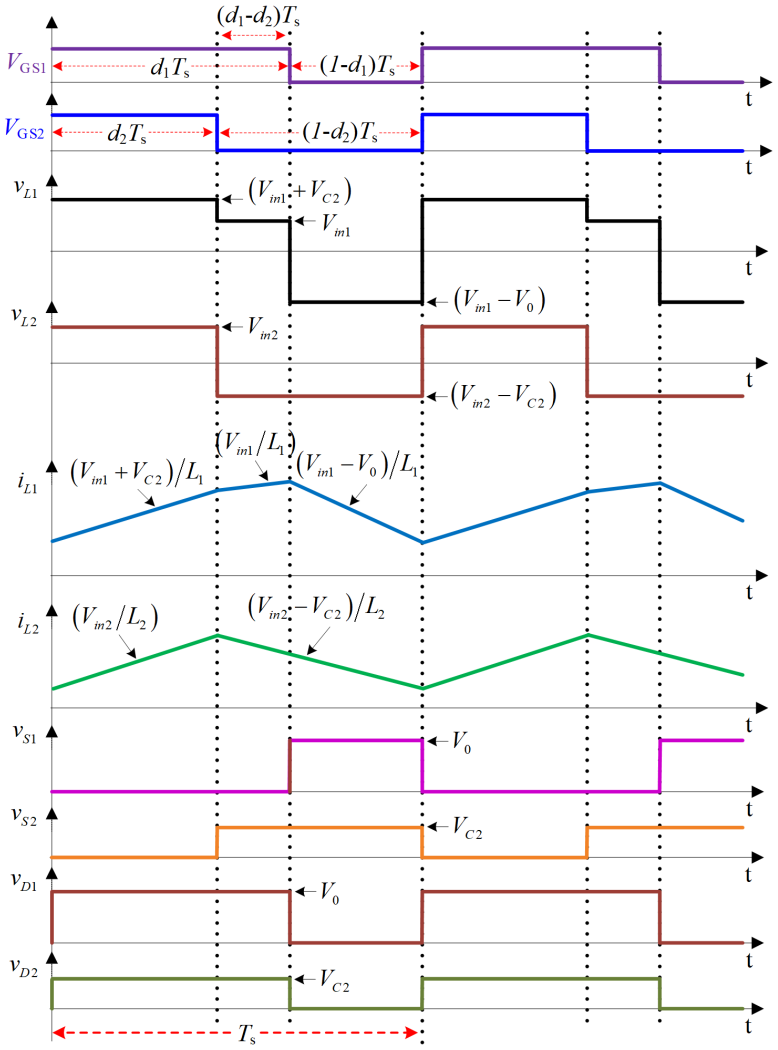


Fig 3.10: Key steady-state waveforms of the proposed DISO DC-DC converter.

Modes	Duration	v_{L_1}	v_{L_2}
Mode 1	d_2T_s	$(v_{in_1}+v_{C_2})$	v_{in_2}
Mode 2	$(d_1-d_2)T_s$	v_{in_1}	$(v_{in_2}\text{-}v_{C_2})$
Mode 3	$(1-d_1)T_s$	$(v_{in_1}\text{-}v_o)$	$(v_{in_2}\text{-}v_{C_2})$

Table 3.1: Inductor Voltages

In steady-state, the average voltages across inductors are zero within one switching period (Ts), commonly known as volt-sec balance. In view of this concept, the following equations can be written for both the inductors (L_1 and L_2).

$$\frac{1}{T_s}\left(\int_0^{d_2T_s} v_{L_1}dt + \int_{d_2T_s}^{d_1T_s} v_{L_1}dt + \int_{d_1T_s}^{T_s} v_{L_1}dt\right) = 0 \tag{3.1}$$

$$\frac{1}{T_s}(\int_0^{d_2T_s} v_{L_2}dt + \int_{d_2T_s}^{d_1T_s} v_{L_2}dt + \int_{d_1T_s}^{T_s} v_{L_2}dt) = 0 \tag{3.2}$$

Modes	Duration	i_{c_1}	i_{c_2}
Mode 1	d_2T_s	$-i_0$	$-i_{L_1}$
Mode 2	$(d_1 - d_2)T_s$	$-i_0$	i_{L_2}
Mode 3	$(1 - d_1)T_s$	$(i_{L_1} - i_0)$	i_{L_2}

Table 3.2: Capacitor currents

Substituting L_1 and L_2 voltages, stated in Table 3.1 into 3.1 and 3.2, the following voltage equations are obtained, respectively.

$$(V_{in_1} + V_{c_2})(d_2) + (V_{in1})(d_1 - d_2) + (V_{in1} - V_0)(1 - d_1) = 0 \tag{3.3}$$

$$(V_{in_2})(d_2) + (V_{in2} - V_{c2})(d_1 - d_2) + (V_{in2} - V_{c_2})(1 - d_1) = 0 \tag{3.4}$$

Solving equation 3.4, the voltage across capacitor C_2 is obtained as:

$$V_{c_2} = \frac{V_{in2}}{(1 - d_2)} \tag{3.5}$$

Now, by substituting V_{C2} in 3.3, the output voltage expression in terms of both the inputs (Vin_1 and Vin_2) is established as follows:

$$V_o = [\frac{V_{in1}}{(1 - d_1)}] + [\frac{d_2V_{in2}}{(1 - d_1)(1 - d_2)}] \tag{3.6}$$

Similarly, the average currents across capacitors are zero within one switching period (T_s). Now by applying capacitor charge balance to C_1 and C_2 , the following equations can be written:

$$\frac{1}{T_s}(\int_0^{d_2T_s} i_{c_1}dt + \int_{d_2T_s}^{d_1T_s} i_{c_1}dt + \int_{d_1T_s}^{T_s} i_{c_1}dt) = 0 \tag{3.7}$$

$$\frac{1}{T_s}(\int_0^{d_2T_s} i_{c_2}dt + \int_{d_2T_s}^{d_1T_s} i_{c_2}dt + \int_{d_1T_s}^{T_s} i_{c_2}dt) = 0 \tag{3.8}$$

Substituting C_1 and C_2 currents, as stated in Table 3.2 in 3.7 and 3.8, the following averaged current equations are obtained, respectively in terms of inductor and load currents.

$$(-I_0)(d_2) + (-I_0)(d_1 - d_2) + (I_{L1} - I_0)(1 - d_1) = 0 \tag{3.9}$$

$$(-I_{L1})(d_2) + (I_{L2})(d_1 - d_2) + (I_{L2})(1 - d_1) = 0 \tag{3.10}$$

Solving 3.10, the following relation between I_{L1} and I_{L2} can be attained.

$$I_{L2} = \frac{d_2}{(1 - d_2)} I_{L1} \tag{3.11}$$

By utilizing 3.11 in 3.9, the I_{L1} or I_{in1} expression can be easily obtained as follows.

$$I_{L1} = I_{in1} = \frac{I_0}{(1 - d_1)} \tag{3.12}$$

Now from 3.11 and 3.12, the expression for I_{L2} or I_{in2} in terms of load current is obtained as equation 3.13.

$$I_{L2} = I_{in2} = \frac{d_2 I_0}{(1 - d_1)(1 - d_2)} \tag{3.13}$$

3.3.2 Design Expressions for Passive Components

Expanding the inductor voltages listed in Table 3.1, the ripple currents through inductors ($\triangle i_{L1}$ and $\triangle i_{L2}$) are established, and using these ripple expressions the design equations for L_1 and L_2 are formulated in 3.14 and 3.15, respectively. Similarly, from the capacitor currents listed in Table 3.1, the ripple voltage ($\triangle v_{c1}$ and $\triangle v_{c2}$) expressions can be easily attained. Using those capacitor voltage ripple equations, the design equations for capacitors (C_1 and C_2) are obtained as specified by 3.16 and 3.17, respectively.

$$L_1 \geq \left[\frac{V_{in1} d_1}{\triangle i_{L1} f_s} + \frac{V_{in2} d_2}{(1 - d_2) \triangle i_{L1} f_s}\right] \tag{3.14}$$

$$L_2 \geq [\frac{V_{in2} d_2}{d_2 \triangle i_{L2} f_s}] \tag{3.15}$$

$$C_1 \geq [\frac{V_0 d_1}{R \triangle v_{c1} f_s}] \tag{3.16}$$

$$C_2 \geq \frac{V_0 d_2}{(1-d_1) R \triangle v_{c2} f_s} \tag{3.17}$$

In order to design the storage elements, the voltage across the capacitors and the current through the inductors need to be considered along with their design criteria presented in 3.14 to 3.17. From the time-domain analysis, the steady-state voltage of capacitors C_1 and C_2 and the current through inductors L_1 and L_2 are obtained and listed in Table III for designing the DISO step-up converter.

Parameters	Values
Voltage V_{in1}	78V
Voltage V_{in2}	108V
Switching frequency f_s	50 kHz
Output Voltage V_o	400V
d_1	0.6
d_2	0.42
Inductor 1	2mH
Inductor 2	800uH
P_0	250W
C_1	220uF, 400V
C_2	100uF, 150V

Table 3.3: Parameter Specifications

3.3.3 Voltage and Current Stress on Semiconductor Devices

The switches and diodes should withstand the maximum voltage and current stresses as per the operating conditions. The maximum capacitor voltage stresses can be obtained from the analysis discussed in Section II. Using these steady-state capacitor voltage expressions, the maximum voltage stresses across switches and diodes are derived as listed in 3.18 to 3.21.

$$V_{S1} = V_0 \tag{3.18}$$

$$V_{S2} = V_{c2} = \frac{V_{in2}}{(1-d_2)} \tag{3.19}$$

$$V_{D1} = V_0 \tag{3.20}$$

$$V_{D2} = V_{c2} = \frac{V_{in2}}{(1-d_2)} \tag{3.21}$$

The maximum current stresses on inductors are obtained using their average values and ripple expressions obtained in section II. The peak current stress on switches and diodes can be obtained using equivalent circuit analysis as detailed below.

$$i_{S1(Peak)} = i_{L1(Peak)} = I_{L1} + [\frac{V_{in1}d_1}{L_1 f_s} + \frac{V_{in2}d_2}{(1-d_2)L_1 f_s}] \tag{3.22}$$

$$i_{S2(Peak)} = (i_{L1(Peak)} + i_{L2(Peak)})$$

$$\Rightarrow I_{L1} + I_{L2} + [\frac{V_{in1}d_1}{L_1 f_s} + \frac{V_{in2}d_2}{(1-d_2)L_1 f_s} + \frac{V_{in2}d_2}{L_2 f_s}] \tag{3.23}$$

$$i_{D1(Peak)} = i_{L1(Peak)} = I_{L1} + [\frac{V_{in1}d_1}{L_1 f_s} + \frac{V_{in2}d_2}{(1-d_2)L_1 f_s}] \tag{3.24}$$

$$i_{D2(Peak)} = i_{L2(Peak)} = I_{L2} + [\frac{V_{in2}d_2}{L_2 f_s}] \tag{3.25}$$

The voltages across both capacitors and both inductor currents are given as follows:

$$V_{C1} = [\frac{Vin1}{(1-d_1)} + \frac{d_2 V_{in2}}{(1-d_1)(1-d_2)}] \tag{3.26}$$

$$I_{L1} = \frac{I_0}{(1-d_1)} \tag{3.27}$$

$$V_{C2} = [\frac{Vin2}{(1-d_2)}] \tag{3.28}$$

$$I_{L2} = [\frac{d_2 I_0}{(1-d_1)(1-d_2)}] \tag{3.29}$$

3.3.4 Loss Analysis and Efficiency Calculation

The sub-optimal elements cause power losses in the proposed DISO DC-DC converter and a power loss computation is necessary to verify the converter's operation

in real-time applications. In order to simplify the analytical computations, the inductor current ripples and capacitor voltage ripples are ignored. The power losses in the proposed DISO topology are mainly from the switches, diodes, inductors, and capacitors. The losses from switches are due to the conduction losses caused by the ON-state resistance and switching losses, from, the turn-ON and turn-OFF intervals. Thus, the total switch losses can be obtained as:

$$P_s = I^2_{S(RMS)} R_{DS} + \frac{1}{2T_s}[I_{s(Peak)} V_s (t_{ON} + t_{OFF})] \tag{3.30}$$

Using 3.30, the power losses from switches S_1 and S_2 can be obtained by using their respective RMS currents, peak currents, and voltage stress expressions. The RMS currents of both switches are given as follows.

$$I_{S1(RMS)} = \frac{I_o \sqrt{d_1}}{(1 - d_1)} \tag{3.31}$$

$$I_{S2(RMS)} = \frac{I_o \sqrt{d_2}}{(1 - d_1)(1 - d_2)} \tag{3.32}$$

The power losses from the diodes are mainly due to the forward voltage drop and forward resistance across it. This can be obtained by using following equation for the diodes.

$$P_D = I^2_{D(RMS)} R_D + V_{Df} I_{D(Avg)} \tag{3.33}$$

The power losses from D_1 and D_2 can be obtained by using the following RMS current and average current expressions.

$$I_{D1(RMS)} = \frac{I_0}{\sqrt{(1 - d_1)}} \tag{3.34}$$

$$I_{D2(RMS)} = \frac{I_0}{(1 - d_1)(1 - d_2)} \sqrt{(d_1 - d_2) + d_2^2 (1 - d_1)} \tag{3.35}$$

$$I_{D1(Avg)} = I_0 \tag{3.36}$$

$$I_{D2(Avg)} = \frac{I_0 d_1}{(1-d_1)} \tag{3.37}$$

Similarly, the corresponding series resistance of inductors and capacitors is responsible for power losses in the passive components, as stated in 3.43 and 3.39.

$$P_L = I^2_{L(RMS)} r_L \tag{3.38}$$

$$P_C = I^2_{C(RMS)} r_C \tag{3.39}$$

The RMS current through inductors are stated in 3.12 to 3.13 and the RMS current through capacitors (C_1 and C_2) are stated in 3.40 to 3.41.

$$I_{C1(RMS)} = I_0 \sqrt{\frac{d_1}{(1-d_1)}} \tag{3.40}$$

$$I_{C2(RMS)} = \frac{I_0}{(1-d_1)} \sqrt{\frac{d_2}{(1-d_2)}} \tag{3.41}$$

Now, the total power loss in the proposed DISO DC-DC converter can be computed as:

$$P_{L_{OSS}} = P_{S1} + P_{S2} + P_{D1} + P_{D2} + P_{L1} + P_{L2} + P_{C1} + P_{C2} \tag{3.42}$$

The efficiency of this power converter is computed using the output power (P_0) and total power losses ($P_{L_{oss}}$) by using the following expression.

$$Efficiency = [\frac{P_0}{P_0 + P_{L_{0SS}}}] * 100 \tag{3.43}$$

3.4 Experimental Results

In order to build a prototype of the proposed DISO converter, the components need to be properly designed for the desired input-output specifications. The output voltage of the converter prototype is 400 V at 350 W and the switching frequency is 50 kHz. The input voltages are V_{in1} = 78 V and V_{in2} = 108 V to generate 400 V

at the output. To select the passive components such as capacitors and inductors, the maximum allowable voltage and current ripples should be less than, or equal to 35% and 5%, respectively. The experimental validation is evaluated using DSP Controller TMS320F28379D as shown in Fig. 3.11

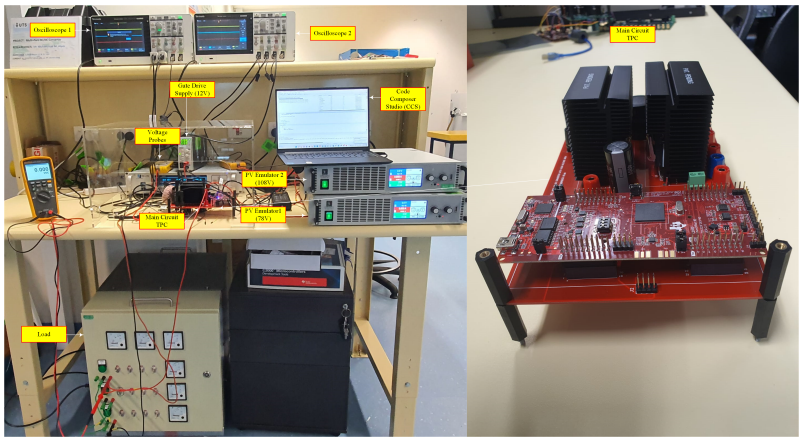


Fig 3.11: Experimental Setup

According to Table 3.2, the duty cycles of both MOSFETs are set to 0.65 and 0.42 with the help of the DSP Controller. Fig. 3.12 shows the gate signals and input voltage waveforms; channel 1 shows the gate-to-source voltage (VGS1) for switch S_1, while the gate-to-source voltage (VGS2) is shown in channel 2. The input voltages of 78V and 108V are shown in channel 3 and channel 4 respectively.

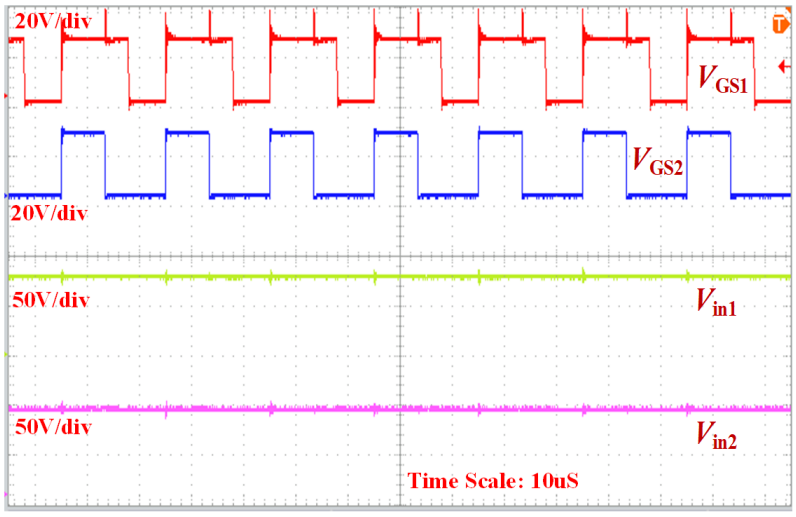


Fig 3.12: Gate signals in channel 1 & 2.
Input voltages waveforms in channel 3 & 4

The output voltage (400V), the output current ,and the inductor current waveforms are shown in channels 1, 2, 3 and 4 in Fig. 3.13 respectively. As mentioned earlier, this converter can provide constant input currents with high voltage gain, as seen in seen in Fig. 3.14 The output voltage (400V), the output current and continuous inductor current waveforms are shown in channel 1, 2, 3 and 4 in Fig. 3.13 and Fig. 3.14 respectively.

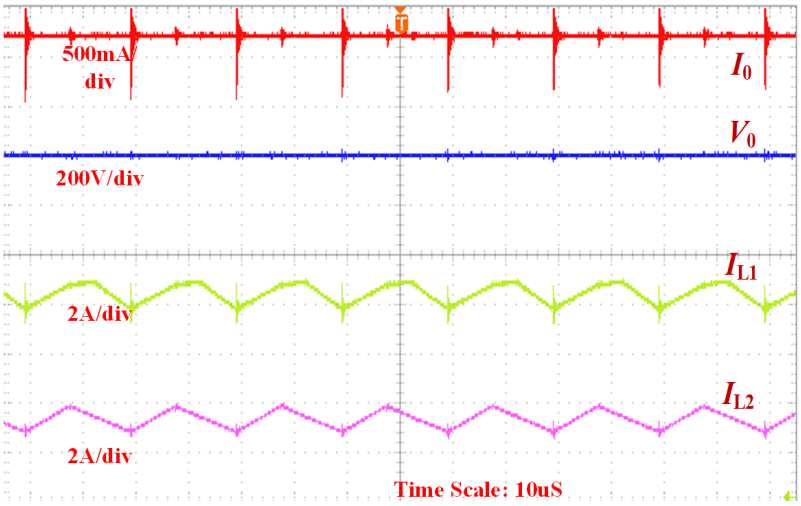


Fig 3.13: Load voltage, load current, and inductor currents waveforms.

As it was mentioned earlier, this converter has an ability of lower stress on MOSFETs as well as the diodes. Therefore, the drain to source voltages (VDS) of both switches S1 and S2 are shown in channel 1 and channel 2 of the Fig. 3.15 Also, the voltages of the diodes D1 and D2 are also shown in channel 3 and channel 4 respectively.

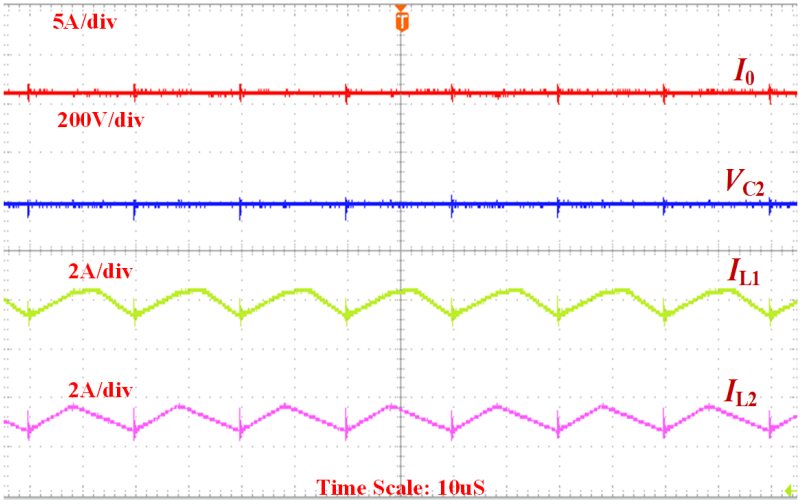


Fig 3.14: Load current, inductor currents, and capacitor C2 voltage waveforms.

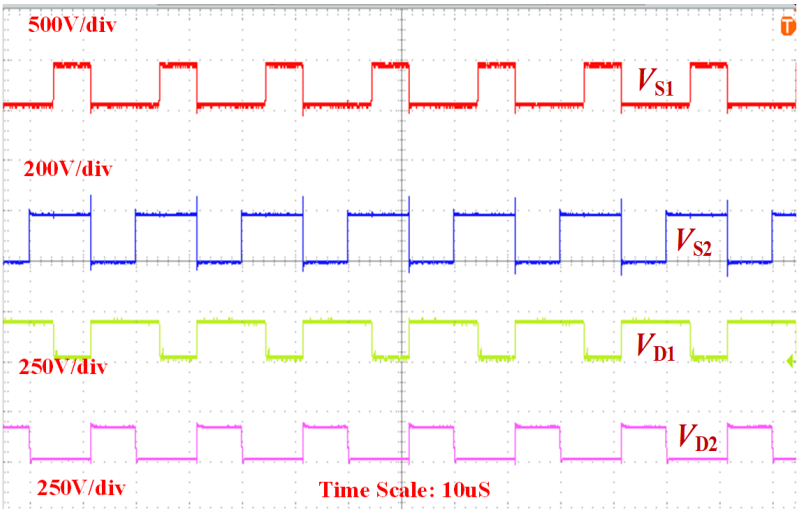


Fig 3.15: Drain to source voltage of S1 & S2 (Channel 1 & Channel 2) Diode voltages of D1 & D2 (Channel 3 & Channel 4) .

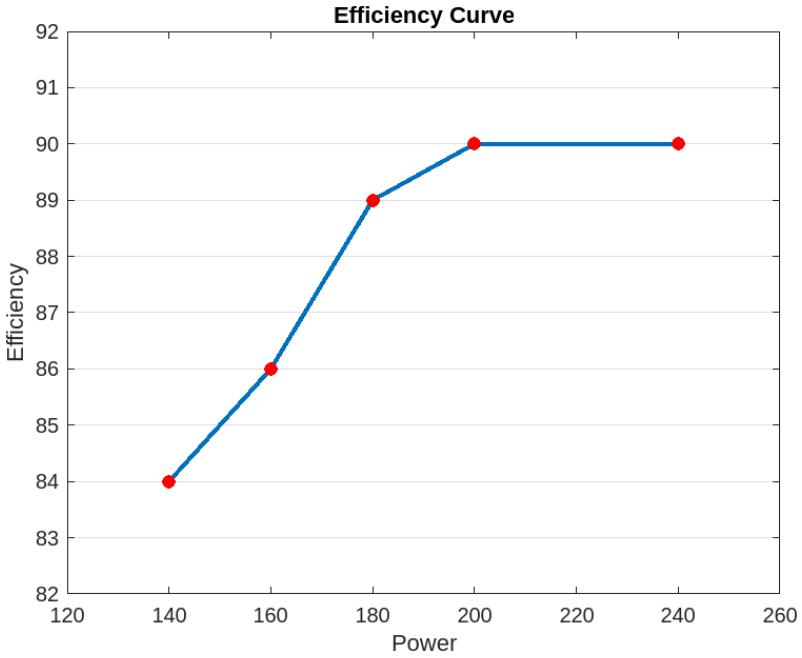


Fig 3.16: Efficiency of the proposed converter

3.5 Summary

In this chapter, a brief comparison for the reported DISO topologies is offered. For a fair comparison with the literature, constraints such as continous input current profile, low number of circuit elements, high output voltage gain and the extension of the current design to other multiport designs have been included. Also, a family novel converters is also discussed. The proposed converter is capable of providing high output voltage and continuous current for both inputs; the mathematical analysis and operational principles are discussed to highlight its key functioning characteristics; and the design criteria of the The L-C components are established through time-domain analysis. Additionally, sample experimental results are presented to validate the converter operation. The simple structure and high voltage gain characteristics make this topology a primary choice for the DC-DC stage in solar grid-tie applications. In the next chapter, the decoupling of power sharing between the dual inputs of the buck converter will be discussed.

Chapter 4

Time Multiplexing and Hysteretic Control for DC/DC Converters

4.1 Introduction

Dual-Input Single Output (DISO) dc-dc power converter architecture is a cost effective solution to applications where multiple input sources are required to be managed with a limited space and cost. However, DISO converters generally present a power sharing issue where the two input sources are not conditioned accurately. This chapter presents a new Time-Multiplexed Hysteretic control (TMHC) scheme for SI-DISO topology to decouple the power sharing among two input sources. Unlike previously reported solutions with discontinous conduction or pseudo continuous conduction operation of the inductor, this chapter focuses on keeping the inductor current in a continuous conduction mode (CCM) and proposed a control scheme with considerably lower ripple current with fast transition time upon switching and higher efficiency. The mathematical proof using the expressions of inductor ripple current, comparison between efficiency and transition time from one level to other is derived. Additionally, a low cost analogue circuitry has been implemented to incorporate the proposed control scheme. Experimental results from the hardware

prototype are given to verify the proposed control scheme.

This chapter is organised as follows. The Section I will discuss the implementation of Time multiplexing technique using hysteretic current control with DCR current sensing method. Section II discusses the literature review related to the control of multiport converters. Section III describes the basic operation principle of the proposed TMC hysteretic control technique and the architecture of the DISO buck converter. Section IV presents the design of the controller. Experimental results are discussed in Section V, followed by the summary in Section VI.

4.2 Literature Review

Single-Inductor Dual-Input Single-Output (SI-DISO) converters have been used for different applications such as battery energy storage, photovoltaic solar energy systems (RES), and electric vehicles (EVs) [40–46]. The SI-DISO converter is a cost-effective option to reduce the size and cost of the converter by using a single inductor as compared to multiple-power-module and multiple-inductor solutions for managing power from different energy sources. However, due to the sharing of the same inductor, the associated converter topologies usually suffer from cross-regulation and power sharing problems.

A power-multiplexed (PM) control scheme has been presented in [47], where the authors tried to completely decouple the operations of multiple outputs in Single-Input Multiple-Output (SIMO) buck converter. Each output is independently regulated upon switching the corresponding output switch. In discontinous conduction mode (DCM), the decoupling can be done by operating the power stage switches relatively at a higher frequency than the output switches. As a result, the cross-regulation between the outputs can be reduced. Based on the operation principle, the authors operated both channels in different modes, i.e, both channels in DCM mode and one channel in CCM mode while the other in DCM mode. The concept can be applied in the applications where both channels are required to operate in CCM

but this technique has a drawback of requiring the inductor current to decrease to zero before charging up for another output branch. This means the inductor current cannot operate fully in CCM.

In short, cross-regulation and power-sharing problems still exist despite of ongoing efforts from researchers. Motivated by the aformentioned challenges of preferred inductor operation and cross-regulation, this chapter proposes a new time-multiplexing hysteretic control (TMHC) technique and applies to a Dual-Input Single-Output (DISO) buck converter. The hysteretic control keeps inductor current in CCM by operating the inductor current in defined bands and completely decouples the two input sources through TMC.

4.3 Circuit Configuration and Operation

Fig. 4.1 shows the simplified circuit diagram of a SI-DISO converter with hysteretic PWM controllers. The input voltage sources V_{dc1} and V_{dc2} are providing power to the output load through a DC/DC converter. These input voltage sources are connected to switches S_1 and S_2 with a single inductor L_o respectively. The controller and sensor for the SI-DISO topology in Fig. 4.1 consists of a comparator with Time multiplexed control (TMC) circuit and DC resistance (DCR) current sensor. In this method, the voltage across the capacitor V_{cf} is proportional to the inductor current. This voltage is then fed as an input to the comparator for hysteretic control. Since the hysteretic control in Fig. 4.1 is not using any external clock or error amplifier to control the switches, therefore there is no need for a compensation circuit to improve the dynamic performance.

The ideal timing diagram of the SI-DISO converter with the proposed TM control scheme is illustrated in Fig. 4.2. As the topology is using hysteretic control, the switching frequency of switches S_1 and S_2 is variable. A time-sharing factor (TSF) has been introduced in the proposed TM control scheme to solve the power-sharing problem, as shown in Fig. 4.2. The TSF helps the controller to supply different in-

puts alternatively in order to achieve more higher control/power conditioning goals. According to the proposed TM control scheme, the TSF should be adjusted in such a way that it determines the switching time slot for each input over a single slot. The proposed control scheme can be further expandable to more than two input ports. An extra schmitt trigger is required to generate the voltage reference for each added input in the circuit.

Fig. 4.2 illustrates the main theoretical waveforms of the TM controlled DISO converter when both of the converters are working in CCM. The figure is divided into different intervals in order to explain the concept and they are explained as follows.

Time Interval 1($t_{10} \sim t_{11}$): During this time interval, the input switch S_1 connected with the first input V_{dc1} is turned on while the switch S_2 remains off. The input voltage V_{dc1} is charging the inductor and causes the inductor current to ramp up.

Time Interval 2($t_{11} \sim t_{12}$): During this interval, the input switch S_1 is turned off while switch S_2 remains off as well. The inductor current discharges into the capacitor to charge and causes the inductor current to ramp down. All the intervals from t_{12} to t_{14} are similar to ($t_{10} \sim t_{11}$) and ($t_{11} \sim t_{12}$).

Time Interval 3($t_{14} \sim t_{20}$): During this interval, the input switch S_1 is turned off while switch S_2 is turned on which is connected with input source V_{dc2}.

Time Interval 4($t_{21} \sim t_{22}$): During this interval, the input switch S_1 is turned off while switch S_2 is turned off.

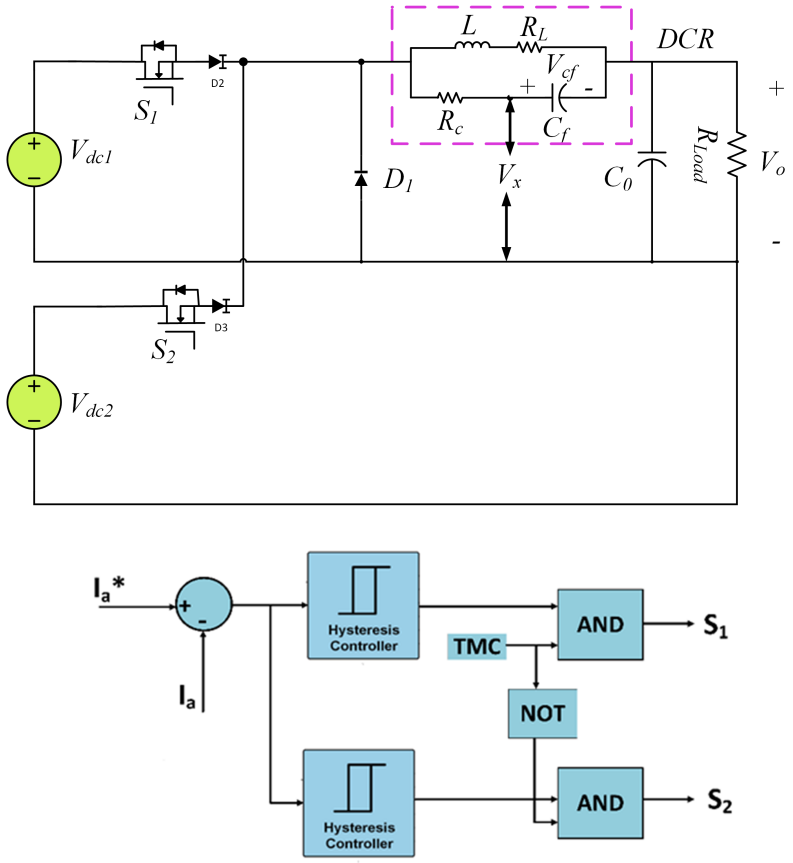


Fig 4.1: Conceptual diagram of DISO DC/DC buck converter.

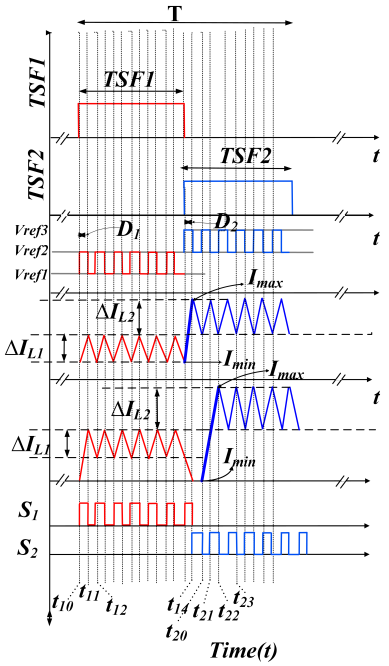
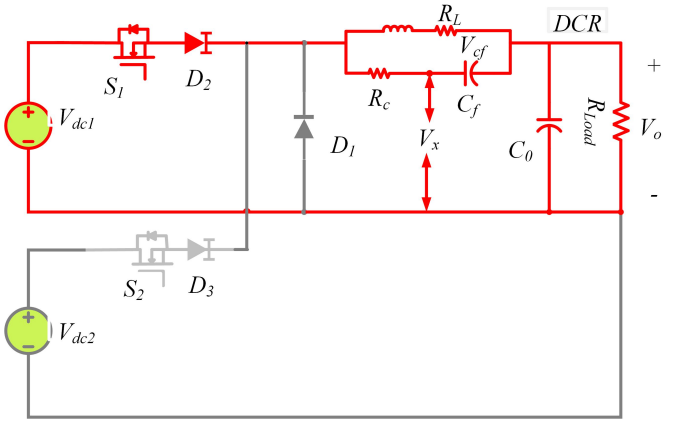
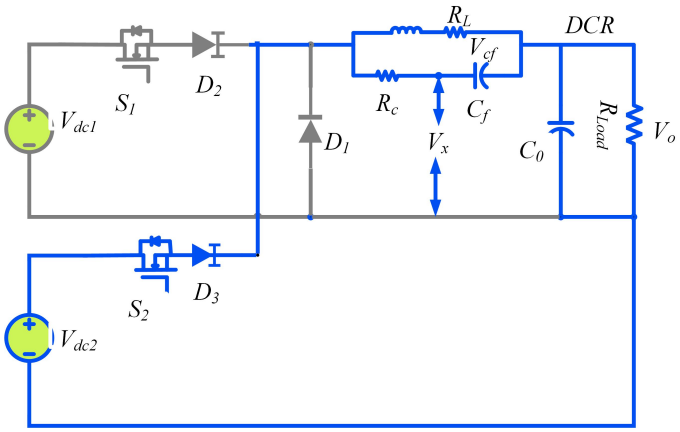


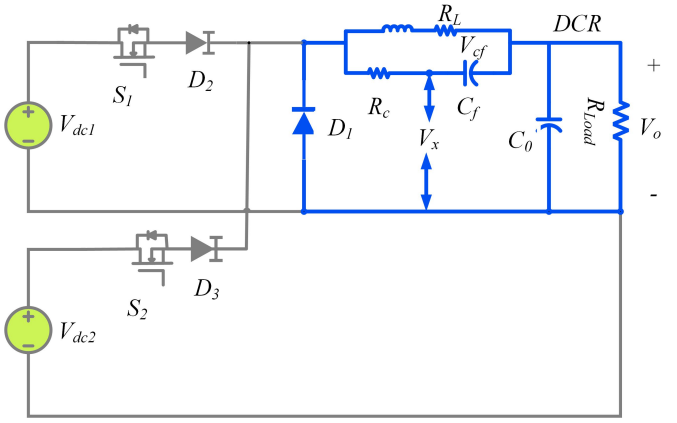
Fig 4.2: Ideal timing diagram of DISO buck converter -T_1 and T_2 show the time multiplexed signals for the switches; -The inductor current of the proposed control method, as shown in the second bottom trace, -The bottom trace shows the wave-shape of inductor current (D.C.M) proposed in [47].



(a) Equivalent circuit when S1 is ON.



(b) Equivalent circuit when S2 is ON.



(c) Equivalent circuit when S1 and S2 is OFF.

Fig 4.3: Equivalent circuits during Time Multiplexing Control

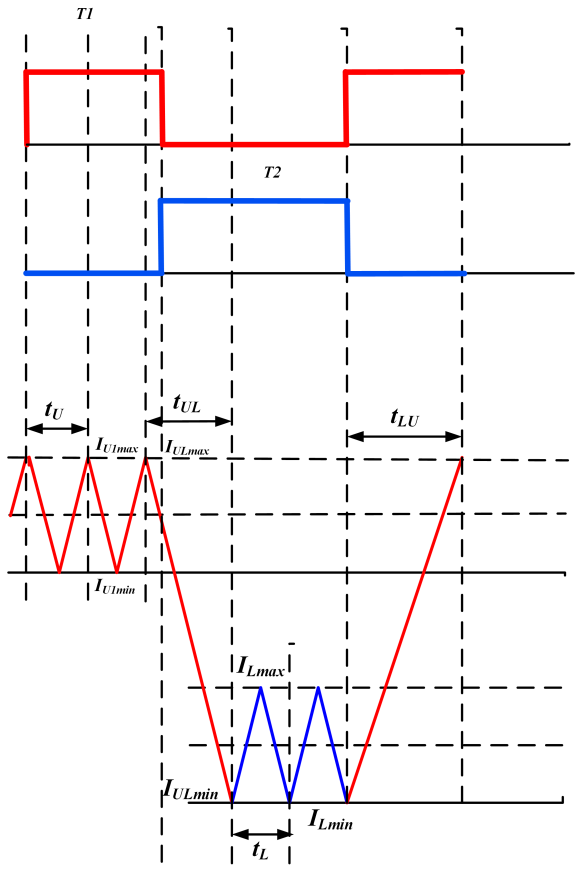


Fig 4.4: Design Example Proposed TMC Control.

4.4 Design of TM Controlled DISO Converter

This section describes and derive the relationships of key circuit parameters and working conditions for the design of the hysteretic controller. The relationships include the relationship between the two switching frequencies with the hysteresis bands and the inductor design equation.

$$\frac{di}{dt} = \frac{V_o}{L} \tag{4.1}$$

$$\Rightarrow \frac{\triangle i}{\triangle t} = \frac{V_o}{L} \Rightarrow \triangle t = \frac{L\triangle i}{V_o} \tag{4.2}$$

From Fig. 4.4, it is evident that both time periods i.e. time period upper to lower "t_{UL}"& time period lower to upper "t_{LU}" are approximately symmetrical, therefore the relation is as follow:

$$t_{UL} \approx t_{LU} = \triangle t = \frac{L\triangle i}{V_o} \tag{4.3}$$

$$L = \frac{Vo(1 - \frac{V_o}{V_i})}{\triangle if} \tag{4.4}$$

As there are two bands, the frequency of upper band is given as:

$$f_1 = \frac{Vo(1 - \frac{V_o}{V_1})}{\triangle i_1 L} \tag{4.5}$$

The frequency of lower band is given as:

$$f_2 = \frac{Vo(1 - \frac{V_o}{V_2})}{\triangle i_2 L} \tag{4.6}$$

To get a relationship between TSF and the inductor for depicted inductor current pattern design example in Fig. 4.4, the equations are as follows:

$$T_{SF} = 2t_u + 2t_L + 2t_{UL} \tag{4.7}$$

$$T_{SF} = \frac{2}{f_1} + \frac{2}{f_2} + 2\frac{L\triangle i}{V_o} \tag{4.8}$$

Substituting (3) & (4) into (7), we get

$$T_{SF} = 2[\frac{\triangle i_1 L}{V_o(1 - \frac{V_o}{V_1})} + \frac{\triangle i_2 L}{V_o(1 - \frac{V_o}{V_2})}] + \frac{2L\triangle i}{V_o} \tag{4.9}$$

$$T_{SF} = \frac{2L}{Vo}[\frac{I_{u1max} - I_{u1min}}{(1 - \frac{V_o}{V1})} + \frac{I_{Lmax} - I_{Lmin}}{(1 - \frac{V_o}{V2})} + I_{uLmax} - I_{uLmin}] \tag{4.10}$$

The equation (9) is the inductor design equation and it also gives the relationship between the TSF and the bands frequency. Next step is to design the controller where the basic building blocks of the proposed TMHC are error amplifier and non-inverting Schmitt trigger, as shown in Fig. 4.5. The Schmitt triggers are built using voltage comparators. For both of the Schmitt triggers, the lower and upper threshold values are governed by (11) and (12) according to [48]:

$$\frac{1}{R_1} = \frac{V_{CC} - V_{TH}}{V_{TH}}(\frac{1}{R_2} + \frac{1}{R_3}) \tag{4.11}$$

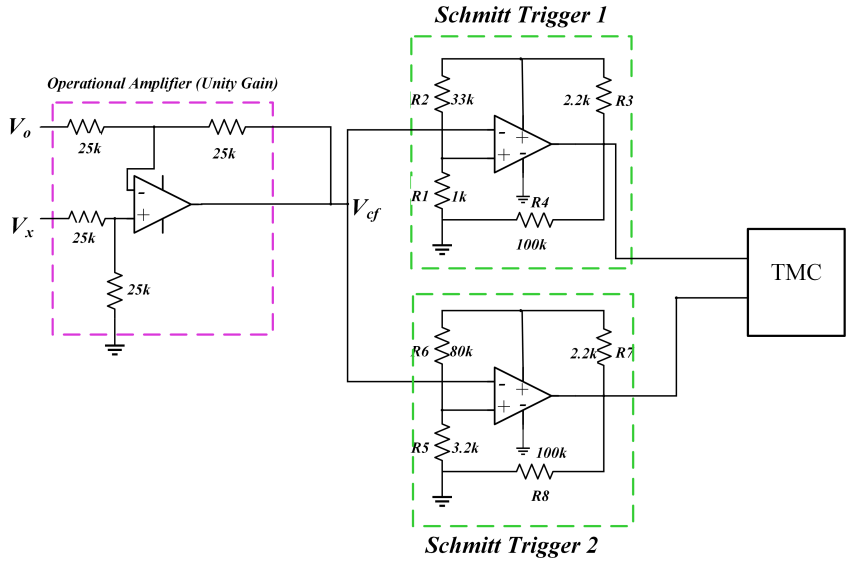


Fig 4.5: Voltage reference design by Schmitt Triggers.

$$\frac{1}{R_2} = \frac{V_{TL}}{V_{CC} - V_{TL}}\left(\frac{1}{R_1} + \frac{1}{R_3}\right) \tag{4.12}$$

After the Schmitt triggers, the next stage of the controller design is a start-up logic. The startup logic can be designed depending upon the output requirement. It includes two AND gates with a NOT gate (depicted in Fig. 4.6) for running the controller smoothly. By using this startup logic along with Schmitt triggers, the proposed control technique easily eliminates the discontinous mode proposed in [47]. The simulation results are shown in Fig. 4.7. The Fig. 4.7 shows the simulation results of the proposed hysteretic control scheme. In Fig. 4.7, the red and green traces show the voltage references created by the Schmitt triggers after sensing the inductor current into voltage and then comparing it with the voltage references. The reason of depicting voltage references in red and green color is to show the successful validation of the proposed idea. As there are two Schmitt triggers in the circuit, therefore the green color waveform is for the voltage reference for first hysteresis band while the red color voltage reference is for the second hysteresis band. In Fig. 4.2 , the timing diagrams for CCM and DCM is shown. The inductor current ramps up at a rate of Vin/L when the switch S1 is ON and ramps down at a rate of -Vo/L when the switch S2 is OFF. In Fig. 4.2 , the red color inductor pattern is showing the switching for S1 while the S2 will be off during this time. Similar inductor

operation is taking place when S2 is on and S1 will be off during this time with the help of time multiplexing control. The inductor current due to V2 when S2 is on is shown in red in Fig. 4.2 . In CCM, the inductor current is not discharging to zero during the transitioning of inductor current changing from one band to another, while in DCM, the inductor current discharges to zero as shown in Fig. 2. Also, the equivalent circuits according to Fig. 4.2 is shown as well in Fig. 4.3(a) to Fig. 4.3(c).

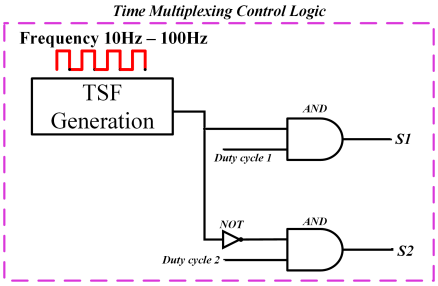


Fig 4.6: Time multiplexing control startup logic.

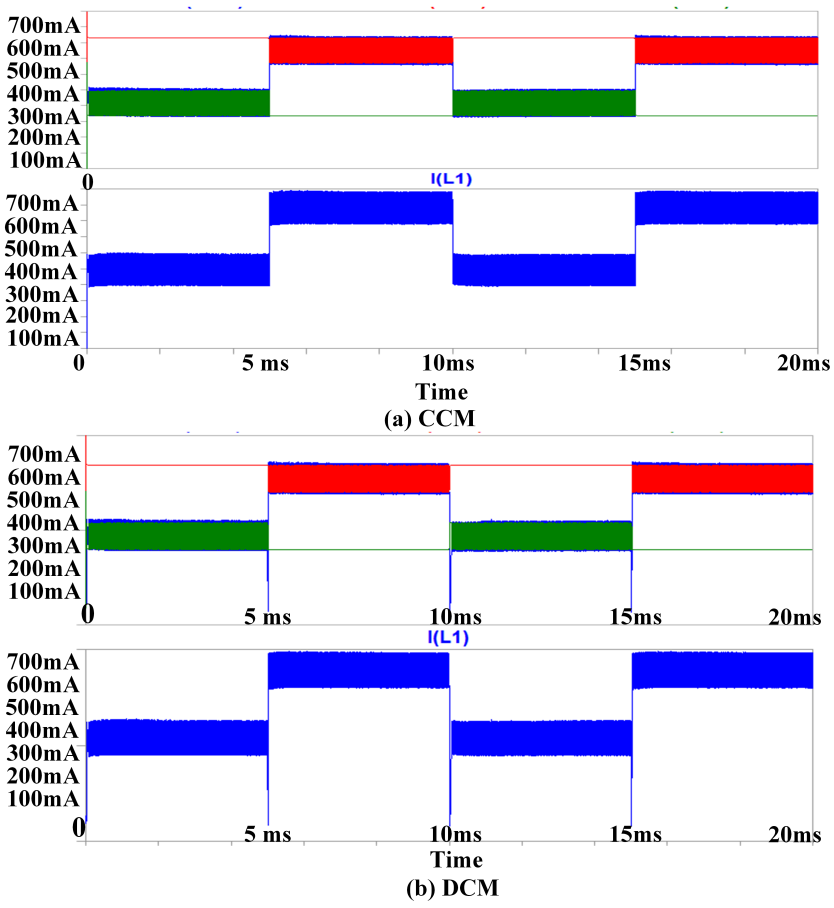


Fig 4.7: LTSpice simulation of two current bands in CCM & DCM respectively.

As there is no discontinuous conduction mode, the proposed control scheme does not requires a current reset time used in [47].

The efficiency and transient response of the converter plays vital role in the overall analysis of any converter. To perform the efficiency comparison between the proposed CCM and the previous DCM control scheme, the circuit is modeled first in Lt-spice and then the results were verified experimentally. All this work will be briefly explained in next section.

Another criterion to prove fast transient response of the proposed time-multiplexed control scheme is the total time in which the current is changing from one level to the other upon switching. The total time for current change from one level to another during time interval ($t_{10} \sim t_{t11}$) given in Fig. 4.2, t is calculated in terms of y(t);

$$y(t) = (I_2 + \frac{\triangle I_{L_{peak2}}}{2}) \tag{4.13}$$

On the other hand, the current is in discontinuous mode during interval ($t_{14} \sim t_{20}$) implying that the current will always start from zero.

$$y(t) = (I_1 - \frac{\triangle I_{L_{peak1}}}{2}) + 2I_2 + \triangle I_{L_{peak2}} \tag{4.14}$$

It can be seen from inspection that the total time depicted in (13) for current moving from one level to another in one cycle is always less than (14) proposed in [47] roughly by 3 times. The proposed total time in (13) will affect the peak current resulting in lower RMS current. The lower RMS current will then cause lower conduction and switching losses which will increase the efficiency of the converter in CCM mode. Also, for the capacitive filter the equation as follows:

$$C = \frac{\triangle I_{L_{peak}} f_s (1 - D)}{8(V_{dc} - V_o) D f_s^2} \tag{4.15}$$

The RMS switch currents S_1 & S_2 for are given as follows.

$$I_{s_{RMS1}} = I_o\sqrt{D_1\left[1+\frac{r^2}{12}\right]} \Rightarrow r = \frac{\triangle I_1}{I_o} \tag{4.16}$$

$$I_{s_{RMS2}} = I_o\sqrt{D_2\left[1+\frac{r^2}{12}\right]} \Rightarrow r = \frac{\triangle I_2}{I_o} \tag{4.17}$$

The voltage stress equations for S_1 & S_2 are given as follows:

$$V_{stress1} = V_{dc1} + V_{D1} \tag{4.18}$$

$$V_{stress2} = V_{dc2} + V_{D2} \tag{4.19}$$

In Fig. 4.2, the current ripple is shown in CCM and DCM respectively. The ripple current equations for CCM and DCM from Fig. 4.2 are given as follows:

$$\triangle i_{rip} = i_{max} - i_{min} \tag{4.20}$$

$$\triangle i_{rip(new)} = (I_2 + \frac{\triangle i_{L_2}}{2}) - (I_1 - \frac{\triangle i_{L_1}}{2}) \tag{4.21}$$

$$\triangle i_{rip(old)} = (I_2 + \frac{\triangle i_{L_2}}{2}) \tag{4.22}$$

From inspection, it can be seen that the proposed ripple current in equation (16) is always less than the ripple current in equation (17) proposed in [47]. This is another contribution of the proposed hysteretic control and it will be validated experimentally in next section.

4.5 Experimental Results

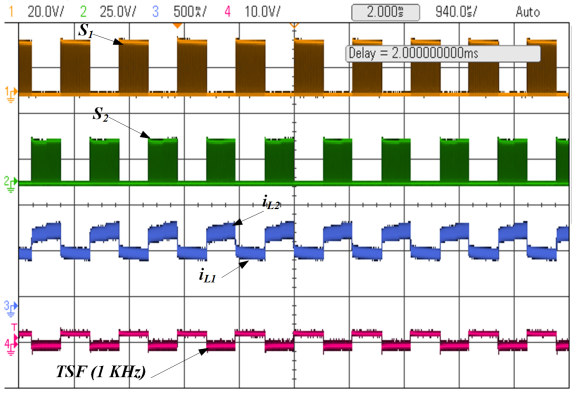
The performance of SI-DISO buck converter with time-multiplexed hysteretic control (TMHC) was evaluated on the setup shown in Fig. 4.9. To perform a comparison for inductor operation in CCM and DCM, the range of TSF and efficiency results

Table 4.1: Design Specifications for SI-DISO Prototype.

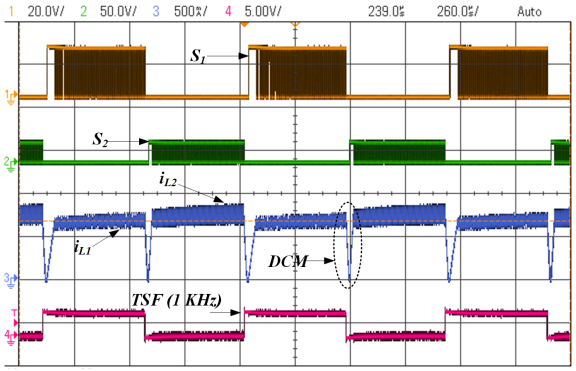
Elements	**Values**
Voltage V_{dc1}	18V
Voltage V_{dc2}	24V
Switching frequency f_s	100 kHz to 150 kHz
Output Current I_o	500 mA
Load	15 Ohm
Inductor	270uH
MOSFET	IRF540Z
Capacitor C_o	100uF
Voltage (Current) Stress S1	19V (330mA)
Voltage (Current) Stress S2	25V (550mA)

are shown in Table 2. The values of the components of the experimental circuit are shown in Table 1 and Fig. 4.5.

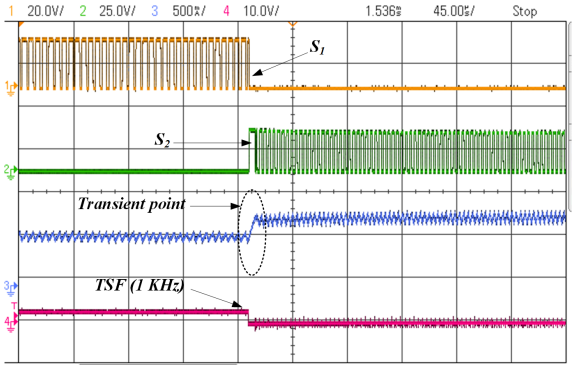
Fig. 4.8(a) shows the TSF, TM gate-drive and inductor current in CCM. Similarly, Fig. 4.8(b) shows the TSF, delayed TM gate-drive and inductor current in DCM. From (10), the critical inductance is L_{cri}=270 uH. As can be seen from Fig. 4.8(a), the inductor current is in CCM while staying in two bands. Also, Fig. 4.8(b) is showing the inductor current in DCM. In order to force the inductor current to DCM, an additional delay circuitry was added in the control circuitry. With this circuit, a delay was added between the time-sharing switching PWM signals to study the efficiency and transient response of the DISO converter in DCM mode. Later on, these results are then compared with the results of CCM current control scheme. During the experiment, it was observed if the same reference values are kept for DCM, then the average output current reduces resulting in a different operating point. In order for fair comparison, it is always mandatory to keep the operating point same in both control schemes. Therefore, the lower band in DCM mode was adjusted by shifting the band level higher so that it will compensate the change in operating point due to DCM. Fig. 4.8(c) is a magnified version of Fig. 4.8(a). It shows the transition of inductor current from lower to upper band upon switching at transient point. This is the proof of the proposed concept to keep the inductor current in CCM with defined bands. Likewise, the Fig. 4.8(d) is the magnified version of Fig. 4.8(b).



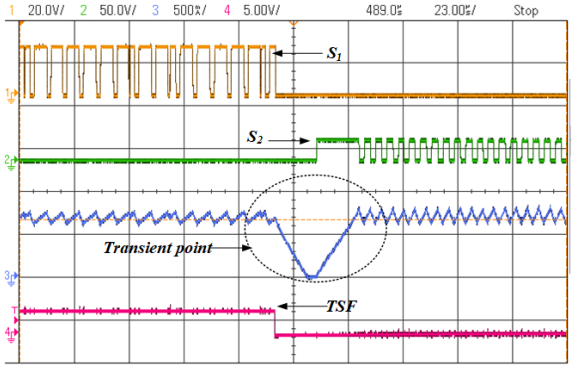
(a) Time base: 940us.



(b) Time base: 260us.



(c) Transition from lower to upper band in CCM.



(d) Transition from lower to upper band in DCM.

Fig 4.8: Key switching wave-forms of the proposed TMHC (a) and (c), and the conventional method (b) and (d). Switch S1 (top trace), Switch S2 (second trace), inductor current in CCM & DCM (third trace) and TSF signal (bottom trace) Time base: 45us & 23us.

This magnified version shows how the additional delay circuitry produced a delay at transient point upon transition from lower to upper band in DCM. This delay contains total three delays in order to enforce the inductor current to reach zero. The first delay is the point where S_1 stops and slope of inductor current start decreasing. So, the first delay was calculated from the decreasing slope of the inductor current when S_1 is off. The second delay is the point where the inductor current touches zero. This delay is not calculated and it is obtained through the additional delay circuitry containing potentiometer and capacitor along with non-inverting schmitt trigger inverter IC. The potentiometer is used to create the zero inductor current scenario for DCM currents. The third delay is calculated when S_1 is off and S_2 is on. The delay can be calculated from the increasing slope of the inductor current. We added all of these three delays in order to get the total delay required to force the inductor current in DCM shown in Fig. 4.8(d).

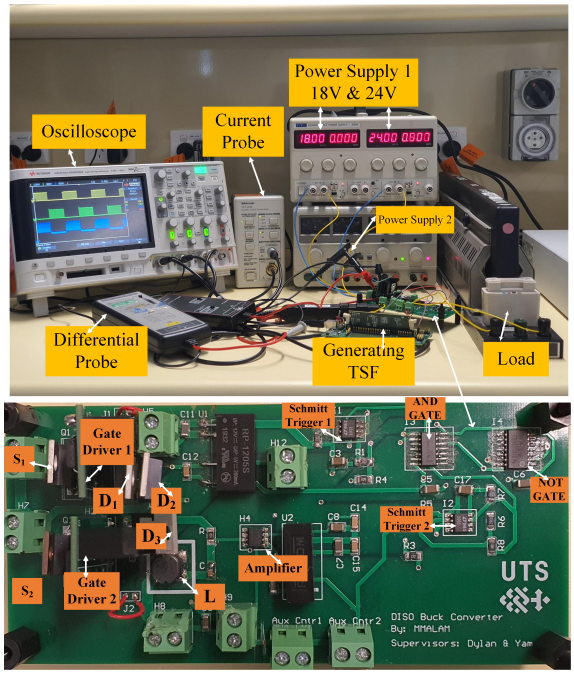
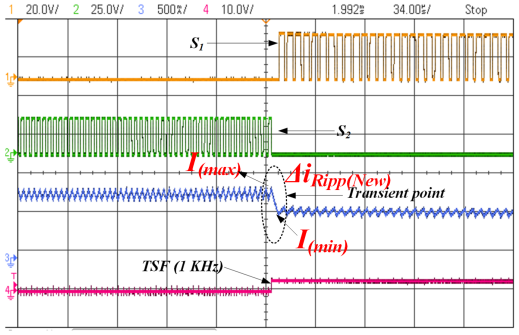
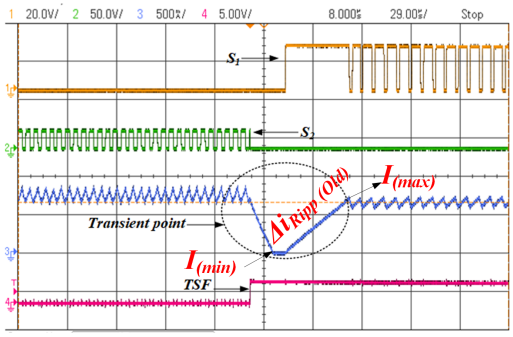


Fig 4.9: Experimental setup and hardware prototype of the proposed TMHC of DISO buck converter.

Fig. 4.10(a) and 4.10(b) are also magnified version of Fig. 4.8(a) and 4.8(b) respectively. The reason of explaining both of these figures is to show how the induc-

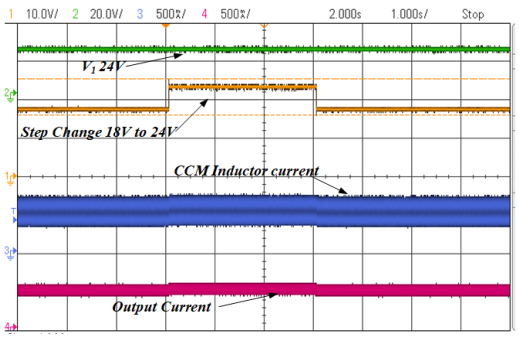


(a) Inductor current's transition: upper to lower band in CCM.

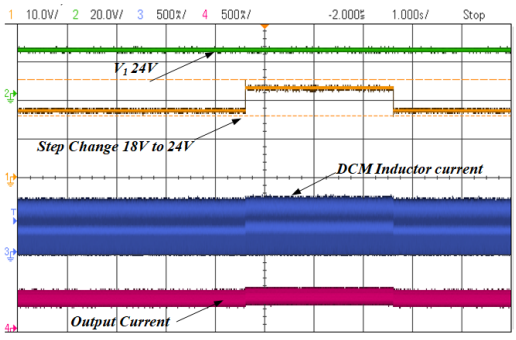


(b) Inductor current's transition: upper to lower band in DCM.

Fig 4.10: Transient responses of proposed control method (a) and conventional method (b). Switch S1 (top trace), Switch S2 (second trace), inductor current in CCM & DCM (third trace) and TSF signal (bottom trace). Time base: 34us & 29us.

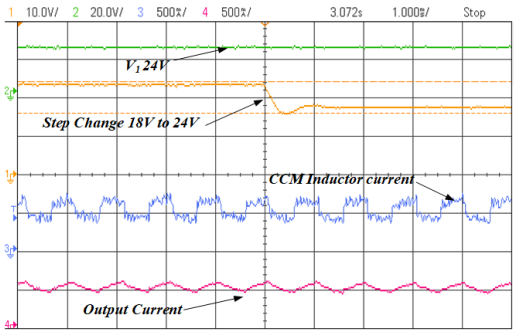


(a) Line change implementation in CCM.

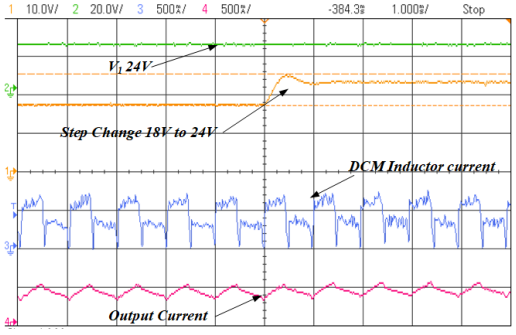


(b) Line change implementation in DCM.

Fig 4.11: Input 1: 24 V (top trace), Line change at Input 2: 18 V to 24 V (second trace), inductor current in CCM & DCM (third trace) and TSF signal (bottom trace). Time base: 1s.

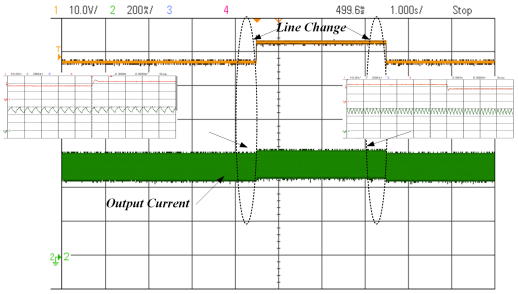


(a) Magnified version: Line change implementation in CCM.

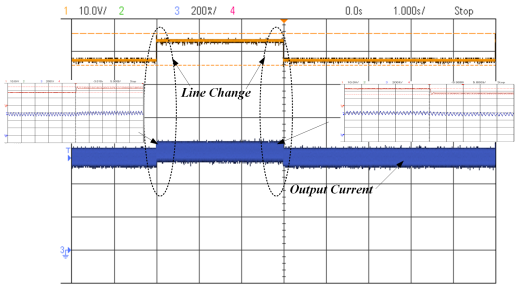


(b) Magnified version: Line change implementation in DCM.

Fig 4.12: Input 1: 24 V (top trace), Line change at Input 2: 18 V to 24 V (second trace), inductor current in CCM & DCM (third trace) and TSF signal (bottom trace). Time base: 1ms.



(a) Magnified version: Line change implementation in CCM.



(b) Magnified version: Line change implementation in DCM.

Fig 4.13: Line Change 18 to 24 V (top trace), Output-current (second trace, Timebase: 1s).

Table 4.2: Comparison of Efficiencies b/w CCM & DCM current control schemes

Experimental Results for Efficiency		
TSF Frequency (kHz)	**Efficiency (DCM)**	**Efficiency (CCM)**
1kHz	89.02%	93.86%
2kHz	91.40%	94.69%
3kHz	93.47%	96.13%
4kHz	94.41%	96.25%

tor current is transitioning from upper to lower band in CCM and DCM at transient point. Both figures show gate drive signals, inductor current either in CCM or DCM and the TSF. The delay in DCM was calculated during transition in the same way as mentioned before. The ripple current has also been shown in Fig. 4.10(a) and 4.10(b). From inspection, it can be clearly seen that the ripple current in CCM is far more less than the ripple current in DCM which is one of the main contribution of this paper and has been proved experimentally.

In the next step, the comparison of conversion efficiency is carried out. To achieve fair comparison, the DISO converter was operated under CCM and DCM modes keeping same input/output parameters and changing the TSF frequency from 1kHz to 4kHz. It has been verified experimentally that the efficiency of DISO converter with the CCM control technique improves by a maximum of 3% as compared to the efficiency with the DCM control scheme. All the results are shown in form of Table 4.2.

As mentioned before, the objective of this study is not only to prove that CCM in DISO converter has higher efficiency but also the transient response of the DISO

converter in CCM is better than DCM control scheme. For this reason, a line change was implemented with the help of programmable DC power supply experimentally. Fig. 4.11(a) and 4.11(b) is showing the line change implementation in CCM and DCM respectively. Fig. 4.11(a) shows a line change of 18 V to 24 V in one of the input ports and the corresponding inductor current in CCM and the TSF. Similarly, Fig. 4.11(b) shows a similar line change scenario for DCM case. The magnified version of line change implementation and the output current in CCM can be seen in Fig. 4.13(a). The figure experimentally validates the output current remains unchanged even if there is a line change occurring at one of the input port, which proves the stability and fast transient response of proposed CCM control scheme. The line change implementation in DCM and output current can be easily seen in Fig. 4.13(b). In this figure, the change in the output current can be easily seen in case of DCM. The system is not as stable as compared to CCM results and the transient response is also not fast enough. The results of the proposed CCM technique have demonstrated the effectiveness of CCM control scheme as compared to the existing DCM technique.

4.6 Summary

In this chapter, an improved control scheme for solving the power sharing problem among the two input sources of DISO buck converter has been proposed. This control scheme decouples the power sharing while maintaining the inductor current in defined bands. For this purpose, hysteretic control scheme has been utilized. A buck-derived SI-DISO power converter has been used with a low-cost analogue circuitry to verify the proposed TMC control. Experimental results demonstrated the effectiveness of proposed converter. In order to prove the effectiveness of proposed control, a delay circuitry was added make the inductor operating in DCM as previously reported. The efficiency and transient response of SI-DISO converter were

compared in CCM and DCM operations experimentally. The experimental results have proved that the proposed TMC scheme has improved the efficiency of the same converter under DCM operation by a maximum of 3%. In addition, the transient response has also improved accordingly. In the next chapter, the fault tolerant design of dual-input buck converter will be discussed.

Chapter 5

Design, Implementation & Reliability Assessment of Novel TPC with Fault Tolerant Ability

5.1 Introduction

This chapter focuses on the fault-tolerant capability of three-port converters (TPCs). A fault-tolerant converter with an effective fault diagnostic technique comprises of generally three stages, including the first stage as fault detection stage, secondly fault isolation stage, and thirdly, the fault reconfiguration stage. The first stage identifies the type of fault, either OCF or SCF. Then, the next stage provides a reconfiguration to the converter assuring uninterruptible power supplies to the load. Fault diagnosis can be done in three different ways, i.e., hardware-based, model-based, and history-based diagnosis [49]. All three types of fault diagnoses are categorized into further subtypes for fault detection. One of these fault diagnostic techniques is the hardware redundancy method, which is a basic, fast and effective way to improve the converter's performance. In this chapter, the hardware redundancy method will be used to proposed fault tolerant multiport dc-dc converter.

This chapter proposed a novel three-port converter with a fault-tolerant (FT) capability to reconfigure automatically under different switching fault conditions, i.e., open circuit fault (OCF) and short circuit fault (SCF) of the power transistors, and to continue achieving different control objectives such as effective battery charging, maximum power point tracking (MPPT) and output voltage regulation. This chapter is organised as follows. Section. I will discuss different FT converter structures and their downsides. Section II will discuss the proposed fault-tolerant design with a one-level redundancy structure enhancing the reliability of traditional three-port converters (TPCs). Experimental results of a laboratory prototype has proven the effectiveness of the proposed. converter. Section III will discuss the reliability assessment of conventional and proposed converter. Section IV will discuss the experimental results followed by the conclusion in Section V.

5.2 Literature review

Multiport DC/DC converters (MPCs) have attracted much attention in the recent decade due to their ability to perform power conditioning and conversion and interface with multiple sources and loads efficiently and simultaneously. They have been applied to DC microgrids [50–53], electric vehicles [54, 55], and renewable energy systems in [56–60]. However, MPCs with an intergrated structure has higher failure rate than the conventional cascased designs. Therefore, there is a genuine need of improved reliability through such as better component selection and fault-tolerance (FT) operation.

Different research studies have presented the fault tolerance, and the necessary remedial actions after the fault occurrence in the power converters [61–66]. According to these studies, the main reason for the converter failure is semiconductor failure, either due to catastrophic fault provoking an abrupt loss of performance or due to a parametric failure because of device aging that causes continuous degradation in semiconductor performance. The degraded converter's performance becomes the

necessity of FT converters.

A non-isolated dc-dc converter with fault-tolerant feature and both step-up/down capability is presented in [61] as shown in Fig. 5.1. It automatically reconfigures itself upon a switch fault to provide an alternative path for continuous converter operation. However, this topology is restricted to two-port applications.

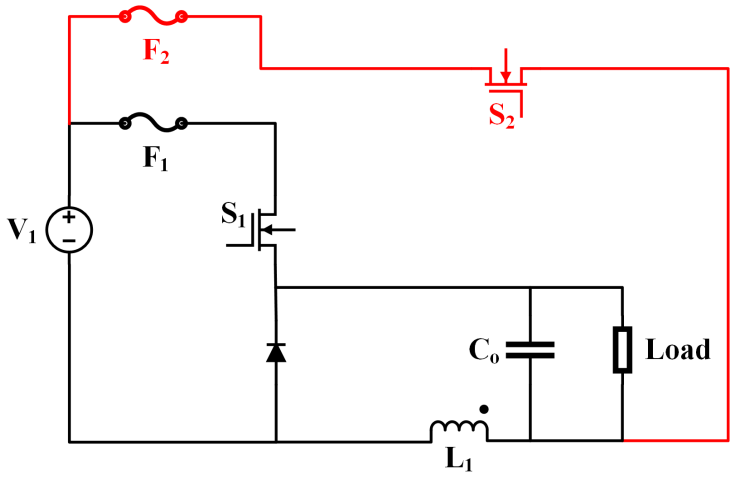


Fig 5.1: Fault tolerant two port converter in [61] .

In [62], an FT TPC with redundant switches is proposed to calculate the reliability of the converter for aerospace applications shown in Fig. 5.2. This converter has an extra redundant switch for each of the main switches in the circuitry.

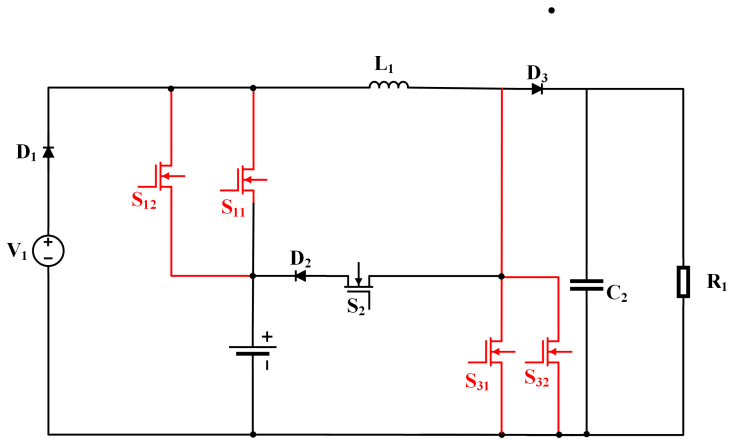


Fig 5.2: Fault tolerant Module in [62] .

Another FT multiport cascaded dc-dc converter has been presented in [63] for PV power generation systems as shown in Fig. 5.3. The main contribution of this

study was the design of the multiple fault-tolerant modules (FTMs) placed between the system's LV and HV sides.

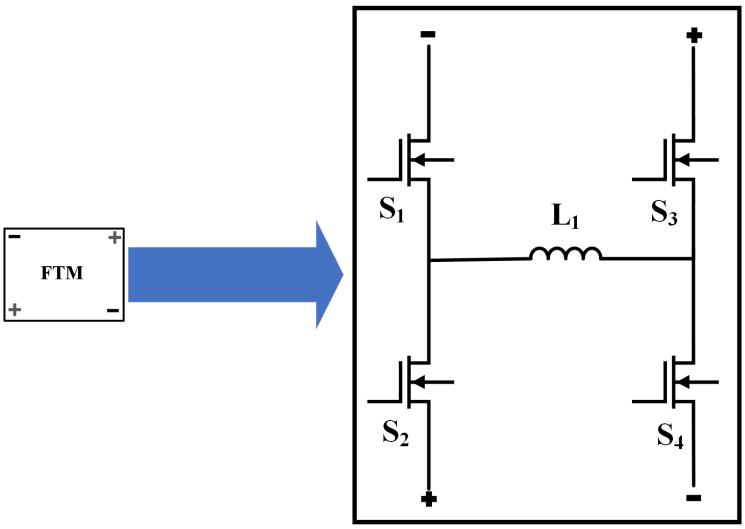


Fig 5.3: Fault tolerant Module in [63] .

A single FTM consists of two main switches, two PWM switches, and one inductor for every PV panel connected on the LV side. Whenever an LVF occurs, both main switches will remain on while the other two PWM switches will turn on complementarily with a 50% duty cycle. The FTM modules working as the buck-boost converter will help hold the actual voltage of the faulty PV submodule, and the remaining submodules are not affected. However, there was no mention of possible OCF or SCF in MOSFETs used either in LLC converter or FT topology itself.

An FT series resonant converter (SRC) using the damaged MOSFET as a conduction path is proposed in [64] as shown in Fig. 5.4.The isolated full-bridge converter has a redundant capacitor leg with a midpoint on the input and output sides. In the case of an SCF at the primary side, instead of a full bridge, the converter reconfigured to keep running as a half-bridge using the faulty MOSFET as a conduction path.The downsides of such approach are potential over-stressing of remaining components post-fault and uncertain characteristics of the damaged MOSFET which may be partially open-circuit like instead of fully short-circuited.

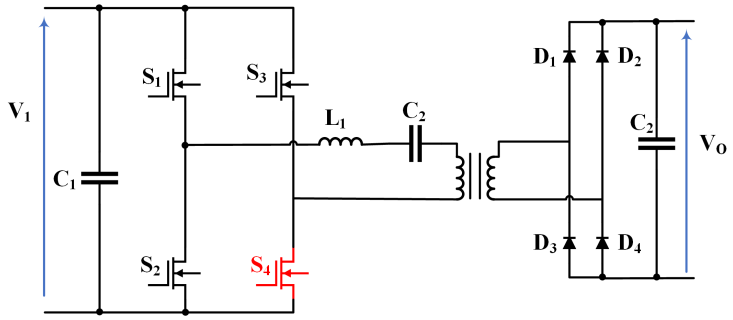


Fig 5.4: FT series resonant converter (SRC) in [64].

These technical downsides have been resolved by a full-bridge series resonant converter (FB-SRC) with a redundant half-bridge circuit proposed in [65] as shown in Fig. 5.5.

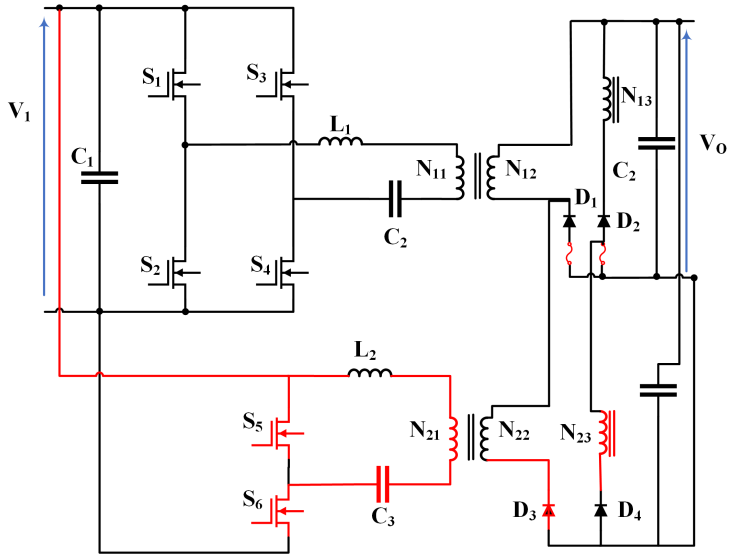


Fig 5.5: FT series resonant converter (FB-SRC) in [65].

In the case of SCF, the proposed converter reconfigures to a half-bridge series resonant converter (HB-SRC) to ensure the output voltage and power remain the same as in the original FB-SRC.

Similarly, a dual-active bridge (DAB) with an abiliity of bypassing the entire full bridge arm on secondary side has been proposed in [66] as shown in Fig. 5.6.

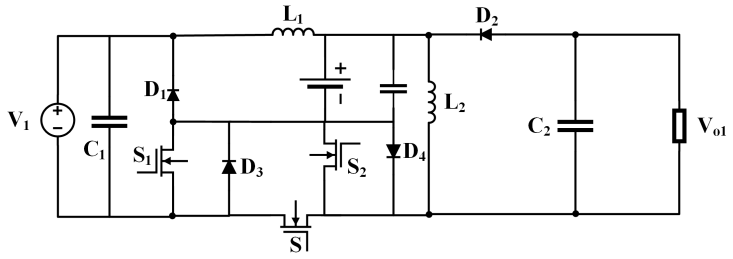


Fig 5.6: Dual-active bridge (DAB) in [66].

However, this converter is not able to handle multiple OCFs and could result in catastrophic malfunction.

5.3 Fault Tolerant Three Port Converter

5.3.1 Proposed Configuration

Fig. 5.7 shows the circuit configuration of a TPC-based DC/DC converter with fault-tolerant capability. The proposed TPC consists of three ports: a bidirectional battery port and unidirectional input and output ports. The PV and the battery are connected to switches S_1 and S_2 through a dual-input buck converter using a single inductor L_1. While the PV is connected to the battery through an extra inductor L_2 along with S_3 and S_4 acting as a boost converter. An extra diode is connected to provide a current path from the PV to the battery in case of a fault.

5.4 Operating Principle of the Proposed FT Converter

The operation modes for the proposed fault-tolerant three-port converter can be described in two conditions, i.e., normal operating conditions and post-fault conditions. This section briefly discusses the working of the converter under both conditions.

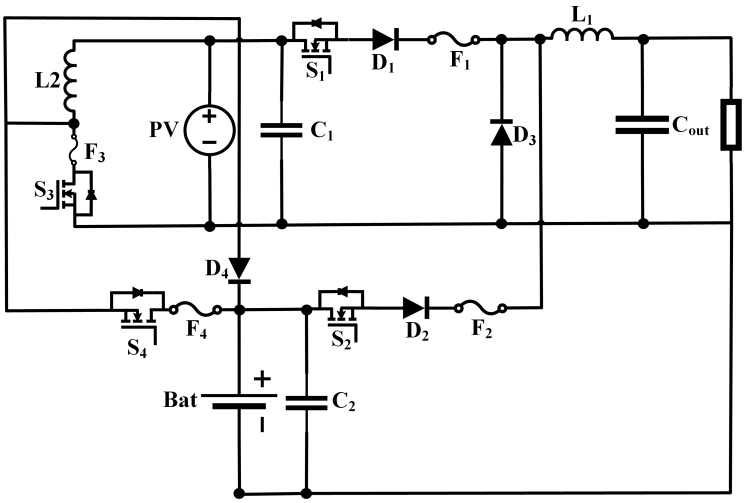


Fig 5.7: Proposed fault tolerant three port converter.

5.4.1 Normal Modes of Operations

1. Mode 1: This mode is SISO mode and it occurs when the PV module starts supplying the power to the load, assuming the battery being the second power source, is either not in service or it does not have enough power to supply the load, as depicted in Fig. 6.4.

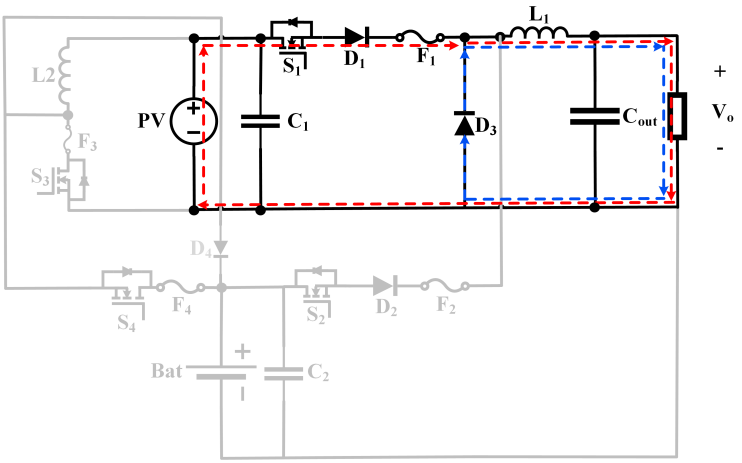


Fig 5.8: Mode 1: S_1 performing OVR (PV-Load).

2. Mode 2: This mode is SISO mode and it starts when the PV module has shading or the PV module is unable to power the load due to insufficient irradiance; therefore the battery takes over to power and sustain the load, as depicted in Fig. 5.9.

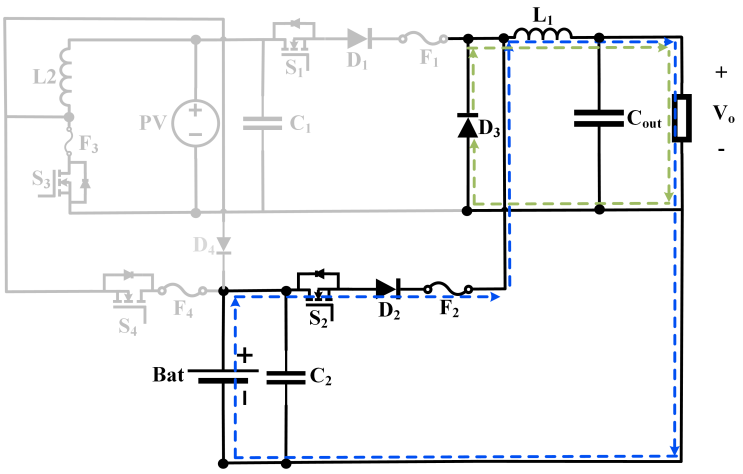


Fig 5.9: Mode 2: S_2 performing OVR (Battery-Load).

3. Mode 3: This mode is the PV+Battery mode and it happens when the PV module has partial shading, or the PV has lower irradiance due to external conditions, and the battery does not have enough power to meet the load demand. Therefore, in this mode, both the battery and the PV supply the power to the load using Time Multiplexing control (TMC), as depicted in Fig. 5.10.

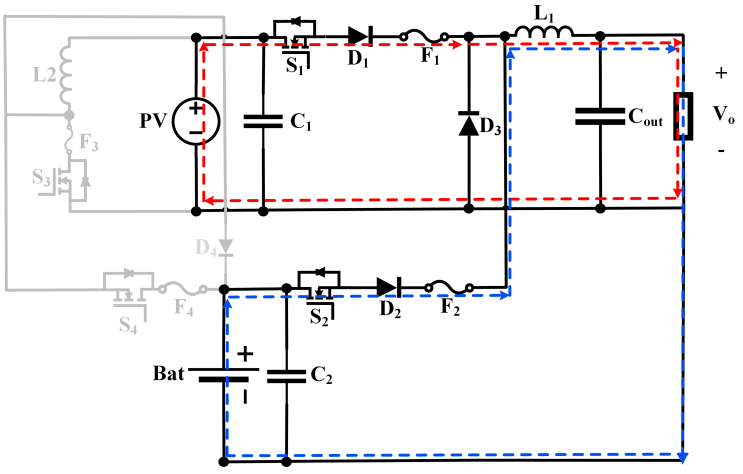


Fig 5.10: Mode 3: S_1 & S_2 performing OVR (PV+Battery-Load).

4. Mode 4: This mode is PV-Battery and Load mode and it will operate when the PV module has more power; however, the load does not require all PV power. Therefore, the excess power is stored in the battery for charging purposes, as depicted in Fig. 5.11.

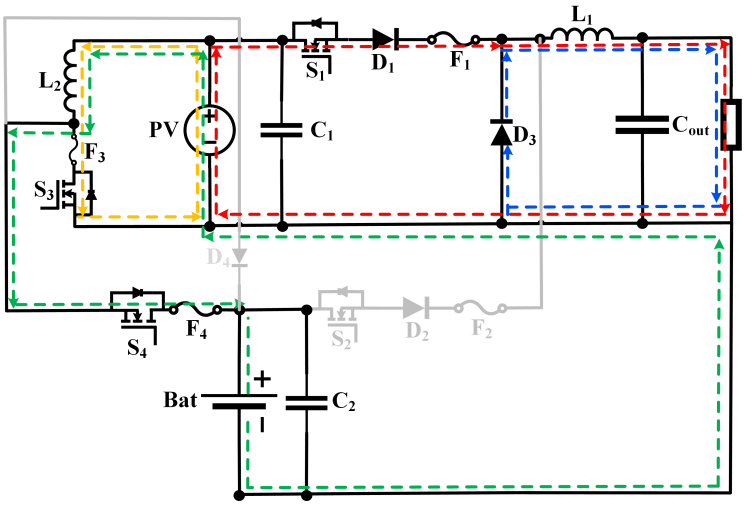


Fig 5.11: Mode 4:S_1 & S_3 performing OVR and Battery Charging (PV-Battery & Load).

5. Mode 5: This is PV-battery mode and it will operate under the no-load condition where the PV module stores the power in the battery, as depicted in Fig. 5.12.

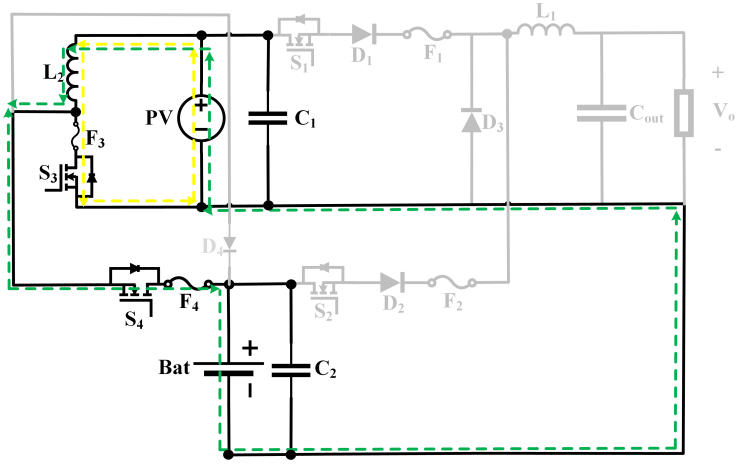


Fig 5.12: Mode 5:S_3 & S_4 performing battery charging (PV-Battery).

5.4.2 Post-Fault Operating Modes (Reconfiguration)

This section explains how the proposed topology can still achieve all targeted objectives, such as output voltage regulation, MPPT, and battery management, despite having a fault at any of the four switches from S_1 to S_4 using the low number of components. It will also show the working of respective fuses, which will isolate

the faulty power switch in case of SCF and prompt the controller to turn on the reconfiguration modes so the entire system may not shut down and keep supplying power to load. The reconfiguration phase due to the failure of any of the power switches is explained as follows:

1. When Switch S_1 is faulty:

   As it is explained earlier, S_1 performs the output voltage regulation in three different modes. If S_1 is at fault due to OCF or SCF, then there will be three different states. Firstly in the case of SCF, fuse F_1 will isolate S_1 from the remaining circuit, and then the reconfiguration will take place in three states as follows:

   - In the first state, Switch S_3 performs MPPT while charging inductor L_2. The battery provides power to the load while S_2 performs output voltage regulation. During this state, S_4 remains off, as depicted in Fig. 5.13.

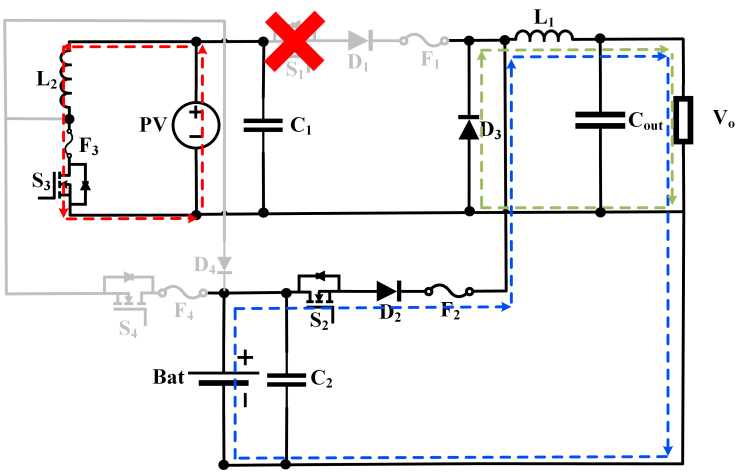


Fig 5.13: State-I.

   - In the second state, a reconfiguration takes place in such a way that the PV module and battery keep supplying power to the load through S_4 and S_2 performing the output voltage regulation. During this mode, S_3 will remain off in this state. This reconfigures the converter to a conventional two-stage cascaded converter, as depicted in Fig. 5.14. The diode D_1 is

reverse biased when S_2 performs output voltage regulation and vice-versa.

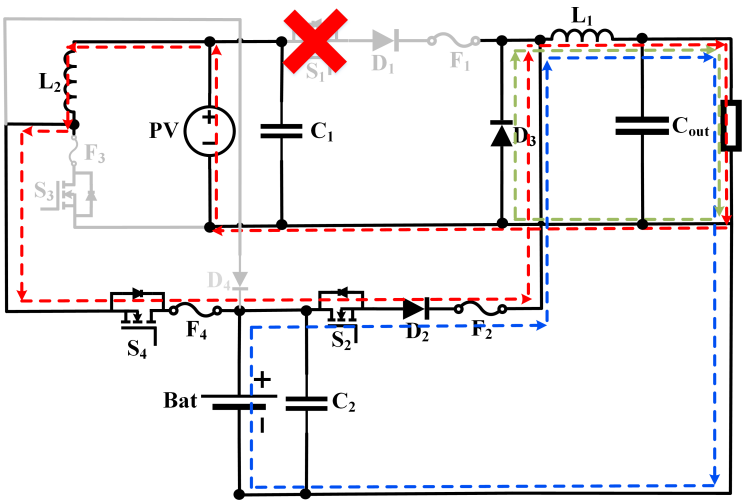


Fig 5.14: State-II.

- In the third state, Switch S_3 is turned off and S_4 is turned on to perform two different objectives depending upon the state of charge (SOC) of the battery. If the battery requires charging, then S_4 operates to charge the battery while S_3 is off, as depicted in Fig. 5.15. If the battery is charged, then S_4 allows the power flow from the PV module through S_4 to S_2 to perform output voltage regulation.

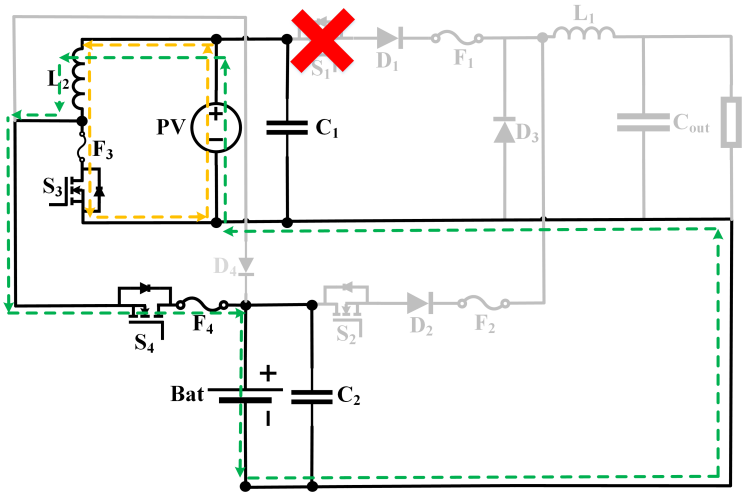


Fig 5.15: State-III.

2. When Switch S_2 is faulty:

Similarly to S_1, if an SCF occurs in S_2, fuse F_2 isolates the switch S_2 from the rest of the circuit and the fault detection will activate the reconfiguration which will take place in three states explained as follows:

- In the first state, Switch S_3 charges inductor L_2 while performing MPPT while the switch S_4 is off in this state, as depicted in Fig. 5.16. Switch S_1 performs the output voltage regulation in this state.

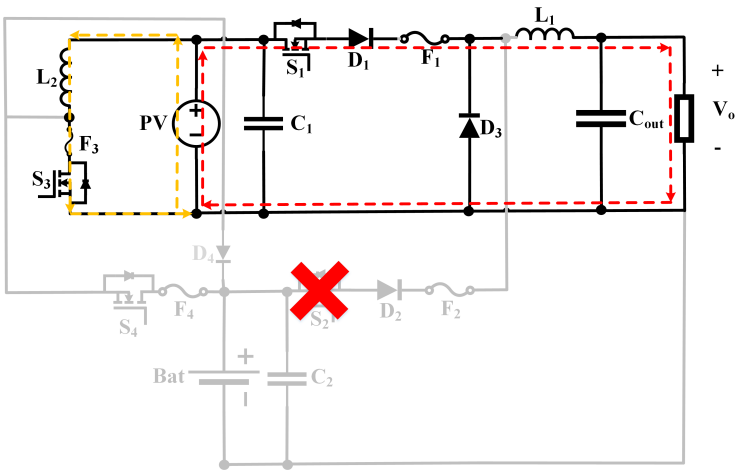


Fig 5.16: When S_2 at fault: State-I.

- In the second state, the power flows from the PV module and battery towards the load through S_4 while S_1 performing the output voltage regulation as depicted in Fig. 5.17. Diode D_4 is reverse biased to prevent backflow of power, and diode D_1 will be reversed biased when S_1 is on and vice-versa. This state can be called a Bi-directional boost/buck.
- In the third state, Switch S_3 is OFF while S_4 is on, which allows the inductor to discharge into the battery and perform battery charging, as depicted in Fig. 5.18. Switch S_1 performs the output voltage regulation in this mode.

3. When Switch S_3 is faulty:

   If a short-circuit fault occurs in Switch S_3, then fuse F_3 isolates S_3 from the remaining circuit. The associated reconfiguration will activate, which is explained as follows:

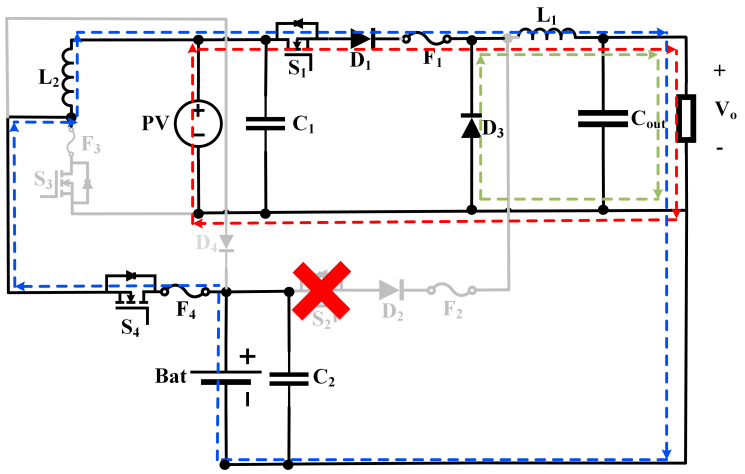


Fig 5.17: When S_2 at fault: State-II.

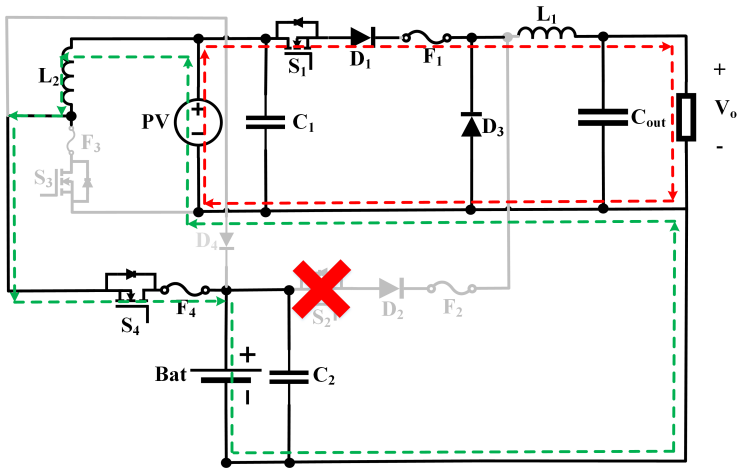


Fig 5.18: When S_2 at fault: State-III.

- When there is a fault on S_3, there will be no MPPT or battery charging. In this case, the power flows from the PV and the battery to the load, while S_1 & S_2 perform OVR in a time-multiplex fashion as depicted in Fig. 5.19. The battery charging will continue until the SOC level of the battery goes lower than the defined threshold. Diode D_4 will be reversed biased in this state.
- In the second state, when the battery requires charging, the PV can do limited battery charging through diode D_4. While S_1 is performing the output voltage regulation, as depicted in Fig. 5.20.

4. When Switch S_4 is faulty:

   Fuse F_4 isolates switch S_4 from the rest of the circuit in case of an SCF event

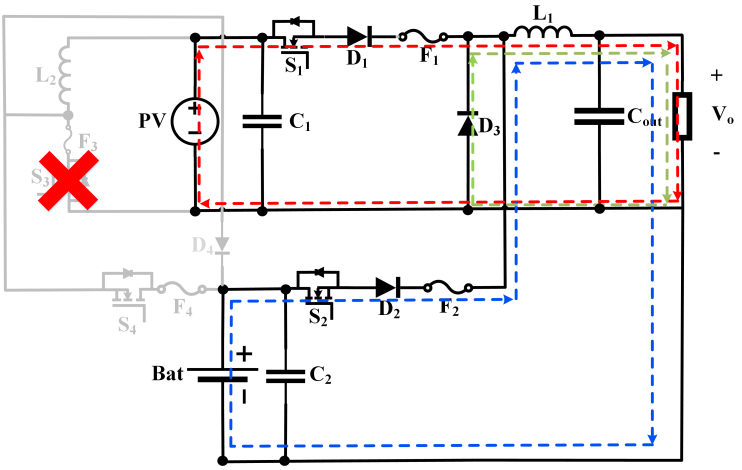


Fig 5.19: When S_3 at fault: State-I.

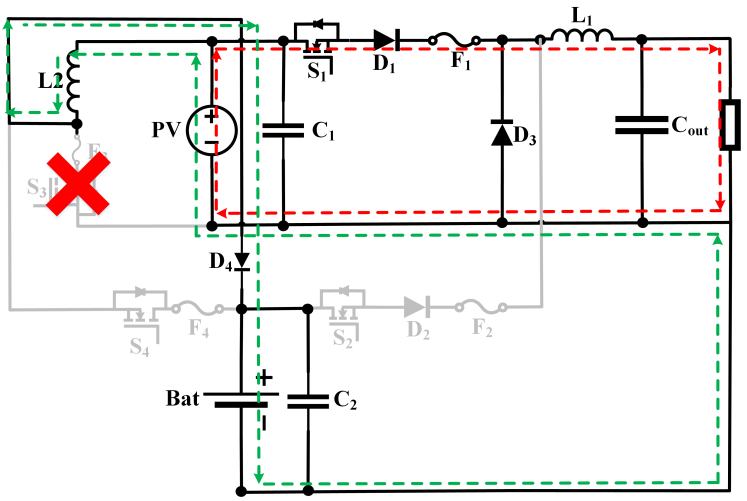


Fig 5.20: When S_3 at fault: State-II.

and activates the reconfiguration as explained as follows:

- In the first state, switch S_1 and S_2 are turned on complementarily with the help of Time Multiplexing Control (TMC), the power will flow from both PV module and battery and S_1 & S_2 performs the output voltage regulation. This mode can be regarded as DISO buck mode, as depicted in Fig. 5.21. Switch S_3 will perform MPPT while charging the L_2, as illustrated in Fig. 5.21. The SCR is off in this mode.
- In the second state, the SCR is turned on and it allows the power flow from PV to battery to perform battery charging, as depicted in Fig. 5.22

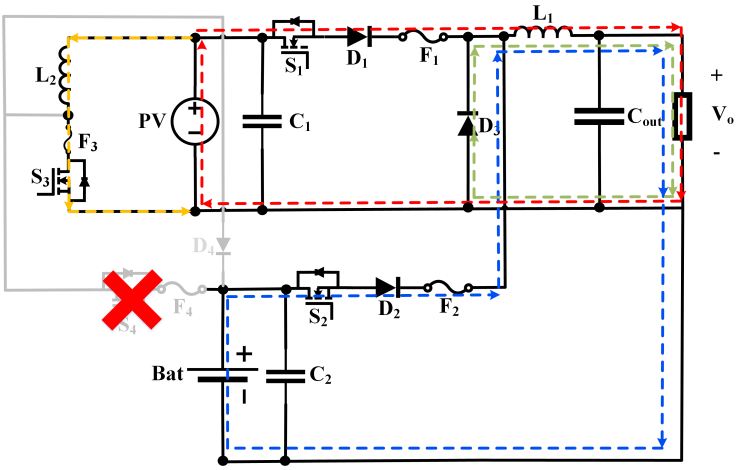


Fig 5.21: When S_4 at fault: State-I.

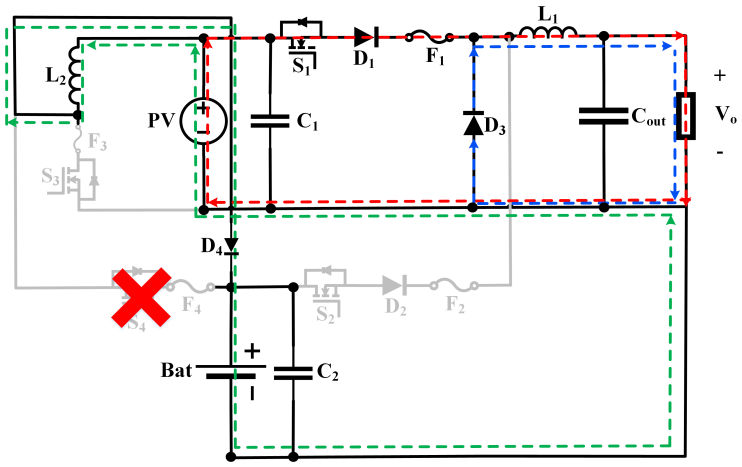


Fig 5.22: When S_4 at fault: State-II.

5.5 Reliability Assessment

This section represents the reliability assessment of the conventional and proposed FT converters using a convenient tool called the Markov model, which is represented by a set of a diagram known as the Markov Chain Model. The different relevant states of the conventional buck or boost and proposed FT buck-boost converter are represented as nodes in circle units, while arrows represent the possible transition states with a particular transition rate. The possible transition states and their associated transition rate helps to calculate the mean time to failure of a component (MTTF) under different experimental conditions. The MTTF can be computed by integrating the reliability function during the time interval from 0 to infinity as

follows:

$$MTTF = \int_0^\infty R(t)d(t) \tag{5.1}$$

This section will compare the MTTFs of conventional buck and boost converter with the proposed FT buck-boost converter. For this comparison, this research will use the probabilities of different transition paths in the Markov chain model derived from [67].

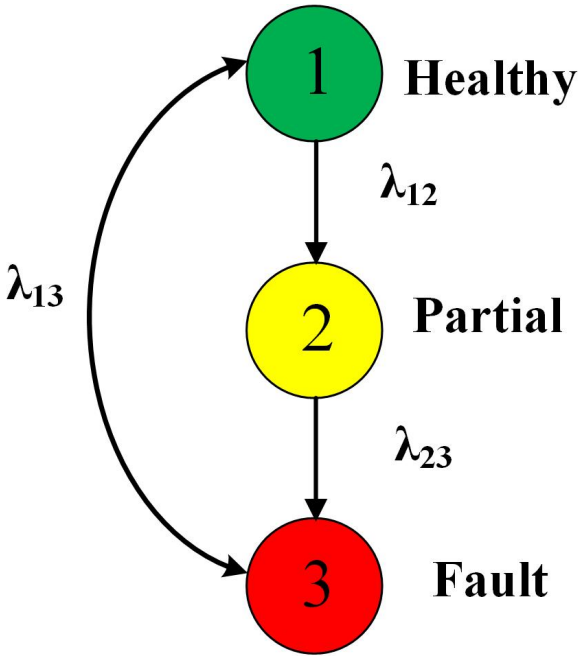


Fig 5.23: Markov chain for conventional converter.

5.5.1 Conventional Buck & Boost Converter

Fig. 5.23 shows the Markov chain model having three states for a conventional buck or boost converter. The first state shows the healthy state of MOSFET when there is no fault, represented by a green circle, while the second state is when the input capacitor or load capacitor of the buck or boost converter is faulty due to transient over-voltage. This state is in yellow and is called a partial fault state. In the Markov chain model, the transition path λ_{12} represents the partial fault from the healthy state to the partial faulty state. In most cases, ceramic capacitors have been used as input or load capacitors due to their high reliability compared to electrolytic

Converter topologies	Markov transition chain of associated converters
Conventional	$\lambda_{12} = \lambda_{C_1} + \lambda_{C_2}$ $\lambda_{13} = \lambda_{S_1} + \lambda_{D_1} + \lambda_{L_1} + \lambda_{C_2} + \lambda_{F_1}$ $\lambda_{23} = \lambda_{S_1} + \lambda_{D_1} + \lambda_{L_1} + \lambda_{C_2} + \lambda_{F_1}$
FT mode 1	$\lambda_{12} = \lambda_{C_1}, \lambda_{24} = \lambda_{S_1} + \lambda_{C_1}, \lambda_{34} = \lambda_{C_2}$ $\lambda_{13} = \lambda_{S_1} + \lambda_{F_1} + \lambda_{D_1}$ $\lambda_{15} = \lambda_{D_1} + \lambda_{C_1} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}}$ $\lambda_{25} = \lambda_{D_1} + \lambda_{C_1} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}}$ $\lambda_{35} = \lambda_{S_1} + \lambda_{D_1} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}} + \lambda_{F_2}$ $\lambda_{45} = \lambda_{S_1} + \lambda_{D_1} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}} + \lambda_{F_1}$
FT mode 2	$\lambda_{12} = \lambda_{C_2}, \lambda_{24} = \lambda_{S_2} + \lambda_{C_2}, \lambda_{34} = \lambda_{C_2}$ $\lambda_{13} = \lambda_{S_2} + \lambda_{F_2} + \lambda_{D_1}$ $\lambda_{15} = \lambda_{D_2} + \lambda_{C_2} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}}$ $\lambda_{25} = \lambda_{D_2} + \lambda_{C_2} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}}$ $\lambda_{35} = \lambda_{S_2} + \lambda_{D_2} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}} + \lambda_{F_2}$ $\lambda_{45} = \lambda_{S_2} + \lambda_{D_2} + \lambda_{D_3} + \lambda_{L_1} + \lambda_{C_{out}} + \lambda_{F_2}$
FT mode 3	None
FT mode 4	$\lambda_{12} = \lambda_{C_1}, \lambda_{24} = \lambda_{S_4}$ $\lambda_{13} = \lambda_{S_4} + \lambda_{F_4}$ $\lambda_{15} = \lambda_{S_3} + \lambda_{C_1} + \lambda_{L_2} + \lambda_{C_{out}}$ $\lambda_{25} = \lambda_{S_3} + \lambda_{C_2} + \lambda_{D_3} + \lambda_{L_2} + \lambda_{C_{out}}$ $\lambda_{35} = \lambda_{C_1} + \lambda_{D_4} + \lambda_{L_2} + \lambda_{C_{out}}$ $\lambda_{45} = \lambda_{C_1} + \lambda_{D_4} + \lambda_{L_2} + \lambda_{C_{out}}$

Table 5.1: Markov transition chain

capacitors; therefore, the probability of partial fault due to input or load capacitor is as low as zero [61]. Even though in case of a partial fault, the faulty input or load capacitor can be removed, and the converter can still operate with an increased voltage ripple in a steady state. The third state is in red, where any of the crucial components of the converter are faulty, including MOSFET, diode, load capacitor or inductor, leading to a full system failure. This state is called the absorption state and is the end of the Markov chain model. The transition path, λ_{13}&λ_{23} indicates the transition from either a healthy or partial state to the absorption state.

A summary of all the transition paths with the associated transition rates in conventional buck or boost and proposed buck-boost converter is given in Table I. In Table I, the failure rates of the MOSFET (as represented by λ), inductor, input capacitor, output capacitor, diodes and fuses are represented by $\lambda_{S_1}, \lambda_{C_1}, \lambda_{D_1}, \lambda_{L_1}, \lambda_{C_o}$&$\lambda_{F_1}$ respectively.

This can be represented by taking a derivative of the probability function from Fig. 5.23 as follows:

$$\frac{\mathrm{d}P}{\mathrm{d}t} = M \times P \tag{5.2}$$

The probability of staying in state "k" at time "t" is denoted by $p_{k(t)}$ [68]. The probability of each state changes over time as follows:

$$P_{k+1} = M \times P_k \triangle t + P_k \tag{5.3}$$

According to Markov chain model for conventional buck converter and boost converter, the probability transition matrix M_{buck} and M_{boost} are as follows:

$$M_{buck} = \begin{bmatrix} -(\lambda_{13}+\lambda_{12}) & 0 & 0 \\ \lambda_{12} & -\lambda_{23} & 0 \\ \lambda_{13} & \lambda_{23} & 0 \end{bmatrix} \tag{5.4}$$

$$M_{boost} = \begin{bmatrix} -(\lambda_{13}+\lambda_{12}) & 0 & 0 \\ \lambda_{12} & -\lambda_{23} & 0 \\ \lambda_{13} & \lambda_{23} & 0 \end{bmatrix} \tag{5.5}$$

In case of both conventional buck and boost converters, it is assumed that initially the converter's components are healthy, therefore the probability of P_0 can be written as

$$P_0 = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{5.6}$$

According to 5.2, the derivative of the probability function of both conventional converters will be the same as follows:

$$\frac{d}{dt}\begin{bmatrix} P_1(t) & P_2(t) & P_3(t) \end{bmatrix} = \begin{bmatrix} -(\lambda_{13}+\lambda_{12}) & 0 & 0 \\ \lambda_{12} & -\lambda_{23} & 0 \\ \lambda_{13} & \lambda_{23} & 0 \end{bmatrix} \times \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{5.7}$$

The reliability of the conventional buck and boost converters can be find out by following equations:

$$R(t) = P_0(t) + P_1(t) + P_2(t) \tag{5.8}$$

The MTTFs of both conventional buck and boost converters can be find out using MATLAB and similarly, the reliability curve is shown for the conventional converters in Fig. 5.24.

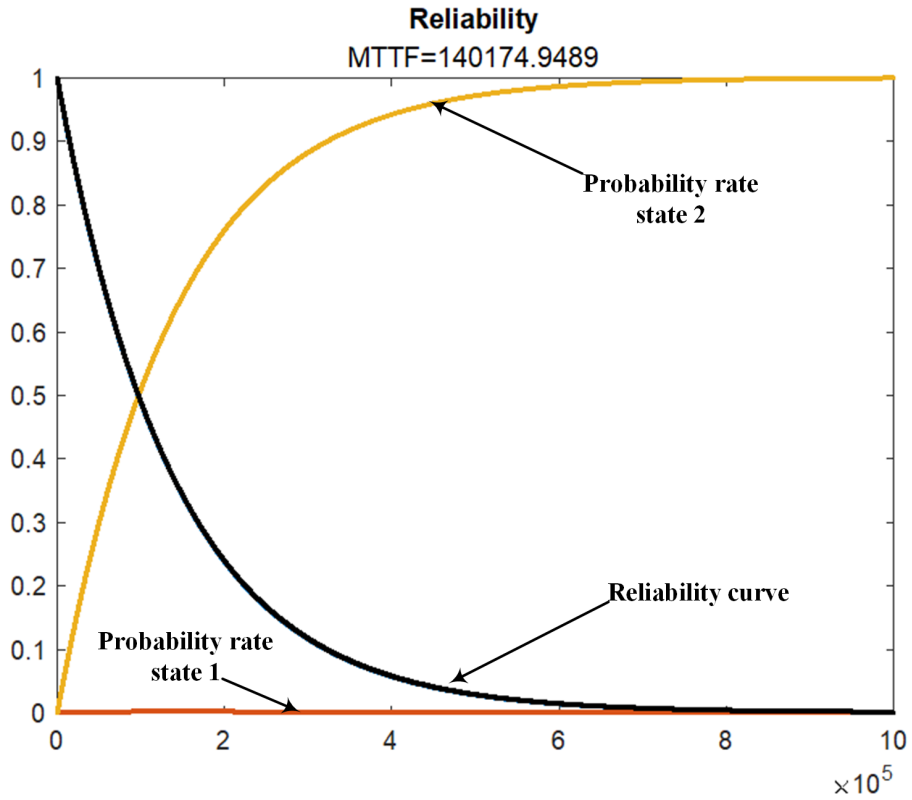


Fig 5.24: Reliability & state probability curves for conventional converter.

5.5.2 Proposed FT Buck-Boost Converter

In this section, the reliability assessment for the proposed converter is performed for all the possible fault scenarios.

5.5.3 Reliability assessment when S_1 or S_2 is faulty

As both S_1 & S_2 are parallel to each other; therefore their reliability will be the same. The corresponding Markov chain model for fault at S_1 or S_2 will also be same and shown in Fig. 5.25.

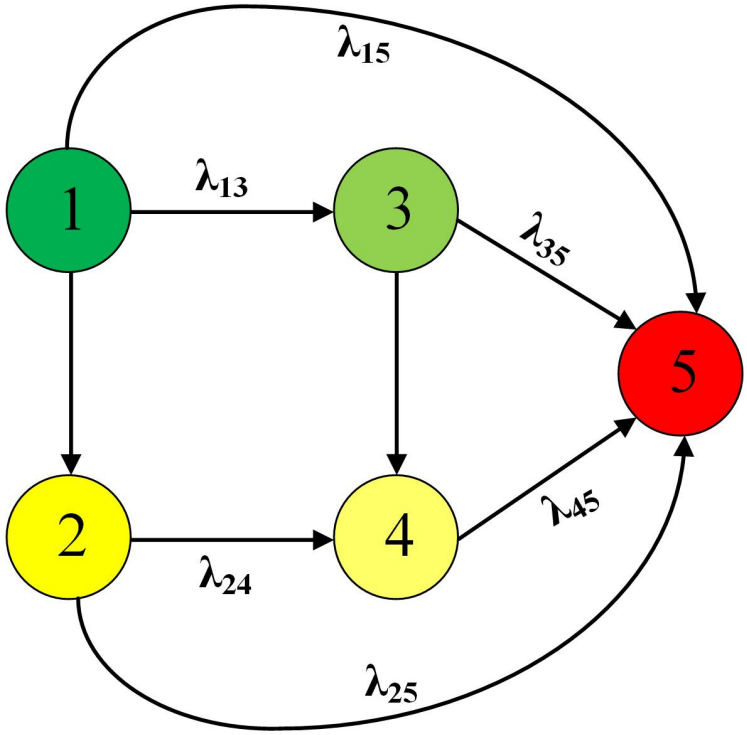


Fig 5.25: Markov chain when S_1 or S_2 is faulty.

The Markov chain model can be divided into five possible states with eight different transition paths having different transition rates. In a healthy state, the converter was providing voltage to load under buck mode, while depending on the SOC level of the battery, the left side of the converter was performing either MPPT or battery charging. The transition path λ_{13} indicates the scenario when the FT converter reconfigured from single-stage buck operation to parallel single-stage buck-operation when S_1 fails and the fuse F_1 blows. Here it is important to observe that the switch S1 failure does not enforce the converter to absorption state 5 due to the multi-port structure having a parallel switch S_2. The transition paths with transition rate $\lambda_{12}\&\lambda_{34}$ represent the transition of buck operation mode from a healthy state to a partial fault state, where there is a partial fault in C_1 in state 1 or state 3 but the corresponding MOSFET is still healthy. At this stage, the converter is suffering from a partial fault, but it is still operational with the increase in voltage ripple at steady-state conditions.

Moreover, λ_{24} shows the transition from state 2 to state 4 with the fault in S_1 due

to transient over-voltage. The converter will move to absorption state 5 through any of the four associated transition paths λ_{15}, λ_{25}, λ_{35} and λ_{45}. The transition paths λ_{35} & λ_{45} refer to the failure of parallel switch S_2 from healthy and partial fault states to the final absorption state, respectively. Furthermore, the transition paths λ_{15} & λ_{25} represents the single-point failure scenario from L_1, C_1, D_3 & D_1. The transition paths and associated transition rates are represented in Table. I. The transition matrix of the proposed FT converter under fault at switch S_1 can be modeled as follows:

$$dP = (M_{S_1} \times P)dt \tag{5.9}$$

Also, the probability of the states staying in state "k" with time "t" is given as follows:

$$P_{k+1} = M_{S_1} \times P_k \triangle t + P_k \tag{5.10}$$

Here the probability of state P_0 is already known as initially the converter is healthy, therefore the initial probability will be added for computing the probability of remaining four states using equation 10.

$$P_0 = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{5.11}$$

The probability transition matrix in this case as given as follows:

$$M_{S_1} = \begin{bmatrix} -(\lambda_{12}+\lambda_{13}+\lambda_{12}) & 0 & 0 & 0 & 0 \\ \lambda_{12} & -(\lambda_{24}+\lambda_{25}) & 0 & 0 & 0 \\ \lambda_{13} & 0 & -(\lambda_{34}+\lambda_{35}) & 0 & 0 \\ 0 & \lambda_{24} & \lambda_{34} & -\lambda_{45} & 0 \\ \lambda_{15} & \lambda_{25} & \lambda_{35} & \lambda_{45} & 0 \end{bmatrix} \tag{5.12}$$

The reliability of the proposed FT converters can be find out by following equations:

$$R_1(t) = P_0(t) + P_1(t) + P_2(t) + P_3(t) + P_4(t) + P_5(t) \tag{5.13}$$

The MTTFs of proposed FT converter under fault at S_1 or S_2 can be find out using MATLAB and similarly, the reliability curve is shown in Fig. 5.26.

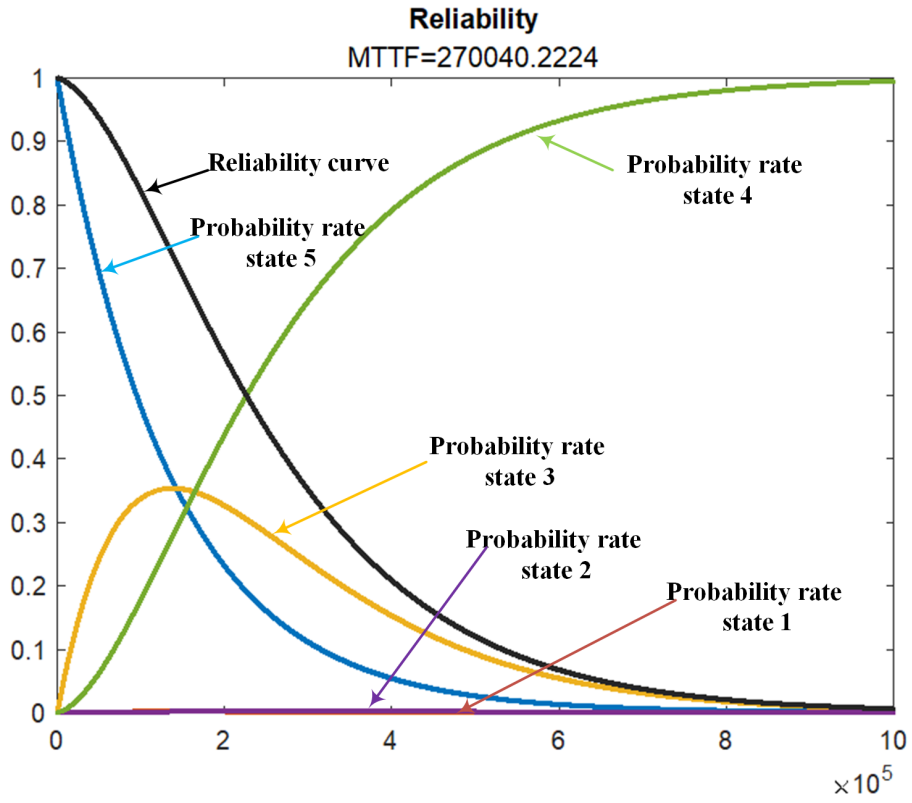


Fig 5.26: Reliability and state probability curves for proposed converter.

5.5.4 Reliability assessment when S_3 is faulty

As mentioned in previous sections, the proposed FT converter can do limited battery charging but no MPPT when S_3 is faulty. Initially, V_{BAT} is always higher than the V_{PV}; therefore, without S_3, there will be only voltage regulation in this case. The battery will be charged only when its voltage is lower than the PV voltage, either through S_4 or diode D_4. The reliability of the boost converter will be the same as conventional converters because there is no redundant switch.

5.5.5 Reliability assessment when S_4 is faulty

Fig. 5.22 shows the reconfiguration of the proposed FT circuit when S_4 is faulty. In this case, the proposed converter has a redundant diode D_4. The corresponding Markov chain model can be divided into five states with eight transition paths with associated transition rates.

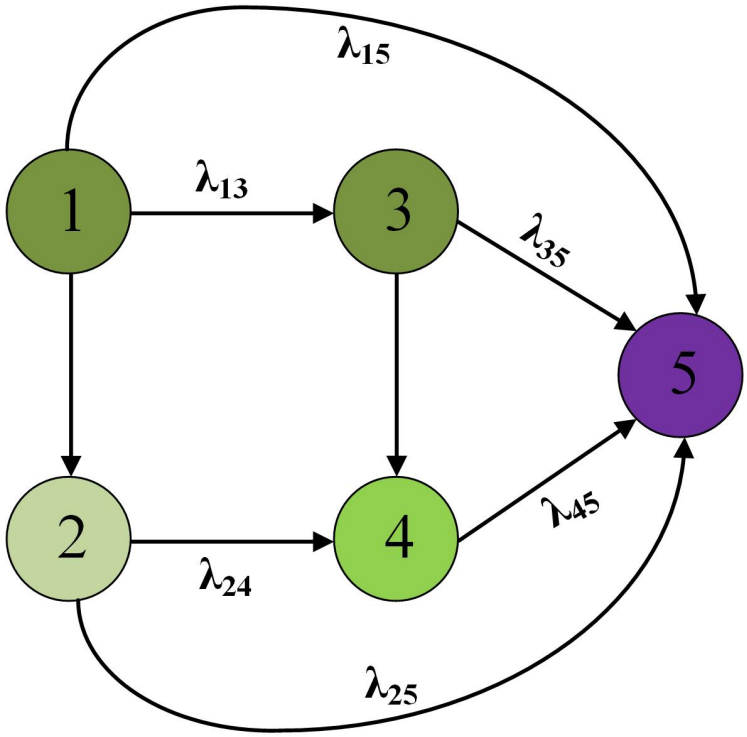


Fig 5.27: Markov chain when S_4 is faulty

When S_4 is healthy, the converter is working under boost operation, where it is either performing battery charging or MPPT, depending upon the SOC of the battery. The transition path λ_{13} indicates the scenario when the reconfiguration occurs; the redundant diode D_4 will start performing the MPPT or battery charging when there is a fault in S_4 and the fuse F_4 blows. The redundant diode D_4 will not let the converter move to the absorption state. The transition paths with transition rate $\lambda_{12}\&\lambda_{34}$ represent the transition of boost operation mode from a healthy state to a partial fault state, where there is a partial fault in C_1 in state 1 or state 3 but S_4 is still healthy. At this stage, the converter suffers from a partial fault, but it is still operational with an increase in voltage ripple at steady-state conditions. Moreover,

λ_{24} shows the transition from state 2 to state 4 with the fault in S_4. Similar to the previous MOSFET fault scenarios, the converter will move to absorption state 5 through any of the four associated transition paths λ_{15}, λ_{25}, λ_{35} & λ_{45}. The transition paths λ_{35} & λ_{45} refer to the failure of parallel diode D_4 from healthy and partial fault states to the final absorption state, respectively. Furthermore, the transition paths λ_{15} & λ_{25} represents the single-point failure scenario from L_2, C_1, C_2 & S_3.

The transition matrix of the proposed FT converter under fault at switch S_4 can be modeled as follows:

$$dP = (M_{S_4} \times P)dt \tag{5.14}$$

Also, the probability of staying in state "k" with time "t" is given as follows:

$$P_{k+1} = M_{S_4} \times P_k \triangle t + P_k \tag{5.15}$$

Here the probability of state P_0 is already known as initially the converter is healthy, therefore the initial probability will be added for computing the probability of remaining four states using equation 15.

$$P_0 = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{5.16}$$

The probability transition matrix in this case as given as follows:

$$M_{S_4} = \begin{bmatrix} -(\lambda_{12}+\lambda_{13}+\lambda_{12}) & 0 & 0 & 0 & 0 \\ \lambda_{12} & -(\lambda_{24}+\lambda_{25}) & 0 & 0 & 0 \\ \lambda_{13} & 0 & -(\lambda_{34}+\lambda_{35}) & 0 & 0 \\ 0 & \lambda_{24} & \lambda_{34} & -\lambda_{45} & 0 \\ \lambda_{15} & \lambda_{25} & \lambda_{35} & \lambda_{45} & 0 \end{bmatrix} \quad (5.17)$$

Similar to previous section, all the transition paths with transition rate are given in Table. I. The reliability of the proposed boost converter can be find out by following equations:

$$R_4(t) = P_0(t) + P_1(t) + P_2(t) + P_3(t) + P_4(t) + P_5(t) \quad (5.18)$$

The MTTFs of proposed FT converter under fault at S_4 can be find out using MATLAB and similarly, the reliability curve is shown in Fig. 5.28

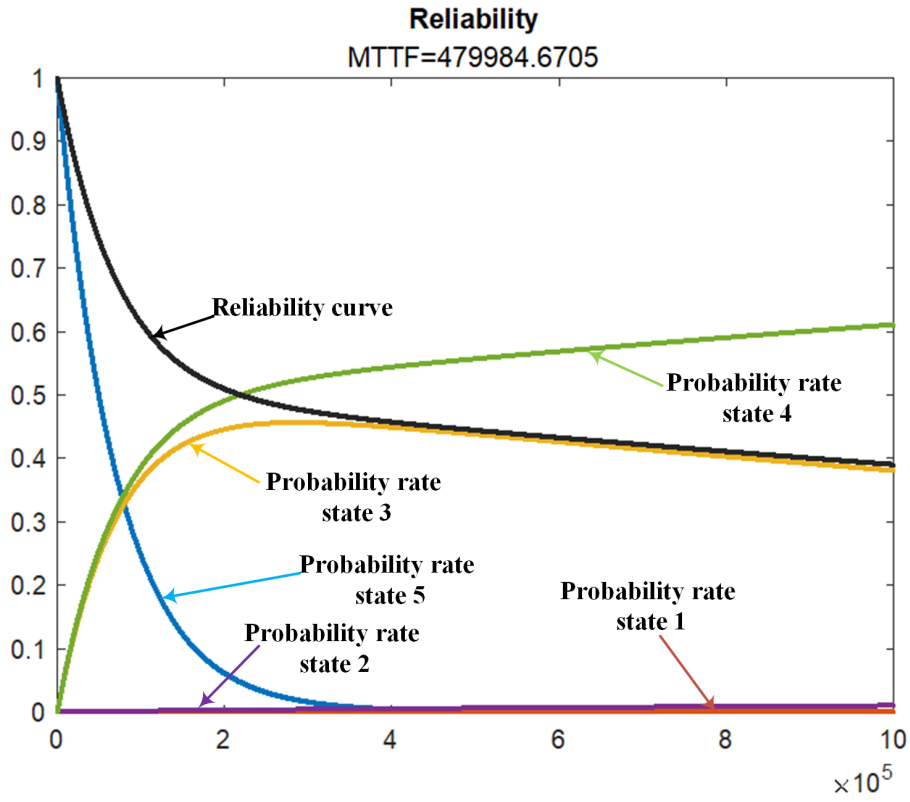


Fig 5.28: Reliability and state probability curves for proposed converter.

Converter topologies	Normal mode	FT mode	Transition paths	MTTF (hours/failure)
Conventional	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_1} = 6.8705, \lambda_{D_1} = 0.072$ $\lambda_{L_1} = 0.117, \lambda_{F_1} = 0.02$	**None**	$\lambda_{12} = 0.02436, \lambda_{13} = 7.1282$ $\lambda_{23} = 7.1282$	$MTTF = \int_0^\infty R(t)d(t)$ $MTTF = 0.140x10^6$
FT Mode 1	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_1} = 6.8705, \lambda_{D_1} = 0.072,$ $\lambda_{D_3} = 0.072$ $\lambda_{L_1} = 0.117, \lambda_{F_1} = 0.02$	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_1} = 6.8705, \lambda_{D_1} = 0.072, \lambda_{D_3} = 0.072$ $\lambda_{L_1} = 0.117, \lambda_{F_1} = 0.02$	$\lambda_{12} = 2.4360, \lambda_{13} = 6.9625$ $\lambda_{15} = 3.0972, \lambda_{24} = 6.8705, \lambda_{25} = 3.0972$ $\lambda_{34} = 2.4360, \lambda_{35} = 7.1759, \lambda_{45} = 7.1759$	$MTTF = \int_0^\infty R(t)d(t)$ $MTTF = 0.27x10^6$
FT Mode 2	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_2} = 6.8705, \lambda_{D_2} = 0.072$ $\lambda_{D_3} = 0.072$ $\lambda_{L_1} = 0.117, \lambda_{F_2} = 0.02$	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_2} = 6.8705, \lambda_{D_2} = 0.072, \lambda_{D_3} = 0.072$ $\lambda_{L_1} = 0.117, \lambda_{F_2} = 0.02$	$\lambda_{12} = 2.4360, \lambda_{13} = 6.9625$ $\lambda_{15} = 3.0972, \lambda_{24} = 6.8705, \lambda_{25} = 3.0972$ $\lambda_{34} = 2.4360, \lambda_{35} = 7.1759, \lambda_{45} = 7.1759$	$MTTF = \int_0^\infty R(t)d(t)$ $MTTF = 0.27x10^6$
FT Mode 3	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_3} = 6.8705,$ $\lambda_{L_2} = 0.117, \lambda_{F_3} = 0.02$	**None**	$\lambda_{12} = 0.02436, \lambda_{13} = 7.1282$ $\lambda_{23} = 7.1282$	$MTTF = \int_0^\infty R(t)d(t)$ $MTTF = 0.140x10^6$
FT Mode 4	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_4} = 6.8705, \lambda_{S_3} = 6.8705$ $\lambda_{D_4} = 0.072$ $\lambda_{L_2} = 0.117, \lambda_{F_4} = 0.02, \lambda_{F_3} = 0.02$	$\lambda_{C_1} = 0.02436, \lambda_{C_{out}} = 0.02436$ $\lambda_{S_4} = 6.8705, \lambda_{S_3} = 6.8705, \lambda_{D_4} = 0.072$ $\lambda_{L_2} = 0.117, \lambda_{F_4} = 0.02$ $\lambda_{F_3} = 0.02$	$\lambda_{12} = 2.4360, \lambda_{13} = 6.8905$ $\lambda_{15} = 7.0362, \lambda_{24} = 6.8705, \lambda_{25} = 7.0362$ $\lambda_{34} = 0.02436, \lambda_{35} = 2.5772, \lambda_{45} = 2.5772$	$MTTF = \int_0^\infty R(t)d(t)$ $MTTF = 0.47x10^6$

Table 5.2: Converter Reliability Profile.

5.6 Numerical Reliability Assessment

This section provides information about the numerical reliability assessment of the proposed FT TPC and its comparison with the conventional single-port converters. This comparison is based on the typical failure rates and the associated probabilities of each transition path derived from [67]. The failure rate of any component is given as:

$$\lambda_{component} = \lambda_b \prod_{i}^{n} \pi_i \tag{5.19}$$

where λ_b is the base failure rate dependent upon the component's ambient temperature and packaging type. π_i is the failure factor which depends on voltage stress π_s, application type π_A, temperature effects π_T, capacitance factor π_c, environmental effect π_E and quality factor π_Q [67]. The failure rate of components, including MOSFET, diode, capacitor, and fuse, in terms of the above factors, are presented in Table II. From Table II, the details of the considered factors and their calculation procedure in different components are as follows: 1. For the Diode, π_s can be used to find the failure rate for any diode besides other factors given in Table II. π_s represents the voltage stress factor for the diode. The voltage stress factor is a function of forward and reverse diode voltages and can be computed as:

$$\pi_s = (\frac{V_d}{V_r})^{T_s} \tag{5.20}$$

2. Similarly, apart from factors shown in Table II, π_v is the voltage stress factor of a capacitor required to calculate its failure rate. It depends on the voltage rating and open circuit voltage of the capacitor. The relation to find π_v is as follows:

$$\pi_v = (\frac{V_{OC}/V_R}{0.5})^{17} + 1 \tag{5.21}$$

3. For a transistor, π_a is the application factor, used along with other factors given in Table II, and it depends on the type of transistor (BJT, JFET, MOSFET) and output power of the circuit. The value of π_a can be chosen from [67].

4.π_Q & π_T are the component's quality and temperature factors, respectively. Usually, π_Q represents the screening level of the semiconductor prefixes, i.e., JANTX, JAN, R, P, B, M and their values can be found in the military handbook MIL-HDBK-217 [67].

Similarly, π_T represents the junction temperature of the MOSFET and diodes. For finding the junction temperature (due to power losses) of a MOSFET and diode can be calculated as follows:

$$T_C = T_a + \theta_{CA} P_{DS} \tag{5.22}$$

$$T_J = T_C + \theta_{JC} P_{DS} \tag{5.23}$$

Here P_{DS} represents the power dissipation of a MOSFET or diode. It can be either calculated using the relation in Table II or estimated using PLECs or LTspice simulation. θ_{JC} θ_{CA} & are thermal resistance of a MOSFET or diode between junction to case temperature and case to the ambiance, respectively. Both of these thermal resistances can be found in the data sheet of the MOSFET or diode.

To find the failure rate of inductors, instead of using junction temperature, alternatively, hot-spot temperature T_{HS} is used and can be computed with the following relationship [61]:

$$T_{HS} = T_a + 1.1 \triangle T \tag{5.24}$$

$$\triangle T = 125 \frac{P_L}{A} \tag{5.25}$$

Here $\triangle T$ is the inductor's average temperature swing, and its value can be used from [67].

The converter reliability profile for proposed TPC-based Buck-Boost and conventional converters are given in the form of Table II. The associated transition matrices with be computed with a change in time at each step and prior state probability. Calculating the numerical values used for the comparison of converter reliability profiles is based on the components listed in Table III. By comparing Fig. 18 with Fig. 20 and 22, the comparison indicates the superiority of the proposed converter.

The longer lifetime of the proposed TPC converter can be seen from the exponential distribution curve shown in these figures. The proposed converter has a redundant diode in some of its operation modes, which will guarantee higher reliability than the conventional converter.

5.7 EXPERIMENTAL VERIFICATION

The experimental verification of the FT converter has been evaluated under various emulated fault conditions. The circuit parameters are listed in Table III. The hardware prototype has been tested for transitions using the faults emulated with the help of DSP Controller TMS320F28379D shown in Fig. 5.29.

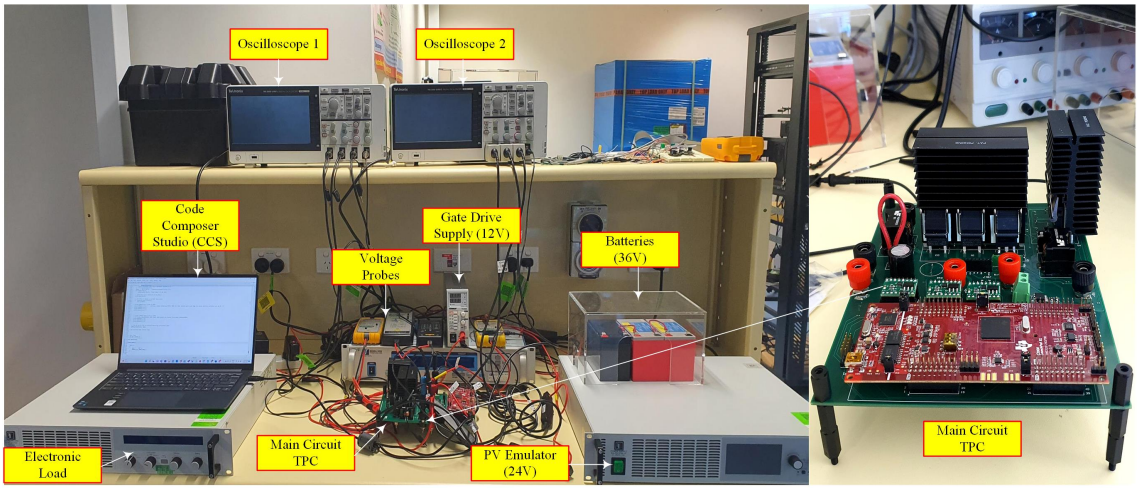


Fig 5.29: Experimental Setup.

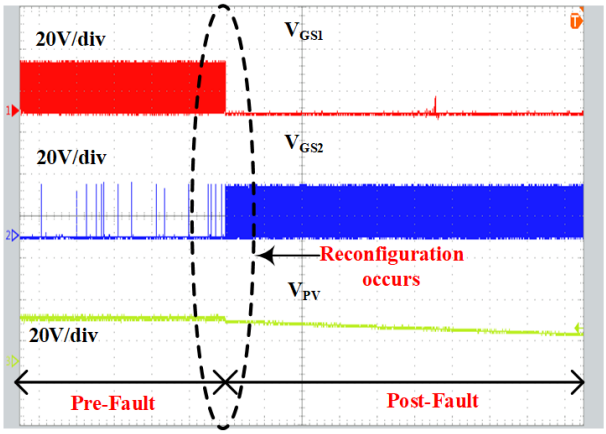
Parameters	Values
Voltage V_{dc1}	24V
Voltage V_{dc2}	36V
Switching frequency f_s	100 kHz
Output Voltage V_o	15V
Output Current I_o	2A
Load	8 Ohm
Inductor 1	270uH
Inductor 2	220uH
MOSFET	IRF540Z
Capacitor C_o	100uF

Table 5.3: Parameter Specifications

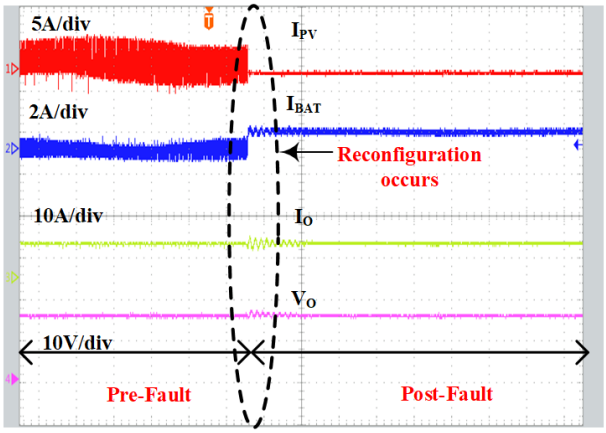
All four fault scenarios for the four MOSFETS during different circuit operation modes have been emulated, and the results are given in this section.

5.7.1 Emulation of faulty switch in Mode 1 (SISO)

Initially, the performance of the proposed converter was evaluated by emulating the fault on S_1 in Mode 1. Before the fault on S_1, the converter is in mode 1 where PV source is providing power to the load and S_1 is performing OVR. When the fault occurs on S_1, the reconfiguration occurs where instead of a PV source, the battery starts providing power to the load. The circuit reconfigures to SISO mode 2, where S_2 starts performing OVR and keeps the output voltage constant, as shown in Fig. 5.30.



(a) Figure A

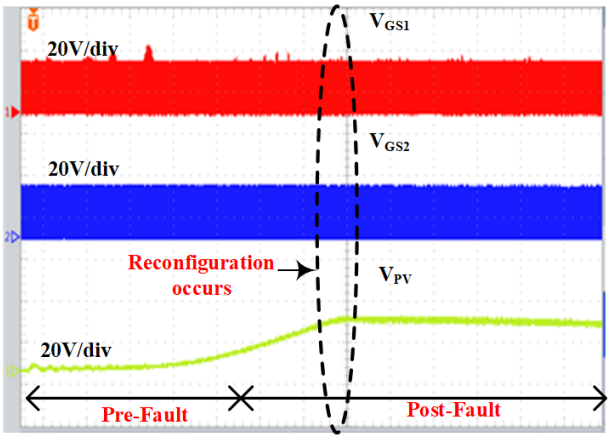


(b) Figure B

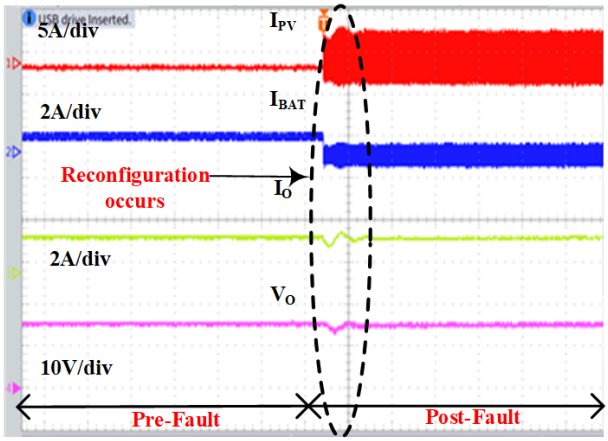
Fig 5.30: SISO Mode Reconfiguration: S_1 faulty

5.7.2 Emulation of faulty switch in Mode 2 (SISO)

Next, the converter's performance was evaluated by emulating the fault on S_2 in Mode 2. Before the fault on S_2, the battery provided power to the load and S_2 was performing OVR in Mode 2. However, when the fault occurs on S_2, the controller detects the fault and reconfigures the circuit to Mode 1, where instead of S_2, S_1 will start performing OVR as shown in Fig. 5.31.



(a) Figure A

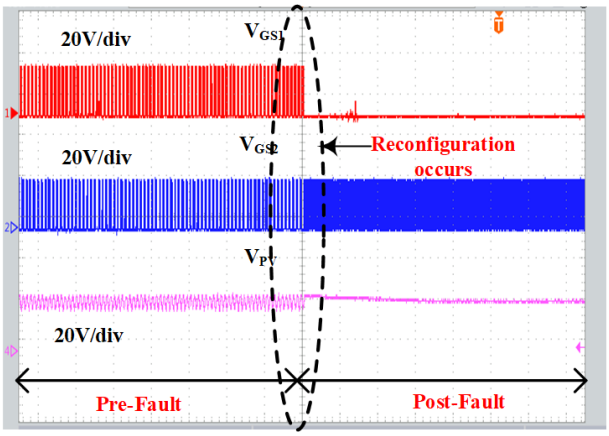


(b) Figure B

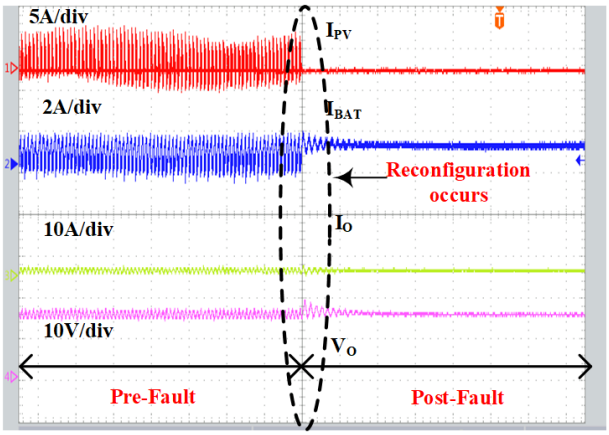
Fig 5.31: SISO Mode Reconfiguration: S_2 faulty

5.7.3 Emulation of faulty switch in Mode 3 (DISO)

Similarly, for DISO mode, the faults are emulated on S_1, S_3 and S_4 to show the associated circuit reconfigurations, where the time multiplexing has been performed using the PV source and the battery. In this mode, as the required power is higher than the power of the PV, the battery will support the PV by providing additional required power in a time-multiplexed fashion, as shown in Fig. 5.10. However, when the fault occurs on S_1, the circuit reconfigures to Mode 2, and the battery provides power to the load, where S_2 is performing OVR, as shown in Fig. 6.9.



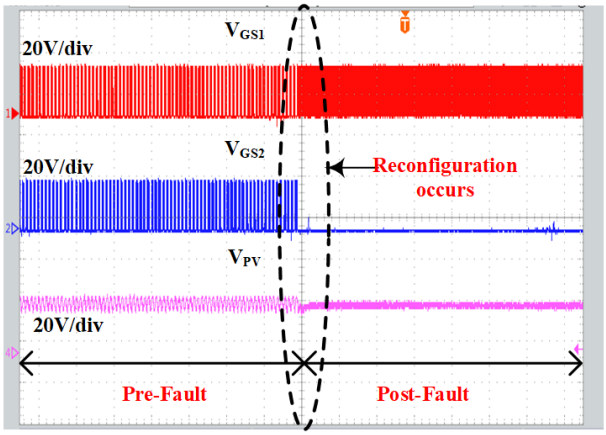
(a) Figure A



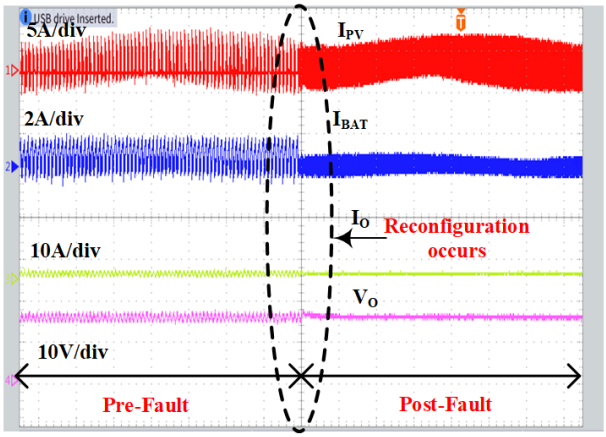
(b) Figure B

Fig 5.32: DISO Mode Reconfiguration: S_1 faulty

When there is a fault on S_2 during DISO mode, the circuit will reconfigure to mode 1. The controller keeps checking the voltage of the PV, and if the required power is more than the power of the PV, then the power will still be supplied from the battery through S_3 & S_4, resulting in a two-stage converter. The experimental results of the emulated faults w.r.t fault at S_2 is shown in Fig. 5.33.



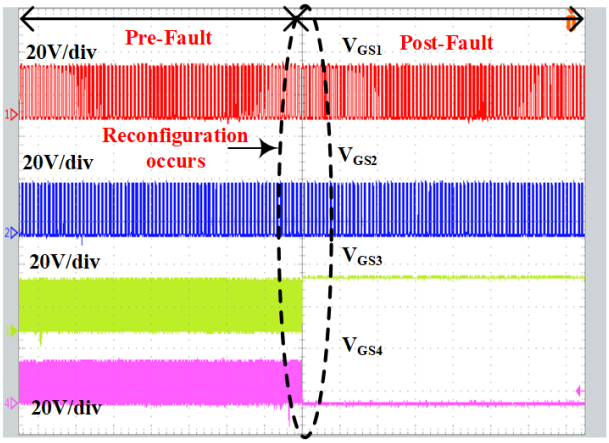
(a) Figure A



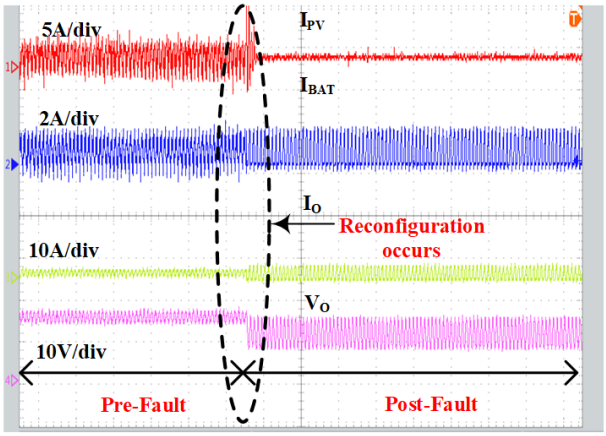
(b) Figure B

Fig 5.33: DISO Mode Reconfiguration: S_2 faulty

During DISO mode, switch S_3 & S_4 is performing MPPT complementarily. If the fault occurs at any of these switches, then there will be no MPPT as there is no additional switch to perform MPPT. This fault was also emulated at S_3, and results are shown in Fig. 5.34.



(a) Figure A

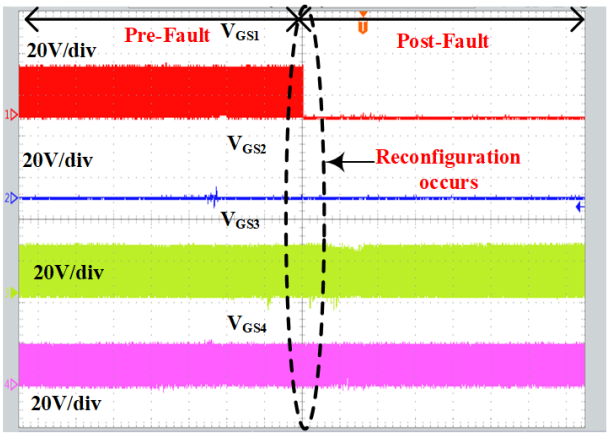


(b) Figure B

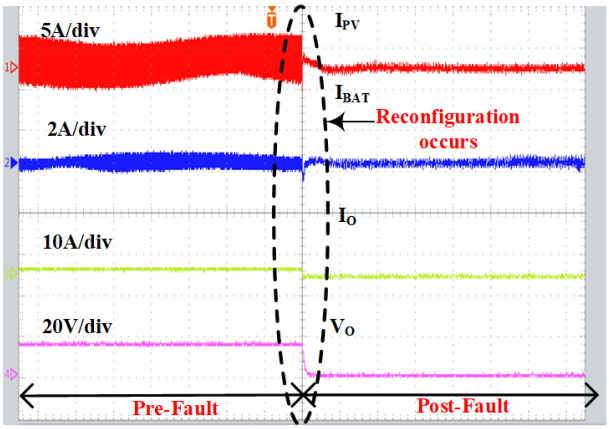
Fig 5.34: DISO Mode Reconfiguration: S_3 faulty

5.7.4 Emulation of faulty switch in Mode 4 (SIDO)

As mentioned in section II, the proposed FT circuit can operate under SIDO (Mode 4). Therefore, different fault scenarios were emulated for SIDO mode where the converter was evaluated during fault occurs on S_1, S_3 and S_4. According to the experimental findings, if there is a fault on S_1 during SIDO mode, where the PV is providing power to the battery and output load, then the circuit reconfigures to Mode 2, where the battery will start providing power to the load shown in Fig. 5.35.



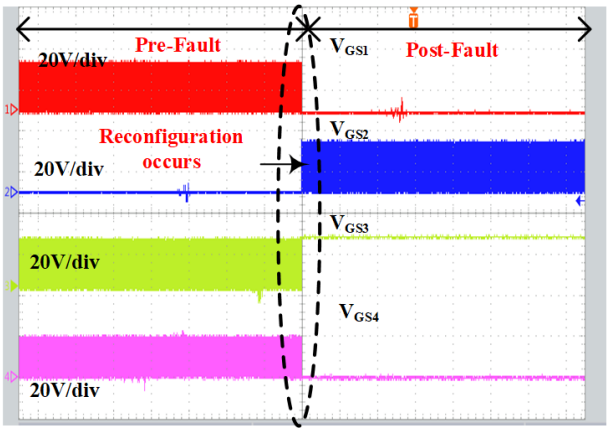
(a) Figure A



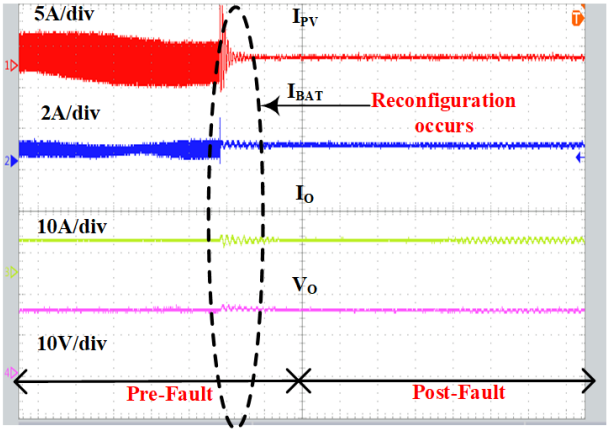
(b) Figure B

Fig 5.35: SIDO Mode Reconfiguration: S_1 faulty

The controller checked the SOC level of the battery, and if it is lower than the recommended level, then the power flows from the PV using the path from S_3 and S_4 resulting in a two-stage converter. As the power processing stage is doubled, it affects the converter's efficiency. The faults on S_3 and S_4 were also emulated when the converter is running under SIDO operation, when there is a fault on S_3, instead of performing SIDO operation, the converter will reconfigure to Mode 2, where the battery supplies the power to the load as shown in Fig. 5.36.



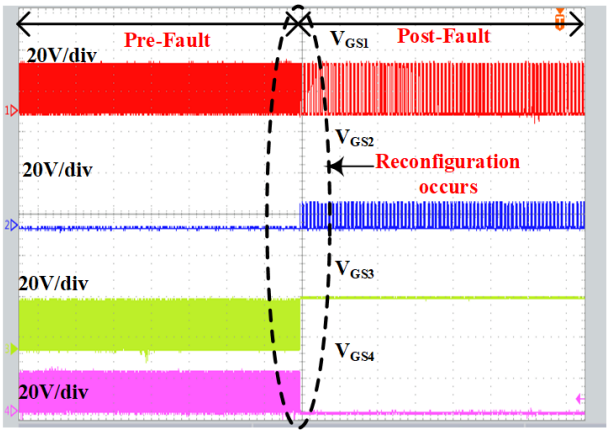
(a) Figure A



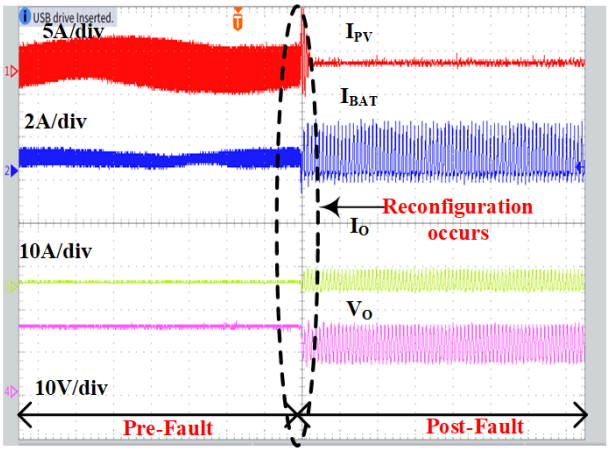
(b) Figure B

Fig 5.36: SIDO Mode Reconfiguration: S_3 faulty

In case of a fault on S_4 during SIDO operation, the circuit reconfigures to DISO mode where the PV and the battery both will provide power to the load. The associated experimental results are shown in Fig. 5.37.



(a) Figure A



(b) Figure B

Fig 5.37: SIDO Mode Reconfiguration: S_4 faulty

5.8 Summary

This chapter presented a new three-port dc-dc topology to perform MPPT, Battery Charging and Voltage regulation with fewer components. The reliability assessment using the Markov chain model has shown that the proposed converter is two times less likely to fail than conventional buck/boost converters. The technical limitation of this work is a single battery storage element and the diodes in series with both PV and the battery will limit its application in higher power applications. In order to solve the storage downside, the next chapter will discuss design of multiport converter having more than one storage element.

Chapter 6

A Novel Non-Isolated Three-Port Converter for Battery Management Systems

6.1 Introduction

As most reported TPC topologies only cater for a single battery or battery string, this chapter extends the TPC capability further and proposes a novel three-port converter using a single-shared inductor for output voltage regulation and a single-shared inductor for battery management. The converter is capable of not only performing maximum power point tracking (MPPT) but it can also charge multiple batteries and control the amount of current going into individual battery. The detailed circuit configuration is provided in this chapter, and the concept was verified using simulation results from the LTspice simulator.

This chapter is organised as follows. Section I discusses different converter structures and their downsides in the literature. Section II provides the information about the configuration of the proposed converter, while Section III provides the detailed simulation analysis for the proposed converter; finally a conclusion is offered in

Section IV.

6.2 Literature review

The key to dealing with the intermittent nature of renewable energy resources is to add multiple energy storage devices to the existing renewable energy systems. Conventionally, different multi-stage three port converters have been proposed in [69–73] where only a single energy storage device is connected to the renewable energy resources and the circuitries involve high number of components, which increases the cost and reduces the efficiency of such renewable energy systems.

In [74], a dual-input single-output converter with fault-tolerant ability is proposed, with five operating modes. This converter can regulate the output voltage, perform MPPT, and charge the single battery as shown in Fig. 6.1.

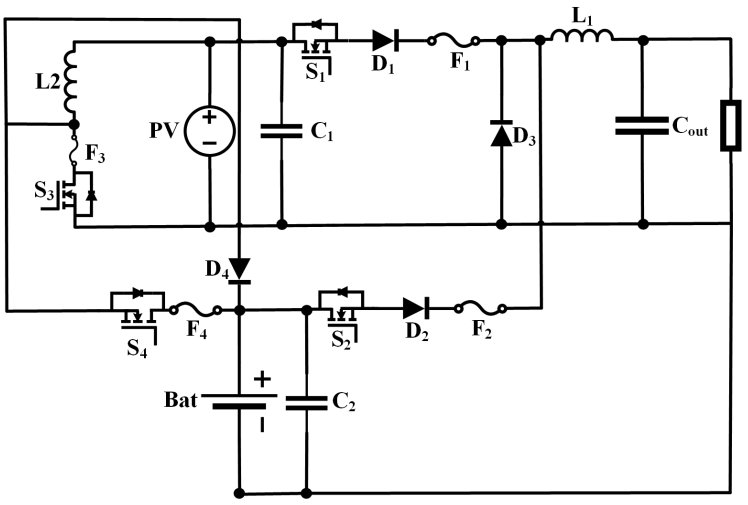


Fig 6.1: FT DISO converter with fault tolerant ability in [74].

In [75], another three-port converter is proposed, which can operate in five different modes. Again, the converter can only store energy in a single storage device. In [76], a three-level three-port bi-directional DC-DC converter is presented where the converter has a bi-directional port. The converter is fault-tolerant and can provide power to the load even in the case of a fault. The limitation is again the presence of a single-stage device in the system.

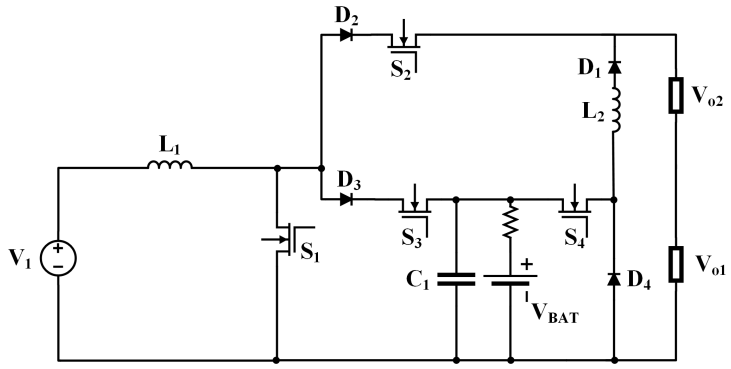


Fig 6.2: Multiport converter with five modes in [75].

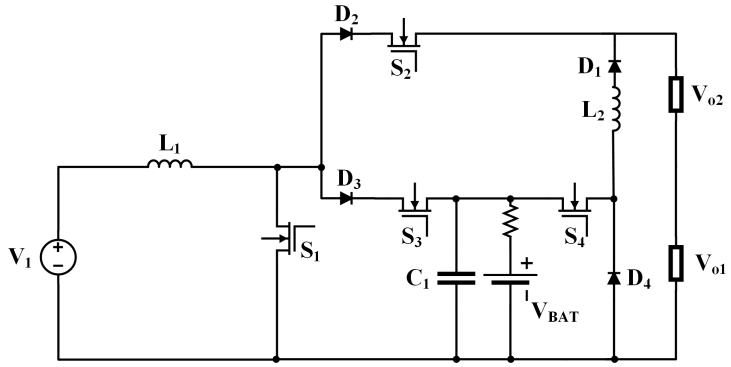


Fig 6.3: Multiport bi-directional converter in [76].

Motivated by the challenge of adding more storage units to a three-port converter-based system, this paper proposes a converter that can use a single inductor to charge multiple storage units using different switching patterns. The additional advantage is the sharing of a single inductor for output voltage regulation.

6.3 Proposed Three-Port Converter Configuration

A Non-Isolated Three-Port DC-DC converter is shown in Fig. 6.4. This converter has uni-directional input and output ports with a bi-directional battery port for battery charging and discharging. The proposed converter has two inductors regulating the output voltage and charging both batteries with four switches, four diodes, and two filter capacitors. The proposed converter can perform output voltage regulation,

MPPT, and multiple battery charging using a single inductor in all five modes. It consists of a PV panel V_{PV} as the first source and two batteries, namely V_{BAT1} and V_{BAT2} as the second source. Both input sources are connected to the load through a dual input buck converter where the power can be equally shared from both input sources. On the other side, both the batteries are connected to the PV through a single shared inductor that allows battery charging/discharging to be monitored and regulated when required.

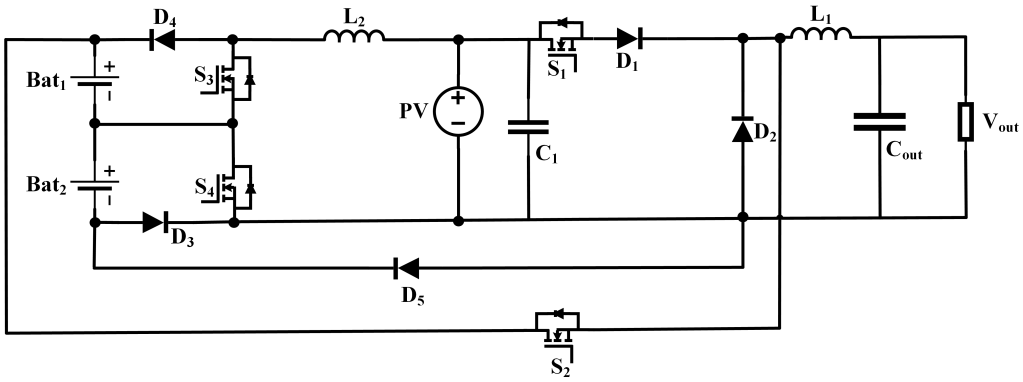


Fig 6.4: Proposed three port converter with multiple storage devices.

6.3.1 Operating Principle of Proposed Three Port Converter

The operating principle of the proposed three-port converter (TPC) can be explained in five different operating modes. These modes depend on the PV irradiance, battery power, and load requirements.

1. Mode-I: When PV has enough power:

   The proposed converter is battery-powered with an additional PV input source that will provide all the required power for the load at maximum irradiance. Therefore, the PV , as the main source will supply the required power to the load in the first mode, involving S_1, L_1, D_1, D_2, C_1, C_O, and can be referred to as a single-input single-output (SISO) mode, as depicted in Fig. 6.5.

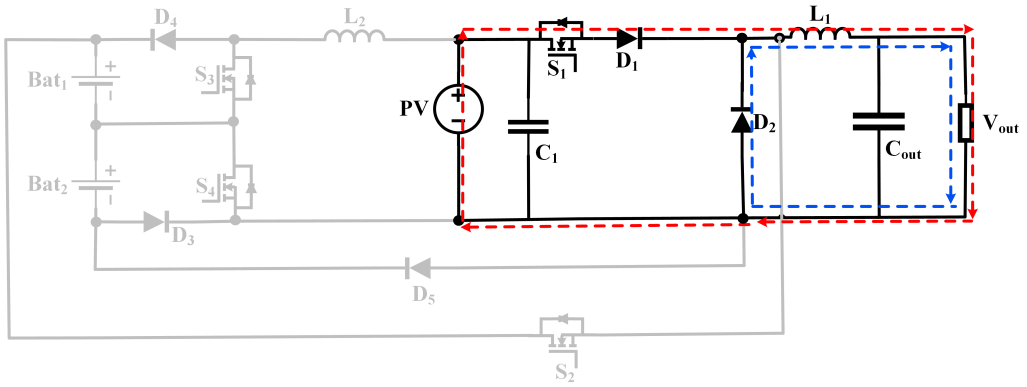


Fig 6.5: Mode 1: When PV has enough power.

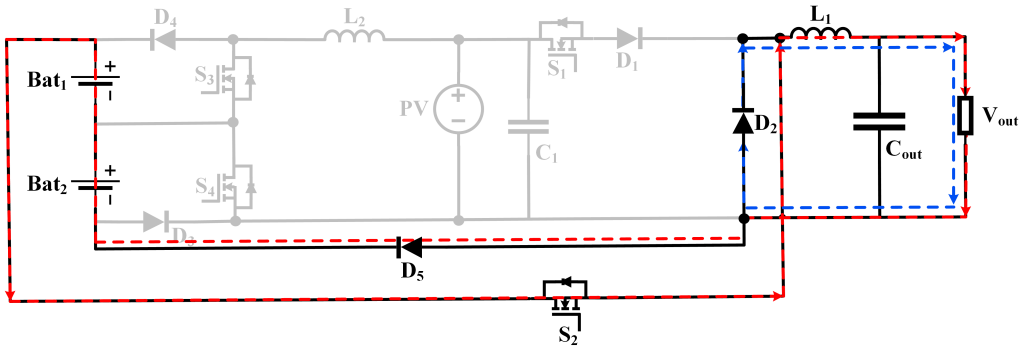


Fig 6.6: Mode 2: When the battery has enough power but no PV power.

2. Mode-II: When Battery is in service and have enough power

   As explained before, the proposed converter is battery-powered; therefore, when there is no power from the PV, either due to night or under cloud cover, the battery will provide all the power to the load. In this mode, the main controller will check the open-circuit voltage V_{OC} of the PV after every specified time period. As soon as the controller detects PV power, the battery to load mode will automatically transition to PV to load mode. This mode involves S_2, L_1, D_2, C_O and can be referred to as a single-input single-output (SISO) mode, as depicted in Fig. 6.6.

3. Mode-III: When PV has insufficient power to supply the load

   This mode will be deployed when the PV has some power, but it is insufficient to supply the required power to the load, in which case the battery will take up the slack. Since both the converters are connected at a single node and

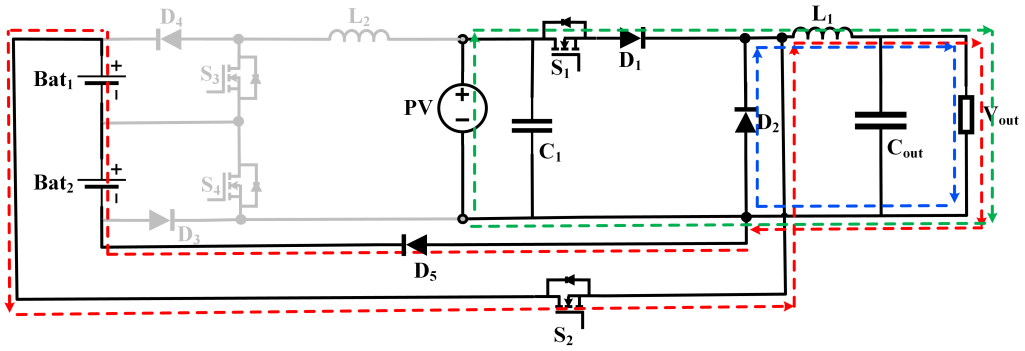


Fig 6.7: Mode 3:Dual input mode.

the power sources are parallel, switches S_1 and S_2 should be complementary. Thus, in this mode, both switches will be turned on in a time-multiplexed fashion to simultaneously supply the power from PV and battery. This mode can be referred to as a dual input single output (DISO) mode as depicted in Fig. 6.7.

4. Mode-IV: When PV has more power than the required load

   There are periods when the PV generates more power than required and a well-designed converter, must not waste this extra power, but rather store it in batteries, as depicted in Fig. 6.8. In this mode, the controller is not only regulating the output voltage but also the voltage and current of both batteries. If the voltage of the batteries and currents are below the predefined values, the converter will start charging the batteries. As there are two batteries connected in series, the converter can check each battery status either V_{BAT1} or V_{BAT2}. In this mode, two different switching patterns charge V_{BAT1} and V_{BAT2} respectively. Firstly, S_3 and S_4 turn on together to charge L_2 and then either S_3 or S_4 will turn off to charge V_{BAT1} or V_{BAT2} as depicted in Fig. 6.9(a) and Fig. 6.9(b), respectively. This mode can be referred to as a single-input dual-output (SIDO) mode.

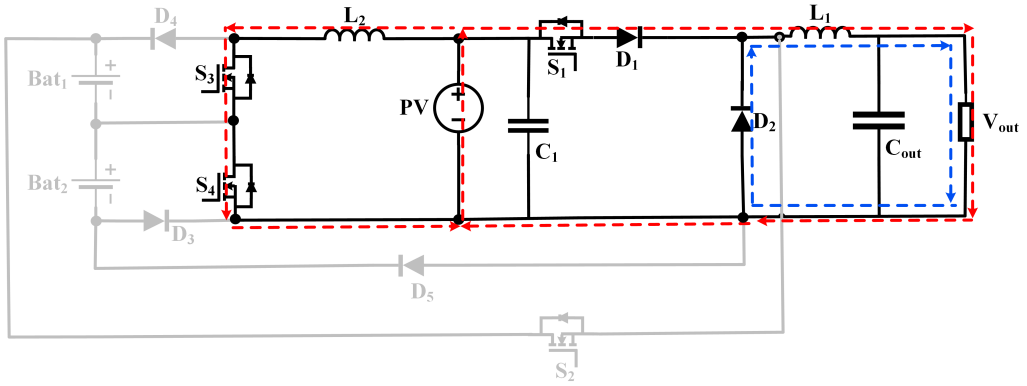
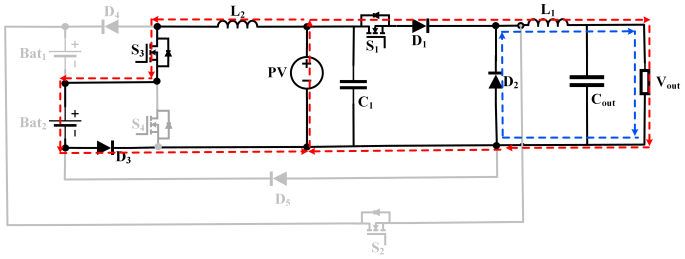
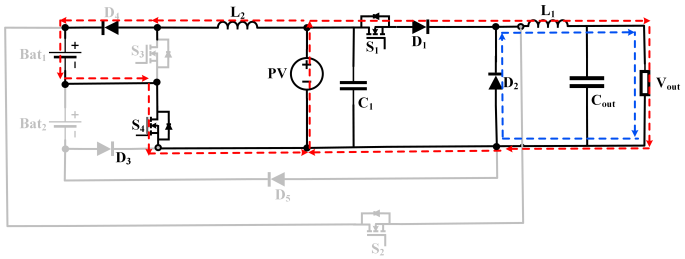


Fig 6.8: Mode 4: When PV has excess power.



(a) PV regulating output voltage and charging battery 1.



(b) PV regulating output voltage and charging battery 2.

Fig 6.9: Mode4: When PV has excess power.

5. Mode-V: When there is no output power required

   During this mode, there is no power required, so the converter will charge the batteries as explained in SIDO mode. This mode is depicted in Fig. 6.10, Fig. 6.11(a) and Fig. 6.11(b).

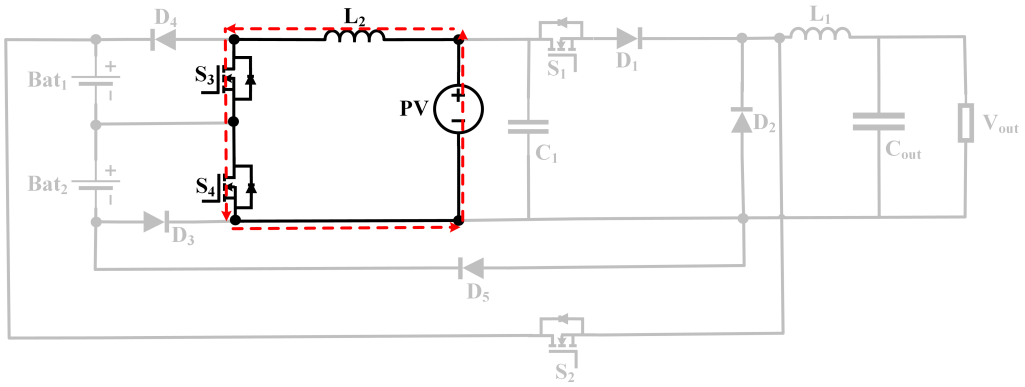
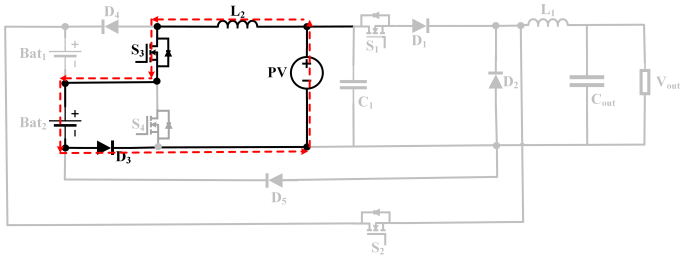
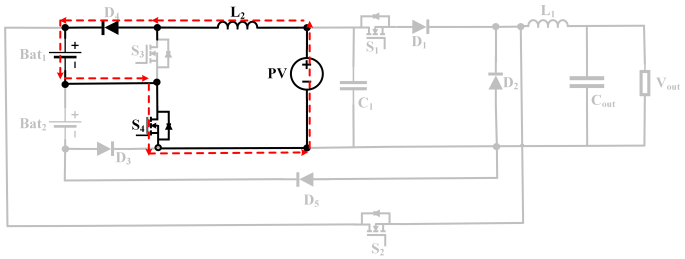


Fig 6.10: Mode5:Inductor Charging.



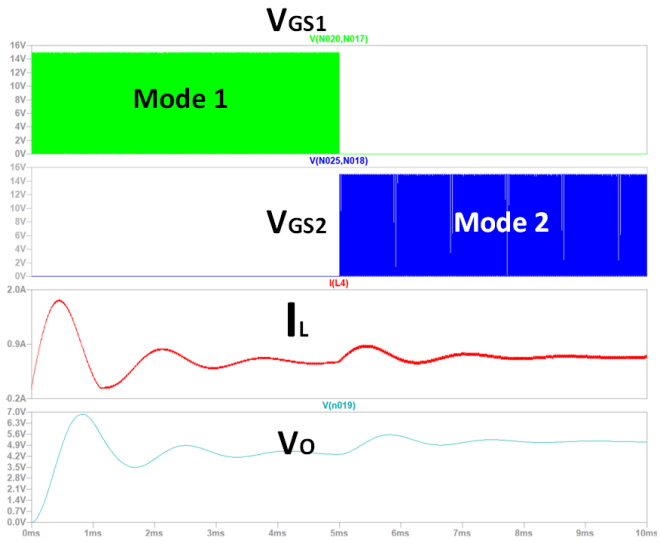
(a) Battery Charging 1.



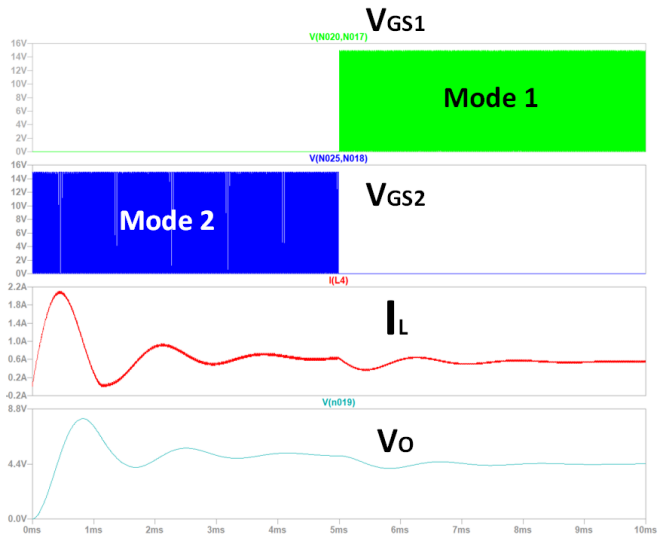
(b) Battery Charging 2.

Fig 6.11: Mode 5:No load condition and Battery Charging

For reference, the study on mode-change is current under investigation but some of the simulation results related with mode change are as follows.



(a) Mode-Change: From Mode 1 to Mode 2.



(b) Mode-Change: From Mode 2 to Mode 1.

Fig 6.12: Mode-Change

6.4 Experimental Results

Numerous experiments were carried out in the laboratory to verify the open-loop characteristics of proposed three-port converter. All the results show the control objectives in all the operating modes for the proposed converter, including output current, battery current, PV voltage, and output voltage, respectively.

The PV to load mode can be seen in Fig. 6.13. As mentioned before, in this mode, the PV has maximum irradiance; therefore, the PV can provide power to the load. The switch S_1 regulates the output voltage in this mode. The simulation results show the gate drive signal V_{GS} for S1 (Channel 1), the output voltage V_O (Channel 2), the output current I_O (Channel 3), and PV voltage V_{PV} (Channel 4).

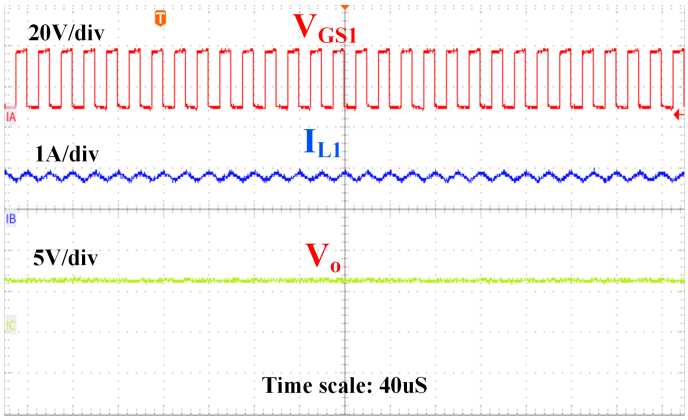


Fig 6.13: Mode 1: PV have maximum power to supply load Channel1: The Gate drive signal V_{GS} for S1, Channel2: The Output voltage V_O, Channel3: The Output current I_O, Channel4: PV voltage V_{PV}

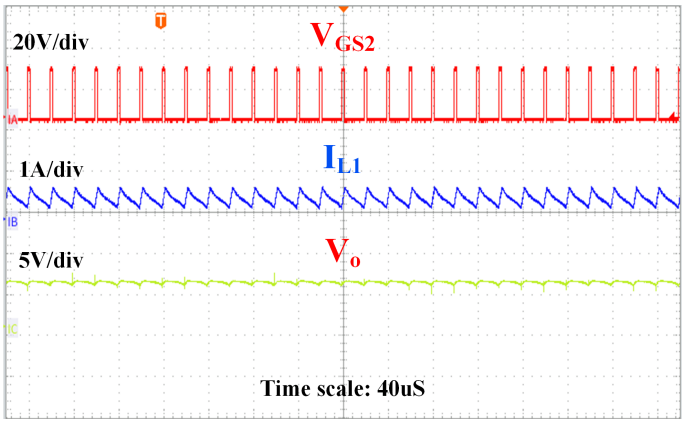


Fig 6.14: Mode 2: No PV & Battery have enough power to supply load Channel1: The Gate drive signal V_{GS} for S2, Channel2: The Output voltage V_O, Channel3: The Output current I_O, Channel4: Battery voltage V_{BATT}, Channel5: Battery current I_{BATT}

In the second mode, the assumption is there is no PV either due to night time or any PV fault. Therefore, the battery provides power to the output load, and here S_2 will perform output voltage regulation as shown in Fig. 6.14. Here it is important to note that this converter is battery-powered; therefore, whenever the

converter is switched on, it will go to battery to load mode by default. In this mode, it will keep checking the power of the PV.

If there is no PV power, the battery provides the power to the load. Otherwise, if the sensor senses the PV power, the mode will automatically be shifted to PV to load mode. The simulation results show the gate drive signal V_{GS} for S_2(Channel 1), the output voltage (Channel 2), the output current (Channel 3), battery voltage V_{BATT} (Channel 4) and battery current I_{BATT} (Channel 5).

The third mode represents where PV has power but its not enough to power the load alone. Therefore, the battery will help the PV and both PV and battery will provide power using time-multiplexing technique using single inductor shown in Fig. 6.15. In this mode, both S_1 and S_2 will perform output voltage regulation. The simulation results shows the gate drive signal V_{GS} for S_1 (Channel 1), the gate drive signal V_{GS} for S_2 (Channel 2), the output voltage (Channel 3) and the output current (Channel 4).

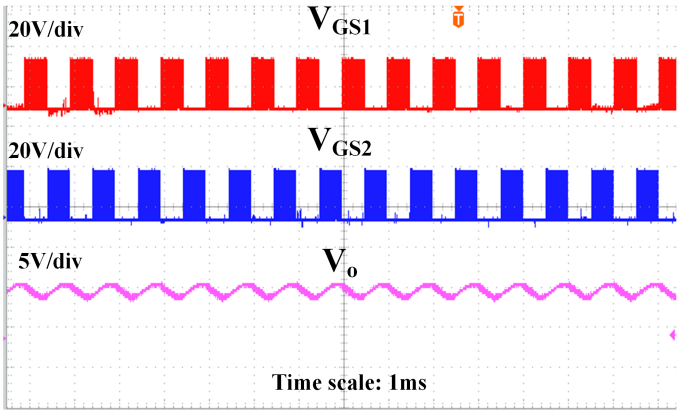


Fig 6.15: Mode 3: PV & Battery both providing power to supply load Channel1: The Gate drive signal V_{GS} for S1, Channel2: The Gate drive signal V_{GS} for S2, Channel3: The Output voltage V_O, Channel4: The Output current I_O

The PV to load and battery together is a SIDO mode where PV has excess power, and the output successfully gets its required power. Therefore, the excess power will be stored in both batteries. This characteristic is where the role of this converter becomes crucial. Conventionally, it was not possible to charge two batteries by controlling the individual current using a single inductor within this

topology. But, the proposed converter can now charge battery 1 and battery 2 by using different switching patterns, making sure that both batteries will be charge by a proper control using a single inductor as shown in Fig. 6.16 & Fig. 6.17.

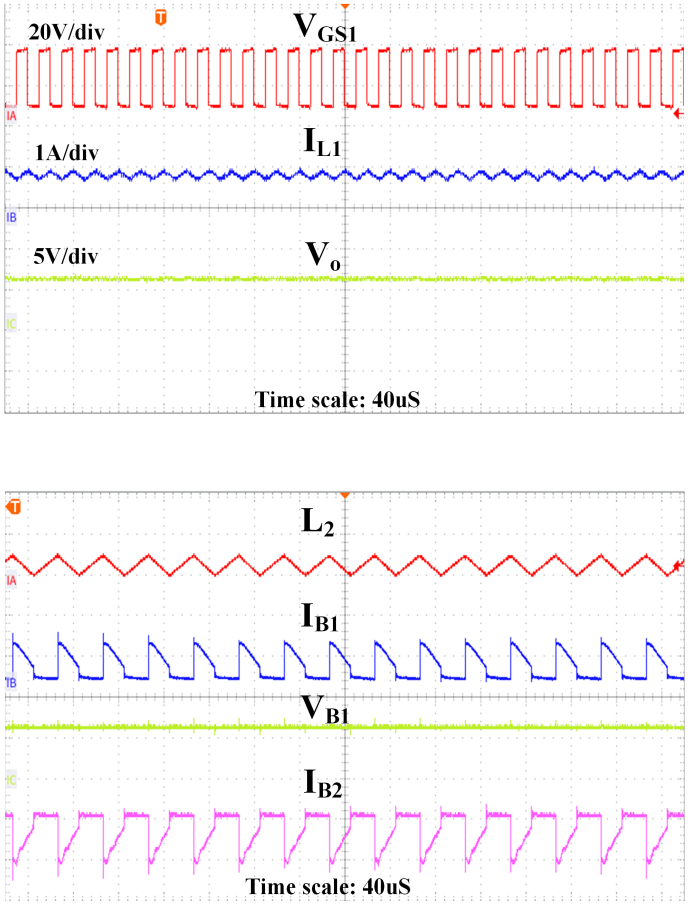


Fig 6.16: Mode 4: PV to Load and Battery 1 Channel1: The Output voltage V_O, Channel2: Inductor current of Buck converter I_{L1}, Channel3: inductor current of Boost converter I_{L2}, Channel4: Battery 1 current I_{BATT1}, Channel5: Battery 2 current I_{BATT2}

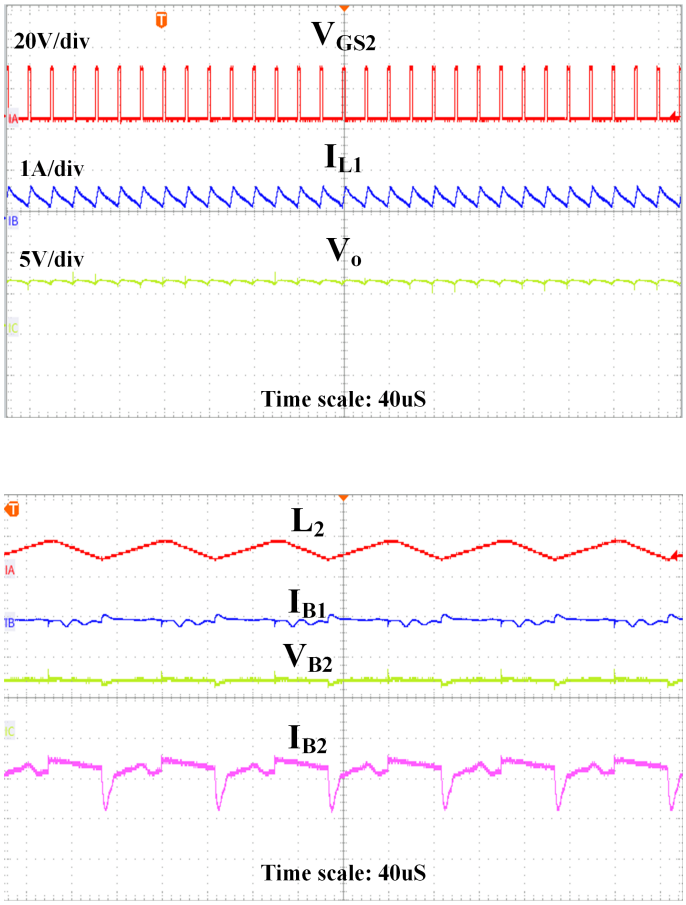


Fig 6.17: Mode 4: PV to Load and Battery 2 Channel1: The Output voltage V_O, Channel2: Inductor current of Buck converter I_{L1}, Channel3: inductor current of Boost converter I_{L2}, Channel4: Battery 1 current I_{BATT1}, Channel5: Battery 2 current I_{BATT2}

The simulation results shows the output voltage V_o (Channel 1), the inductor current of Buck converter I_{L1} (Channel 2), the inductor current of Boost converter I_{L2} (Channel 3) and both batteries' current (Channel 4), respectively.

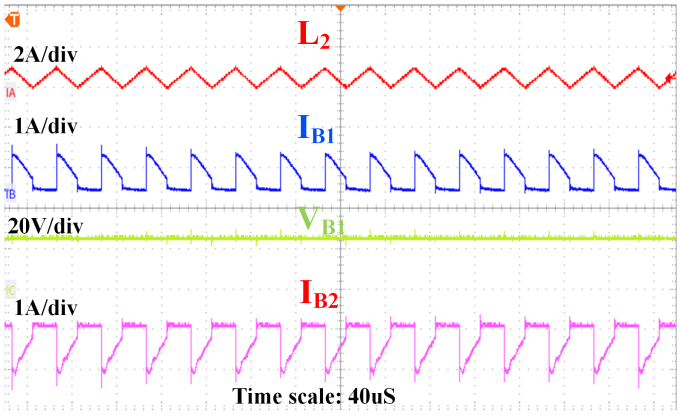


Fig 6.18: Mode 5a: PV to Battery: Battery Charging 1 Channel1: The PV voltage V_{PV}, Channel2: inductor current of Boost converter I_{L2}, Channel3: Battery 1 current I_{BATT1}, Channel4: Battery 2 current I_{BATT2}

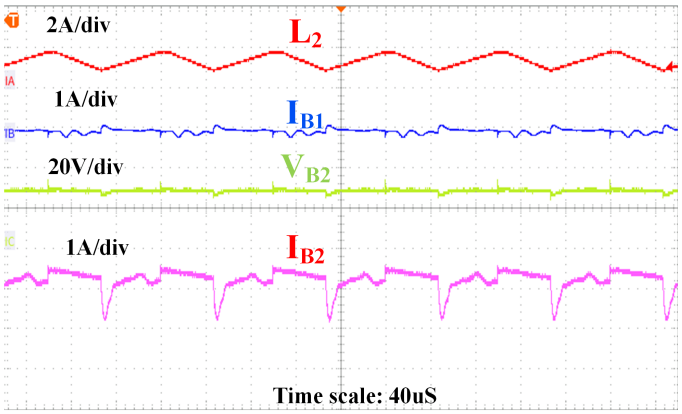


Fig 6.19: Mode 5b: PV to Battery: Battery Charging 2 Channel1: The PV voltage V_{PV}, Channel2: inductor current of Boost converter I_{L2}, Channel3: Battery 1 current I_{BATT1}, Channel4: Battery 2 current I_{BATT2}

The last mode is the mode where there is no load condition. This scenario implies that if the user doesn't want power in some cases. It may be possible that at a certain, the user doesn't need power; therefore, the output load is switched off. When there is no load, still the PV is generating the power, and instead of wasting the power, the converter will check the status of both batteries, and it will charge both batteries using the switching patterns shown in Fig. 6.18 and Fig. 6.19. The simulation results show the PV voltage V_{PV} (Channel 1), the inductor current of Boost converter I_{L2} (Channel 2), and both batteries' current (Channel 3) & (Channel 4), respectively.

6.5 Summary

This chapter proposes a novel TPC where multiple storage units can be managed using a shared inductor. The converter can perform MPPT, dual battery management, and output voltage regulation using a low component count and with higher efficiency. The theoretical results compared with the simulation and hardware results show the conceptual efficacy of the proposed converter.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

Multi-port DC-DC converters play an important role in applications such as electric vehicles and DC microgrids, but they do come with several technical limitations. In chapter 2, the benefits and downsides of different non-isolated converters were discussed, and we found that multi-port converters are widely used in various applications to provide power from different renewable energy resources by sharing components. This sharing of components helps reduce the power processing stages and increases the converter's efficiency. However, reliability and performance are also crucial, and Chapter 2 provides a brief insight into different non-isolated multi-input topologies that have tried to increase the output voltage gain and share the power between the multiple inputs with increased reliability. Non-isolated converters do not require galvanic isolation, resulting in a transformerless converter structure that is smaller and cheaper to produce.

In Chapter 4, a brief comparison is presented of the reported DISO topologies. For a fair comparison, constraints like input current profile, number of circuit elements, high gain, and extension of the current design to other multi-port designs, were set. The proposed converter is capable of providing high output voltage and continu-

ous current for both inputs. The mathematical analysis and operational principles were discussed to highlight its key functioning characteristics. The design criteria of the L-C components were established through time-domain analysis, thereby allowing for a simulation to be performed on the LTspice platform; various results are presented to verify the mathematical analysis of the proposed DISO high step-up DC-DC converter. Additionally, sample experimental results are presented at the end to validate the converter operation. The simple structure and high voltage gain characteristics make this topology a primary choice for the DC-DC stage in solar grid-tie applications.

In Chapter 4, an improved control scheme for solving the power-sharing problem between the two input sources of a DISO buck converter is proposed. This control scheme decouples the power-sharing while maintaining the inductor current in defined bands. For this purpose, a hysteretic control scheme is utilised. A buck-derived SI-DISO power converter is used with a low-cost analogue circuit to verify the proposed TMC control. The experimental results demonstrate the effectiveness of the proposed converter. To prove the effectiveness of the proposed control, a delay circuit was added to make the inductor operate in DCM as previously reported. The efficiency and transient response of the SI-DISO converter were experimentally compared in CCM and DCM operations and the results prove that the proposed TMC scheme improves the efficiency of the same converter under DCM operation by a maximum of 3%. The transient response also improved.

Chapter. 5 presents a new three-port DC-DC topology to perform MPPT, battery charging, and voltage regulation, with fewer components. The reliability assessment using the Markov chain model shows that the proposed converter is two times less likely to fail than conventional buck/boost converters. The technical limitation of this work is the single battery storage element, and having the diodes in series with both PV and the battery will limit its application in higher power applications.

Chapter 6, proposes a novel TPC where multiple storage units can be managed using a shared inductor. The converter can perform MPPT, dual battery management,

and output voltage regulation, with a low component count and high efficiency. The theoretical results, when compared with the simulation results, show the conceptual efficacy of the proposed converter.

7.2 Future Work

In this thesis, a control scheme, a novel high step-up topology, and two FT topologies are investigated. The recommendations for future work, as a result of this research study, are as follows:

1. To extend the scope of this work for FT-related grid-connected applications, the AC ports can be mixed with DC ports to provide AC power.

2. This work is related to FT Non-Isolated Multi-port converters. However, the same line of research can be followed in topologies where galvanic isolation is required.

3. This work is related to uni-directional DC-DC multi-port structures, which can be extended to bi-directional converters by adding single/multiple bi-directional ports into the existing circuit.

4. This work comprises of FT structures created by adding circuits manually to the existing multi-port converter. However, the use of a certain form of computer algorithm could make automatic entries of FT structures into existing structures to create novel FT TPC topologies.

5. The number of PV inputs and battery storage elements can be increased to maximise the importance of future works.

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