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Article

Segment Reduction-Based Space Vector Pulse Width Modulation for a Three-Phase F-Type Multilevel Inverter with Reduced Harmonics and Switching States

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Abstract: An improved segment reduction-based space vector pulse width modulation (SVPWM) for an F-type three-level inverter (FT^{2}LI) is presented in this article. The proposed SVPWM algorithm decreases the additional switching state transition of each triangle with the application of an improved nine- and three-segment reduction switching strategy. The main feature of the segment reduction technique is that it eliminates second-order harmonics in the inverter output side with good total harmonic distortion (THD), low switching losses, and minimum filter requirements when compared with carrier-based PWM (CBPWM) techniques such as multi-carrier sine PWM (MC-SPWM), sixty-degree PWM (60° PWM), and switching frequency optimal PWM (SFO PWM). The proposed modulation algorithm for FT^{2}LI is implemented on the MATLAB/Simulink platform. The performance of the proposed segment reduction-based SVPWM algorithm is tested experimentally on an FT^{2}LI at various amplitude and frequency modulation indices, and the experimental results are verified with the simulation results. Additionally, a comparative analysis carried out to study the relationship between the segment reduction-based SVPWM and CBPWM techniques inferred that the suggested segment reduction-based SVPWM algorithms can optimize high-order harmonic distributions and have a minimum computational burden.

Keywords: F-type three-level inverter; higher-order harmonics; switching losses; segment reduction-based SVPWM; THD

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1. Introduction

Power electronic drives are used in a wide range of applications in industry, including manufacturing sectors, process infrastructure, oil and gas plant sectors, as well as electric and hybrid vehicle transportation systems. Multilevel inverters (MLIs) have become the preferred power electronic converters to supply variable speed drives with a variable voltage and variable supply frequency. MLIs are often employed in applications involving high power owing to the superior performance that they offer in comparison to two-level converters. MLIs lower their output voltage stress on power switching devices in addition to decreasing the THD and the rate of change in voltage (dv/dt) [1]. The three-level converter was used first in [2], and the MLI topologies such as diode-clamped [3], capacitor-clamped, and cascaded H-bridge [4] have played a major role in power electronic applications. Traditional two-level inverters, multilevel inverters, and numerous PWM techniques to control MLIs are explored in abundance in much of the literature. As investigated in much of the literature, PWM methods play a significant role in all inverter circuits, which allow for optimal harmonic performance, as well as reduced switching losses and stress. Several PWM techniques have been devised for recently developed MLI topologies. These modulation techniques can be classified into three types: (1) carrier-based PWM (CBPWM) [5], phase-shifted (PSPWM) [6], and phase disposition (PDPWM) [7]; (2) space vector PWM

(SVPWM) [8]; and (3) nearest-level modulation techniques [9] etc. In that sense, carrier-based PWM (CBPWM) and space vector PWM (SVPWM) are two PWM algorithms that have been extensively used. When compared to CBPWM, the SVPWM has many advantages, including the ability to produce the maximum attainable fundamental output voltage, the minimum THD in the inverter output terminal, and the capability of being digitally implemented. Paper [10] summarizes the SVPWM techniques for MLIs such as the α-β frame, g-h frame, K-L frame, α′-β′ frame, and SVPWM based on an imaginary coordinate system. In the above-said SVPWM techniques, G-H frames and K-L frames depend on 60° and 120° coordinate systems, respectively. A comparison of five SVPWM techniques infers that SVPWM-based imaginary coordinate systems provide a simple method to calculate duty ratios. On the other hand, SVPWM can conveniently provide additional flexibility to the switching sequence of sub-sectors and switching state transitions, depending on two simple and general mapping processes. This flexibility includes redundant switching method regions and configurable duty cycles, irrespective of the inverter levels [11]. Paper [12] illustrates the SVPWM implementation of a seven-phase voltage source inverter (VSI); it depicts the complexities of developing the sectors and their dwell times. The problem with the implementation of SVPWM on MLI is that the higher number of levels are the switching states and switching patterns. Additionally, this study compares carrier-based and SVPWM for seven-phase VSI.

Manuscript [13] proposes an optimized configuration of a three-phase, T-structured, three-level inverter for drive applications with sixteen power semiconductor devices and fewer filter requirements. The component count in the above inverter is significantly higher than the normal three-level inverters. Multilevel SVPWM is learned in detail, and its fundamental distinction between SVPWM and CBPWM is outlined in [14]. Four discontinuous SSVM (DSSVM) techniques for three-level inverters were implemented in [15] to lower the switching losses and common mode voltage in the low modulation indices. Improving the linear modulation index to 1.15 is proposed in the paper [16]. Additionally, this paper analyzes the need of maximizing the modulation index with simple PWM techniques for an NPC three-level inverter that has unbalanced capacitor voltages. Article [17] introduces discontinuous synchronized modulation into multimode synchronized modulation methods for a high-power medium-voltage three-level inverter. In article [18], hybrid discontinuous modulation for three-level inverter-fed two-phase loads is covered. For CBPWM applied to a three-level NPC inverter, Article [19] suggests a new simple approach for correlating all three reference voltage signals and two dc-link capacitor voltages, respectively, to identify the injected zero-sequence voltage signal. To obtain fixed switching frequency (FSF) with low current harmonics, an improved model predictive control (MPC) approach is proposed in [20], which makes use of optimized voltage vectors and switching sequences to achieve FSF. Paper [21] analyzes pulse pattern performance and proposes a harmonic-reduced pulse pattern selection technique that accounts for a modulation index. In this study, the operation of MLI in the over-modulation region is evaluated and compared to its effectiveness in a typical modulation region [22,23]. In [24], the author undertakes an extensive study regarding the association among the SVPWM and CBPWM using an offset voltage injection. The paper [25] presents an easier, and less computational SVM technique for four-leg, three-level NPC converters. The paper [26] suggests and examines new switching sequences for a three-level inverter that remains equated to the switching patterns 1012, 2721, 0121, and 7212 for a two-level converter. The implementation of fault detection, localization, and diagnosis of Z-source inverters for vehicle applications is described in [27]. Paper [28] shows an asymmetric five-segment switching scheme for conventional two-level voltage source inverter-fed AC motor drives with FPGA-based current control logics. A carrier-based PWM template for a five-level switch-clamped cascaded H-bridge inverter is investigated in [29]. The research paper [30] proposes a hysteresis SVPWM reconfigurable fault-tolerant control technique for single-phase voltage source multilevel inverters with current tracking. The idea of employing the selective torque component elimination method is presented in article [31] in order to minimize a specific frequency of mechanical

pulsations while achieving a full range of speed control. Paper [32] aims to investigate the electrical losses noted in a five-phase synchronous reluctance motor drive system and also attempts to study the electrical losses observed in this motor.

From the above literature, it is understood that the implementation of SVPWM for higher-level MLI is a difficult task owing to the complexity that lies in the determination of switching states and redundant switches. Because of the above-mentioned challenges of SVPWM methods, segment reduction-based SVPWM is attracting much attention, particularly for MLIs. Segment reduction-based SVPWM reduces the switching state transition, which in turn decreases switch losses.

This article analyzes the performance of SVPWM-based FT^{2}LI [33] to optimize the efficacy of high-order harmonics and output waveform quality. The following are the main findings of this paper:

(a) Nine- and three-segment SVPWM algorithms different from conventional CBPWM are developed for an FT^{2}LI.
(b) The array of switching state transitions and profiles is broadly studied in detail for various SVPWM algorithms and compared with CBPWM.
(c) An analysis and comparison of the magnitude of harmonic concentration around the switching frequency in CBPWM and segment reduction-based SVPWM in FT^{2}LI are discussed.

A generalized switching scheme for FT^{2}LI based on segment reduction SVPWM is presented. By comparing carrier-based PWM techniques such as sine PWM, 60° PWM, and switching frequency optimal PWM, this technique offers reduced THD in output voltage and current with an increased fundamental output voltage that maintains the availability of a high RMS voltage at the output. Compared to CBPWM FT^{2}LI, the maximum boosted voltage is attained in SVPWM FT^{2}LI for the same modulation index with the minimum switching frequency, reduced switching loss, and inverter size. The segment reduction-based SVPWM technique is able to act under a minimum switching frequency with fewer switching losses, which improves the inverter efficiency. The structure of the manuscript is as follows: Section 2 discusses the analysis used to formulate the SVPWM technique for FT^{2}LI. The primary element of the suggested approach consists of an initiative to analyze and sector identification of SVPWM-based FT^{2}LI with segment reduction presented in this section. The implementation of SVPWM with segment reduction algorithms for four sub-sectors of sector I is outlined in Section 3. The simulation and experimental results are discussed in Section 4 to validate the SVPWM-based FT^{2}LI algorithms. Detailed performance comparisons of various PWM techniques can be found in this section. The core conclusions are presented in Section 5.

2. Implementation of SVPWM for FT^{2}LI

2.1. Diode-Free FT^{2}LI Topology

T-type and neutral point configurations are the two most common three-level inverter topologies described in the literature. For low-voltage applications, the T-NPC inverter is more cost-effective and efficient than the NPC inverter [34]. Figure 1 depicts the fundamental layout of the diode-free FT^{2}LI, which consists of three levels of output for each phase (A, B, and C) and 12 switching devices (four in each leg) with no clamping diodes. In phase A, the labels for the semiconductor devices are SA_{UU}, SA_{UL}, SA_{LU}, and SA_{LL}. Similarly, phase B and phase C can be identified.

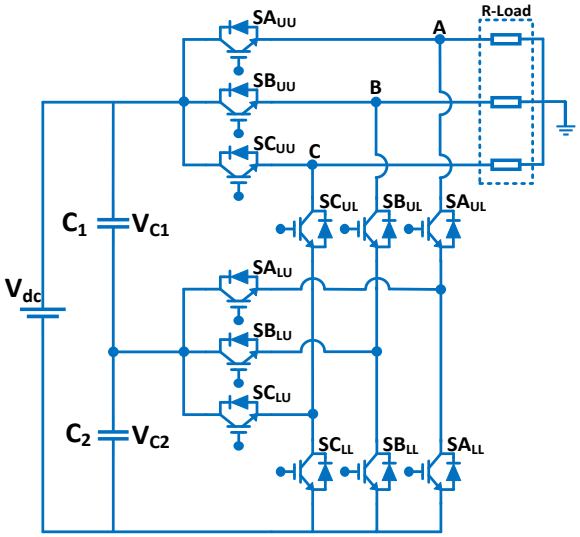


Figure 1. Structure of FT^2LI.

The DC link, which consists of two capacitors ($C_1 = C_2$), is used to couple the FT^2LI with the input dc supply. V_{c1} and V_{c2} denote the voltages of two dc link capacitors, while their values are both set to $V_{dc/2}$. The zero-voltage junction is defined as the point where two dc input sources are connected to the FT^2LI's neutral point. The FT^2LI incorporates the three operational modes in each phase, and their output voltages are listed in Table 1. Each phase arm's operation is designated by three switching states: H, 0, and L. The switching state "H" indicates that two upper arm switches (SA_{UU}, SA_{LU}) in the phase arm A are switched on; the switching state "L" indicates that two lower arm switches (SA_{UL}, SA_{LL}) in the phase arm A are switched on; and the switching state "0" indicates that two internal switches (SA_{UL}, SA_{LU}) in the phase arm A are switched on.

Table 1. Switching states of phase A.

On Devices/A Phase	Off Devices/A Phase	Switching States	Terminal Voltage
SA_{UU}, SA_{LU}	SA_{UL}, SA_{LL}	H	$+V_{dc/2}$
SA_{UL}, SA_{LU}	SA_{UU}, SA_{LL}	O	0
SA_{UL}, SA_{LL}	SA_{UU}, SA_{LU}	L	$-V_{dc/2}$

2.2. Development of the SVPWM Algorithm

Space vector PWM (SVPWM) uses sine wave as a fixed amplitude vector revolving at a fixed frequency along with a reference voltage vector (V_{ref}) that revolves at the angular frequency of $2f_f$ (fundamental frequency, $f_f = 50$ Hz) which is around the origin of the space vector diagram. Figure 2 depicts a space vector diagram of FT^2LI with three phases and three levels. This article examines SVPWM approaches for FT^2LI. It is made up of 24 active voltage vectors (6 large, 6 medium, and 12 small) and triple null vectors (HHH, 000, and LLL). The space vector diagram has been divided into six sectors (I to VI), with each sector subdivided by four triangles (1 to 4), for a total of 24 triangles. In this illustration, sector I comprises of triangles 1, 2, 3, and 4. Table 2, Refs. [30–32], present a comparative study of several three-level inverters, including PN-NPC (positive-negative NPC), T-type MLI, and 3L-ANPC ZCT (zero current transition), based on the number of components (including switches, diodes, inductors, and capacitors).

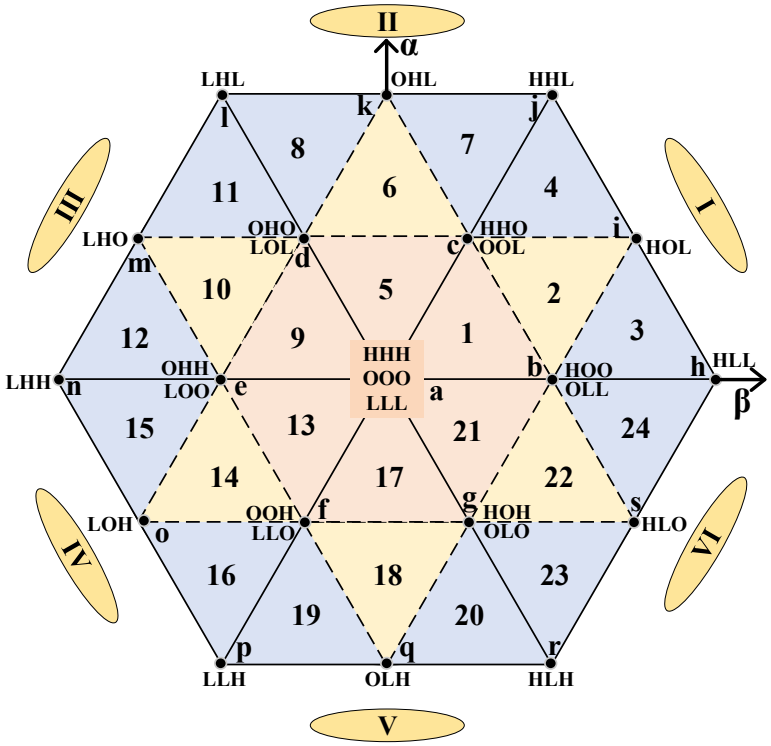


Figure 2. Space vector diagram of three-level inverter("I–VI"—Sectors, "1–24"—Subsectors).

Table 2. Conventional three-level inverter comparison with FT^{2}LI.

Parameters/Phase		PN-NPC [35]	T-Type MLI [36]	3L-ANPC ZCT [37]	FT^{2}LI
Total no of switches/phase		8	4	8	4
Voltage rating of switches/phase	V_{dc}	2	2	6	1
	$V_{dc}/2$	6	2	2	3
No. of clamping diodes		0	2	2	-
Auxiliary inductors		2	-	1	-
Auxiliary capacitors		1	-	1	-

Table 3 lists the possible switching sequences for all sub-sectors of FT^{2}LI. Space vector PWM involves identifying the sector of the reference voltage vector, detecting the three nearest switching vectors, deciding on a suitable switching sequence, and calculating the on-time of the switches for that sequence. Each major sector corresponds to $\pi/3$ of the fundamental cycle.

Table 3. Switching sequence of sub-sectors.

Sector	Sub-Sector	Switching Sequence
1	I	LLL-OLL-OOL-OOO-HOO-HHO-HHH-HHH-HHO-HOO-OOO-OOL-OLL-LLL
	II	OLL-OOL-HOL-HOO-HHO-HHO-HOO-HOL-OOL-OLL
	III	OLL-HLL-HOL-HOO-HOO-HOL-HLL-OLL
	IV	HHO-HHL-HOL-OOL-OOL-HOL-HHL-HHO
2	I	HHH-HHO-OHO-OOO-OOL-LOL-LLL-LLL-LOL-OOL-OOO-OHO-HHO-HHH
	II	LOL-OOL-OHL-OHO-HHO-HHO-OHO-OHL-OOL-LOL
	III	OOL-OHL-HHL-HHO-HHO-HHL-OHL-OOL
	IV	LOL-LHL-OHL-OHO-OHO-OHL-LHL-LOL
3	I	HHH-OHH-OHO-OOO-LOO-LOL-LLL-LOL-LOO-OOO-OHO-OHH-HHH
	II	OHH-OHO-LHO-LOO-LOL-LOL-LOO-LHO-OHO-OHH
	III	LOL-LHL-LHO-OHO-OHO-LHO-LHL-LOL
	IV	OOH-LOH-LLH-LLO-LLO-LLH-LOH-OOH
4	I	HHH-OHH-OOH-OOO-LOO-LLO-LLL-LLL-LLO-LOO-OOO-OOH-OHH-HHH
	II	LLO-LOO-LOH-OOH-OHH-OHH-OOH-LOH-LOO-LLO
	III	OHH-LHH-LOH-LOO-LOO-LOH-LHH-OHH
	IV	OOH-LOH-LLH-LLO-LLO-LLH-LOH-OOH
5	I	HHH-HOH-OOH-OOO-OLO-LLO-LLL-LLL-LLO-OLO-OOO-OOH-HOH-HHH
	II	HOH-OOH-OLH-OLO-LLO-LLO-OLO-OLH-OOH-HOH
	III	OOH-OLH-LLH-LLO-LLO-LLH-OLH-OOH
	IV	HOH-HLH-OLH-OLO-OLO-OLH-HLH-HOH
6	I	HHH-HOH-HOO-OOO-OLO-OLL-LLL-LLL-OLL-OLO-OOO-HOO-HOH-HHH
	II	HOH-HOO-HLO-OLO-OLL-OLL-OLO-HLO-HOO-HOH
	III	HOH-HLH-HLO-OLO-OLO-HLO-HLH-HOH
	IV	HOO-HLO-HLL-OLL-OLL-HLL-HLO-HOO

In any SVPWM based on a voltage-second balance equation, the set of voltage vectors representing the switching states of the inverter are applied to average a reference value in one sampling period. There are 27 transition states when three phases of the inverter are considered. Each of these transitioning states can be expressed as a vector by (1):

$$V_{ref} = V_{c\alpha} + jV_{c\beta} = \frac{2}{3}\left[V_a + (V_b \times e^{j\frac{2\pi}{3}}) + (V_c \times e^{j\frac{4\pi}{3}})\right] \quad (1)$$

where, V_a, V_b, and V_c are reference three-phase voltages of the nearest switching vectors, and $V_{c\alpha}$ and $V_{c\beta}$ are reference vector components in the coordinate system.

2.2.1. Sector Identification

Using the Clark transformation, as shown in Expression (2), the a-b-c three-phase coordinate system is converted into a 2-dimensional frame that facilitates sector identification. As shown in Figure 2, the voltage vectors are positioned at various locations on the two hexagons that are interleaved based on their switching patterns. The large voltage vectors of the three-level space vector diagram have an amplitude of 2Vdc/3 and are situated on the edges of the outside hexagon. The median voltage vector is the voltage vector with the amplitude Vdc/$\sqrt{3}$ positioned at the outer hexagon's one-half. The corners of the inner hexagon contain small vectors with amplitudes of Vdc/3.

When the rotating voltage vector enters a particular sector in a proposed inverter, nearby voltage vectors are picked to create the required rotating voltage vector based on the principle of vector synthesis, which results in three-phase PWM signals. When evaluating

the phase angle and the magnitude of a rotating reference voltage vector Vref, it is possible to ascertain the sector where the inverter output voltage (Vo*) resides.

$$\begin{bmatrix} V_{c\alpha} \\ V_{c\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

The duty values of all four switches corresponding to each phase can be determined based on the status of the two switches that are part of each limb in the applied switching states, as shown in Table 4.This table depicts corresponding line voltages and phase voltages in each phase with respect to their voltage vectors for sub-sector 1 (Δabc).

Table 4. Voltage vectors of sub-sector 1.

Switching States	Period	On Switches in Leg A	On Switches in Leg B	On Switches in Leg C	V_{AN}	V_{BN}	V_{CN}	V_{AB}	V_{BC}	V_{CA}	Voltage Vectors
LLL	$T_O/3$	SA_{UL} SA_{LL}	SB_{UL} SB_{LL}	SC_{UL} SC_{LL}	$-V_{dc}/2$	$-V_{dc}/2$	$-V_{dc}/2$	0	0	0	$V_{01} = 0$
OLL	$T_1/2$	SA_{UL} SA_{LU}	SB_{UL} SB_{LL}	SC_{UL} SC_{LL}	0	$-V_{dc}/2$	$-V_{dc}/2$	$+V_{dc}/2$	0	$-V_{dc}/2$	$V_{21} = \frac{V_{dc}}{3} \times e^{j.0}$
OOL	$T_2/2$	SA_{UL} SA_{LU}	SB_{UL} SB_{LU}	SC_{UL} SC_{LL}	0	0	$-V_{dc}/2$	0	$+V_{dc}/2$	$-V_{dc}/2$	$V_{11} = \frac{V_{dc}}{3} \times e^{j.\pi/3}$
OOO	$T_O/3$	SA_{UL} SA_{LU}	SB_{UL} SB_{LU}	SC_{UL} SC_{LU}	0	0	0	0	0	0	$V_{02} = 0$
HOO	$T_1/2$	SA_{UU} SA_{LU}	SB_{UL} SB_{LU}	SC_{UL} SC_{LU}	$+V_{dc}/2$	0	0	$+V_{dc}/2$	0	$-V_{dc}/2$	$V_{22} = \frac{V_{dc}}{3} \times e^{j.0}$
HHO	$T_2/2$	SA_{UU} SA_{LU}	SB_{UU} SB_{LU}	SC_{UL} SC_{LU}	$+V_{dc}/2$	$+V_{dc}/2$	0	0	$+V_{dc}/2$	$-V_{dc}/2$	$V_{12} = \frac{V_{dc}}{3} \times e^{j.\pi/3}$
HHH	$T_O/3$	SA_{UU} SA_{LU}	SB_{UU} SB_{LU}	SC_{UU} SC_{LU}	$+V_{dc}/2$	$+V_{dc}/2$	$+V_{dc}/2$	0	0	0	$V_{03} = 0$

2.2.2. Determination of Adjacent Vectors for V_{ref}

As indicated previously, the switching states of redundant vectors result in a similar voltage vectors at the output. The location in the reference vector must be determined before calculating the three nearest voltage vectors and their duty cycles. Where ($V_{c\alpha}$, $V_{c\beta}$) is the coordinate values of V_{ref} in α_β coordinates, (V_a, V_b, V_c) is the coordinate values of V_{ref} in a three-phase coordinate system. A V_{ref} could be identified within any sub-sector (1–4) in one of the sectors (I–VI), as depicted in Figure 3a.

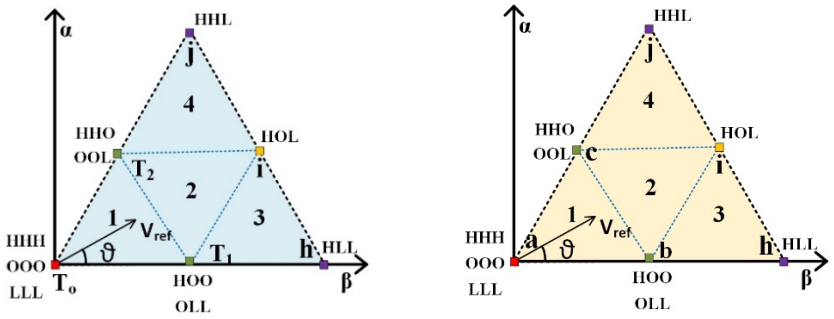


Figure 3. (**a**) Switching time representation of sub-sector 1. (**b**) Voltage vectors of sub-sector 1.

When considering the reference vector, V_{ref} is located in sub-sector 1 of sector I. The three nearest switching vectors of sub-sector 1 can be decided by the following: Volt-sec balance equation for sector I, sub-sector 1,

$$V_{ref} \times T_s = (a \times T_o) + (b \times T_1) + (c \times T_2) \quad (3)$$

where

T_s—one switching period;
T_o—vector 'a' switching time;
T_1—vector 'b' switching time;
T_2—vector 'c' switching time.

a, b, and c are the nearest voltage vectors expressed for the inner triangle of sector I, sub-sector 1, shown in Figure 3b. Voltage vector 'a' can be calculated as follows: where V_{01}, V_{02}, and V_{03} are the redundant voltage vectors of this node.

Voltage vector 'a' is equal to

$$a = \begin{cases} V_{01} \\ V_{02} \\ V_{03} \end{cases}$$

where V_{O1} = LLL, V_{O2} = OOO, V_{O3} = HHH,

Apply the Equation (1),

$$V_{01} = \frac{2}{3}\left\{\left(\frac{-V_{dc}}{2}\right) + \left(\frac{-V_{dc}}{2}\right) \times e^{\frac{j2\pi}{3}} + \left(\frac{-V_{dc}}{2}\right) \times e^{j4\pi/3}\right\}$$

$$V_{01} = 0$$

Similarly, $a = V_{01} = V_{02} = V_{03} = 0$

V_{21}, and V_{22} are the redundant voltage vectors expressed for the node 'b' of sector I, sub-asector 1, and their expressions are

$$b = \begin{cases} V_{21} \\ V_{22} \end{cases}$$

where V_{21} = OLL, V_{22} = HOO,

$$V_{21} = \frac{2}{3}\left\{0 + \left(\frac{-V_{dc}}{2}\right) \times e^{j2\pi/3} + \left(\frac{-V_{dc}}{2}\right) \times e^{j4\pi/3}\right\}$$

$$b = V_{21} = V_{22} = \frac{V_{dc}}{3} \times e^{j.0} = \frac{V_{dc}}{3} \times \begin{bmatrix} \cos(0) \\ \sin(0) \end{bmatrix}$$

V_{11}, and V_{12} are the redundant voltage vectors expressed for the node 'c' of sector I, sub-sector 1, and their expressions are,

$$c = \begin{cases} V_{11} \\ V_{12} \end{cases}$$

where V_{11} = OOL, V_{12} = HHO,

$$V_{11} = \frac{2}{3}\left\{0 + 0 + \left(\frac{-V_{dc}}{2}\right) \times e^{j4\pi/3}\right\}$$

$$V_{11} = \frac{V_{dc}}{3} \times e^{j\pi/3}$$

$$c = V_{11} = V_{12} = \frac{V_{dc}}{3} \times e^{j\pi/3} = \frac{V_{dc}}{3} \times \begin{bmatrix} \cos\left(\frac{\pi}{3}\right) \\ \sin\left(\frac{\pi}{3}\right) \end{bmatrix}$$

2.2.3. Dwell Time Calculation of Each Vector

Following the identification of the three nearest vectors, the volt-sec balance strategy can be used to compute the turn on times of the relevant vectors [38], Ref. [39], where T_s is the sampling time and T_o, T_1, and T_2 are the on times for the voltage vectors V_0, V_1, and V_2, respectively. Equation (3) can be written as follows:

$$V_{ref}T_s = V_o \times T_o + V_1 \times T_1 + V_2 \times T_2$$

where $a = V_o$, $b = V_1$, $c = V_2$.

$$T_s = T_o + T_1 + T_2 \quad (4)$$

The dwell time of the related vectors can be calculated by solving Equations (3) and (4).

$$T_o = 2x\sin\left(\frac{\pi}{3} - \vartheta\right) \quad (5)$$

$$T_1 = T_s - 2x\sin\left(\frac{\pi}{3} + \vartheta\right) \quad (6)$$

$$T_2 = 2x\sin(\vartheta) \quad (7)$$

The dwell time of all sub-sectors in sector I is represented in Table 5.

Table 5. Dwell time of sector I.

Sub-Sector	T_o	T_1	T_2
1	$2x\sin\left(\frac{\pi}{3} - \vartheta\right)$	$T_s - 2x\sin\left(\frac{\pi}{3} + \vartheta\right)$	$2x\sin(\vartheta)$
2	$2x\sin(\vartheta) - T_s$	$2x\sin\left(\frac{\pi}{3} - \vartheta\right)$	$2T_s - 2x\sin\left(\frac{\pi}{3} + \vartheta\right)$
3	$T_s - 2x\sin\vartheta$	$2x\sin\left(\frac{\pi}{3} + \vartheta\right) - T_s$	$T_s - 2x\sin\left(\frac{\pi}{3} - \vartheta\right)$
4	$2T_s - 2x\sin\left(\frac{\pi}{3} + \vartheta\right)$	$2x\sin(\vartheta)$	$2x\sin\left(\frac{\pi}{3} - \vartheta\right) - T_s$

Where $x = \sqrt{3}\frac{V_{ref}}{V_{dc}}T_s$. Similar to the method shown in this table, it is possible to calculate the on times for all the connected vectors in all other sectors.

2.2.4. Selection of Redundant Vector Arrangement for a Suitable Pattern

Next in the SVPWM implementation process is the selection of a suitable transition sequence for redundant states. This assists in balancing the DC link capacitor voltages, tolerance in fault, and decreasing the switching frequency. Table 6 displays all the possibilities of the switching pattern configurations for every sub-sector of sector I, and Figure 4a–c

depicts a graphical illustration of sub-sector 1. It displays the switching times of each switch in phase A, B, and C.

Table 6. Redundant states of sector I.

Sub-Sector		Possible Switching Sequence
1	(i)	HHH-HHO-HOO-OOO
	(ii)	LLL-OLL-OOL-OOO
	(iii)	HHO-HOO-OOO-OOL
	(iv)	HOO-OOO-OOL-OLL
2	(i)	HHO-HOO-HOL-OOL
	(ii)	HOO-HOL-OOL-OLL
3	(i)	HOO-HOL-HLL-OLL
4	(i)	HHO-HHL-HOL-OOL

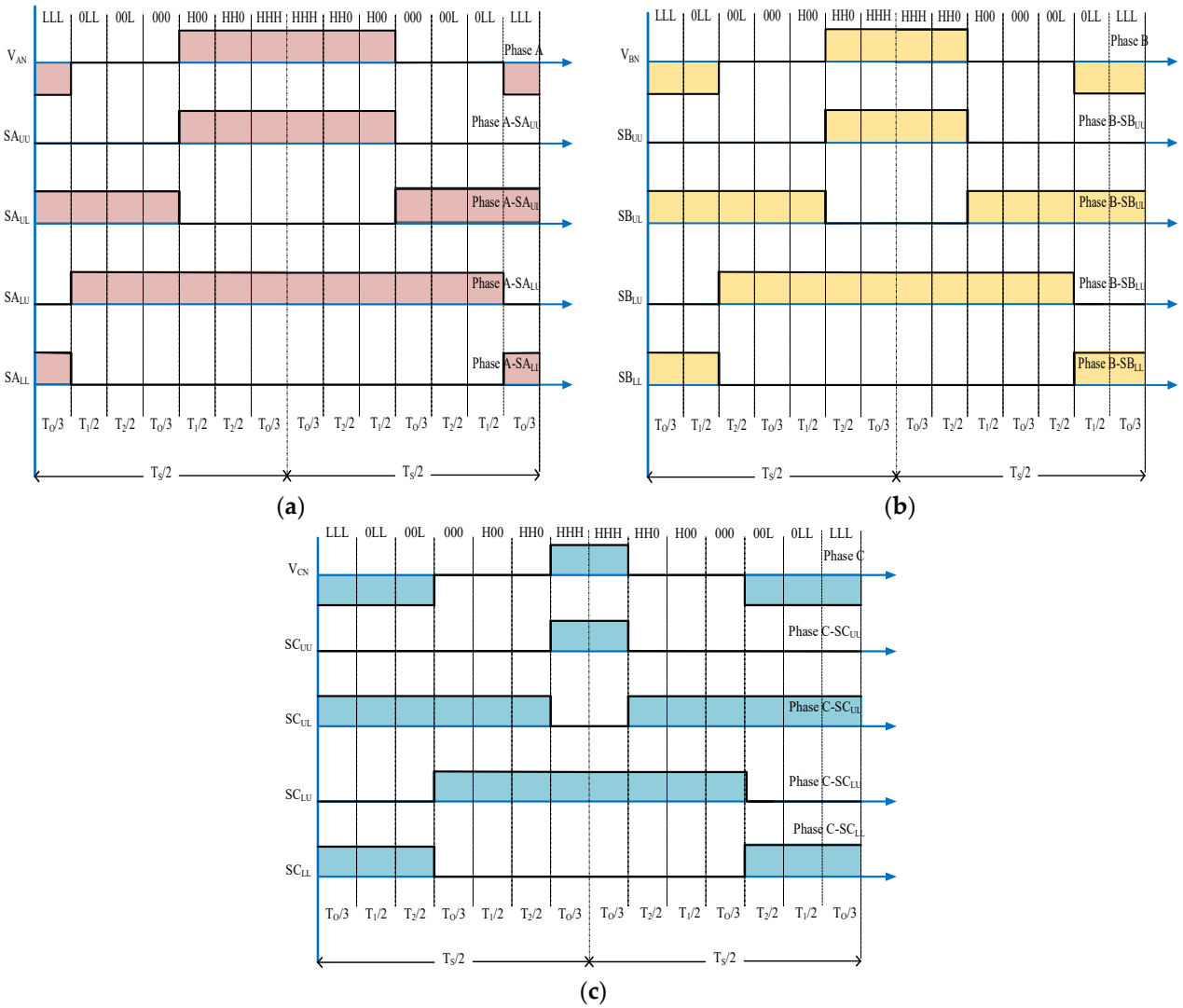


Figure 4. Switching time representation of sub-sector 1; (**a**) phase A; (**b**) phase B; (**c**) phase C.

3. Segment Reduction in SVPWM

The segment reductions in the switching sequence have been chosen for their low switching loss, their simple method for the handling of states, and the online implementation of switching sequence. In this article, three-segment- and nine-segment-based switching sequences are analyzed for sector I.

The number of voltage vectors in one switching period is used in this article to differentiate amongst the SVPWM algorithms. The following are the detailed design procedures for various SVPWMs. Figure 5 depicts a three-level inverter's typical modulation index, which has been utilized to locate the sub-sector containing the reference voltage vector. This SVPWM technique is classified into three classes based on the segment reduction count: class 1, class 2, and class 3.

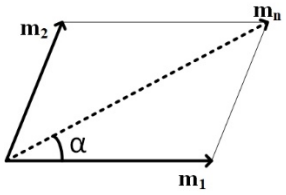


Figure 5. Modulation index of three-level SVPWM.

3.1. Segment Reduction in Sub-Sector 1 (Class 1)

For triangles like triangle Δabc in Figure 3b, where m_1 and m_2 are each less than 0.5 and $m_1 + m_2$ is less than 0.5, the triangle can be classified as a class 1 triangle. The dwell times in sub-sector 1 may be estimated by applying the inverse matrix derived from the voltage-sec balance Equations (3) and (4).

When the reference vector lies in sub sector -1 the dwell time T_0, T_1, T_2 is valid for the linear modulation of m_n = 0.5. This triangle is represented as sub-sector 1, and it shows the tip of the reference vector. By eliminating the redundant voltage vectors HH0-HHH-HHH-HH0-H00 from the middle of the vector sequence, the nine-segment SVPWM method enhances switching frequency utilization. This segment reduction was carried out for sub-sector 1, which is represented as a class 1 triangle. Figure 6a, b depict the fourteen segment and reduced nine segment switching patterns for sub-sector 1.

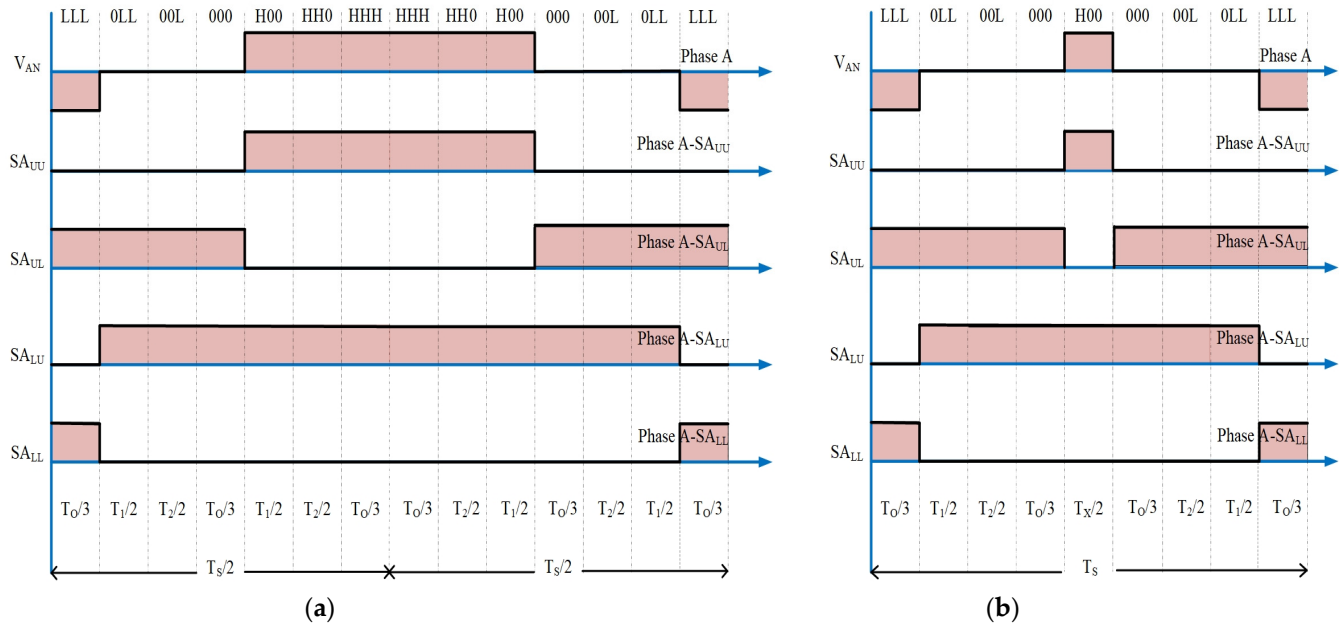


Figure 6. Phase A switching period of Δabc in sub-sector 1. (**a**) Actual fourteen segment sequence. (**b**) Reduced nine segment sequence.

3.2. Segment Reduction in Sub-Sector 2 (Class 2)

When the reference voltage (V_r) lies in sub-sector 2, in which the value of $m_1 + m_2 > 0.5$, the corresponding triangle Δbci can be called a class 2 triangle, and these m_1 and m_2 values could be less than 0.5. Figure 7a,b depicts a segment reduction technique for class 2 triangles in which the switching sequence is counted as 10 segments. For phase voltage V_{AN}, segment reduction can be implemented and reduced to a three-segment format.

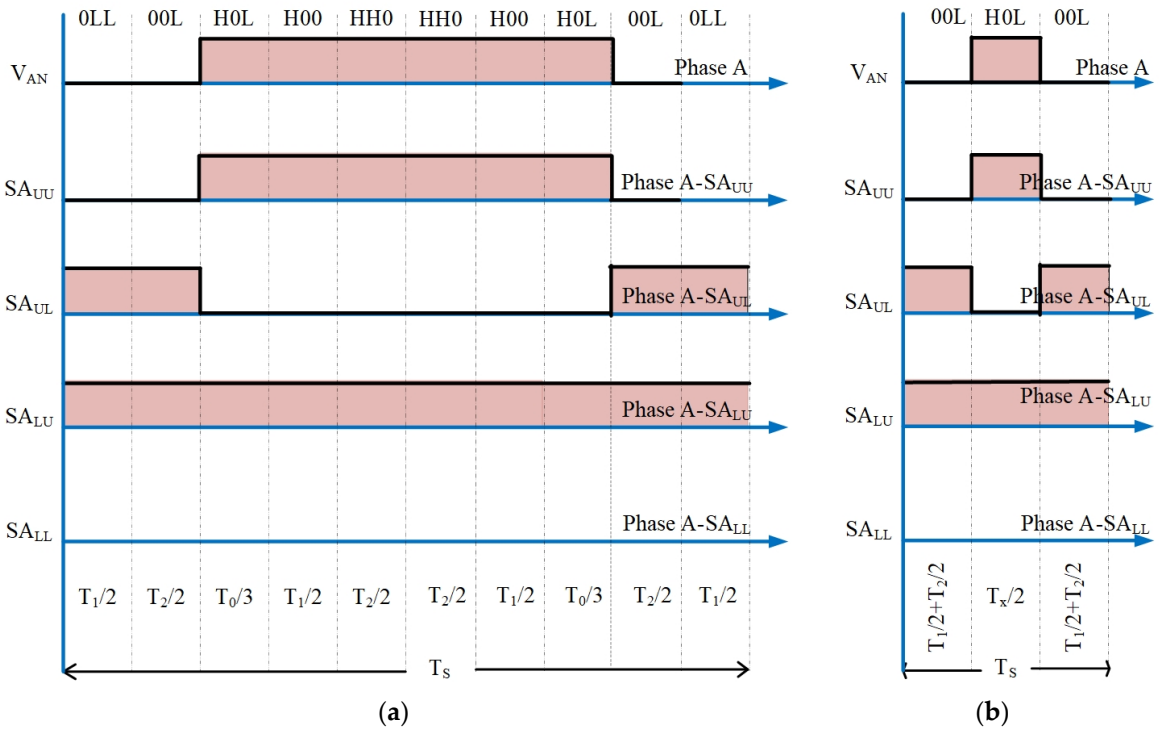


Figure 7. A switching period of Δbci in sub-sector 2. (**a**) Actual ten-segment sequence. (**b**) Reduced three-segment sequence.

3.3. Segment Reduction in Sub-Sector 3 (Class 3)

If the reference voltage (V_r) lies in sub-sector 3, in this case, the value of $m_1 \geq m_2$ and the corresponding triangle Δbhi can be called class 3 triangles, and these m_1 and m_2 values could be greater than 0.5. The actual eight-segment switching sequence for phase voltage (V_{AN}) of sub-sector 3 is depicted in Figure 8a. This segment can be reduced to a three-segment format, known as a class 3 triangle, using segment reduction. A concise SVPWM sequence with three segments is designed as shown in Figure 8b.

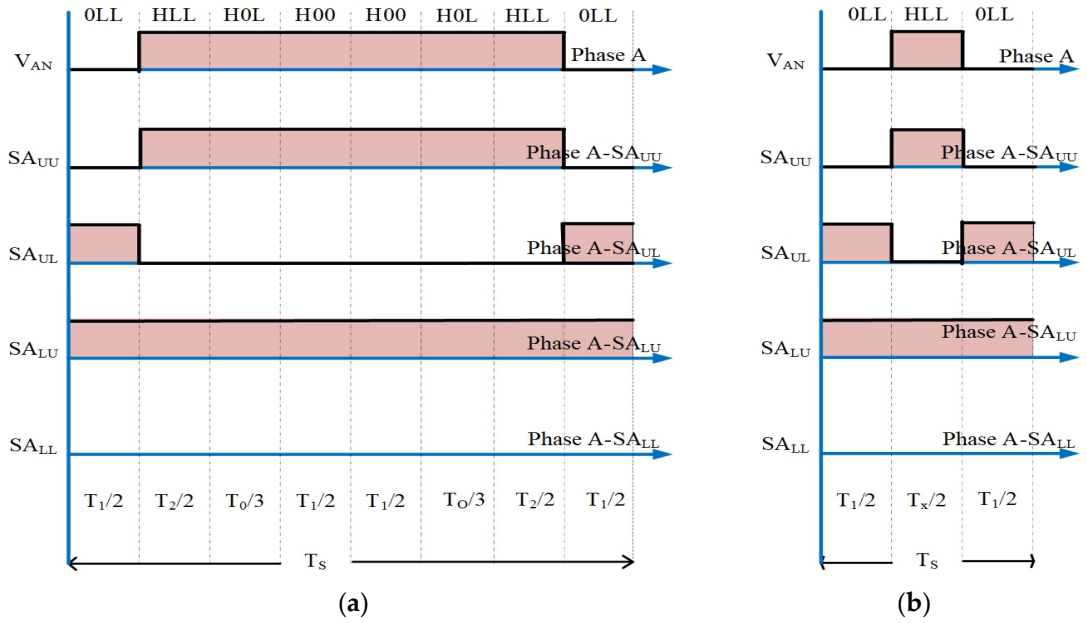


Figure 8. A switching period of Δbhi in sub-sector 3. (**a**) Actual eight-segment sequence. (**b**) Reduced three-segment sequence.

3.4. Segment Reduction in Sub-Sector 4 (Class 3)

When sub-sector 4 is the location of the reference voltage vector (V_r), the values of m_1 and m_2 may both be greater than 0.5, but m_1 must be smaller than m_2 for the triangle Δcij to fall into the class 3 mode. Figure 9 illustrates a segment reduction technique for class 3 triangles, where the actual switching sequence for sub-sector 4 is counted as eight segments and is depicted in Figure 9a. Segment reduction can be implemented for phase voltage V_{AN} and reduced to a three-segment format. Figure 9b depicts the development of a simplified three-segment SVPWM sequence for sub-sector 4.

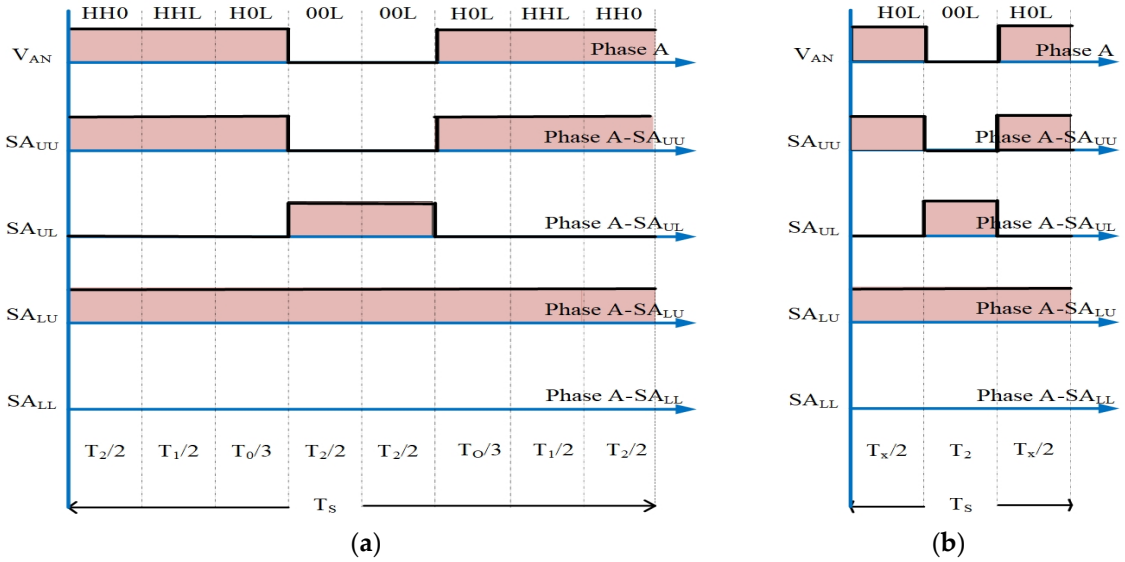


Figure 9. A switching period of Δcij in sub-sector 4. (**a**) Actual eight-segment sequence. (**b**) Reduced three-segment sequence.

4. Result Analysis and Discussion

4.1. Simulation Results

To evaluate the efficacy of FT^{2}LI, extensive simulations were conducted with the help of the proposed nine-segment and three-segment switching schemes. The SVPWM-based FT^{2}LI is simulated in MATLAB for different frequencies and amplitude modulation indices. The information thus obtained about line voltage and %THD is outlined in Table 7. In Table 8, the inference thus obtained with the application of SVPWM is compared with the outputs of carrier-based PWM methods designed for FT^{2}LI. In comparison to carrier-based PWM techniques, the SVPWM technique provides superior performance at all modulation ranges. This study examines the significance between triangle carrier-based PWM and SVPWM for FT^{2}LI. The simulation was performed with two 100 µF capacitors at a DC link voltage of V_{dc} = 400 V. The proposed class 2, three-segment reduction switching scheme was evaluated using FT^{2}LI with switching frequencies of odd and triplen, odd and not triplen, even and triplen, and even and not triplen. Figure 10a–d depicts the output voltage simulation results for FT^{2}LI at various frequency modulation indices (m_f = 63, 100, 120, and 145).

Table 7. Performance parameters of SVPWM-based FT^{2}LI.

Frequency Modulating Index (m_f)	Performance Parameters	Amplitude Modulation Index (m_a)					
		Conventional SVPWM			Proposed SVPWM		
		0.7	0.8	0.9	0.7	0.8	0.9
ODD and TRIPLEN	THD	4.55	4.81	6.32	1.11	1.49	2.66
m_f = 3150/50	V_{Fund}	302.55	344.1	379.33	323.2	369.3	410
= 63	V_{RMS}	213.9	243.3	268.2	228.5	261.2	289.9
EVEN and NON TRIPLEN	THD	3.42	3.05	2.82	0.79	0.66	1.96
m_f = 5000/50	V_{Fund}	301.9	349.8	394.5	321.9	366.3	406.8
= 100	V_{RMS}	213.5	247.38	278.99	227.6	259	287.6
EVEN and TRIPLEN	THD	3.57	1.08	0.75	0.67	0.61	1.58
m_f = 6000/50	V_{Fund}	318.8	365.57	401.37	323.4	369.3	410
= 120	V_{RMS}	225.45	258.53	283.59	228.7	261.3	289.9
ODD and NON TRIPLEN	THD	3.93	0.95	0.73	0.79	0.6	1.59
m_f = 7250/50	V_{Fund}	310.6	341.57	399.43	323.1	368.9	410.1
= 145	V_{RMS}	219.66	241.56	282.48	228.5	260.1	290

Table 8. Comparison of carrier-based and space vector PWM used for FT^{2}LI.

Frequency Modulation Index (m_f)	Performance Parameters	Amplitude Modulation Index (m_a)											
		MC-SPWM			MC-60° PWM			MC-SFO PWM			Proposed SVPWM		
		0.7	0.8	0.9	0.7	0.8	0.9	0.7	0.8	0.9	0.7	0.8	0.9
Odd and Triplen	THD	9.41	9.02	8.36	8.67	8.21	8.59	7.66	7.12	6.04	1.11	1.49	2.66
m_f = 3150/50 = 63	V_{Fund}	235	276.4	311.2	266.4	297.7	340.9	279.6	318.5	360.6	323.2	369.3	410
	V_{RMS}	166.2	195.4	220	188.3	210.5	241.1	197.7	225.2	255	228.5	261.2	289.9
Even and Non Triplen	THD	11.52	12.41	9.12	11.03	8.86	6.49	7.08	11.37	6.01	0.79	0.66	1.96
m_f = 5000/50 = 100	V_{Fund}	235	284.1	310.4	245.2	318.7	336.6	263.2	332	362.1	321.9	366.3	406.8
	V_{RMS}	166.2	200.9	219.5	173.4	225.3	238	186.1	234.8	256	227.6	259	287.6
Even and Triplen	THD	9.86	10.28	8.75	9.27	9.56	8.31	6.88	6.09	6.48	0.67	0.61	1.58
m_f = 6000/50 = 120	V_{Fund}	242.2	276.7	311.3	262.4	299	339.3	280.6	320.6	360.5	323.4	369.3	410
	V_{RMS}	171.5	195.6	220.1	185.5	211.5	239.9	198.4	226.7	254.9	228.7	261.3	289.9
Odd and Non Triplen	THD	8.84	8.55	8.03	9.36	8.72	8.35	8.15	7.46	6.83	0.79	0.6	1.59
m_f = 7250/50 = 145	V_{Fund}	240.4	279.3	311.4	262.3	301.3	338.6	281.2	319.5	360.5	323.1	368.9	410.1
	V_{RMS}	170	197.5	220.2	185.5	213.1	239.4	198.2	225.9	254.9	228.5	260.1	290

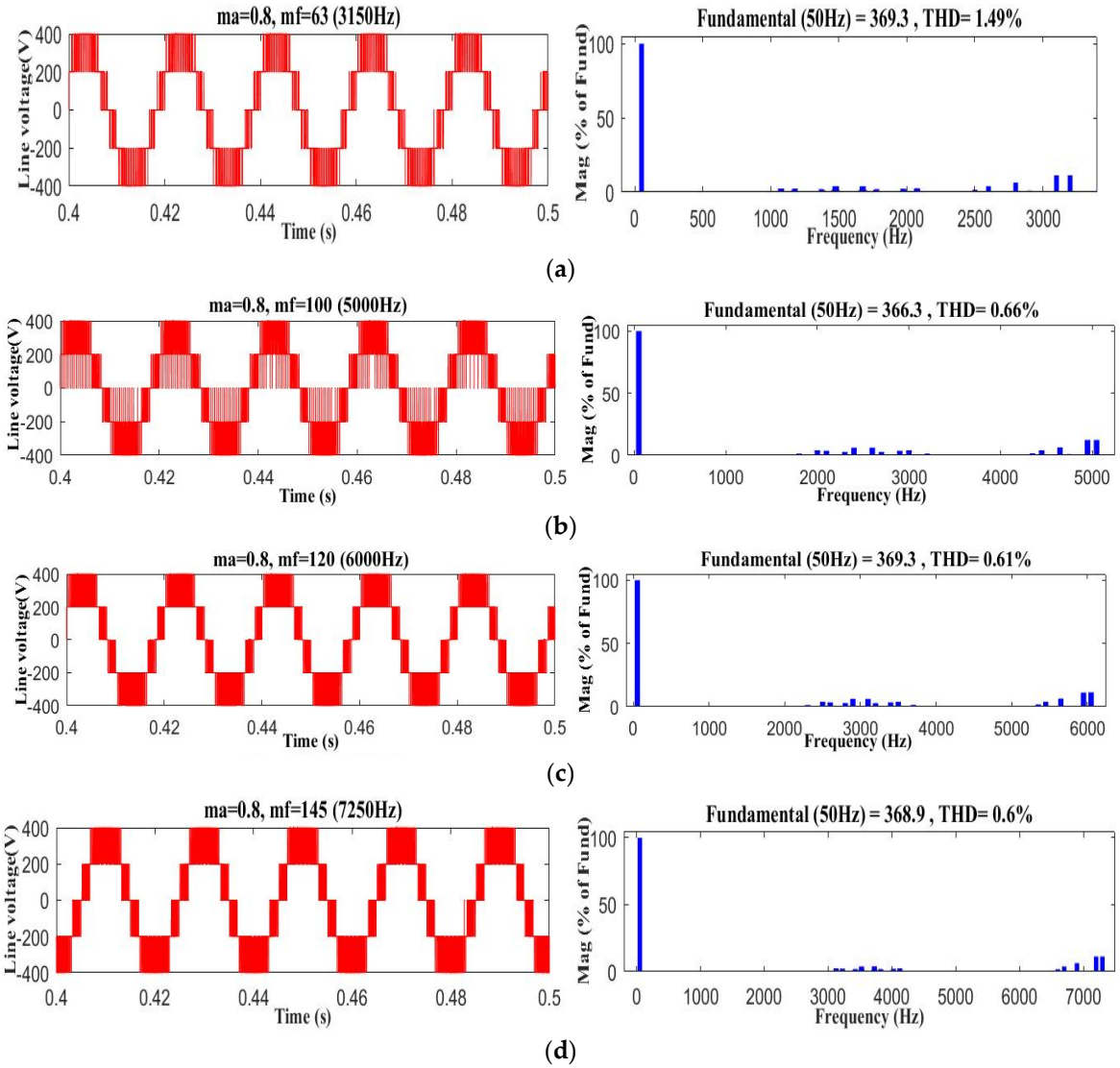


Figure 10. Simulation results of SVPWM based FT^{2}LI fr m_a = 0.8 with different frequency modulation indices (m_f): (**a**) 63, (**b**) 100, (**c**) 120, and (**d**) 145.

The simulation is performed for amplitude modulation indices of 0.7, 0.8, and 0.9 with frequency modulation indices of 63, 100, 120, and 145. The harmonic characteristics of conventional and proposed SVPWM-based FT^{2}LI are demonstrated in Table 7 for different amplitude modulation indices with various switching frequencies. It is inferred from Table 7 that the performance of FT^{2}LI with segment reduction SVPWM showcases better THD and output voltage. To highlight the features further, segment reduction-based SVPWM is compared with carrier-based PWMs such as SPWM, 60° PWM, and SFO PWM, as shown in Table 8. In addition, the outcomes are contrasted based on their THD performance and inverter output voltage. Table 8 presents a summary of the comparative study. Figure 11 depicts the maximum and minimal THD magnitudes in carrier-based PWM and SVPWM for four distinct switching frequencies. This analysis provides the highest output voltage and RMS voltage.

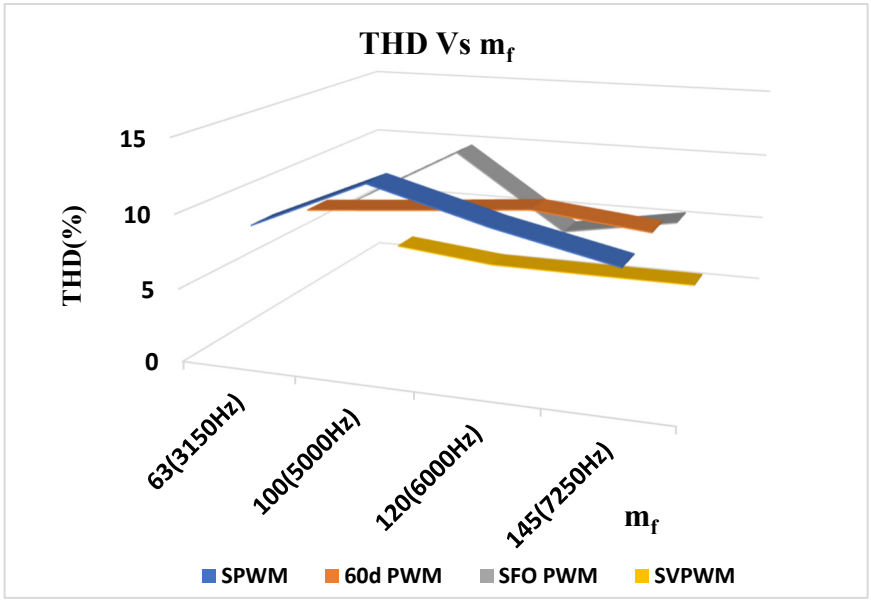


Figure 11. Comparison of THD with different PWM techniques.

4.2. Experimental Results

To validate the simulation results of a three-phase FT^{2}LI system, a 500 W prototype model was developed and tested. The test bench of the proposed system shown in Figure 12 has various components, which include two dc-link capacitors of 100 µF, 12-IGBT power switches, a SPARTAN-6 FPGA controller, and three-phase loads. A dc voltage from the programmable power supply is fed as an input to the inverter. The inverter delivers the output current to the load. Two switches from the upper arm of a phase and two switches from the lower arm of a different phase generate three-level $\pm V_{dc}$, $\pm V_{dc}/2$, and 0. The segment reduction-based SVPWM algorithm is implemented in the SPARTAN-6 FPGA controller. Using the FLUKE meter, the harmonic components of the line voltage (V_{AB}) corresponding to the segment reduction-based SVPWM algorithm have been measured up to the 146th harmonic component. It can be observed that the experimental waveforms of the line voltage V_{AB}, phase voltage V_{AN}, and harmonic spectra corresponding to a modulation index (m_a) of 0.8 are shown in Figures 13 and 14.

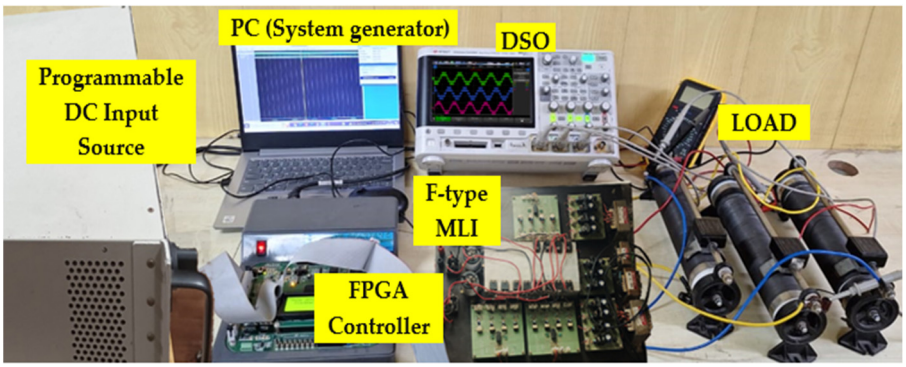
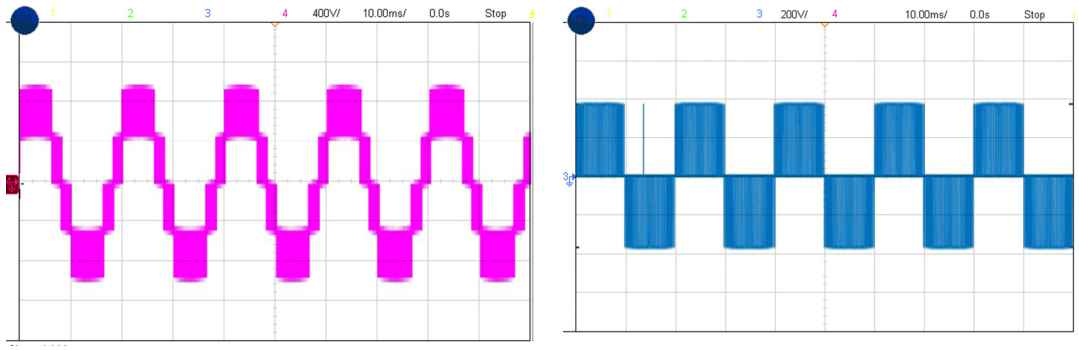


Figure 12. Experimental setup of FT^{2}LI.



(**a**) (**b**)

Figure 13. Prototype results using SVPWM at "m_a = 0.8" and "m_f = 145". (**a**) Line voltage (V_{AB}); (**b**) phase voltage (V_{AN}).

The experimental results show that the higher-order harmonics are distributed randomly between the fundamental frequency (f_f) and the switching frequency (f_{sw}). The dominant high-order harmonics of the SPWM can be observed in the cluster of harmonics distributed around h2, h22, h115, h140, and h146, respectively. Likewise, 60° PWM harmonics are distributed around h2, h99, h121, h140, and h144. The spectrum in SFO PWM is behind h2, h36, h103, h117, h138, and h146. In the vicinity of f_{sw}, the magnitude of the harmonic of SVPWM is considerably less than that of the other carrier-based PWM methods, and the cluster of the harmonic spectrum is distributed around f_{sw}. Figure 14a–d depicts that THD is greater in the three PWM techniques described above than in SVPWM. The prevalent high-order harmonics in SVPWM-based FT^{2}LI are observed to be primarily distributed around the switching frequency. When compared to the other three PWM techniques, second-order harmonics are eliminated in SVPWM, which produces good THD performance. However, because high-frequency harmonics are more readily filtered by the inductor, the THD of the line voltage in the proposed SVPWM-based FT^{2}LI is significantly lower than in conventional ones. Based on this comparison, the modulation scheme of the converter can be designed flexibly by modifying weight coefficients to meet actual performance requirements. The comparison between the conventional SVPWM MLIs and segment reduction-based SVPWM FT^{2}LIs is shown in Table 9. It is evident that the suggested converter with segment reduction-based SVPWM offers low-voltage stress across the switches, low switching loss, and eliminates the presence of even harmonics.

Table 9. Comparative study of SVPWM-based MLI's with FT^{2}LI.

Inverter Specification	**[3]**	**[13]**	**[15]**	**[25]**	**[29]**	**SVPWM-Based FT^{2}LI**
Voltage rating required for switches	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}(S_{UU}) $V_{dc}/2$(S_{UL},S_{LU},S_{LL})
Active switches/switching period	6	5	4	4	4	4
No of clamping diodes/leg	-	-	2	2	2	-
No of DC voltage sources	V_{dc}	4 V_{dc}	V_{dc}	V_{dc}	V_{dc}	V_{dc}
No of capacitors	2	4	2	2	2	2
Switching method applied	Basic modulation method	Zero common mode voltage SV method	Space vector-based hybrid PWM	Minimum switching transition principle	Double switching clamping sequence	Segment reduction Technique
Filter requirement	Medium	Low	Medium	Low	Medium	Low
Even harmonic elimination	Not applied	Not applied	Not applied	Applied	Not applied	Applied

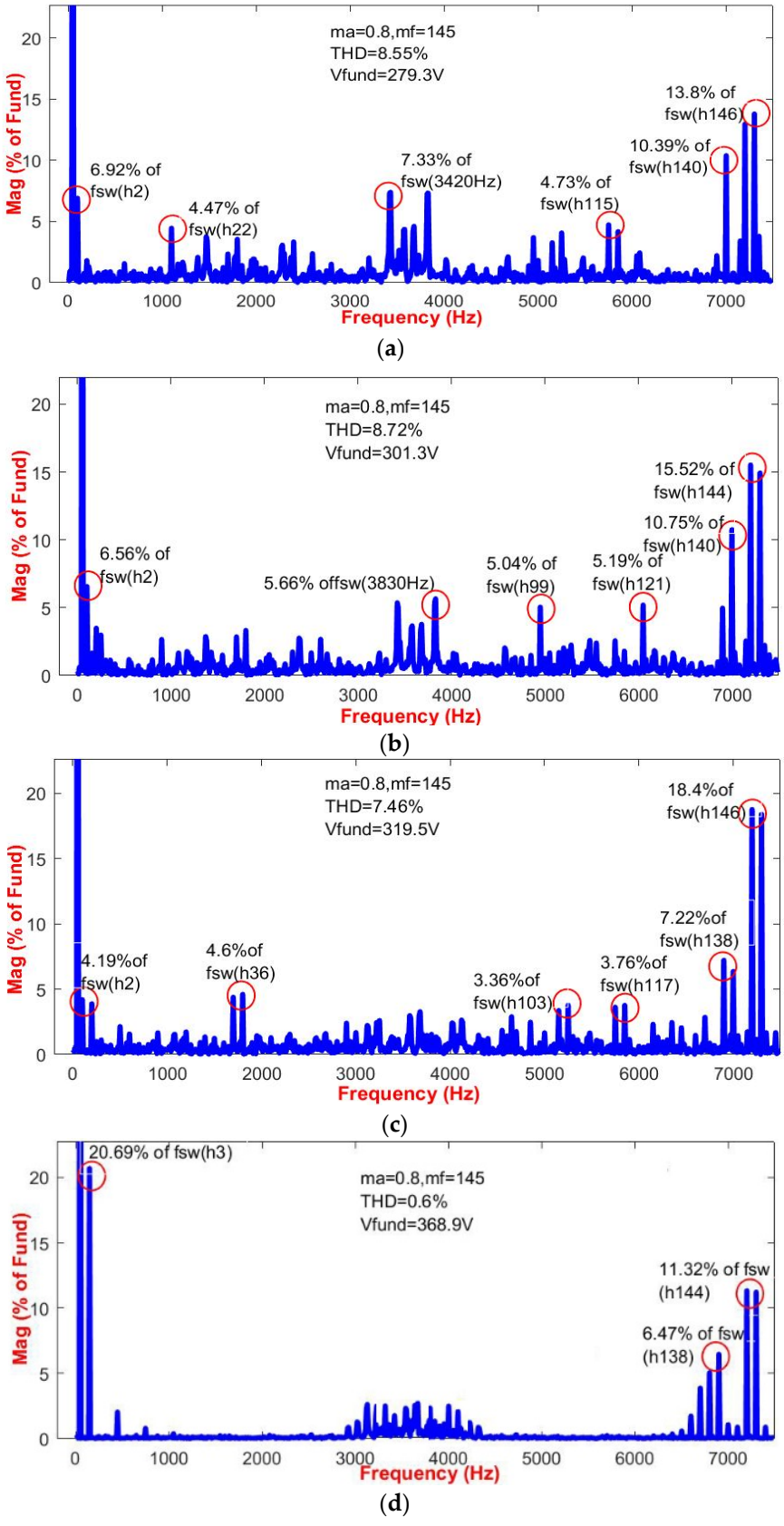


Figure 14. Harmonic spectrums comparison of the voltage V_{ab} (m_a = 0.8, m_f = 145). (**a**) SPWM. (**b**) 60° PWM. (**c**) SFO PWM. (**d**) Proposed SVPWM.

5. Conclusions

A new SVPWM technique based on segment reduction for an F-type multilevel inverter has been proposed and validated using the FT^2LI prototype fabricated in the laboratory. One of the significant features of the segment reduction-based SVPWM algorithm is the reduction of switching state transitions, which in turn reduces switching stress and losses. The total harmonic distortions with various switching frequencies at the output of segment reduction-based SVPWM-fed FT^2LI are less than those of conventional SVPWM-based FT^2LI. As compared to the existing CBPWM techniques of FT^2LI, the proposed segment reduction-based SVPWM technique offers less THD, fewer switching losses, fewer filter requirements, and reduced switching transition counts. The implementation complexity of SVPWM techniques based on the segment reduction algorithm is lower compared to the existing SVPWM approach. In addition to the above-mentioned features, the proposed segment reduction-based SVPWM for FT^2LI has a lower harmonic concentration, which shifts toward the switching frequency. Simulation and experimental results substantiate the effectiveness of segment reduction-based SVPWM algorithms for FT^2LI.

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Abbreviations

The following abbreviations are used in this manuscript:

FT^2LI	F-type three-level inverter
SVPWM	space vector pulse width modulation
CBPWM	carrier-based PWM
MC-SPWM	multi-carrier sine PWM
60° PWM	sixty-degree PWM
SFO PWM	switching frequency optimal PWM
MLIs	multilevel inverters

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