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ORIGINAL RESEARCH

Cost-effective secondary voltage control in dc shipboard integrated power system

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Abstract

Fast and dramatic voltage disturbances caused by the electric propulsion and dynamic positioning process are severe issues in the DC shipboard integrated power system (DC-SIPS). The secondary voltage control (SVC) equipped in the diesel genset (DG) and hybrid energy storage system (HESS) becomes an effective solution. However, the conventional SVC cannot distinguish the different voltage regulation characteristics between DG and HESS in a cost-effective way when allocating the voltage regulation responsibility (VRR). The cost optimization achieved by the conventional tertiary control cannot be used for the DC-SIPS due to frequent and unpredictable load fluctuations. In this paper, a cost-effective secondary voltage control is proposed to realize voltage restoration and cost minimization simultaneously. First, the voltage regulation cost model is developed considering the different voltage regulation characteristics of DG and HESS. Then, the optimization problem of VRR distribution is addressed by minimizing the total voltage regulation cost function using a quadratic programming algorithm. Moreover, the voltage regulation ability of each energy storage system is fully used with the state of charge balance. Thus, the conflict among voltage restoration, cost minimization, and SoC balance is effectively addressed. Finally, promising hardware-in-loop test results illustrate the effectiveness of the proposed method.

1 | INTRODUCTION

The increasing demands for energy conservation and emission reduction in transportation have driven the rapid development of electrification in modern marine vessels [1–3]. In the 1990s, the massive use of power electronics enabled the electrification of propulsion systems in the marine industry [4, 5]. The breakthrough of power electronic converters resulted in the further development of the vessel. In recent years, the shipboard integrated power system (SIPS) is presented, in which the power generated aboard meets the whole shipboard system including propulsion and ship service loads [6–8]. SIPS can provide an efficient, flexible, and environmentally power supply, thus becoming a promising technique in the future maritime industry.

There have been many efforts in introducing some emerging technologies into vessels to improve the system performance, such as energy storage systems (ESSs) [9, 10], photovoltaic [11], fuel cells [12, 13], and gas turbine genset [14]. Among them, ESS can flexibly support slow dynamic generators and intermittent renewable energy, thus becoming the trend of future SIPS. Moreover, as most onboard renewable energy resources are intrinsically dc type, DC-SIPS has more benefits than ac systems due to their higher efficiency, greater controllability, and no concerns on synchronization [15–17]. In this context, future DC-SIPS is expected to flexibly employ various power sources and efficiently support onboard loads with different characteristics, including dynamic and pulsed power loads [18]. For example, the propulsion system introduces power fluctuations due to the hydrodynamic interactions and wave excitations [19]. Similarly, the unique dynamic positioning (DP) process of drilling and supporting vessels causes pulsed load changing to the system [20]. Periodic large voltage disturbances are unavoidable when responding to load fluctuations, making it urgent to develop a simple and practical voltage regulation method.

To satisfy the high-voltage and high-power requirements of marine applications, several advanced controllable power

electronic converters have been designed [21, 22]. However, the fast-switching of controlled power electronic converters has potentially negative effects on reliability and robustness. Moreover, the controllable power electronic devices lead to construction cost and control complexity is also increased, which further limits their wide application in the marine industry [20]. Thus, diode rectifiers are the most popular solution to interface gensets due to their simplicity and reliability [5]. Meanwhile, controllable power electronic converters are indispensable for interfacing ESSs to the dc network. Therefore, the mixed use of uncontrollable and controllable power electronic converters in current DC-SIPS faces unique challenges for control design.

Currently, the hierarchical control architecture has become a promising technique for voltage restoration in the DC-SIPS [23]. In detail, the primary control is applied to achieve load sharing among gensets in proportion to their droop coefficients, and the residual voltage deviation can be eliminated by the secondary voltage control (SVC) [24, 25]. Traditional PI control is simple and has good control accuracy, but it is not economical to be used in the secondary control layer, especially in a multi-source system.

To distribute voltage regulation responsibility (VRR) among various sources in the secondary control layer, fixed-proportion-based secondary voltage control (FP-SVC) and frequency-division-based secondary voltage control (FD-SVC) are further proposed. In the FP-SVC [26], ESSs play a similar role as gensets, and VRR is distributed according to their reserved power. However, the advantages of ESSs in voltage regulation, such as fast response time and high ramping rate, are not exploited in these VRR distribution schemes. To solve this problem, FD-SVC [27, 28] was proposed to distribute the VRR between battery energy storage (BES) and supercapacitor storage (SCS) based on low-pass filters and high-pass filters. However, these SVC methods cannot distinguish the impact of the rated capacity on the VRR distribution, failing to achieve the voltage regulation cost optimization.

To achieve cost optimization in the voltage regulation process, several control algorithms have been investigated in a DC-SIPS, such as model predictive control (MPC) [29] and sliding mode control (SMC) [30]. MPC provides good control accuracy and handles constraints well, but it relies on advanced scheduling, which is unsuitable for the DC-SIPS with frequent and unpredictable power fluctuations. Employing the MPC leads to the primary control and the secondary control being frequently enabled, making the DC system often deviate from the optimal state [31]. Besides, SMC is robust to uncertainties and has a fast response time, but it can cause chattering. Therefore, the conflict between voltage restoration and cost minimization needs to be further analyzed and addressed.

In this paper, a cost-effective secondary voltage control (CSVC) is further proposed for the DC-SIPS equipped with diesel genset (DG) and hybrid energy storage system (HESS) to realize voltage restoration and cost minimization while guaranteeing state of charge (SoC) balance. First, the voltage regulation cost model is developed considering different voltage regulation characteristics of various sources including rated power, capacity, ramping rate, and SoC. Then, the optimization problem of VRR distribution is addressed by minimizing the total voltage regulation cost function. In this manner, the real-time total cost minimization and SoC balance are realized during the secondary voltage regulation process. The major contributions of this paper can be summarized as follows:

1) Compared with the conventional secondary control in microgrids that distributes VRR only according to the capacity of sources, the proposed CSVC comprehensively considers the power generation cost and different characteristics of various sources to realize voltage restoration.
2) In contrast to the conventional tertiary control, the proposed CSVC can realize real-time optimal VRR distribution without relying on any load information obtained in advance.
3) The proposed CSVC achieves the real-time SoC balance for HESS by setting the SoC as one of the impact factors in the voltage regulation cost model.

The rest of the paper is organized as follows. A brief description of a multi-zone DC-SIPS with hierarchical control and its voltage deviation problem is given in Section 2. Details about the proposed CSVC are highlighted in Section 3. The hardware-in-loop (HIL) test results are presented in Section 4. The last section summarizes the conclusions drawn from the investigation.

2 | SYSTEM DESCRIPTION AND MODELLING

An introduction of the multi-zone DC-SIPS structure is described in this section. Based on this system, the detailed models of DG and propulsion system are established in the following. Using this model, the voltage regulation issue with only droop control is illustrated in detail.

2.1 | Multi-zone DC-SIPS structure

Ensuring fault tolerance and reconfiguration capability is the most important rule of the DC-SIPS [20]. Thus, a DC-SIPS should have at least two independent subsystems to keep the vessel always in position. A typical multi-zone DC-SIPS is shown in Figure 1, where gensets are the main sources to supply power to the electric propulsion systems and service loads. Meanwhile, HESS is employed as the auxiliary source to balance the generation and demand sides. In this DC-SIPS, the port-side and starboard of each subsystem can be equivalent to a simplified single-bus microgrid, as presented in Figure 2.

2.2 | System modelling

So far, a diesel engine with a synchronous generator (SG) is the mainstream choice for the DC-SIPS, as displayed in Figure 3 [20]. The mechanical model can be developed by a

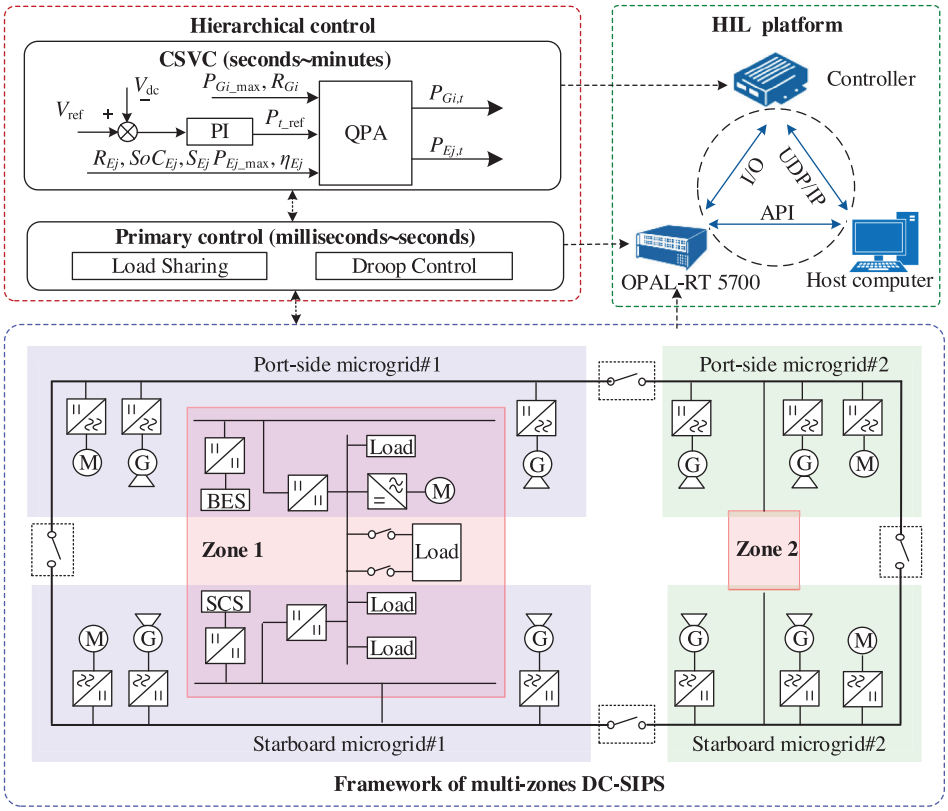

FIGURE 1 A multi-zone DC-SIPS with hierarchical control architecture. SIPS, shipboard integrated power system.

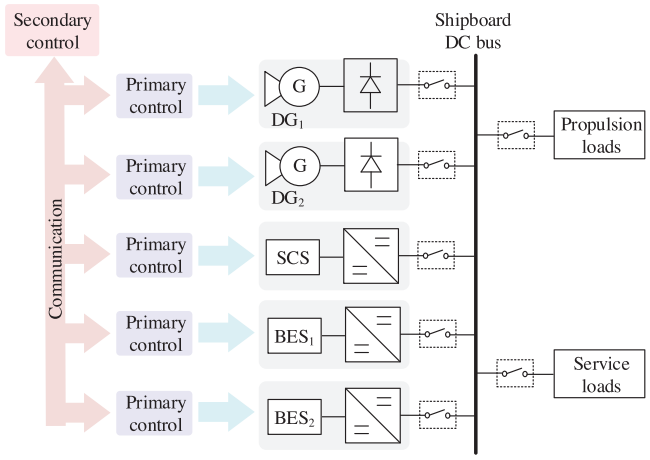

FIGURE 2 Single-bus structure of a microgrid in DC-SIPS with hierarchical control. SIPS, shipboard integrated power system.

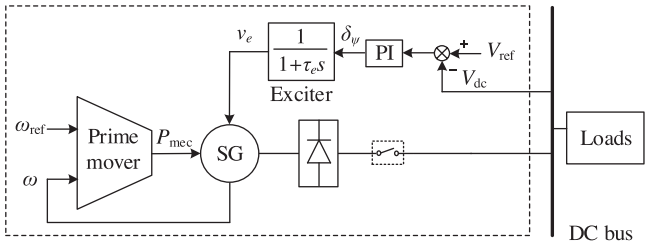

FIGURE 3 DG control scheme. DG, diesel genset.

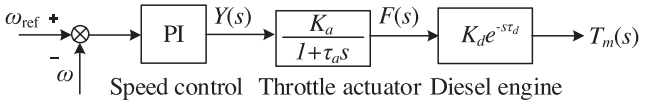

FIGURE 4 Mechanical model of DG. DG, diesel genset.

PI controller, throttle actuator, and engine delay, as shown in Figure 4, expressed as

$$T_m(s) = \frac{K_a}{1+\tau_a s} \times K_d e^{-s\tau_d} \times Y(s) \tag{1}$$

where T_m is the mechanical torque, K_a is the actuator gain, K_d is the diesel engine torque gain, τ_a is the time constant, and $Y(s)$ is the fuel index set by the speed controller. The time delay τ_d is half of the cylinder firing period.

The exciter enables DG to be an automatic voltage regulator, which stabilizes the output voltage of the SG by controlling the excitation current. The voltage regulation principle of the DG can be formulated as (2) to (4).

$$v_e = \delta_\psi / (1 + \tau_e s) \tag{2}$$

$$V_m = \omega_e L_m I_e == \sqrt{V_{ds}^2 + V_{qs}^2}\Big|_{I_{ds}=I_{qs}=0} \tag{3}$$

$$V_{dc} = \frac{3}{\pi}\left(\sqrt{3}\omega_e L_m I_e + \sqrt{3}\omega_e \delta_\psi - \omega_e L_s I_{dc}\right) \tag{4}$$

where

$$V_{ds} = R_{ds}I_{ds} - \omega_e L_{qs} I_{qs} \tag{5}$$

$$V_{qs} = R_{qs}I_{qs} + \omega_e L_{ds} I_{ds} + \omega_e L_m I_e \tag{6}$$

$$\delta_\psi = K_p + \left(V_{ref} - V_{dc}\right) + K_i \int \left(V_{ref} - V_{dc}\right) dt \tag{7}$$

where V_{dc} is the nominal DC bus voltage, V_{ref} is the DC voltage reference, v_e is the exciter voltage, V_m is the peak value of phase voltage, ω is the rotating speed (rad/s), ω_{ref} is the rotating speed reference, ω_e is the electrical angular speed, δ_ψ is the control signal of the exciter, L_m is the magnetizing inductance of the SG, L_s is the stator inductance, I_{dc} is the average value of output DC current. I_e is the excitation current, τ_e is the time constant of the exciter, P_{mec} is the mechanical power, K_p and K_i are the proportional gain and integral coefficient of the PI controller, respectively. V_{ds}, V_{qs}, I_{ds}, I_{qs}, R_{ds}, R_{qs}, L_{ds}, and L_{qs} are the stator voltage, current, resistance, and inductance components expressed in the *d-q* reference frame, respectively.

Moreover, the DC-SIPS experiences large power fluctuations from the drive shaft due to the propeller rotational motion and waves. The propeller hydrodynamics and the motor are mechanically coupled, influencing each other through internal feedback. Then, the propeller model can be established as

$$P_{PR} = K_T \rho D^5 n^3 \tag{8}$$

where P_{PR} is the power demand of the propeller, K_T is the torque coefficients, ρ is the density of water (kg/m^3), D is the diameter of the propeller (m), and n is the propeller shaft speed (rpm).

Furthermore, to improve the efficiency and reliability of the DC-SIPS, ESS and associated management technologies are necessary. In marine applications, batteries take a majority of the existing shipboard ESSs because of their high energy density. Meanwhile, supercapacitors-based or flywheels-based ESSs are also gaining popularity in high-power density applications, especially in response to pulsed loads [32]. Since marine applications have high requirements on both transient power and capacity, a HESS consisting of batteries and supercapacitors is a promising solution in voltage regulation scenarios.

2.3 | Voltage regulation issue

As shown in Figure 1, hierarchical control architecture is a promising technique in the field of DC-SIPS to enhance the system performance. In general conditions, the mature droop control is employed as the primary control layer for the DG to realize VRR distribution in proportion to the droop coefficient, Then, the relation between the V_{dc} and voltage reference V_{ref} can be expressed as

$$V_{dc} = V_{ref} - k_{Gi} P_{Gi\text{out}} \tag{9}$$

where P_{Gi_out} is the output power of the ith DG, k_{Gi} is the droop coefficient of the ith DG.

As indicated by (9), the voltage deviation between V_{dc} and V_{ref} cannot be eliminated by droop control, which has negative impacts on achieving system-level interconnection. Thus, the SVC is necessary when distributing VRR P_{t_ref} among sources.

Several secondary control schemes can eliminate the bus voltage deviation by distributing VRR according to the capacity [33], [34]. This means that the source with a larger capacity will be allocated more power. However, large capacity does not mean cheap power generation. Therefore, the power generation cost model with different voltage regulation characteristics of DGs and ESSs will be analyzed in the following section. Then, the CSVC is further proposed on the secondary layer to achieve voltage restoration while guaranteeing cost minimization.

3 | PROPOSED COST-EFFECTIVE SECONDARY VOLTAGE CONTROL DESIGN

In this section, the voltage regulation cost function is established to reveal the effect of different characteristics of various sources on the voltage regulation cost. Then, the optimization problem of VRR distribution is defined to minimize the total voltage regulation cost using a quadratic programming algorithm (QPA) with the constraints of power tracking and operation characteristics. It is worth noting that the sensitivity analysis of various system parameters is not considered here, but the relevant analysis results can be easily found in recent research results [35, 36].

3.1 | Voltage regulation cost function

Generally, the voltage regulation loss of DG mainly comes from fuel cost, which can be equivalent to the quadratic function of the output power, as described in (10). Similarly, according to the non-linear relationship between voltage regulation loss and SoC of the ESS, the ESS voltage regulation loss function considering SoC as the impact factor is expressed as (11).

$$C_{Gi,t} = a_{Gi} P_{Gi,t}^2 \tag{10}$$

$$C_{Ej,t} = a_{Ej} P_{Ej,t}^2 + b_{Ej} {S_{Ej}}^2 \left(SoC_{Ej,t} - {SoC_{Ej}}_{\text{ref}}\right)^2 \tag{11}$$

where $C_{Gi,t}$ is the voltage regulation cost of the ith DG at the tth moment. $C_{Ej,t}$ is the voltage regulation cost of the jth ESS at the tth moment. $P_{Gi,t}$ is the output power reference of the ith DG to regulate voltage at the tth moment. $P_{Ej,t}$ is the output power reference of the jth ESS to regulate voltage at the tth moment, $P_{Ej,t}$ is positive when ESS is discharging, and negative when ESS is charging. S_{Ej} is the rated capacity of the jth ESS. Coefficients a_{Gi} represent the weight coefficient of the voltage regulation cost of the ith DG due to power deviation ($a_{Gi} > 0$). a_{Ej} ($a_{Ej} > 0$) is the weight coefficient of the voltage regulation cost of the jth ESS due to power deviation. b_{Ej} ($b_{Ej} > 0$) is the weight coefficient of

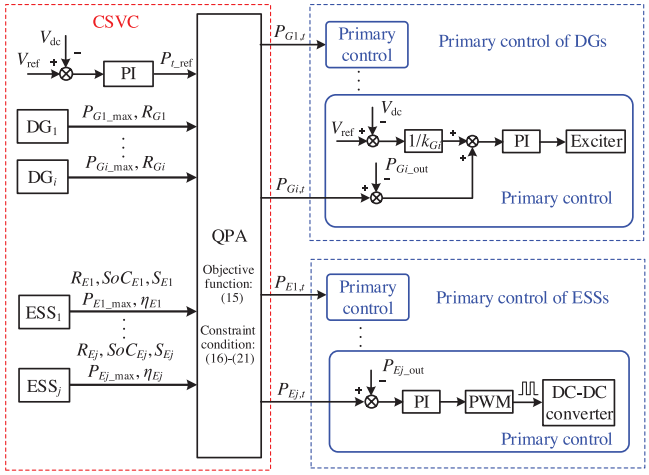

FIGURE 5 The proposed CSVC considering different voltage regulation characteristics among DGs and ESSs. CSVC, cost-effective secondary voltage control; DG, diesel genset.

the voltage regulation cost of the jth ESS due to SoC deviation. SoC_{Ej_ref} is the SoC reference representing the optimal state of the jth ESS.

Furthermore, the real-time SoC can be calculated as

$$SoC_{Ej,t} = \begin{cases} SoC_{Ej,t-1} - \eta_{Ejc} P_{Ej,t} \Delta t / S_{Ej}, & P_{Ej,t} < 0 \\ SoC_{Ej,t-1} - (P_{Ej,t}/\eta_{Ejd}) \Delta t / S_{Ej}, & P_{Ej,t} > 0 \end{cases} \tag{12}$$

Then, the regulation cost of ESS can be rewritten as (13), which is in the form of a quadratic function without the variable SoC.

$$C_{Ej,t} = \begin{cases} \alpha_{Ej\_c} P_{Ej,t}^2 + \beta_{Ej,t\_c} P_{Ej,t} + \gamma_{Ej,t\_c}, & P_{Ej,t} < 0 \\ \alpha_{Ej\_d} P_{Ej,t}^2 + \beta_{Ej,t\_d} P_{Ej,t} + \gamma_{Ej,t\_d}, & P_{Ej,t} > 0 \end{cases} \tag{13}$$

where

$$\begin{cases} \alpha_{Ej\_c} = a_{Ej} + b_{Ej} (\eta_{Ej\_c} \Delta t)^2 \\ \beta_{Ej,t\_c} = -2 b_{Ej} S_{Ej} (SoC_{Ej,t-1} - SoC_{Ej\_ref}) \Delta t \eta_{Ej\_c} \\ \gamma_{Ej,t\_c} = \gamma_{Ej,t\_d} = b_{Ej} {S_{Ej}}^2 (SoC_{Ej,t-1} - SoC_{Ej\_ref})^2 \\ \alpha_{Ej\_d} = a_{Ej} + b_{Ej} (\Delta t / \eta_{Ej\_d})^2 \\ \beta_{Ej,t\_d} = -2 b_{Ej} S_{Ej} (SoC_{Ej,t-1} - SoC_{Ej\_ref}) \Delta t / \eta_{Ej\_d} \end{cases} \tag{14}$$

where, η_{Ej_c} and η_{Ej_d} represent the charge and discharge efficiency of the jth ESS, respectively.

3.2 | Definition of optimization problem

According to the cost model, the implementation diagram of the proposed CSVC is depicted in Figure 5. The objective function of VRR distribution can be defined as an optimization problem to minimize the total voltage regulation cost, and the objective function is expressed as (15). The optimized variables $P_{Gi,t}$ and $P_{Ej,t}$ obtained by the QPA are assigned to each DG and ESS, respectively.

$$\min \left\{ \sum_{i=1}^{I} C_{Gi,t} \left(P_{Gi,t} \right) + \sum_{j=1}^{J} C_{Ej,t} \left(P_{Ej,t} \right) \right\} i \in I, j \in J \tag{15}$$

To ensure the tracking accuracy, the distribution results should be equal to the VRR, which can be expressed as

$$\sum_{i=1}^{I} P_{Gi,t} + \sum_{j=1}^{J} P_{Ej,t} = P_{t\_ref} \tag{16}$$

Also, each power source involved in CSVC is constrained by its voltage regulation characteristics, such as rated power, ramping rate, and real-time SoC as (17) to (21).

$$P_{Gi\,min} \le P_{Gi,t} \le P_{Gi\,max} \tag{17}$$

$$R_{Gi\,min} \le \frac{P_{Gi,t} - P_{Gi,t-1}}{\Delta t} \le R_{Gi\,max} \tag{18}$$

$$P_{Ej\,min} \le P_{Ej,t} \le P_{Ej\,max} \tag{19}$$

$$R_{Ej\,min} \le \frac{P_{Ej,t} - P_{Ej,t-1}}{\Delta t} \le R_{Ej\,max} \tag{20}$$

$$SoC_{Ej\,min} \le SoC_{Ej,t} \le SoC_{Ej\,max} \tag{21}$$

where P_{t_ref} is the VRR reference at the tth moment. P_{Gi_min}, P_{Gi_max}, P_{Ej_min}, and P_{Ej_max} are the minimum and maximum output power of the ith DG and jth ESS, respectively. R_{Gi_min}, R_{Gi_max}, R_{Ej_min}, and R_{Ej_max} are the minimum and maximum ramping rate of the ith DG and jth ESS, respectively. SoC_{Ej_min} and SoC_{Ej_max} are the minimum and maximum real-time SoC of the jth ESS.

3.3 | Solution to optimization problem

The proposed optimization problem can be transformed into a standard form of the quadratic programming as (22), where the objective function is a multivariate quadratic function with linear constraints. The QPA can be applied to solve the convex optimization problem and obtain the globally optimal solution.

$$\min_{\mathbf{x}} \left(\frac{1}{2} \mathbf{x}^{\mathrm{T}} \mathbf{H} \mathbf{x} + \mathbf{f}^{\mathrm{T}} \mathbf{x} \right) \quad s.t. \begin{cases} \mathbf{A}\mathbf{x} = \mathbf{b} \\ \mathbf{l} \le \mathbf{x} \le \mathbf{u} \end{cases} \tag{22}$$

where $\boldsymbol{x} = [P_{Gi,t}, P_{Ej,t}]$‘($i \in I, j \in J$) is a free variable, $\boldsymbol{H}$ and $\boldsymbol{f}$ are the quadratic coefficient matrix and the linear coefficient

column vector of the objective function, respectively, corresponding to a_{Gi}, α_{Ej}, and $\beta_{Ej,t}$ in (10), (13), and (14). $\boldsymbol{A}$ is the row vector of equality constraint coefficients. $\boldsymbol{b}$ is the right vector of the equality constraint corresponding to P_{t_ref}, $\boldsymbol{l} = [l_{Gi,t}, l_{Ej,t}]'$ and $\boldsymbol{u} = [u_{Gi,t}, u_{Ej,t}]'$ are the lower and upper bounds of the inequality constraints.

$$l_{Gi,t} = \max\left(P_{Gi\,\min}, P_{Gi,t-1} + R_{Gi\,\min}\Delta t\right) \tag{23}$$

$$u_{Gi,t} = \min\left(P_{Gi\,\max}, P_{Gi,t-1} + R_{Gi\,\max}\Delta t\right) \tag{24}$$

$$l_{Ej,t} = \max\left(P_{Ej\,\min}, S_{Ej}\frac{SoC_{Ej,t-1} - SoC_{Ej\,\max}}{\Delta t}, P_{Ej,t-1} + R_{Ej\,\min}\Delta t\right) \tag{25}$$

$$u_{Ej,t} = \min\left(P_{Ej\,\max}, S_{Ej}\frac{SoC_{Ej,t-1} - SoC_{Ej\,\min}}{\Delta t}, P_{Ej,t-1} + R_{Ej\,\max}\Delta t\right) \tag{26}$$

When solving (22), all DGs or ESSs have the same marginal cost without reaching the limitations defined by (17) to (21). The marginal cost of ESSs under the discharging condition is given by (27). In the QPA, the variable $\lambda_{Ej,t}$ is the system cost estimate of jth ESS, and the algorithm aims to reach an optimal consensus value among all the ESSs on the system cost presented as (28). The variable $\lambda_{Ej,t}$ is also the input signal for the ESS dispatch $P_{Ej,t}$ expressed as (29). It shows that if all $\lambda_{Ej,t}$ converge to $\lambda_{t\_\max}$, the distributed dispatch converges to the centralized dispatch. Assuming the weight coefficient α_{Ej_d} is constant, (14) shows that the impact on β_{Ej,t_d} mainly comes from the SoC stabilizer. Combining (14) and (29), it can be obtained that for the same $\lambda_{Ej,t}$, ESS with high SoC will be turned to discharging whereas ESS with low SoC will be turned to charging, which facilitates the SoC balance.

$$\lambda_{t\,\max} = \frac{\partial C_{Ej,t}}{\partial P_{Ej,t}} = 2\alpha_{Ejd}P_{Ej,t} + \beta_{Ej,td} \tag{27}$$

$$\lambda_{Ej,t} \to \lambda_{t\,\max}, \forall j \tag{28}$$

$$P_{Ej,t} = \left(\lambda_{Ej,t} - \beta_{Ej,td}\right) / \left(2\alpha_{Ejd}\right) \tag{29}$$

A flowchart provided in Figure 6 summarizes the proposed adaptive scheme. First, the output power and SoC at the last moment are updated for over-charge/over-discharge protection. If the constraints given in (17) to (21) are satisfied, the voltage deviation ΔV can be measured to obtain the sum of VRR. Then, the optimal objective function is set up to distribute the VRR among various sources using QPA. After that, the SoC is updated according to the actual output power of each ESS at tth moment, and thus the voltage regulation cost at this moment can be calculated.

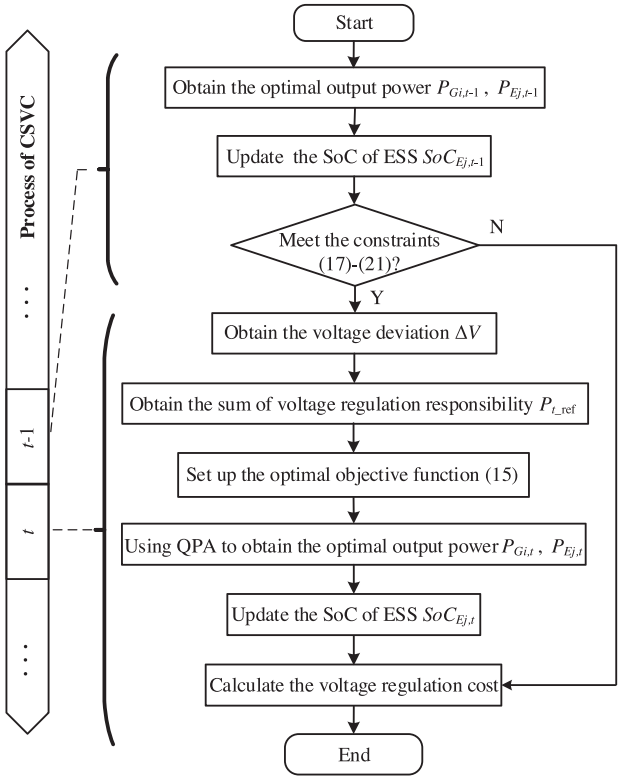

FIGURE 6 Voltage regulation cost calculation process.

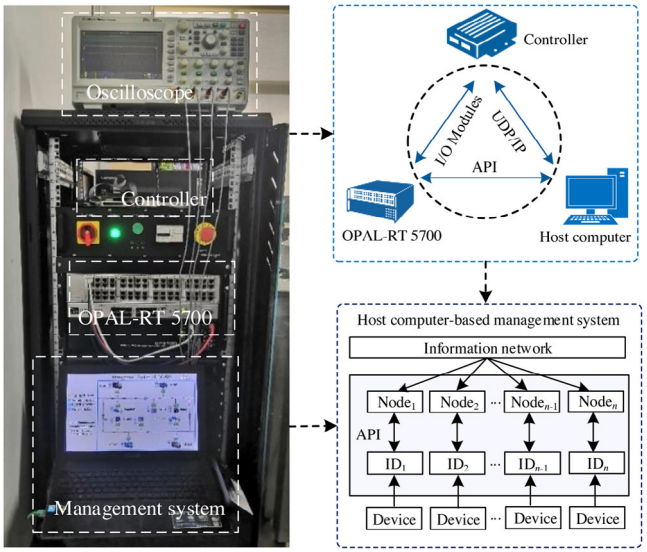

FIGURE 7 HIL platform of the DC-SIPS with CSVC. CSVC, cost-effective secondary voltage control; HIL, hardware-in-loop; SIPS, shipboard integrated power system.

4 | EXPERIMENTAL VALIDATION

To further verify the performance of the ship dynamic model and the proposed CSVC, a DC-SIPS HIL platform with the same configuration illustrated in Figure 1 is established, as presented in Figure 7. The target machine employed in the HIL platform is OPAL-RT 5700 real-time simulator. As shown in

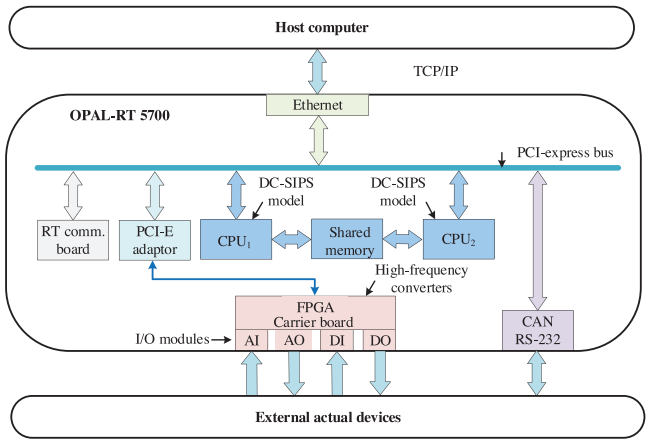

FIGURE 8 RT-LAB 5700 system.

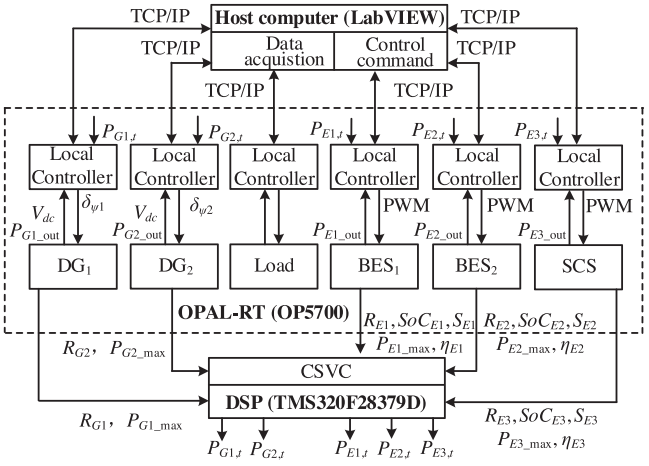

FIGURE 9 HIL platform implementation architecture. HIL, hardware-in-loop.

Figure 8, the simulator consists of an upper section containing analogue and digital input/output (I/O) signal modules, and a bottom section containing a multi-core processor computer and a field-programmable gate array (FPGA) chip [37, 38]. The minimum simulation step size of the OPAL-RT processor is 10 μs to ensure fast and accurate calculation. FPGA in OPAL-RT can further reduce the simulation step size to even nanoseconds to show the best real-time performance of the high-frequency power electronic devices in the DC-SIPS. Moreover, the expandability is enhanced by the presence of six peripheral component interconnect (PCI) expansion slots, allowing the connection of external actual devices. Apart from high-speed I/O modules, OPAL-RT also provides Ethernet and RS-232 as the communication interfaces, supporting multiple industrial communication protocols.

The full schematic of the HIL platform is composed of the developed host computer-based management system, the simulated DC-SIPS in OPAL-RT 5700, and the proposed CSVC in actual DSP controller TMS320F28379D. As shown in Figure 9, the physical models of DG, ESS, converters, and local control strategy are implemented in the OPAL-RT real-time simulator

TABLE 1 Characteristics of HESS.

Parameters	SCS	BES_1	BES_2
Rated capacity	25 kWh	204 kWh	170 kWh
Power limit	700 kW	300 kW	250 kW
Ramping limit	± 2000 kW/s	± 80 kW/s	± 60 kW/s
Efficiency	0.98	0.95	0.95
Cost coefficient a_j	0.8	0.4	0.4
Cost coefficient b_j	0.8	0.6	0.6

BES, battery energy storage; HESS, hybrid energy storage system; SCS, supercapacitor storage.

TABLE 2 Characteristics of DGs.

Composition	DG_1	DG_2
Power limit	700 kW	140 kW
Ramping limits	±50 kW/s	±20 kW/s
Cost coefficient a_i	0.8	1

DG, diesel genset.

TABLE 3 Electrical and control parameters of DC system.

Parameters	Value
Rated DC bus voltage V_{ref}	1500 V
Rated propulsion power P_L	625 kW
Droop coefficient of DG_1 k_1	0.21
Droop coefficient of DG_2 k_2	1.07
Switching frequency	10 kHz
Time interval of voltage regulation Δt	0.1 s
Proportion item of power controller	15
Integral item of power controller	3000
Proportion item of the secondary controller	1.5
Integral item of the secondary controller	30

DG, diesel genset.

to show the actual behaviours of the DC-SIPS. The CSVC is downloaded to the DSP controller to distribute VRR between DG and HESS. To meet the real-time requirements in the communication system, the high-speed I/O hardware interfaces are used to connect the external controller and the simulator. Then, the main functions of the host computer-based management system are data acquisition and control commands, in which the different load conditions are triggered and the experimental waveforms are collected through an application programming interface (API). As shown in Figure 7, each device involved in the voltage control must be configured with a unique identifier called device ID, and the communication network contains n network nodes. With the application of API, the bidirectional mapping relation between the ship device ID and the network node is established.

The system electrical and control parameters are given in Tables 1 to 3. First, the effectiveness of the CSVC in voltage

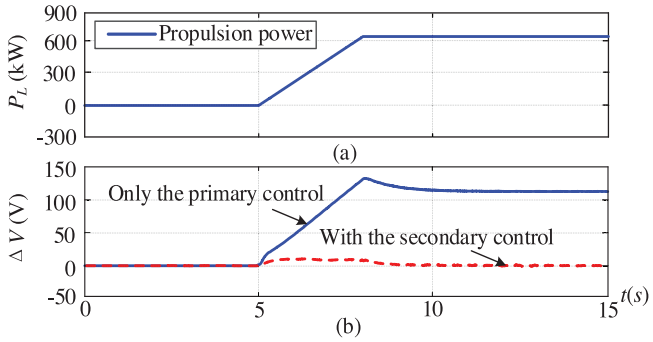

FIGURE 10 Performance comparison when only using the primary control and using the proposed CSVC. CSVC, cost-effective secondary voltage control.

restoration is assessed by comparing with the system only using the primary control. Then, two different operating cases, including acceleration and emergency braking process, and the DP process are carried out to verify the proposed CSVC. Furthermore, the operation performance of the DC-SIPS with the CSVC is assessed when one of the DGs breaks down. Finally, the advantages of the proposed CSVC are validated by comparing with the conventional FP-SVC and FD-SVC.

4.1 | Voltage regulation effectiveness test

The test is employed to assess the voltage regulation performance with the proposed CSVC. Figure 10 shows the system responses with only the primary control and CSVC, respectively. As presented in Figure 10a, the ship starts to accelerate at $t = 5$ s, and the propulsion load power P_L increases to its rated power 625 kW. In this acceleration process, Figure 10b shows if only the primary control is enabled, the voltage deviation ΔV determined by the droop coefficient is large. Once the proposed CSVC is activated, the voltage deviation ΔV is eliminated successfully, which proves the effectiveness of the proposed control method.

4.2 | Acceleration and emergency braking process test

The acceleration and emergency braking process is a common case in the vessel practical operation. The process has three stages, as displayed in Figure 11. The first stage between 0–t_1 is also called the grid-forming stage. In the following acceleration stage t_1–t_2, propulsion power reaches its maximum value 625 kW by three-step, as shown in Figure 11a. The CSVC is activated to distribute VRR between the DG and HESS, and the results are depicted in Figure 11b. In particular, DGs take the long-term VRR with the relatively slow ramping rate, while BES and SCS take the short-term VRR with the fast response characteristics. It is worth noting that the rising edge of the acceleration process is 1.67 s, which is enough for BES to response. Thus, the BES provides more power than SCS

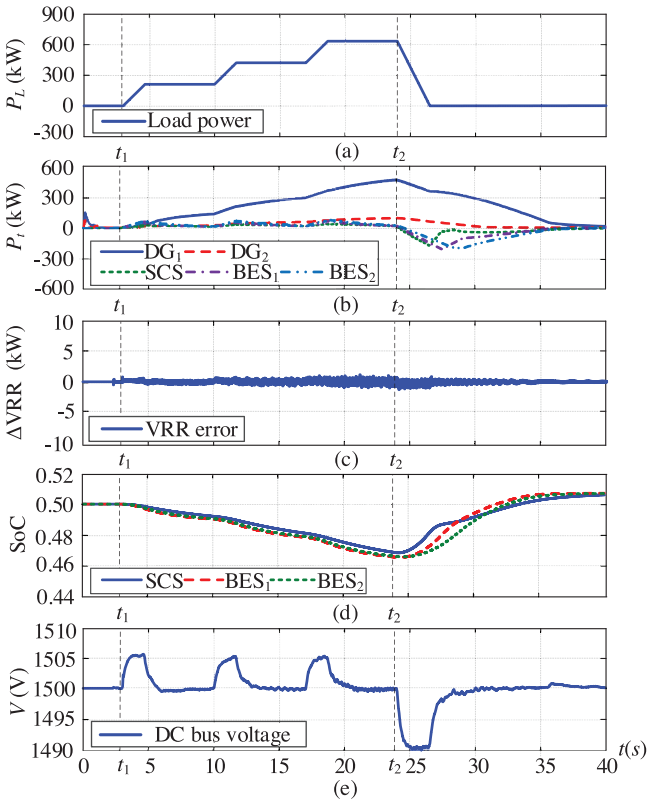

FIGURE 11 System response in the acceleration and emergency braking process.

to mitigate voltage fluctuations. Meanwhile, the VRR-tracking performance shown in Figure 11c verifies the accuracy of the distribution in real time. Figure 11d shows that the BES and SCS work cooperatively to keep SoC balance. In this operation process, the instantaneous DC bus voltage is 1505 V, and the voltage error can be eliminated within 2.6 s, as seen in Figure 11e.

During the last period, the ship encounters the emergency braking stage at t_2, and propulsion power decreases sharply to 0 within 2.5 s, as displayed in Figure 11a, which causes the instantaneous DC bus voltage to drop to only 1490 V, as seen in Figure 11e. In response to the sudden decrease of VRR, HESS especially SCS are charged to absorb the extra power, and the voltage error is mitigated in Figures 11b and 11e. SoC balance of HESS is also achieved continuously to restore its optimal state 0.507, as presented in Figure 11d.

4.3 | DP process test

In this test, the load power varies between 25% and 100% periodically to simulate the highly dynamic DP process of drilling and supporting vessels, the system response with the proposed CSVC is depicted in Figure 12. In the following DP process, the load varies in a pulsed form presented in Figure 12a. The desirable VRR distribution between the DG and HESS can be achieved by the CSVC regardless of the pulse conditions

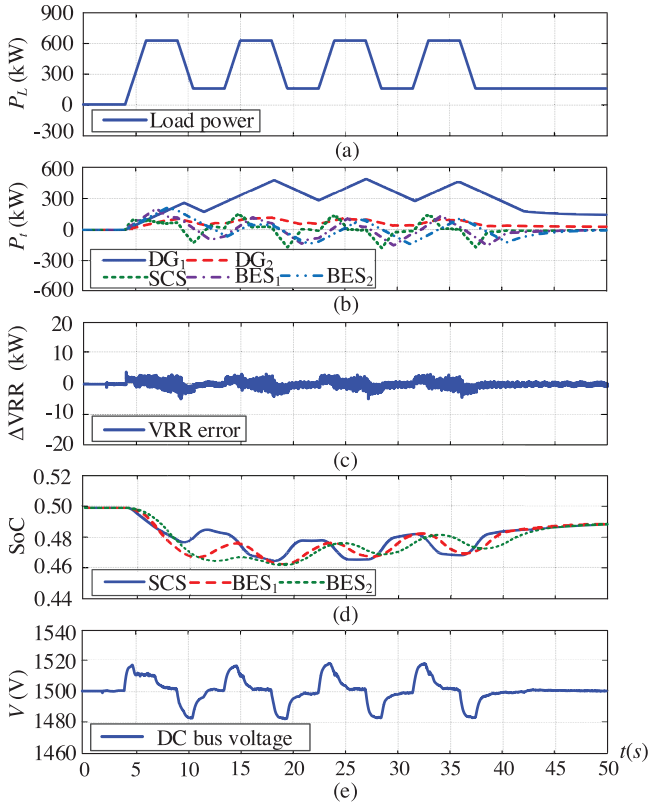

FIGURE 12 System response in the DP process. DP, dynamic positioning.

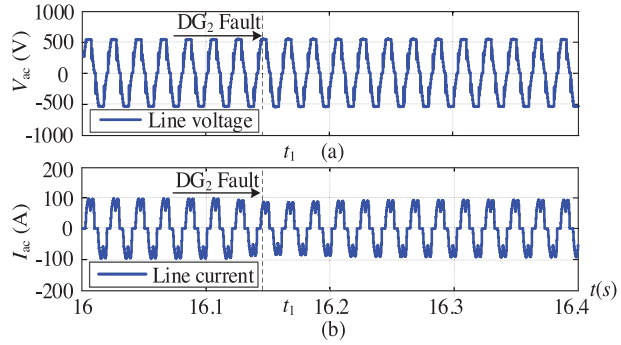

FIGURE 13 Line voltage and current of DG_1. DG, diesel genset.

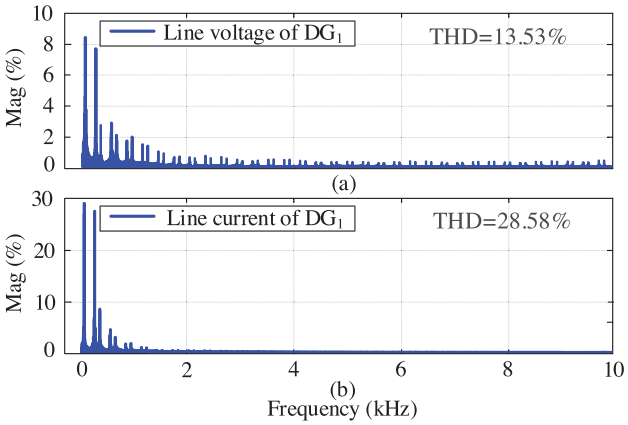

FIGURE 14 THD of line voltage and current of DG_1 during normal operation. DG, diesel genset; THD, total harmonic distortion.

(rising, duration, or falling), as shown in Figure 12b. Furthermore, different from the acceleration process, the rising edge of the VRR from 156 to 625 kW in the DP process is 1.5 s, resulting in severe and frequent voltage fluctuations. As shown in Figure 12e, the instantaneous DC bus voltage deviation is close to 20 V, which needs more power coming from SCS than BES to mitigate the voltage fluctuations in the transient states. The VRR-tracking error in Figure 12c shows slight fluctuations around zero, reflecting the accuracy of VRR distribution in a steady state without advanced scheduling. Meanwhile, benefiting from the CSVC, the SoC of BES and SCS can be restored to their optimal balance point after each pulse period, as illustrated in Figure 12d. At last, the voltage deviation can always be eliminated within 2.8 s in the whole DP process.

4.4 | Fault process test

This case is carried out to validate the effectiveness of the proposed control during fault process. Under normal operation conditions, the commutation overlap issue of the diode rectifier causes inherent harmonic distortion of line voltage and current at generator terminals, as shown in Figure 13. The total harmonic distortion (THD) of line voltage and current at DG_1 terminals is 13.53% and 28.58%, as presented in Figure 14. It is worth noting that these harmonics will not affect the stability of DC voltage by using diode rectification technology. Then, the pulsed loads presented in Figure 15a are connected to the DC bus. At t_1, the DG_2 is out of operation due to a fault, which causes a significant reduction in the VRR capacity of gensets, and thus leads to the instantaneous DC voltage rising sharply to 1515 V, as depicted in Figures 15b and 15e. During this fault process, the SCS provides transient power support with a fast response, as illustrated in Figure 15b. In this manner, there is only a slight increase in the THD of line voltage and current during the fault thanks to SCS, as shown in Figure 16. Finally, the DC voltage is restored to the rated value by the CSVC within 525 ms and the SoC can still keep balance.

4.5 | Comparison test

To verify the advantages of the proposed control scheme in voltage stability, cost optimization, and SoC balance, four comparison tests are carried out as follows:

1) *Final SoC is 100%:* In the first test case, the initial SoC of each ESS is 100%, and the optimal SoC value is also set as 100%. As shown in Figures 17a and 17b, in the three-step acceleration process, the ideal VRR distribution result is similar to Figure 11. Moreover, the SoC of HESS can keep balance and the DC bus voltage can be regulated to the

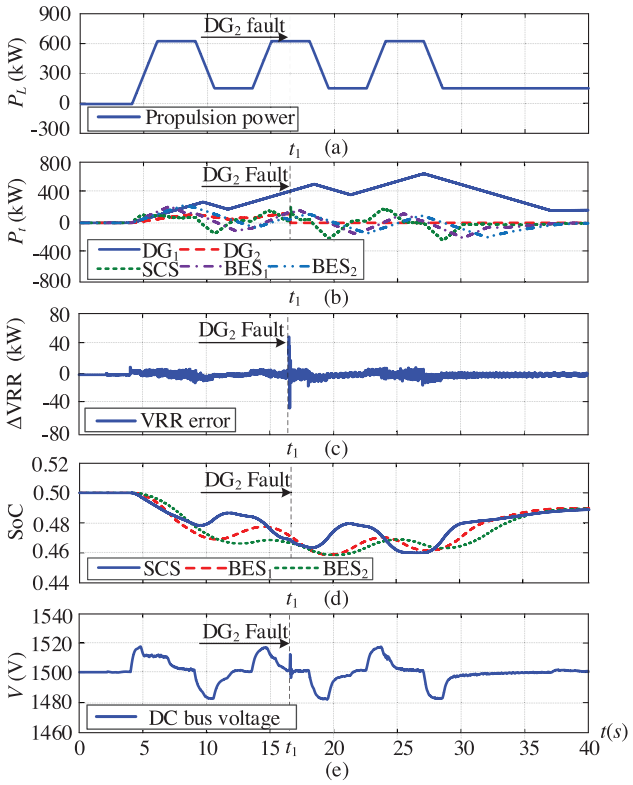

FIGURE 15 System response in the DG_2 fault process. THD, total harmonic distortion.

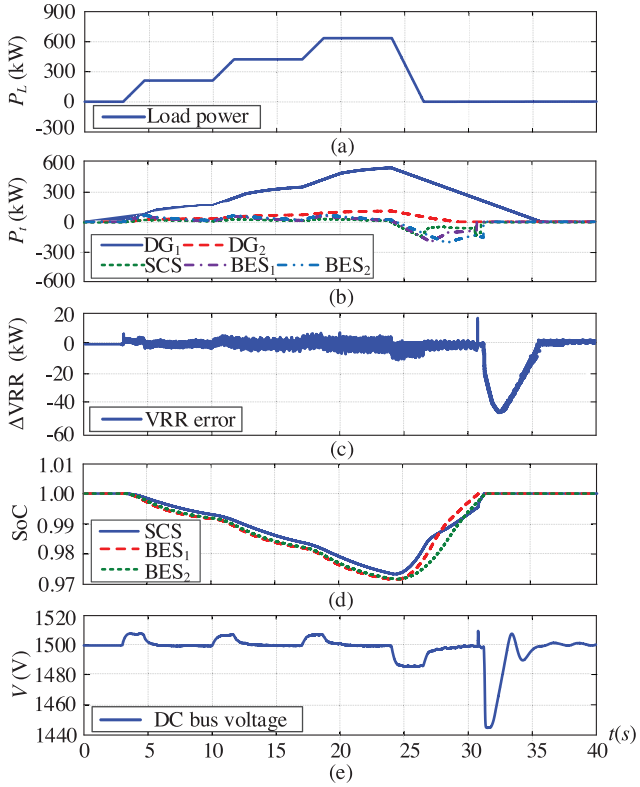

FIGURE 17 System response when final SoC is 100% in the acceleration and emergency braking process. SoC, state of charge.

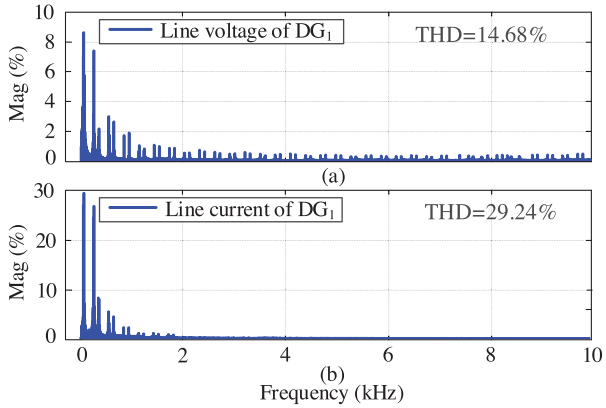

FIGURE 16 THD of line voltage and current of DG_1 during fault process. DG, diesel genset; THD, total harmonic distortion.

rated value within 2.6 s, as shown in Figures 17d and 17e. Then, under the emergency braking process, the HESS works to absorb the extra power to regulate voltage. When the SoC of BES_1 reaches 100% and cannot absorb energy, it causes severe instantaneous fluctuations in the DC voltage and the instantaneous voltage is 1510 V, as presented in Figures 17d and 17e. To address this problem, the SCS and BES_2 work corporately to absorb more energy to stabilize the voltage. However, when both the SoC of SCS and BES_2 reach 100%, the HESS cannot provide transient power support. As a result, severe deviation in VRR is caused and the instantaneous voltage is reduced to 1445 V, as presented in Figures 17c and 17e. Finally, as the generator continues to provide power, the voltage deviation will gradually be eliminated. These results prove that the optimal state of SoC for all ESSs cannot be set to 100% at the same time.

2) *Only using BES:* In the second test case, DG and BES are installed aboard to provide power source. Under pulsed load conditions, the desirable VRR-sharing effect among DGs and BESs can be achieved while the SoC balance is ensured, as shown in Figures 18b, 18d, and 18e. However, the maximum VRR deviation when only using BES is 10 kW, which is two times larger than that in Figure 12c. Also, the instantaneous DC voltage deviation increases to 28 V and the voltage recovery time is 4 s, as shown in Figure 18e, which is slower than that in Figure 12e. These results indicate that voltage regulation is limited by the control bandwidth of the BES controller.
3) *FP-SVC method:* Moreover, the BES and SCS-based HESS works cooperatively and the FP-SVC method is employed in the DC-SIPS, as shown in Figure 19. During the acceleration process, as each power source undertakes VRR at the ratio of rated capacity presented in Figure 19b, the ESSs discharge continuously until they are exhausted. In specific, around $t = 29$ s, Figure 19d shows that the SoC of SCS and BES reach the bound 0.1 and exit voltage regulation control. As a result, the FP-SVC causes severe VRR-tracking error and the instantaneous DC bus voltage rises sharply to 1610 V, as shown in Figures 19c and 19e.

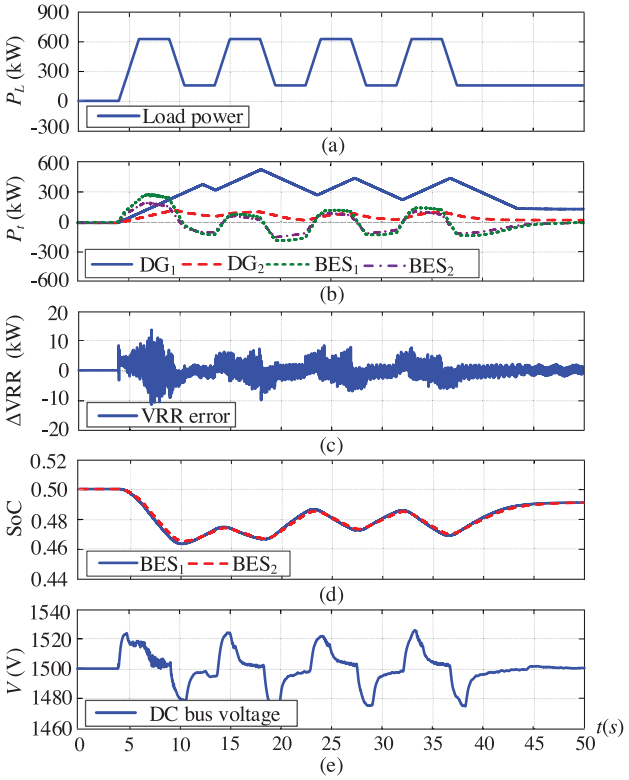

FIGURE 18 System response when equipped with only BES in the DP process. BES, battery energy storage; DP, dynamic positioning.

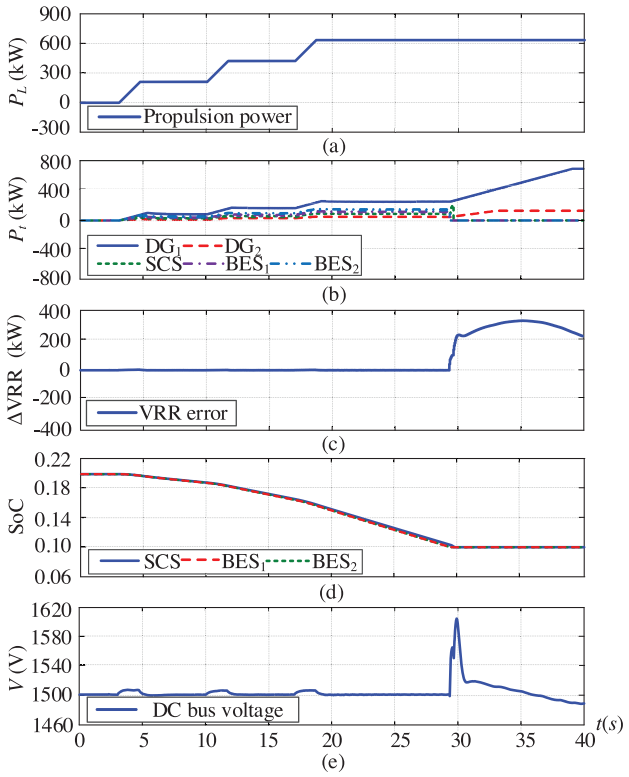

FIGURE 19 System response with the FP-SVC method in the acceleration process. FP-SVC, fixed-proportion-based secondary voltage control.

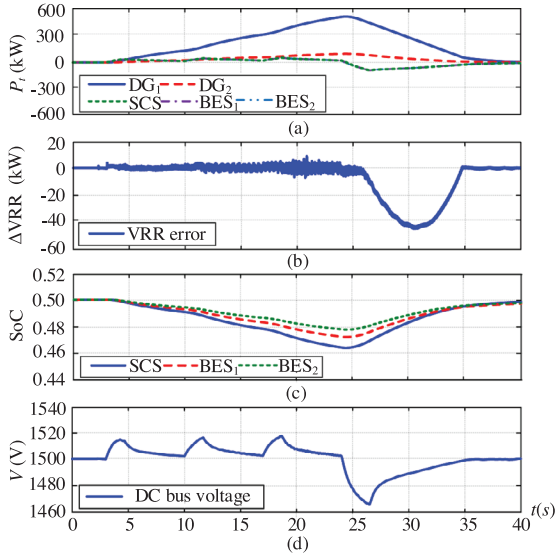

FIGURE 20 System response with the FD-SVC method. FD-SVC, frequency-division-based secondary voltage control.

TABLE 4 Voltage regulation and SoC balance performance comparison during acceleration and emergency braking process.

Method	SoC	Maximum transient voltage deviation	Voltage recovery time
CSVC	Balance	10 V	2.6 s
FP-SVC	Over-discharge	110 V	15 s
FD-SVC	Balance	35 V	10 s

CSVC, cost-effective secondary voltage control; FD-SVC, frequency-division-based secondary voltage control; FP-SVC, fixed-proportion-based secondary voltage control; SoC, state of charge.

4) *FP-SVC method:* Finally, the FD-SVC method is used in the third case, where VRR signals are divided into low-frequency VRR and high-frequency VRR, and DGs and HESS take the corresponding VRR according to their ramping rate. The system response with the FD-SVC in the acceleration process is shown in Figure 20. Compared with Figure 11, two noteworthy differences can be derived, although the HESS compensates for the shortage of DGs' ramping rate in both methods. Firstly, VRR is distributed equally between SCS and BES in the steady state, as depicted in Figure 20a. As a result, the SoC cannot achieve balance due to the difference in power and capacity of HESS is not distinguished, as illustrated in Figure 20c. Moreover, Figure 20d shows that the instantaneous DC bus voltage in the emergency braking process droops to 1465 V and the voltage error takes 10 s to be eliminated because of the huge VRR-tracking error, as shown in Figure 20b. Finally, the comparison of voltage regulation and SoC balance performance during acceleration and emergency braking process is summarized in Table 4. Obviously, with the proposed CSVS, the fast voltage restoration can be achieved while the SoC balance is ensured.

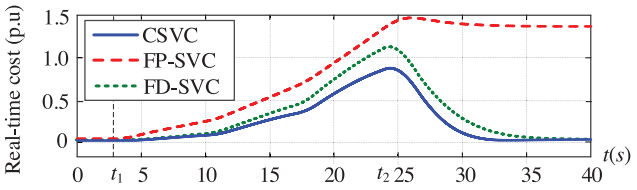

FIGURE 21 Real-time cost comparison in the acceleration and emergency braking process.

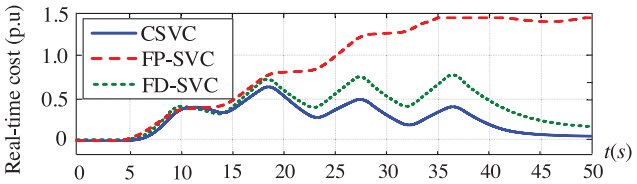

FIGURE 22 Real-time cost comparison in the DP process. DP, dynamic positioning.

TABLE 5 Cumulative voltage regulation cost comparison (p.u).

Method	Three-step acceleration process	DP process
CSVC	1.00	1.54
FP-SVC	4.42	5.12
FD-SVC	1.46	2.08

CSVC, cost-effective secondary voltage control; DP, dynamic positioning; FD-SVC, frequency-division-based secondary voltage control; FP-SVC, fixed-proportion-based secondary voltage control.

Furthermore, according to the cost function (10) to (11), the real-time voltage regulation cost of the CSVC, FP-SVC, and FD-SVC methods in the acceleration and emergency braking process, and the DP process is described in Figures 21 and 22, respectively. It is worth noting that the real-time cost of the proposed CSVC is always minimal since the SoC can keep balance. In the FP-SVC, over-discharge causes enormous deviation of the SoC from the reference value, and thus leads to a rapid increase in voltage regulation cost. Then, the cumulative cost of voltage regulation is also calculated in Table 5. It clearly shows that the voltage regulation cost using the CSVC is about 350% less than FP-SVC and about 50% less than FD- SVC. In summary, compared with the FP-SVC and the FD-SVC, the CSVC has better technical and cost performance during the DC-SIPS voltage regulation process without relying on predicting load information.

5 | CONCLUSION

In this paper, a CSVC is proposed to solve the problems of voltage restoration and cost minimization in the DC-SIPS. To support the exploration of VRR distribution solutions, a HIL platform is built to capture the dynamic behaviour of the multi-zone DC-SIPS. Acceleration and emergency braking process, DP process, and DG fault process are set as typical cases. In these cases, the proposed CSVC distributes VRR accurately and economically by considering different characteristics of DGs and HESS including rated power, rated capacity, ramping rate, and SoC. Also, real-time SoC balance of HESS can be achieved simultaneously as the voltage regulation cost function involves SoC. Furthermore, a comparison among the proposed CSVC, conventional FP method, and FD method is presented. These results prove that the proposed method has advantageous in bus voltage restoration, real-time SoC balance, and cost minimization over the conventional method.

NOMENCLATURE

Abbreviations

API	application programming interface
BES	battery energy storage
CSVC	cost-effective secondary voltage control
DC-SIPS	DC shipboard integrated power system
DG	diesel genset
DP	dynamic positioning
ESS	energy storage system
FD-SVC	frequency-division-based secondary voltage control
FPGA	field-programmable gate array
FP-SVC	fixed-proportion-based secondary voltage control
HESS	hybrid energy storage system
HIL	hardware-in-loop
MPC	model predictive control
PCI	peripheral component interconnect
QPA	quadratic programming algorithm
SCS	supercapacitor storage
SG	synchronous generator
SMC	sliding mode control
SoC	state of charge
THD	total harmonic distortion
VRR	voltage regulation responsibility

Parameters

a_{Ej}	weight coefficient of the voltage regulation cost of the jth ESS due to power deviation
a_{Gi}	weight coefficient of the voltage regulation cost of the ith DG due to power deviation
b_{Ej}	weight coefficient of the voltage regulation cost of the jth ESS due to the SoC deviation
$C_{Ej,t}$	voltage regulation cost of the jth ESS at the tth moment
$C_{Gi,t}$	voltage regulation cost of the ith DG at the tth moment
D	diameter of the propeller
I_e	excitation current
K_a	actuator gain of the DG
K_d	diesel engine torque gain of the DG
k_{Gi}	droop coefficient of the ith DG
K_T	torque coefficients of the propeller

k_v	voltage constant of the SG
L_m	magnetizing inductance of the SG
N	propeller shaft speed
$P_{Ej,t}$	output power reference of the jth ESS to regulate voltage at the tth moment
$P_{Ej\_\min}$, $P_{Ej\_\max}$	minimum and maximum output power of the jth ESS
P_{Ej_out}	actual output power of the jth ESS
$P_{Gi,t}$	output power reference of the ith DG to regulate voltage at the tth moment
$P_{Gi\_\min}$, $P_{Gi\_\max}$	minimum and maximum output power of ith DG
P_{Gi_out}	actual output power of the ith DG
P_{PR}	power demand of the propeller
$R_{Ej\_\min}$, $R_{Ej\_\max}$	minimum and maximum ramping rate of the jth ESS
$R_{Gi\_\min}$, $R_{Gi\_\max}$	minimum and maximum ramping rate of the ith DG
S_{Ej}	rated capacity of the jth ESS
$SoC_{Ej\_\min}$	minimum real-time SoC of the jth ESS
SoC_{Ej_ref}	SoC reference of the jth ESS
T_m	mechanical torque of the DG
V_{dc}	nominal voltage of DC bus
v_f	exciter voltage
V_{ref}	DC voltage reference
ΔV	voltage deviation
η_{Ej_c}, η_{Ej_d}	charge and discharge efficiency of the jth ESS
τ_e	time constant of the exciter
Ω	rotating speed of the SG
ω_e	electrical angular speed
ω_{ref}	rotating speed reference of the SG

AUTHOR CONTRIBUTIONS

Tianling Shi: Writing – original draft; Writing – review & editing; Conceptualization; Methodology; Validation. **Fei Wang**: Validation; Methodology; Supervision; Funding acquisition. **Shengqi Zhang**: Writing – review & editing; Funding acquisition; Project administration. **Heyu Liu**: Software; Data curation; Resources. **Li Li**: Validation; Supervision.

CONFLICT OF INTEREST STATEMENT

The authors declare no conflict of interest. .

DATA AVAILABILITY STATEMENT

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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