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RESEARCH ARTICLE

A Baseband-Noise-Cancelling Mixer-First CMOS Receiver Frontend Attaining 220 MHz IF Bandwidth With Positive-Capacitive-Feedback TIA

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ABSTRACT In this paper, by using the baseband noise cancellation, a CMOS mixer-first analog receiver with power reduction is proposed. Based on a current-mirror transimpedance amplifier structure, positive capacitive feedback is applied to manipulate poles/zeros location, enabling a wide baseband bandwidth and out-of-band second-order filtering profile. The additional radio frequency N-path filtering and baseband 40dB/dec roll-off absorb out-of-band interferences. The presented receiver frontend is fabricated in a standard 65 nm CMOS process. Measured results demonstrate a minimal noise figure of 2.2 dB, and an average voltage gain of 32.2 dB across the 220 MHz intermediate frequency range. The in-band and out-of-band third-order input intercept point manifests −12.8 dBm and 15.5 dBm respectively. The presented receiver circuit draws ∼32 mW at a typical 1 GHz local oscillator stimulus.

INDEX TERMS Mixer-first receiver, noise cancellation, wideband IF, capacitive feedback.

I. INTRODUCTION

Featured with a high-speed air interface, the fifth generation (5G) mobile communication market is skyrocketing across many countries of the world. Both 28 GHz and sub-6 GHz channels coexist in the 5G era [1]. Regarding the 28 GHz channel, it has been disclosed that the millimeter wave (mmW) signals can be severely sensitive to shadowing, leading to outages and intermittent channel quality. Moreover, the phase array's power burning to support numerous concurrent antennas is also a key challenge [2]. In one word, wide bandwidth at the mmW band is attractive but also problematic. In turn, at sub-6 GHz channel to support enhanced data rate, a common way is to use a carrier aggregation (CA) technique. Namely, multiple radio frequency (RF) frontends are jointed in parallel to increase the whole channel bandwidth (BW) coverage. But, the budget increase in hardware and power consumption is proportional, too. Recently, as an economic and efficient solution, enlarging baseband (BB) BW, typically > 100 MHz has become welcome. What is even more, to limit the cost surge, eliminating the discrete off-chip filter inevitably is exerting a large burden on BB filtering. Consequently, at the sub-6 GHz band, good blocker compatibility often has the alike importance as boosting bandwidth, when considering large numbers of communication devices' coexistence thereof.

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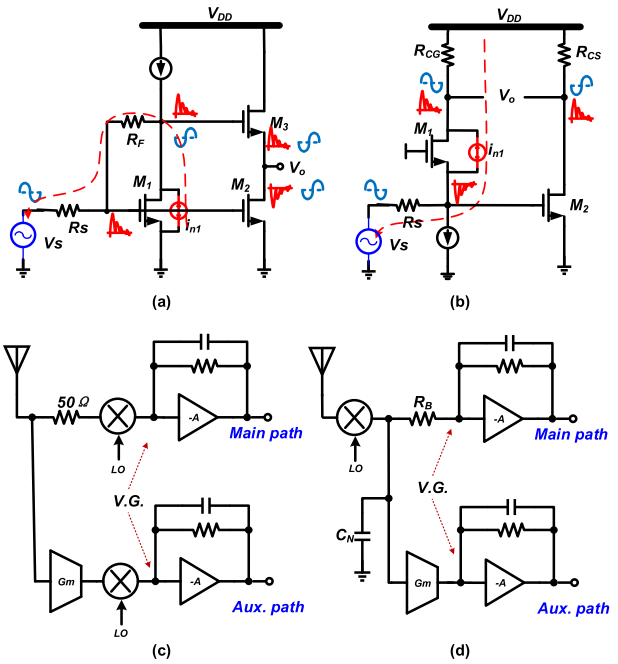

FIGURE 1. Classical noise-canceling low-noise amplifiers of (a) resistive feedback topology, and (b) common-gate and common-source topology. Representative noise-canceling receivers of (c) noise cancellation after frequency conversion, and (d) baseband noise cancellation plus N-path filter.

A noise cancellation (NC) technique was presented for the first time in low-noise amplifiers (LNAs) design, of which the two classical structures are shown in Fig. 1(a) and (b) [3], [4]. The fundamental principle is simply interpreted here. The NC LNA includes the main and auxiliary paths along the signal transmission direction. The main path ensures input matching while the auxiliary path is introduced to cancel the main path's noise. Therefore, a low-noise target is achieved. Thereafter, the NC technique has been extended to numerous variants to handle new requirements. For example, [5], [6] a current-mirror load replacing resistors is presented to enable current mode operation, alleviating amplifiers' distortion issues. Accompanying that, some receiver designs, also learn from the NC technique and have realized attractive low-noise performance. Fig. 1(c) just shows such a noise-canceling receiver topology, based on the popular receiver chain combination of LNA+mixer+transimpedance amplifier (TIA), where the RF input match is directly rendered with a 50 Ω resistor at the RF side [7]. The noise leakage by the matching resistor is mitigated by the additional auxiliary path. More interestingly, putting mixers of Fig. 1(c) very close to the antenna nearly reaches Fig. 1(d) [8]. The direct benefit of doing that is that an N-path filter via the capacitor C_N and nonoverlapped-clock-driven switch inhibits out-of-band (OOB) RF interference injection. The low noise and high blocker resilience are highly desirable for sub-6 GHz receivers. For large IF bandwidths coverage that is vital for high data rate transmission, the mixer-first (MF) receivers in [9], [10] have achieved 130 and 200 MHz levels based on BB current-mode filters. The used current-mode filters are based on a regulated cascode structure. With the reactance variation of the embedded active inductor in proportion to the angular frequency, ω, a positive resistor-capacitor-feedback amplifier is appended to yield a reactance filtering profile with a $1/\omega^2$ slope. A third-order filter is thus realized. Conversely, the traditional closed-loop TIA using an operational transconductance amplifier (OTA) has difficulty in covering wide bandwidth while delivering high gain to guarantee the TIA virtual ground approximation at the input, simultaneously. After all, the gain-bandwidth product for a given OTA structure often is fixed under certain power constraints. In practice, power consumption can be greatly burned to increase bandwidth or gain-bandwidth product, proportionally. For example, a closed-loop TIA based on a three-stage OTA in [8] reports a charming 175 MHz bandwidth but with over large power.

Furthermore, note that the receiver technique for low noise and low power presented in [21] is attractive but mainly applicable to biomedical imaging areas under low-frequency bands. Targeted for the internet of thing scenario, the impressive power reduction of the receiver reported in [22] by biasing transistors in weak inversion region sacrifices the speed and noise, appreciably. Thereby, low noise and low power desired to be achieved in our work should not impair the high-frequency coverage of receivers that intentionally serve the high data rate transmission target.

In this paper, we propose a CMOS MF receiver with a current mirror NC BB. The NC technique desirably ensures a low noise of the receiver. The current mirror also acts as a TIA building block as in a conventional receiver structure. With proper positive capacitive feedback manipulation, the presented receiver features second-order BB low-pass filtering and RF N-path filtering, simultaneously. It meets giant bandwidth, excellent OOB filtering, and low noise by consuming reduced power, successfully. The coming sections will show the presented receiver architecture /circuits and simulation results on the prototype chip.

II. PROPOSED FRONT-END CIRCUIT

Shown in Fig. 2 is the simplified diagram of the presented MF CMOS receiver frontend utilizing BB NC and current mirror-based TIA architecture. The BB current mirror structure plays multiple roles: 1. it enables NC for a low-noise target; 2. input resistance of BB current mirror structure substantially matches the antenna resistance, owing to the mixer's reciprocity; 3. the mixer-down-converted BB current signal is further converted into an output voltage signal, fulfilling traditional TIA' function. Specifically, the BB current mirror consists of the input common-gate(CG) stage, M_1 and current mirror M_3 and M_4 in the main path, and common-source (CS) stage M_2 in the auxiliary path. Pushing the traditional RF current-mirror-based NC structure to the BB location, on the one hand, maintains low noise under a reduced power budget. Furthermore, the inherent wideband trait of the current mirror facilitates a large BB BW implementation, replacing

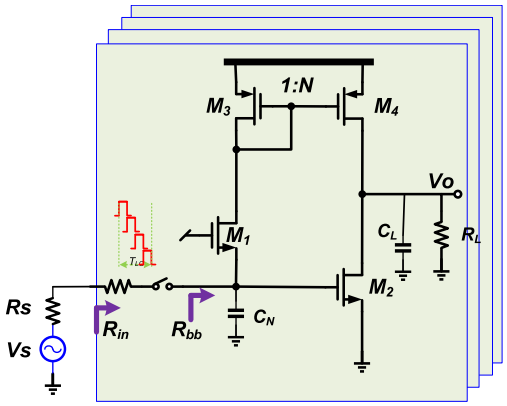

FIGURE 2. Simplified mixer-first receiver macro-model using baseband noise cancellation and current mirror structure.

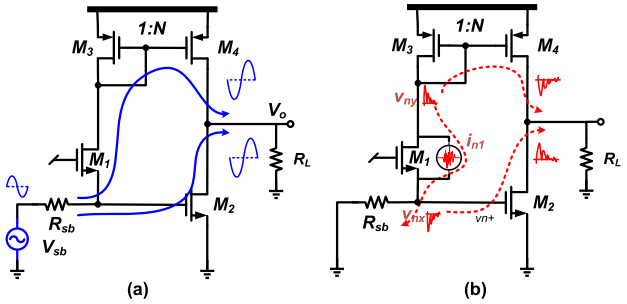

FIGURE 3. (a) Signal flows along the main/auxiliary paths. (b) Noise cancellation by the auxiliary path.

the previous feedback Opamp structure. To maintain the resilience of interferences, the capacitor C_N combined with the passive mixers renders an RF N-path filter. Meanwhile, the capacitor C_L addition ensures the BB's transfer function curve with the wanted filtering profile, under proper capacitive positive feedback manipulation. Thus, OOB blockers are absorbed, at RF and BB sides, simultaneously.

A. INPUT IMPEDANCE

According to Fig. 2, if the parasitic capacitance effect is neglected, the input resistance of the receiver circuit is approximately written as

$$R_{in} = R_{sw} + \frac{2}{\pi^2} R_{bb} = R_{sw} + \frac{2}{\pi^2}\frac{1}{g_{m1}} \tag{1}$$

Particularly, the coefficient $2/\pi^2$ comes from a resistance translation by a 25% duty-cycle local oscillator (LO) stimulus [7]. Then, the parameters of R_{sw} and R_{bb} stand for the switch-on resistance of mixer switches and the equivalent input BB resistance. The g_{m1} is the transconductance of transistor M_1. More strict derivation using charge sharing [11] is not used here for simplicity. The R_s in Fig. 2 denotes the internal resistance of signal source Vs, or receiver antenna, equivalently. The relationship of $R_s = R_{in}$ normally has to be met to ensure input matching. In [8], the RF port matching is provided by the translated impedance of a BB matching resistor of the main path, owing to the mixer's reciprocity. To cancel the resistor's noise output, an auxiliary LNTA+TIA chain is added. Here, the input resistance of the CG stage is naturally deemed as a BB matching resistance while the auxiliary CS stage is to cancel the CG stage noise.

B. NOISE CANCELLATION AT BASEBAND

The NC mechanism is analyzed in this part. Fig.3 displays the simplified BB circuit schematic view. And parameters V_{sb} and R_{sb} in Fig.3(a) denote the BB source signal and source resistance seen towards the mixer side. Then, note that the BB signal can flow along the main path, amplified in phase by the CG stage, and out of phase by the current mirror stage, reaching the output terminal v_o, finally. On the other hand, along the auxiliary path, the BB signal is solely amplified out of phase by the CS stage and summed itself with the amplified signal by the main path, additionally. The BB gain contributed by the main and auxiliary paths thus can be shown below

$$Gain = \frac{-1}{1 + g_{m1}R_{sb}}\left(Ng_{m1} + g_{m2}\right) r_o. \tag{2}$$

The parameters N and g_{m2} stand for the scaling ratio of M_3 and M_4, and the transconductance of M_2while the total output resistance r_o takes

$$r_o = r_{o2} \parallel r_{o4} \parallel R_L. \tag{3}$$

The r_{o2} and r_{o4} are the device output resistance of M_2 and M_4, respectively.

Meanwhile, the CG stage noise now is examined. According to the simplified noise model in Fig.3(b), one note that, concerning the noise source in1, the current output portion Δi_{n1}, leads to two noise voltages v_{nx} and v_{ny} below

$$v_{nx} = \Delta i_{n1} R_{sb},\ v_{ny} = -\Delta i_{n1}\frac{1}{g_{m3}}. \tag{4}$$

Then along the red dash line direction, the two noise voltages of v_{nx} and v_{ny} are converted into the two output noise currents, nullifying each other as below,

$$i_{no} = \Delta i_{n1} R_{sb} g_{m2} - \Delta i_{n1}\frac{g_{m4}}{g_{m3}} = \Delta i_{n1} R_{sb} g_{m2} - \Delta i_{n1} N. \tag{5}$$

The g_{m3} and g_{m4} are transconductances of transistors M_3 and M_4. Consequently, a noise-canceling condition is shown as

$$R_{sb} g_{m2} = N. \tag{6}$$

Combining it with the input matching constraint reaches the below compact equation

$$g_{m2} = \frac{N}{R_{sb}} = N g_{m1}. \tag{7}$$

Meeting the NC condition (7), however, does not achieve optimal noise performance. The reason is that, besides the CG stage of M_1, the CS stage M_2 also yields noise output by itself although it suppresses M_1 and even the whole main path noise output, efficiently. With this consideration, larger g_{m2}

TABLE 1. Comparisons of NC located at RF and BB.

NC@RF side	Parameter	R_s	N	g_{m1}	g_{m2}
	Value	50 Ω	3	20 mS	70 mS
NC@BB side	Parameter	R_{sb}	N	g_{m1}	g_{m2}
	Value	286 Ω	5.8	3.5 mS	41 mS

is designed by simulation, instead of strictly following the theoretical equation (7). What is interesting here, applying the NC at the baseband has a significant power reduction advantage.

To better understand this point, a comparison referring to Fig.3, is conducted based on simulations between RF NC and BB one, which is summarized in the table below. Regarding the conventional RF noise cancelation, it is known that source resistance, R_s takes 50 Ω, then CG stage transconductance g_{m1} equals 20 mS. Under typical N = 3, using g_{m2} = 70 mS leads to a low-noise level of NF = 2.1 dB. Comparatively, in the proposed BB noise cancelation, thanks to ∼6x larger BB source resistance R_{sb}, g_{m1} is reduced proportionally. And g_{m2} is also reduced obviously due to a larger N adopted. Power consumption reduction is thus clearly manifested while a comparable NF level is attained. Of course, the dynamic power absorbed by the frequency divider of MF receivers partially cancels this BB NC power reduction benefit.

To further check the effectiveness of BB NC, another comparison is done between enabling the auxiliary path or not. The comparison result via simulations is reported in Fig.4. Particularly, the LO frequency takes 2 GHz as an example. notice that, in the NC off mode, the main noise contributors are transistors M_3 and M_1, accounting for a stunning 54.9 and 28.5 %. In contrast to that, with the NC enabled, the input antenna port, overwhelmingly, dominates the noise percentage with 72.2 %, followed by the diode-connected transistor M_3 with 9 %, and the preceding mixer with 7.9 %. It thus is clearly seen that the auxiliary NC path suppresses the noise contributor of M_1 and M_3 along the main path, effectively. Soon in the following section, the noise figure (NF) comparison result again verifies the NC effectiveness.

C. BB TRANSFER FUNCTION AND BANDWIDTH

To fulfill a large BW for high data transmission, enlarging BB BW is designed in our circuit. Fig.5 shows the simplified circuit model for BW analysis, considering multiple lumped capacitors. By following the simple method in [12], each net along the signal transfer path is treated as a pole. Then the nets, v_o and v_i can be related by the below equation

$$\frac{v_o}{v_i} = \left(\frac{g_{m1}g_{m4}}{g_{m3}+sC_E} + g_{m2}\right)\left(r_o \parallel \frac{1}{sC_L}\right). \tag{8}$$

At the input port, the source signal v_{sb} is divided by resistor and capacitor, and then leads to the input signal v_i, which is

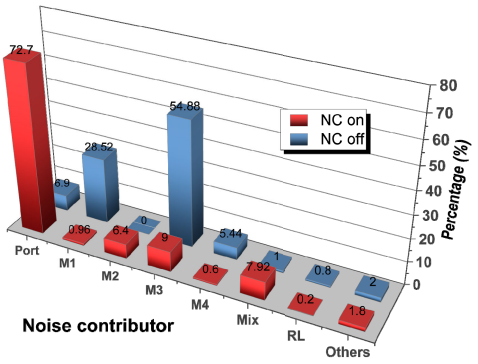

FIGURE 4. Noise percentage comparison by individual circuit parts between NC on and off modes.

shown as

$$\frac{v_i}{v_{sb}} = \frac{1}{R_{sb}}\left(R_{sb} \parallel \frac{1}{g_{m1}+sC_N}\right). \tag{9}$$

The C_N, C_E, and C_L indicate the N-path filter capacitor, current mirror parasitic, and load capacitor, respectively. Then combining the two equations above, we deduce the transfer function (TF) of the circuit as

$$\begin{aligned} TF &= \frac{v_i}{v_{sb}}\frac{v_o}{v_i} \\ &= \frac{1}{R_{sb}\left(\frac{1}{R_{sb}}+g_{m1}+sC_N\right)}\frac{g_{m2}\left[g_{m3}\left(1+\frac{Ng_{m1}}{g_{m2}}\right)+sC_E\right]}{g_{m3}+sC_E} \\ &\quad \times \frac{1}{\frac{1}{r_o}+sC_L} \end{aligned} \tag{10}$$

The resulting poles and zero are further given by the two below equations

$$p_1 = \frac{\frac{1}{R_{sb}}+g_{m1}}{2C_N}, p_2 = \frac{g_{m3}}{C_E}, p_3 = \frac{1}{r_oC_L}, \tag{11}$$

$$z_1 = \frac{g_{m3}\left(1+\frac{Ng_{m1}}{g_{m2}}\right)}{C_E} = p_2\left(1+\frac{Ng_{m1}}{g_{m2}}\right). \tag{12}$$

According to them, the transfer function has three real poles and one zero, being a third-order system in the control theory perspective. The zero generation is due to the coexistence of the CG stage and current mirror-slow path and CS stage-fast path. Unfortunately, this method gains simplicity but ignores the miller capacitance effect on poles/zeros [12], [13]. In this paper, to avoid the impractical high-order polynomial function derivation and solving, we turn to simulation for design insight. Meanwhile, to double the power efficiency, the circuit in Fig.5 evolutes into complementary n/pMOS structures, which is provided in Fig.8. In addition, the complementary n/pMOS structures reduce second-order distortion as well. Ultimately, the BB circuit based on stacked n/pMOS structures is simulated to check the zero/pole and TF traits. According to Spectre simulations at the schematic level, a fourth-order TF indeed exists there, including four poles and

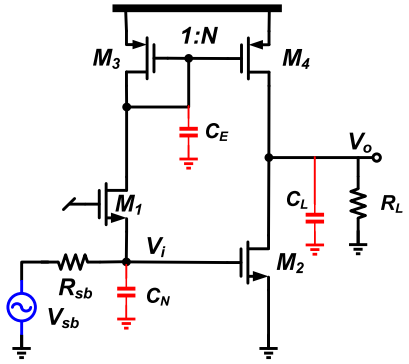

FIGURE 5. Simplified circuit model for bandwidth analysis.

two zeros. It goes against the speculation by the above simple equation. More interestingly, as shown in Fig.6 (a)&(b), adding a neutralized capacitor C_{ntr0} can drive two real poles thereof into a complex conjugate pair, while the other two real poles are roughly compensated by additional two real zeros. A second-order filtering function is thus formed.

Fig.6(c) demonstrates the BB TF with respect to the C_{ntr0} variations. Firstly, A 40 dB/dec OOB roll-off appears clearly. one may also notice that tuning C_{ntr0} will adjust the quality factor and 3-dB BW coverage of the second-order TF function. Of course, over large C_{ntr0} means the TF overshooting and instability and should be avoided in practical implementation. Moreover, The C_{ntr1} addition has a similar function. The final simulation indicates that the optimal C_{ntr0} and C_{ntr1} take 250 and 120 fF to comprise the tradeoff between overshooting and quality factor. Accordingly, the stability is explained in the next section.

III. RESULTS AND DISCUSSION

An MF CMOS receiver prototype using the baseband NC was designed and fabricated in a standard 65 nm CMOS technology. Displayed in Fig. 7(a) is the general schematic view of the presented circuit. The related sub-circuits are shown in Fig.8 too, including the current mirror main path, and the inverter auxiliary path. As discussed above, the neutralized capacitors, C_{ntr0} and C_{ntr1} are to manipulate the zero/pole locations to facilitate the OOB filtering profile. On the whole, the BB MOSFET devices' length in signal path uses longer values of 120 nm to alleviate flicker noise issues. Specifically, one-quarter duty-cycle LO clocks are obtained via an on-chip frequency divider [14]. It converts an off-chip 2x sinusoidal input frequency source to the corresponding clock pulse signals, first. Then, the resulting differential clock pulse signals of clk+/- drive the D-latch loop core, periodically, subsequently generating 4-phase pulse outputs of phi0∼3. The phi0∼3 signals are overlap and further shaped by the NAND logic and inverter chain into the required 4 phases of nonoverlapping LO signals, to feed I/Q mixers. The power of the signal path dissipates 21.9 mW under a 1.8 V supply. And the dynamic power of the digital logic takes ∼10 mW/GHz, with another 1.2 V supply. Fig. 7(b) depicts the power breakdown of the presented receiver frontend, and the chip micrograph is given in Fig. 7(c), occupying an area of 645 × 384 um^2 without pads included.

Fig. 9 shows the data of the simulated and measured input reflection coefficient, S_{11} where the f_{LO} can be continuously tuned from 1 to 3 GHz, although only three typical curves are sketched. Meanwhile, as in Fig. 10, the measured voltage gain of the receiver is roughly around 32.2 dB with average 3 dB BB bandwidth of 220 MHz upon the 2 GHz LO, agreeing with the simulation well. Compared to the flat gain curve reported in Fig. 6(c) with optimal neutralized capacitors, the slight gain overshoot at the band edge is ascribed to additional routing parasitics of the C_{ntr0} and C_{ntr1} in the layout design phase. Thanks to the larger baseband bandwidth, the reduced C_N and C_L greatly save the chip area as well. What is more important, the large BB BW directly means a high data rate, while not necessitating the CA technique at the cost of multiple receivers in parallel.

As shown in Fig. 11, the measured NF result, at f_{LO} = 2 GHz, is below 2.7 dB, approaching the BB high passband edge. Moreover, owing to the longer MOSFET device's channel adopted, the flicker noise appearing at the NF curve is not prominent, as well. Quantitatively, the measured NF value in minimum takes 2.2 dB, located at f_{IF} = 50 MHz, which already is a decent result. In contrast, the auxiliary path is disenabled and the resulting NF is also appended in the figure. One can see that ∼8 dB ΔNF degeneration happens there. The BB NC is again verified. Because there are capacitor-positive feedback paths around the BB, the stability concern needs to be checked cautiously. By inserting the detecting probe into the inverter positive feedback loop at the auxiliary path, a Spectre simulation is performed. The extracted data curve given in Fig. 12 displays that the loop gain of greatly lower than 0 dB at the interested IF, forcefully maintains stability. Similarly, the positive feedback on the main path was also examined with enough stability, although not shown as a standalone.

The NF result under blocker injection is depicted in Fig.13. The blocker offset frequency over the BB bandwidth, Δf/BW takes the typical 1 and 3 to examine the close-in blocker suppression level of the presented circuit. Correspondingly, the obtained NF in simulation is ∼5 dB at the ratio of Δf/BW = 1, and ∼2.5 dB at Δf/BW = 3, both under 0 dBm blocker interference injection. Meanwhile, with Δf/BW = 3, the measured NF deteriorates to ∼3 dB upon 0 dBm blocker injection. It means that the OOB filtering greatly absorbs the blocker interference. In addition, there is a slight noise reduction for the Δf/BW = 1 setup. The reason possibly is that the strong blocker interference pushes/pulls the CG stage from the small signal state, and affects the small signal NF slightly. Differently, when Δf/BW = 3, the interference mainly is absorbed by C_N, and does not affect CG stage small signal operation, thus resulting in a fairly flat small signal NF curve. In turn, with the same offset configuration, the gain compression is also checked and given in Fig. 14. It displays that the resulting b1dB manifests around −17 dBm

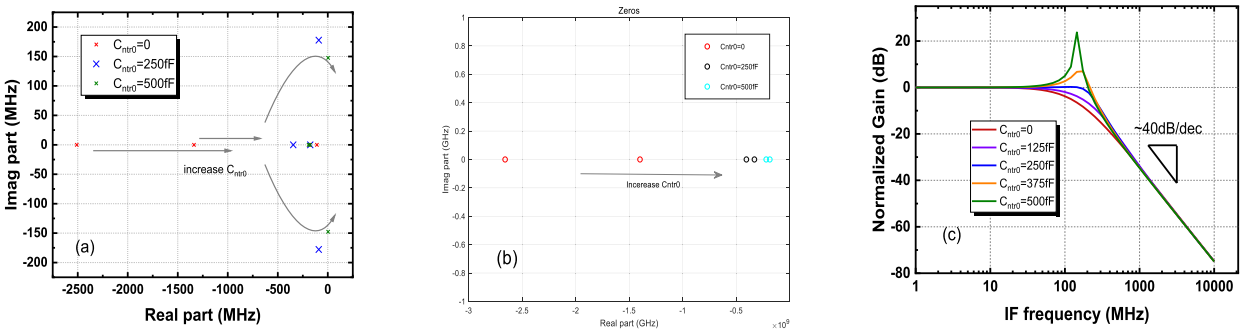

FIGURE 6. Neutralized capacitor influence on (a) poles, (b) zeros, and (c) BB TF.

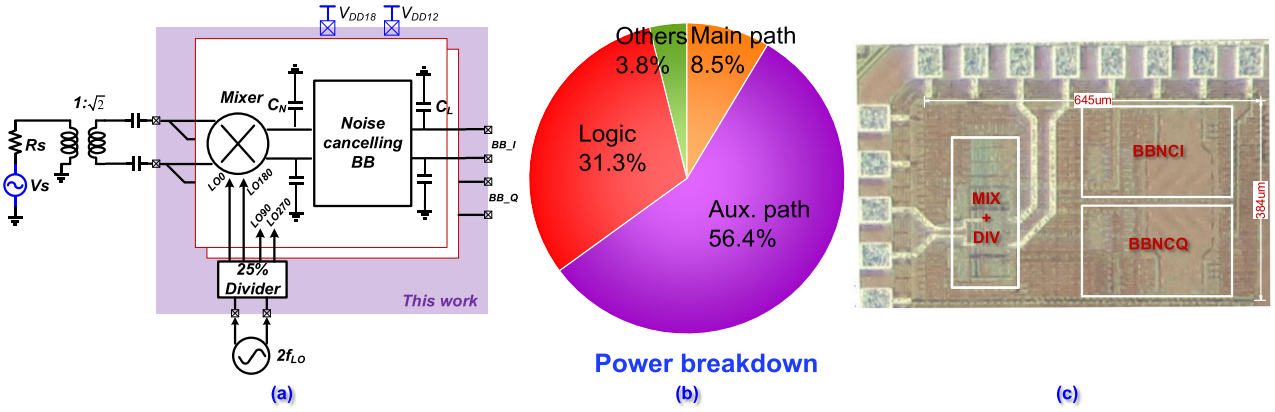

FIGURE 7. (a)Diagram of the presented receiver. (b) Power breakdown of the receiver. (c) Chip micrograph.

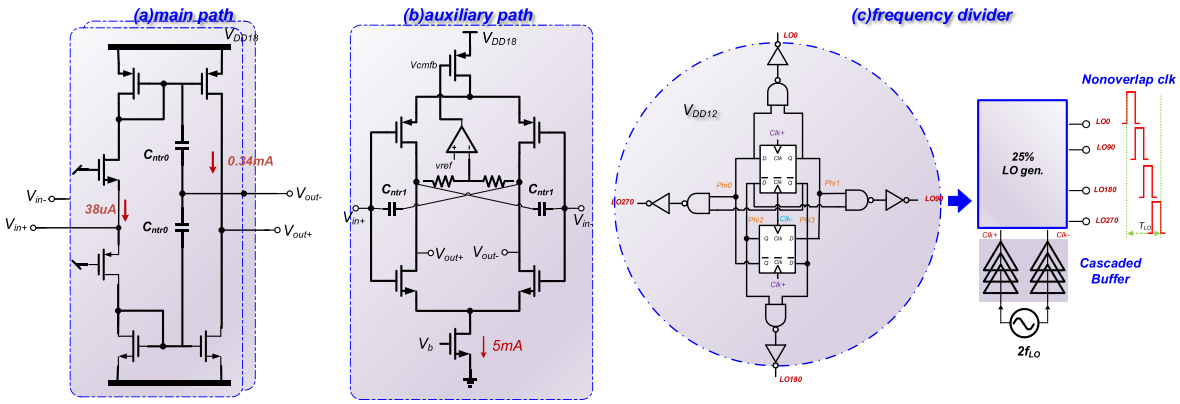

FIGURE 8. Subcircuit schematic of NC baseband of(a) main path and (b) auxiliary path, and (c) frequency divider.

in simulation at the frequency ratio of $\Delta f/BW = 1$, and -4 dBm in measurement at the ratio of $\Delta f/BW = 3$. The effective OOB filtering is again manifested in blocker gain perspective.

Nonlinearity is a common phenomenon in the electronic and communication world, couples of models are developed to explain this complex mechanism embedded and provide insightful predictions [15], [16]. The compact IP3 metric, however, is commonly used in the electronic domain to describe the distortion behaviors of active devices [17]. Specifically, a two-tone test with $f_{IF1} = 40$ MHz and $f_{IF2} = 50$ MHz under 2 GHz f_{LO}, indicates an inband (IB) IIP3 of -12.8 dBm in measurement, as shown in Fig. 15. The IB linearity is deduced to be limited by the non-ideal virtual ground nets, Vin+/− (Fig.8) seen by the larger IB interferences, inevitably creating unwanted voltage swings at BB input and

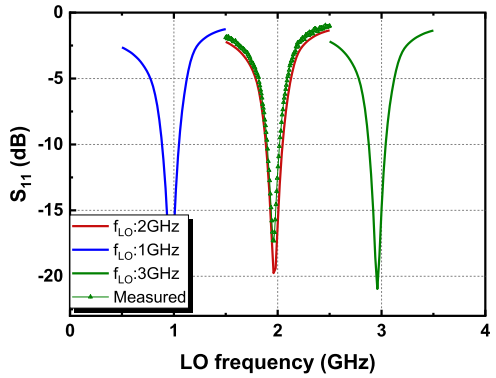

FIGURE 9. Input reflection coefficients, S11.

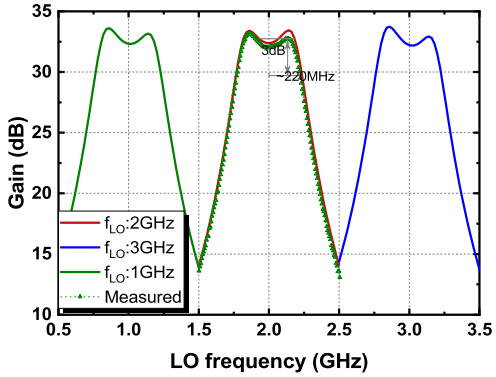

FIGURE 10. Conversion voltage gain.

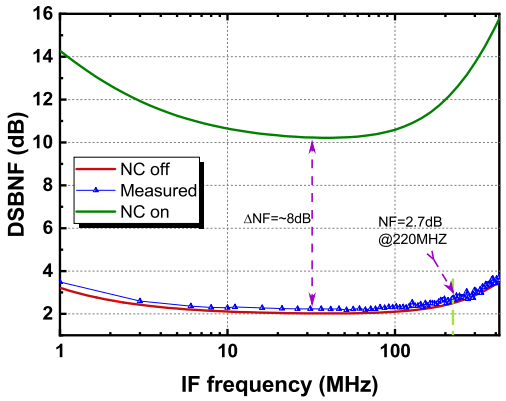

FIGURE 11. Noise figure versus IF variations under the auxiliary path on/off.

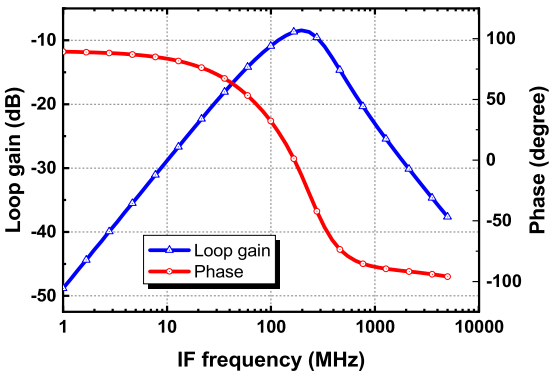

FIGURE 12. Stability simulation results.

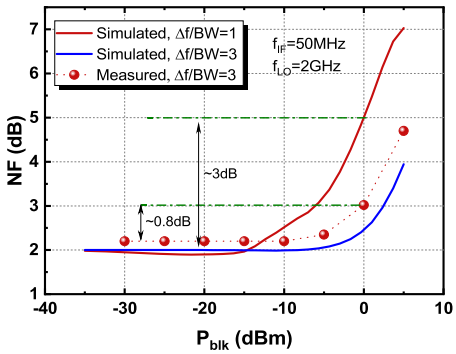

FIGURE 13. NF degeneration under large blocker interference with different frequency offsets.

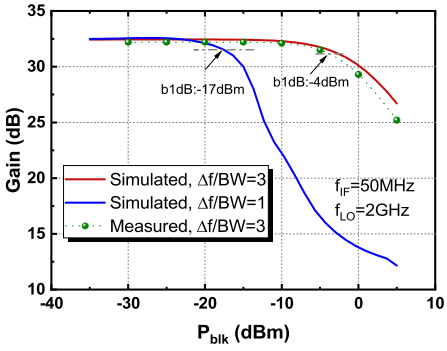

FIGURE 14. Gain compression under large blocker interference with different frequency offsets.

contributing distortions. Meanwhile, the auxiliary inverter stage cancels the distortions along the main path as per the NC principle, desirably. Nevertheless, the inverter stage itself also contributes considerable distortion. The report [8] uses degenerated resistors to form local feedback, improving IB linearity. But the gain and power consumption metrics significantly deteriorate. By considering this adverse influence, this linearity optimization via the degenerated resistor is not applied in our circuit. As far as the OOB IIP3 measurement is concerned, two test tones, including f1 and f2 are chosen at Δf and 2Δf -30MHz so that the third-order inter-modulation IM3s always sit at 30 MHz. Particularly, as given in Fig. 16, the measured OOB IIP3 of 15.5 dBm is obtained by setting $f_{IF1} = 660$ MHz $f_{IF2} = 1290$ MHz (namely, $\Delta f/BW = 3$) with the same $f_{LO} = 2$ GHz. The OOB IIP3 further increases up to $\sim$22 dBm when the $\Delta f/BW$ ratio takes as large as 7. The desirable OOB IP3 is contributed by the efficient dual-fold filtering of RF N-path + BB 40 dB/dec. It is worth pointing out that, although 3 GHz LO in maximum is reported in the above figures, an even higher operating frequency of the receiver frontend is still possible by adopting a more advanced CMOS process. Then the frequency divider with less parasitic is expected to cover a larger frequency band.

Table 2 summarizes the proposed receiver performances in comparison with state-of-the-art reports. By applying the capacitor positive feedback at the BB, the presented circuit has achieved a decent 220 MHz BB bandwidth, which is the best result among comparisons, according to the authors'

TABLE 2. Performance comparison to state of the arts.

Parameter	Architecture	Baseband BW	f_{RF}	Gain	NF	OB-IIP3	IB-IIP3	Power	Supply volt.	CMOS
Unit		MHz	GHz	dB	dB	dBm	dBm	mW	V	nm
[20]RFIC20[#]	LF ♥	40	1-6.2	48.2	3.4-4.2	-3.7(10[$])	-10	22.2	1.8/1	28
[14]MPLB20[*]	LF	13	0.2-3.3	45	2.4	4(8)	2.5	50.5	2.2/1.8	180
[9]JSSC20	MF♠	130	0.5–2	32.4	5.5	21(3)	-12	21.6[◊]+7.8[♦]	1.8/1.2	28
[10]RFIC22	MF	200	1-3	33.5	2.3	19(3)	-7.5	34+26	1.8/1.2	65
[19]JSSC19	MF	18	0.2–2	13	4.3-7.6	20(3)	0	143+18	1.2	28
[8]RFIC19	MF+NC♣	175	1-6	22	2.5-5	13(3)	9	172	0.83	22FDSOI
[18]JSSC20	MF+NC	18	0.2-1.2	31.4	3.4-4	26(3)	14.5	19.8+108	1.8	180
This work	MF+NC	220	1-3	32.2	2.2	15.5(3)	-12.8	21.9+10	1.8/1.2	65

[*]Simulation, [$]Δf/BW, [◊]single path, [♦]LO generation, [#]balun integrated, ♥ LNA first, ♠ mixer first, ♣ noise cancellation.

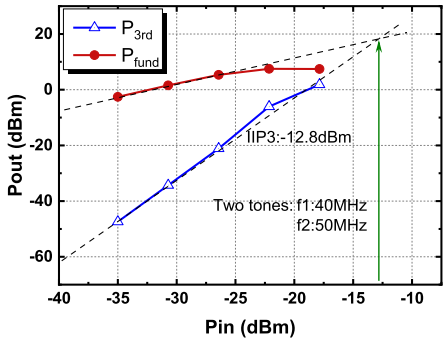

FIGURE 15. In-band linearity result plots.

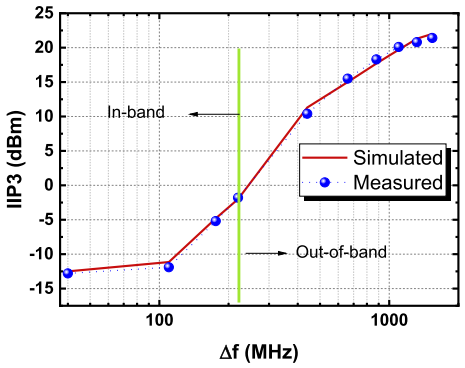

FIGURE 16. Out-of-band linearity result versus blocker frequency offsets.

knowledge range. The large BB bandwidth, also avoids bulky filtering capacitors appearing at the BB, greatly reducing the chip size budget. Moreover, thanks to the BB NC structure, the receiver circuit has achieved a competitive NF advantage while burning moderate power consumption. In contrast, the report [9] has shown much higher NF while the paper [8] burns a stunning power of 172 mW to enable a wideband operation. In terms of OOB IP3 performance, the paper [18] using a noisy second-order Nauch filter combining BB NC obtains the best result of that, but with larger NF. Furthermore, high-order BB filtering in [9] and [10] and enhanced N-path RF filtering in [19] realized excellent results as well. Closely following that, the second-order BB filter plus the N-path RF filter in the paper guarantees moderate OOB linearity. In contrast, the LF architectures have shown worse OOB IP3 than the MF architectures.

IV. CONCLUSION

In this paper, we present a CMOS mixer-first analog receiver with remarkable power reduction and excellent performance characteristics. Leveraging the current-mirror TIA structure and positive capacitive feedback, the proposed receiver achieves a wide baseband bandwidth and a second-order filtering profile while mitigating out-of-band interferences with RF N-path filtering and BB 40dB/dec roll-off. The presented receiver is fabricated using a standard 65 nm CMOS process and draws a minimal power of 32 mW at a typical 1 GHz LO stimulus. The measured results showcase, minimal noise figure, moderate voltage gain across a wide intermediate frequency range, and acceptable linearity both in-band and out-of-band. These results demonstrate the effectiveness of developing low-power and high-performance analog receivers that can be useful for the high data rate transmission of the sub-6 GHz band.

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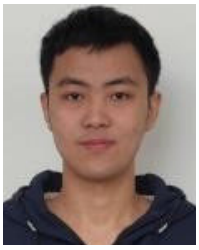

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