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A Single-Stage Switched-Boost Grid-Connected Five-Level Converter With Integrated Active Power Decoupling Under Polluted Grid Voltage Condition

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ABSTRACT Grid-connected inverters with a multilevel output voltage and an integrated dynamic voltage boosting feature are promising to achieve higher overall efficiency/power density, reduced output filter size, and better power quality. However, the input current of such a single-stage system might be pulsating with low- and high-frequency ripple contents in a single-phase grid-connected application. To tackle this challenge, active power decoupling (APD) can be used to keep the input current flat and reduce the current stress of the devices with an efficient performance. On the other hand, the grid voltage is usually nonideal in practice, polluted with the harmonics. This causes additional complexity in the closed-loop control system to maintain the injected power quality. The aim of this article is to apply a tailored closed-loop APD control on a recently proposed single-source single-stage switched-boost (SB) five-level converter leading to further enhancing its overall efficiency without adding any extra circuit components. A distinctive feature of the proposed solution is using a single proportional–resonant controller with a filtered feedforward term to achieve APD, even under a distorted grid voltage condition. This solution can also be applied to other single-stage SB-based converters as long as their input current before integration of the APD control contains a low-frequency ripple content. A 2-kW SiC-based prototype is built to validate the feasibility and accurate performance of the proposed method via experiments when connected to a grid with harmonic pollution.

INDEX TERMS Active power decoupling (APD), grid voltage disturbance, single-stage multilevel inverter, switched-boost (SB) technique.

I. INTRODUCTION

Single-phase grid-connected inverters with a high performance in terms of overall efficiency, compactness, voltage/current stress on devices, and reliability are widely used in many renewable-energy (RE)-based applications like photovoltaic (PV) grid-tied and electric vehicle (EV) systems [1]. The overall energy conversion architecture for the commercially available power converters usually consists of a two-stage process [2], [3], i.e., a dedicated front-end dc–dc bidirectional boost converter plus an inverter stage, as shown in Fig. 1. The dc source of the abovementioned RE-based applications is usually provided through a battery-integrated system, PV arrays, or fuel cells. The role of the front-end dc–dc bidirectional boost converter is to enhance/stabilize the dc-link voltage, making it compatible with the peak voltage magnitude of a standard grid. In the case of having a single-phase inverter stage free from any pulsating discontinuous inrush spike in its input current profile, the input dc source of the front-end stage must provide a double-line frequency ripple, which degrades maximum power point tracking (MPPT)

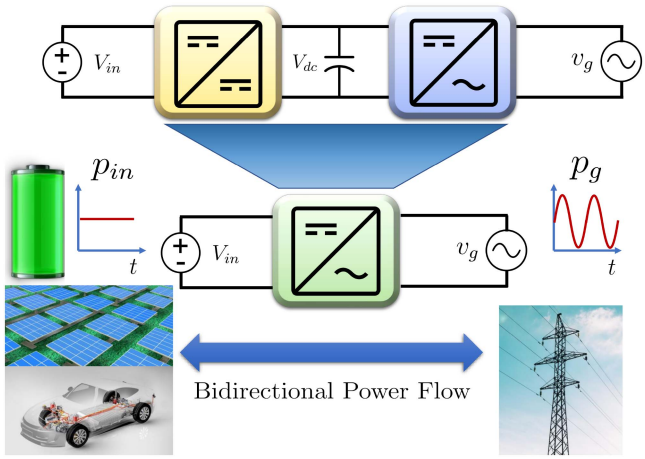

FIGURE 1. Differences in the energy conversion process between the conventional two-stage and boost-integrated single-stage dc–ac power converter architectures with APD control capability.

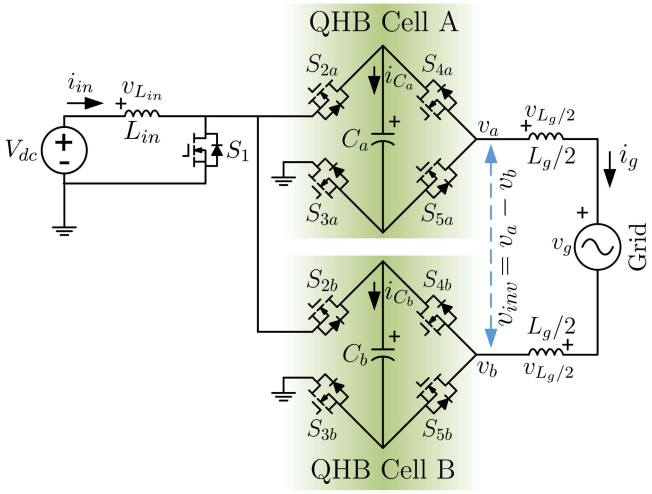

FIGURE 2. Circuit diagram of the S^{5}B5L grid-connected dc–ac converter proposed in [21].

in PV or smooth battery charging operation for EV applications [4], [5], [6].

The so-called power decoupling approaches, i.e., active power decoupling (APD) or passive power decoupling (PPD), are mandatory tasks for such a single-phase grid-tied system. Through the PPD solutions, the physical size of the passive elements, i.e., input boost inductor or dc-link electrolyte capacitor of the inverter stage, might be large and heavy, which, in turn, sacrifices the power density and reliability of the entire system [3], [7], [8]. On the contrary, the idea of APD control is to divert the low-frequency ripple content of the input current of the front-end dc–dc bidirectional boost converter to another energy storage element, i.e., the dc-link capacitor voltage of the inverter stage [6], [9], [10]. Alternatively, an APD control can be implemented using a dedicated buffer converter inserted between the dc source and the inverter stage [11], [12] or integrated into the dc–dc front-end bidirectional boost converter [13]. In both cases, the size of the energy storage elements can be kept low, while a good tradeoff between the overall efficiency and power density can be achieved. Nonetheless, the major drawback of implementing an APD is the requirement of another power processing stage, i.e., the dedicated dc–dc front-end boost converter or an additional/external buffer converter. This further hinders overall efficiency improvement of the whole system and can cause reliability and low power density issues [3], [8], [14].

Conversely, single-stage boost-integrated inverters have been recently put forward, in which they can boost the input dc voltage and synthesize an ac voltage at the output simultaneously. As shown in Fig. 1, with the integration of an APD control, an efficient energy conversion process for both PV and EV grid-connected applications is achievable. The single-stage two-level (2L) converters proposed in [15], [16], [17], and [18], the single-stage three-level (3L) buck–boost inverter presented in [19], and the single-stage common-grounded 3L boost inverter proposed in [20] are some of the recently rehearsed ideas with the possibility of an integrated APD control. Even though they use a low number of semiconductors, the output voltage of these single-stage inverters is only 2L or 3L, and their voltage boosting ability is limited within a certain range, while bidirectional power flow is not possible due to the presence of the diode in their circuit design. Moreover, within a single-stage control design, the presence of grid voltage harmonics, which is usual in many real applications, has not been adequately explored yet.

Alternatively, the concept of single-stage boost-integrated multilevel inverters with a higher number of output voltage levels, e.g., five-level (5L), has recently emerged with several notable features that can improve the power quality and power density of the whole system while achieving a lower total harmonic distortion (THD) and smaller size of output filters [21], [22], [23]. Among many topologies recently released, a single-source single-stage switched-boost 5L (S^{5}B5L) grid-connected converter has been presented in [21], which is shown in Fig. 2. It is a notable topology in terms of the number of semiconductor devices, improved dynamic voltage conversion gain, low value of the required passive elements, bidirectional power flow performance, and continuous input current profile. Despite these advantages, this topology still presents a double-line frequency ripple in the dc input current that can affect the overall efficiency.

The aim of this article is to further enhance the circuit performance of the abovementioned S^{5}B5L converter with an integrated APD capability in the presence of grid voltage harmonics for applications that require constant and ripple-free dc current (e.g., PV, battery, fuel-cell systems, etc.). As for the APD control, two simple proportional–integral (PI) controllers are used for the dc-link side, while only a single proportional–resonant (PR) controller is employed to govern the converter to inject the required current to the grid at the ac side. A general method based on a grid voltage observer

(GVO) technique has also been applied to synchronize the system with the fundamental component and obtain a filtered version of the grid voltage with low-frequency harmonics. The main features/contributions of this article are as follows.

1) To the best of the authors' knowledge, integration of APD into a single-stage switched-boost (SB) 5L converter without introducing additional circuit components has not been fully studied yet. This article aims to add APD capability to the S^{5}B5L converter, which is one of the promising types of available SB-based 5L converters in the literature. The same solution can also be applied to other types of SB-based converters as long as their input current before integration of APD contains only low-frequency ripple contents.
2) Increasing the overall efficiency of the previously proposed S^{5}B5L converter over a wide range of input dc voltage/power levels by reducing the current stress profile of the passive/active elements. This is achieved without changing the size of passive elements of the original circuit or adding any extra components.
3) Implementing a closed-loop grid current controller under a distorted grid voltage by only using a single PR controller, as opposed to the conventional multiresonant-based architecture, thus simplifying the overall control system design process.
4) Investigating the system performance under a polluted grid voltage with a straightforward GVO-based solution with inherent filtering capabilities. This improves the robustness of the system against high-frequency measurement noises and reduces the controller complexity using a feedforward technique.

To this end, an overview of the working principle for the abovementioned S^{5}B5L converter is presented in Sections II and III. The details of the closed-loop control strategy are given in Section IV. A comparative performance investigation in terms of overall efficiency, power losses, and size of the passive elements with and without APD control is performed in Section V. In addition, extensive experimental results obtained from a 2-kW SiC-based grid-connected prototype are shown in Section VI to prove the effectiveness of the proposed solution. Finally, Section VII concludes this article.

II. WORKING PRINCIPLE OF THE S^{5}B5L GRID-CONNECTED CONVERTER

The S^{5}B5L grid-connected converter proposed in [21] and shown in Fig. 2 is comprised of two quasi H-bridge (QHB) cells connected differentially with an input inductor, L_{in}, and a discrete power switch S_1. As can be seen, the topology requires nine power switches and two capacitors, while the converter is connected to the grid via split inductors L_g. The working principle of the converter for QHB cell A has been tabulated in Table 1, while v_{C_a} is the boosted voltage across the capacitor C_a. Depending on different values of D, which is the boost duty cycle for the switch S_1, the average voltage across C_a can be balanced at $V_C = \frac{V_{\text{dc}}}{1-D}$. Having taken v_a and v_b as the 3L switched output voltages of the QHB cells

TABLE 1. Working Principles and the List of ON Switching States for the Upper Side of the S^{5}B5L Converter Proposed in [21]

Switching States	ON-State Switches	Input Inductor Status	v_a
1	S_1, S_{3a}, S_{4a}	Charging	$+v_{C_a}$
2	S_{2a}, S_{3a}, S_{4a}	Discharging	$+v_{C_a}$
3	S_1, S_{3a}, S_{5a}	Charging	0
4	S_{2a}, S_{3a}, S_{5a}	Discharging	0
5	S_1, S_{2a}, S_{5a}	Charging	$-v_{C_a}$

TABLE 2. Working Principle of the S^{5}B5L Converter Proposed in [21]

Switching States	v_a	v_b	v_{inv}	v_{CM}
1	$+v_{C_a}$	$-v_{C_b}$	$v_{C_a} + v_{C_b} = 2v_C$	0
2	$+v_{C_a}$	0	$v_{C_a} = v_C$	$+v_C/2$
3	0	$-v_{C_b}$	$v_{C_b} = v_C$	$-v_C/2$
4	0	0	0	0
5	0	$+v_{C_b}$	$-v_{C_b} = -v_C$	$+v_C/2$
6	$-v_{C_a}$	0	$-v_{C_a} = -v_C$	$-v_C/2$
7	$-v_{C_a}$	$+v_{C_b}$	$-v_{C_a} - v_{C_b} = -2v_C$	0

A and B with respect to the ground, respectively, a resultant 5L inverter output voltage, v_{ab}, is synthesized, as tabulated in Table 2. Regarding this, details of the current flowing paths of the converter are illustrated in Fig. 3 [21]. Considering v_C as the same boosted voltage across C_a or C_b, the maximum output voltage of this S^{5}B5L grid-connected converter will be $\frac{1+D}{1-D}$, while the common-mode voltage, v_{cm}, is varying between zero and $v_C/2$. Regarding the operating principle of this circuit, some attractive features can be realized.

1) The structure does not need any extra energy storage element, i.e., a dc-link capacitor to be interfaced between the RE-based dc resource and the grid.
2) The voltage stress across all the semiconductor devices is uniform and equal to half of the inverter peak output voltage, i.e., $\frac{V_{\text{dc}}}{1-D}$.
3) The input current, i_{in}, is continuous and free from large pulsating inrush spikes, while due to the absence of diodes, a bidirectional power flow between the input dc source and the grid is possible. This makes the structure suitable for EV applications when both vehicle-to-grid and grid-to-vehicle operation modes are obtainable.
4) Due to the uniform switching performance in both half-cycles of the grid voltage, a phase-shifted pulsewidth modulation (PS-PWM) is possible to provide the gate switching pulses, which makes the apparent switching frequency at the inverter output twice the switching frequency. Therefore, a much smaller output filter is needed to interface the converter to the grid.

III. CLOSED-LOOP CONTROL STRATEGY APPLIED TO THE S^{5}B5L CONVERTER WITHOUT APD

According to the working principle of the abovementioned S^{5}B5L grid-connected converter, two control inputs, i.e., the boost duty cycle $D \in (0, 1)$ and the ac modulation reference

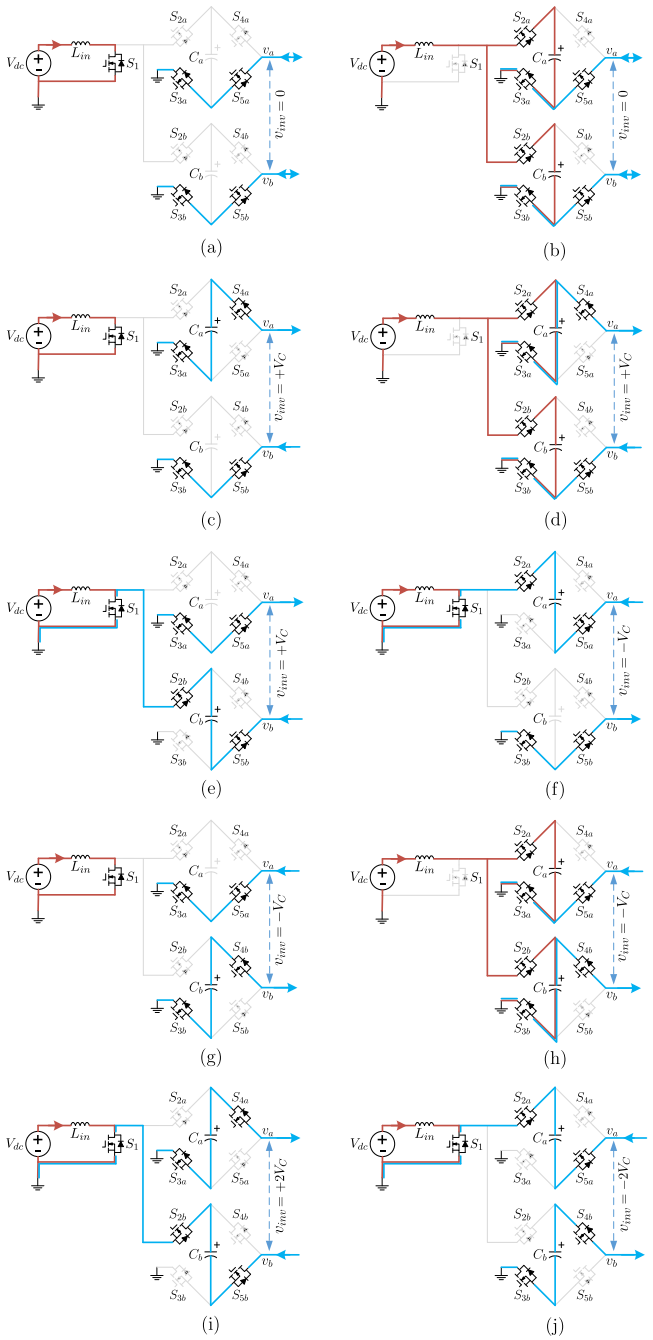

FIGURE 3. Current flowing paths of the proposed S^{5}B5L-VSI at (a) $v_{inv} = 0$, L_{in}: Charging; (b) $v_{inv} = 0$, L_{in}: Discharging; (c) and (e) $v_{inv} = +V_C$, L_{in}: Charging; (d) $v_{inv} = +V_C$, L_{in}: Discharging; (f) and (g) $v_{inv} = -V_C$, L_{in}: Charging; (h) $v_{inv} = -V_C$, L_{in}: Discharging; (i) $v_{inv} = +2V_C$, L_{in}: Charging; and (j) $v_{inv} = -2V_C$, L_{in}: Charging [21].

$u \in [-1, 1]$, must be generated by the closed-loop control strategy and sent to the PS-PWM stage to provide the required gate switching pulses. Hence, considering (1) as the average voltage across each of the involved capacitors, the inverter output voltage and its maximum fundamental value are expressed as (2) and (3), respectively:

$$V_c = \frac{V_{\rm dc}}{1 - D} \tag{1}$$

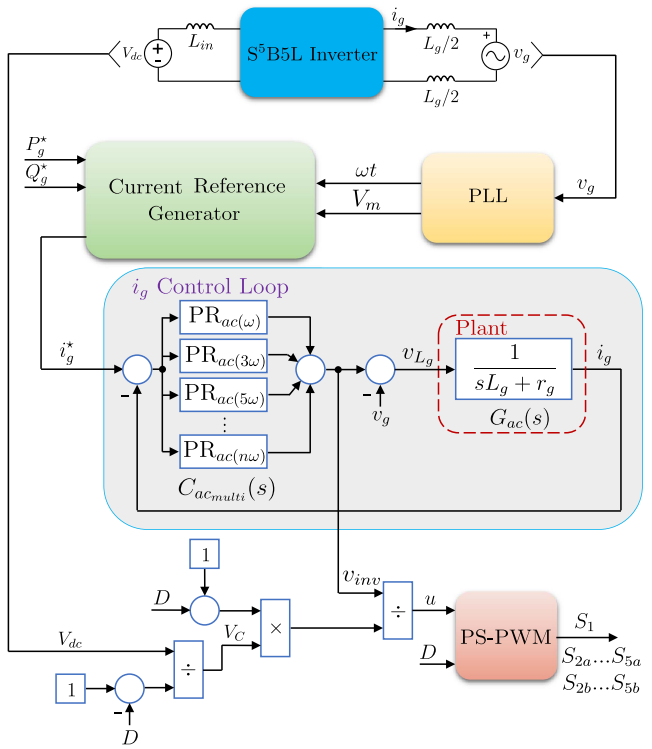

FIGURE 4. Conventional control strategy without APD control.

$$v_{\rm inv} = v_{\rm max} u \tag{2}$$

$$v_{\rm max} = (1 + D)V_c. \tag{3}$$

The aim of the conventional closed-loop control technique implemented in [21] is to govern the system to inject active and reactive power to a standard grid without applying the APD control. This is achieved by obtaining the ac reference u from the output of multiple PR controllers tuned at the expected grid voltage harmonic frequencies, as shown in Fig. 4. Here, a simple phase-locked loop (PLL) is used to detect the fundamental phase and amplitude of the grid voltage, i.e., ωt and V_m. Then, through the current reference generation stage and the desired active and reactive power references, $P_g^\star$ and $Q_g^\star$, a grid current reference, $i_g^\star$, is generated. As for an available input dc voltage, an appropriate value of boost duty cycle D is also defined based on the peak grid voltage and (3) to inject the power into the grid. Here, $G_{\rm ac}(s)$ is a first-order system plant based on the equivalent series resistance (ESR) and inductance of the grid-interface filter, describing the relationship between grid current, i_g, and the voltage across the grid-interface filter, v_{L_g}, in the frequency domain. Moreover, in this control strategy, the grid voltage v_g acts as an input disturbance for the PR controller, which can be rejected by multiple PR controllers tuned at the fundamental frequency and expected harmonics of the grid voltage [24], [25], [26]. Through this control design, the injected current is controlled; however, the input current contains a dominant double-line frequency ripple component leading to excessive conduction losses of the input dc inductors and semiconductors.

IV. PROPOSED CONTROL STRATEGY WITH APD

As opposed to the conventional solution, the proposed closed-loop control strategy applied to the described S^5B5L grid-connected converter includes an integrated APD control strategy that is able to operate under a grid voltage polluted with harmonics. Hence, to derive an expression for the injected grid power, p_g, it is necessary to define the grid voltage in the presence of the low-frequency harmonics, and the injected grid current, i.e.,

$$v_g = \sum_{h\in H} V_{g,h}\cos(h\omega t + \phi_h) \tag{4}$$

$$i_g = I_m\cos(\omega t + \phi) \tag{5}$$

where h, $V_{g,h}$, ϕ_h, ω, I_m, and ϕ are the harmonic order, the amplitude and phase of the hth harmonic of the grid voltage, the grid fundamental angular frequency, the peak value of the injected current, and the phase angle of the injected grid current with respect to the fundamental harmonic of the grid voltage, respectively. Moreover, $H = \{1, 3, 5, \ldots, M\}$ is the measured harmonics, where M is the highest harmonic order considered, and $\phi_1 = 0$. Hence, the expression for p_g can be derived as follows:

$$\begin{aligned} p_g &= v_g i_g \\ &= \sum_{h\in H} \frac{V_{g,h}I_m}{2}[\cos((h-1)\omega t + \phi_h - \phi) \\ &\quad + \cos((h+1)\omega t + \phi_h + \phi)]. \end{aligned} \tag{6}$$

From (6), it can be deduced that p_g in the single-phase grid-tied application consists of a dc, $p_{g,\mathrm{dc}}$, and a low-frequency ripple, $p_{g,r}$, term as

$$\begin{aligned} p_{g,\mathrm{dc}} &= \frac{V_m I_m}{2}\cos(\phi) \\ p_{g,r} &= p_g - p_{g,\mathrm{dc}} \end{aligned} \tag{7}$$

where V_m is the fundamental amplitude of the grid voltage, i.e., $V_m = V_{g,1}$.

On the other hand, according to the concept of APD control strategy, the input dc source power p_{in} has to be free from any low-frequency ripple/pulsating content. Hence, the ripple ac power $p_{g,r}$ must be provided by the integrated energy storage elements, e.g., the boost inductor L_{in} or the capacitors C_a or C_b in the described S^5B5L converter. Considering that the aim of an APD control strategy is to cancel out any low-frequency ripple from the input current, $p_{g,r}$ is provided through the contribution of the capacitors in the S^5B5L grid-connected converter. Therefore, considering p_C as the required instantaneous power of the involved capacitors, it follows that

$$p_g = p_{\mathrm{in}} + p_C \tag{8}$$

$$p_C = p_{C_a} + p_{C_b} = p_{g,r}. \tag{9}$$

Hence, considering identical capacitance C for both integrated capacitors, the instantaneous capacitor voltages, which include a low-frequency ac ripple term, are expressed as follows:

$$v_C^2(t) = \frac{1}{C}\int p_{g,r}(t)dt \tag{10}$$

$$\begin{aligned} v_C^2(t) &= \frac{V_m I_m}{2C}\frac{\sin(2\omega t + \phi)}{2\omega} \\ &\quad + \frac{I_m}{2C}\sum_{h\in H, h\neq 1} V_{g,h}\left(\frac{\sin((h-1)\omega t + \phi_h - \phi)}{(h-1)\omega}\right. \\ &\quad \left. + \frac{\sin((h+1)\omega t + \phi_h + \phi)}{(h+1)\omega}\right) + K \end{aligned} \tag{11}$$

$$\tilde{v}_C^2 = v_C^2 - K \tag{12}$$

where K is the integration constant value related to the average capacitor voltage requirement of each of the involved capacitors to meet the peak grid voltage value as per (3).

Considering the above discussion, the overall control block diagram consists of four sections, as shown in Fig. 5, where the aim of APD control is fulfilled by controlling i_{in} free from any low-frequency ripple component, v_C with the required average value, and the injected grid current i_g, following a sinusoidal reference current. Hence, $i_{\mathrm{in}}^\star$, $V_C^\star$, and $i_g^\star$ are defined as the references for the input current, the average capacitor voltages, and the injected grid current, respectively. Here, the GVO or PLL mechanism shown in Fig. 5(a) is in charge of grid synchronization and extracting the first harmonic information of a polluted grid voltage to define the required references. In this article, a GVO is designed as an alternative solution instead of a conventional PLL. The added benefit of using GVO instead of a PLL is its inherent filtering ability against high-frequency noises in the grid voltage measurement. Fig. 5(b) and (c) also indicate the requirement of the APD control for the dc input current and capacitor voltages, while Fig. 5(d) and (e) show the details of the controller to inject the desired active and reactive power to the grid at the ac side and its modulator, respectively. Herein, as for V_C and i_{in} control loops, two PI controllers, i.e., $C_C(s)$ and $C_{\mathrm{dc}}(s)$ in Fig. 5(b) and (c), are needed, where the first-order transfer functions, $G_C(s)$ and $G_{\mathrm{dc}}(s)$, are considered to design the aforementioned controllers.

Regarding the capacitor voltage control loop, the plant transfer function $G_C(s)$ has been derived based on the relationship between the capacitor power and the squared value of the capacitor voltage in the frequency domain, i.e., $P_C = sCV_C^2$. It should be noted that since both C_a and C_b have the same voltage due to the switching states of the S^5B5L converter (see Fig. 3), $G_C(s)$ is derived based on the total equivalent capacitance, i.e., C_a and C_b in parallel. Similarly, the plant transfer functions for the dc input current and grid current control loops are obtained based on the relationship between the current and the voltage across an L-type filter considering its parasitic ESR. As for the injected grid current control loop shown in Fig. 5(d), a single PR controller, $C_{\mathrm{ac}}(s)$, is designed based on $G_{\mathrm{ac}}(s)$. Here, r_C, r_{in}, and r_g are denoted as the ESR

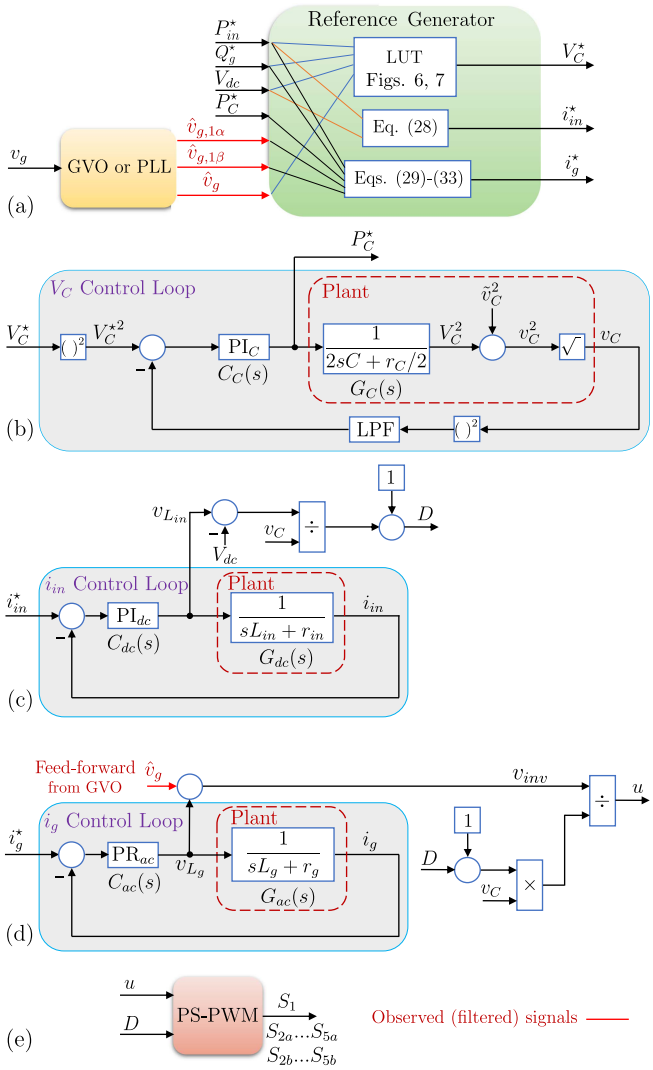

FIGURE 5. Proposed control strategy with APD. (a) Grid synchronization and reference generation. (b) Capacitor voltage controller. (c) DC input current controller. (d) Grid current controller. (e) Modulator.

of the involved capacitors, the input inductor, and the output filter inductors, respectively.

It should be noted that the feedforward term used in the grid current controller is obtained from the GVO; hence, it can be considered as a filtered replica of the grid voltage measurement, while including all the expected low-frequency harmonics. Consequently, the calculated inverter voltage is free from any high-frequency noises. By considering a zero-order hold (ZOH) discretization, the required parameters of the PI and PR controllers for the input current, capacitors voltages, and the injected grid current control are obtained in the z-domain for digital implementation. As indicated in Fig. 5(b), to extract the dc component (average) of v_C, a low-pass filter is required. In the next subsections, the mechanism of the GVO and the reference design for the three main control loops are described in detail.

A. GVO MECHANISM

In the general case of having a polluted grid voltage with several low-frequency harmonics, the fundamental component of the grid voltage is required to be extracted for the current reference generation. Moreover, obtaining a noise-free version of the measured grid voltage is also relevant since it is used as a feedforward term in the i_g control loop. Conventionally, a PLL can be employed for this purpose; however, the whole PLL structure must be replicated for each harmonic component to reconstruct a clean sample of the grid voltage. A more suitable and straightforward alternative for extracting this information is to develop a generalized GVO mechanism. As this is an observer-based synchronization strategy, this single structure can be used not only to decompose the grid voltage in each harmonic component but also to reduce the high-frequency noise of the instantaneous grid voltage measurement. Hence, the measured grid voltage in the stationary reference frame can be expressed as a summation of its harmonic contents:

$$v_{g_{\alpha\beta}} = \sum_{h\in H} v_{g,h_{\alpha\beta}} \tag{13}$$

where $v_{g_{\alpha\beta}} \in \mathbb{R}^2$ and $v_{g,h_{\alpha\beta}} \in \mathbb{R}^2$ are the grid voltage and its harmonic component vectors in a stationary reference frame, respectively. Therefore, $v_{g,h_{\alpha\beta}}$ can be written as

$$v_{g,h_{\alpha\beta}} = \begin{bmatrix} v_{g,h_\alpha} \\ v_{g,h_\beta} \end{bmatrix} = \begin{bmatrix} V_{g,h}\cos(h\omega t + \phi_h) \\ V_{g,h}\sin(h\omega t + \phi_h) \end{bmatrix}. \tag{14}$$

Assuming the steady-state condition or slowly changing harmonic content of the grid voltage, the derivative of each grid voltage harmonic can be derived as follows:

$$\frac{dv_{g,h_{\alpha\beta}}}{dt} = \frac{d}{dt}\begin{bmatrix} v_{g,h_\alpha} \\ v_{g,h_\beta} \end{bmatrix} = Jh\omega v_{g,h_{\alpha\beta}} \tag{15}$$

where

$$J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}. \tag{16}$$

A continuous-time state-space system model can be constructed based on (13)–(15) with the grid voltage harmonics in a stationary reference frame as the system states, x, and the grid voltage as the system output, y:

$$x = \begin{bmatrix} v_{g,1_{\alpha\beta}} & v_{g,3_{\alpha\beta}} & \dots & v_{g,M_{\alpha\beta}} \end{bmatrix}^T \tag{17}$$

$$y = v_{g_\alpha} = \sum_{h\in H} v_{g,h_\alpha}. \tag{18}$$

This leads to the following continuous-time state-space model:

$$\frac{dx}{dt} = A_c x + \varpi \tag{19}$$

$$y = C_c x + \nu \tag{20}$$

where

$$A_c = \begin{bmatrix} J\omega & O_2 & O_2 & \dots & O_2 \\ O_2 & J3\omega & O_2 & \dots & O_2 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ O_2 & O_2 & O_2 & \dots & JM\omega \end{bmatrix} \tag{21}$$

$$C_c = \begin{bmatrix} 1 & 0 & 1 & 0 & \dots & 1 & 0 \end{bmatrix} \tag{22}$$

and O_2 is a zero matrix of dimension 2×2. Moreover, ϖ and ν are the process and measurement noises, respectively.

This dynamic model can be discretized using the ZOH method. Therefore, the following discrete state-space model is formed:

$$\begin{aligned} x_{k+1} &= Ax_k + \varpi_k \\ y_k &= C_c x_k + \nu_k \end{aligned} \tag{23}$$

where A is the resultant state dynamics matrix after discretization. Here, it is important to emphasize that the pair (A, C_c) is observable. Therefore, based on the derived discrete state-space model in (23), an observer can be designed through either a pole placement or a steady-state Kalman filter approach. The pole placement method is based on placing the poles of the closed-loop transfer function at specific locations on the complex plane by normally selecting two dominant poles to achieve the desired behavior. However, using this method for systems with a large number of states might be complicated and not necessarily optimal. On the contrary, the Kalman filter approach can deal with a larger number of states, while the observer parameters can be obtained optimally [27]. In this work, the latter is chosen due to the large number of states. Thus, the GVO is designed to estimate the instantaneous amplitude of each harmonic of the measured grid voltage as

$$\begin{aligned} \hat{x}_{k+1} &= A\hat{x}_k + G_o(y_k - \hat{y}_k) \\ \hat{y}_k &= C_c\hat{x}_k \end{aligned} \tag{24}$$

where G_o, $\hat{x}_{k+1}$, and $\hat{x}_k$ are the observer gain matrix and estimated states at time step k and $k+1$, respectively. Similarly, $\hat{y}_k$ is the estimated output (i.e., grid voltage) at time instant k.

The observer gain matrix G_o can be calculated based on the known system and noise parameters, i.e., discrete state-space model in (23), by solving the following discrete-time algebraic Riccati equation, as explained in [27] and [28]:

$$G_o = APC_c^T(C_cPC_c^T + R_f)^{-1} \tag{25}$$

$$P = APA^T - G_oC_cPA^T + Q_f \tag{26}$$

where P is the estimate covariance matrix, R_f is the measurement noise covariance matrix, and Q_f is the process noise covariance matrix. In this article, as there is only one measurement used for the observer, R_f possesses only a scalar value that depends on the grid voltage sensor noise, i.e., a noisier sensor translates to a higher value of R_f. The value of R_f should be equal to the covariance of the voltage sensor, which can be easily obtained by recording a large number of measurements with constant voltage at the sensor's input and calculating the covariance of the recorded values. In addition, Q_f represents the process noise that can be caused by model errors or uncertainties. Here, Q_f is considered as

$$Q_f = q_f I_n \tag{27}$$

where I_n is the identity matrix with the same dimensions as A, and $q_f > 0$ is a number indicating model errors. Therefore, a larger q_f means that the model is not trusted, and the observer relies more on the sensor information. Conversely, a smaller q_f implies an accurate state-space model, and the observer relies more on the model predictions. Consequently, the value of q_f can be used to set the observer bandwidth [28]. Knowing R_f and Q_f, matrices P and G_o can be calculated using (25) and (26). It should be noted that the observer gain, G_o, is a constant matrix (time-invariant). Hence, it can be calculated offline to reduce the computational overhead of the observer. Here, the function *idare* in MATLAB is used to solve (25) and (26) and obtain G_o.

Therefore, following the described procedure above, as indicated in Fig. 5(a), the GVO gets the measured grid voltage as per (4) and outputs the estimated value of the grid voltage, $\hat{v}_g$. This helps to reject high-frequency measurement noises effectively. Consequently, to define the grid current reference, $i_g^\star$, as for the next stage of the control system shown in Fig. 5(a), the fundamental value of the observed grid voltage in the stationary $(\alpha\beta)$ reference frame, i.e., $\hat{v}_{g,1\alpha\beta}$, is extracted through the GVO stage.

B. REFERENCE DESIGN

As per Fig. 5(a), the reference generator stage receives six inputs, i.e., $P_{\text{in}}^\star$, $Q_g^\star$, V_{dc}, $P_C^\star$, and $v_{g,1_{\alpha\beta}}$, which are the intended reference values of the input active power, grid reactive power, the input dc voltage of the converter, the required capacitors power reference, and the observed fundamental value of the grid voltage extracted from the described GVO mechanism, respectively. Through these, the references $i_{\text{in}}^\star$, $V_C^\star$, and $i_g^\star$ are generated to govern the system as per Fig. 5(b)–(d). Moreover, the active and reactive grid power references, $P_{\text{in}}^\star$ and $Q_g^\star$, are external references, which represent the power level being transferred from/to the power supply to/from the grid and required reactive power compensation level. Consequently, the required references are expressed as follows:

$$i_{\text{in}}^\star = \frac{P_{\text{in}}^\star}{V_{\text{dc}}} \tag{28}$$

$$P_g^\star = P_{\text{in}}^\star + P_C^\star \tag{29}$$

$$i_g^\star = \frac{2P_g^\star}{\hat{V}_m}\cos(\omega t) + \frac{2Q_g^\star}{\hat{V}_m}\sin(\omega t) \tag{30}$$

where

$$\hat{V}_m = \sqrt{\hat{v}_{g,1_\alpha}^2 + \hat{v}_{g,1_\beta}^2} \tag{31}$$

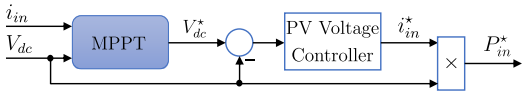

FIGURE 6. Additional MPPT controller providing the input power reference, $P_{\text{in}}^{\star}$, to the proposed APD control strategy.

$$\cos(\omega t) = \frac{\hat{v}_{g,1_\alpha}}{\hat{V}_m} \tag{32}$$

$$\sin(\omega t) = \frac{\hat{v}_{g,1_\beta}}{\hat{V}_m}. \tag{33}$$

It should be noted that an MPPT functionality can be added to the proposed APD solution for PV-based applications. In this case, an MPPT controller is required to decide the PV voltage reference, $V_{\text{dc}}^{\star}$, and a PV voltage controller (e.g., a PI controller) follows the reference by generating the input current reference, $i_{\text{in}}^{\star}$, accordingly. Since the proposed APD control scheme expects the input power reference, $P_{\text{in}}^{\star}$, it is obtained by multiplying $i_{\text{in}}^{\star}$ and V_{dc}. Fig. 6 illustrates such a control scheme.

Regarding the grid-tied operation of the S^{5}B5L converter, the average capacitor voltage V_C should be set high enough to meet the grid voltage at any time instant. Hence, considering (2) and (3), the following relation must be satisfied:

$$v_{\max} > v_g > -v_{\max}. \tag{34}$$

On the other hand, assuming the steady-state condition, by substituting $v_C = \frac{V_{\text{dc}}}{1-D}$ into (3), an alternative expression for $v_{\max}$ can be derived as follows:

$$v_{\max} = 2v_C - V_{\text{dc}}. \tag{35}$$

Therefore, (34) can be rewritten as

$$2v_C - V_{\text{dc}} > v_g > -(2v_C - V_{\text{dc}}). \tag{36}$$

The derived inequality in (36) can be further expanded by substituting (11) into the expression. Consequently, by knowing the operating conditions, i.e., the grid voltage, the amplitude of the injected grid current, the input dc voltage, and the power factor, a minimum value of K in (11) can be found. Hence, there exists a minimum average capacitor voltage that can satisfy (36), which is chosen as the reference value $V_C^{\star}$ for the capacitor voltage loop control, as depicted in Fig. 5(c). In this article, due to the nonlinear behavior of the involved equations, this calculation has been performed offline using numerical and iterative methods, and the value of the minimum average capacitor voltage has been stored in a lookup table for a given range of operating conditions. The resultant values of $V_C^{\star}$ are shown in Figs. 7 and 8 for $C = 75$ µF. Fig. 7 depicts the minimum average capacitor voltage at unity power factor and for different power levels and the input dc voltages. In addition, Fig. 8 shows the variation of this minimum average capacitor voltage at $V_{\text{dc}} = 100$ V and different power factors and power levels.

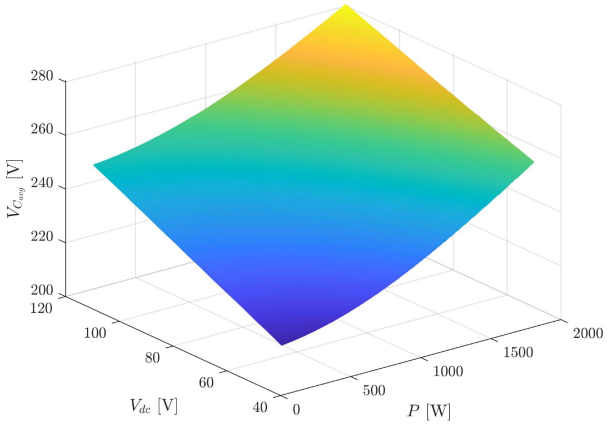

FIGURE 7. Minimum required average capacitor voltage (V_C) for a given grid-tied operating condition at $C = 75$ µF, $L_{in} = 0.19$ mH, and $V_m = 320$ V.

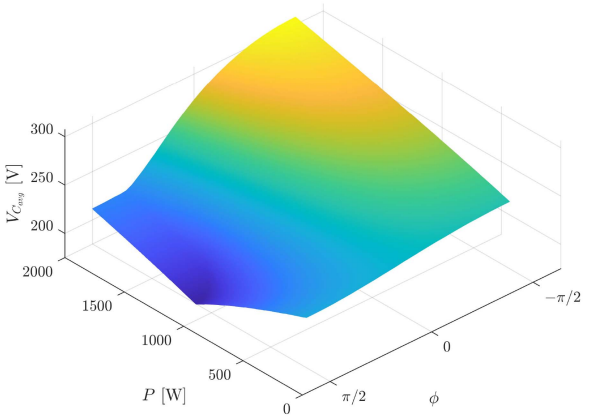

FIGURE 8. Minimum required average capacitor voltage (V_C) for a given ϕ and grid-tied operating condition at $V_{\text{dc}} = 100$ V, $C = 75$ µF, $L_{in} = 0.19$ mH, and $V_m = 320$ V.

TABLE 3. Controller Parameters Used for Simulation and Experimental Prototype

Parameter	Value
Switching Frequency	100 kHz
$L_{g_{\text{nom}}}$	1.2 mH
$C_a, C_b, (r_C)$	75 µF, (3 mΩ)(Film)
L_{in} , (r_{in})	0.19 mH, (60 mΩ)
$L_g, (r_g)$	1.2 mH, (80 mΩ)
ω	$2\pi \times 50$ rad/s
$C_C(s)$	$0.007 + \frac{0.1}{s}$
$C_{\text{dc}}(s)$	$7.103 + \frac{46881}{s}$
$C_{\text{ac}}(s)$	$30.079 + \frac{263190s}{s^2+\omega^2}$

C. STABILITY AND SENSITIVITY ANALYSIS

To ensure the stable operation and robust performance of the proposed control strategy, a detailed stability and sensitivity analysis has been conducted in this section. The circuit/controller parameters are outlined in Table 3. First, the tracking performance and the control input disturbance rejection of the dc input current controller are depicted and verified in Fig. 9. As shown in Fig. 9(a), the controller can track dc references accurately without any steady-state error.

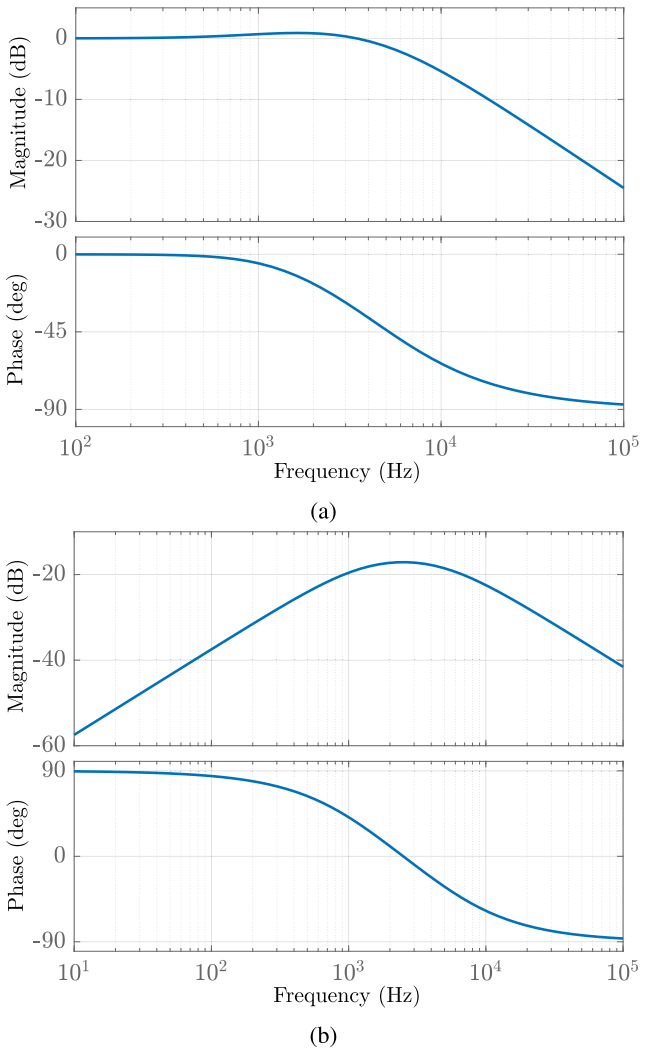

FIGURE 9. Bode plot of (a) closed-loop system: i_{in}^{*} to i_{in} and (b) i_{in} closed-loop input sensitivity against input disturbances.

Moreover, Fig. 9(b) indicates that control input disturbances are always rejected with more than 17-dB attenuation in the worst case.

Next, regarding the uncertain value of L_g, a sensitivity analysis based on the root locus method is performed to show the stability of the controller over a wide range of L_g. Fig. 10 illustrates the root loci plot of the closed-loop poles for the grid current controller with the variable parameter L_g. As can be seen, over the whole range of possible values of L_g (i.e., from 0 to $+\infty$), all the poles have a negative real part. In addition, the location of the poles over the range $[0.5L_{g_{\text{nom}}}, 2L_{g_{\text{nom}}}]$ are shown in red in Fig. 10, in which all the real parts are negative. Furthermore, the gain and phase margins of the grid current controller are obtained and depicted in Fig. 11(c), in which the gain margin is infinite and the phase margin is 71.8°. Therefore, the stable operation of the grid current controller is guaranteed.

Then, the tracking performance and the control input disturbance rejection of the grid current controller are depicted and verified in Fig. 11(a) and (b), respectively. As shown in Fig. 11(a), the controller can track ac references at fundamental grid frequency (50 Hz) accurately without any steady-state error. Moreover, Fig. 11(b) indicates that control input disturbances are always rejected with more than 25-dB attenuation in the worst case. It should be noted that any disturbance at the fundamental grid frequency will be rejected perfectly, as shown in Fig. 11(b).

V. COMPARATIVE STUDY

As early discussed, applying the APD control to the S^{5}B5L converter can enhance the overall efficiency of the whole conversion system by reducing the current stress profile of the switches, and the input inductor. In the following subsections, the performance of the S^{5}B5L converter with and without APD control and a case-to-case comparison over other available solutions/converters are presented.

A. PERFORMANCE INVESTIGATION OF THE S^{5}B5L CONVERTER WITH AND WITHOUT APD

Figs. 12 and 13 show typical key waveforms of the S^{5}B5L converter over four fundamental grid cycles, T, connected to a grid with an ideal sinusoidal and polluted voltage, respectively. During the first two cycles, the APD control is OFF; therefore, the input current i_{in} has a dominant double-line frequency ripple. After this, the APD control strategy is activated, and therefore, the low-frequency ripple components of i_{in} is diverted to v_c. The variation of the boost duty cycle D and the ac modulation reference u is due to applying the APD control and the presence of the harmonics in the grid voltage. It is worth mentioning that although the 5L waveform of the inverter output voltage is affected by the APD control, the injected grid current i_g still has a low THD due to the closed-loop current control.

In the following, a comparative study in terms of current stress and power loss distribution on devices of the abovementioned S^{5}B5L grid-connected converter is conducted to further highlight the performance of the converter with and without APD control strategy. The circuit/controller specifications for this comparative study have been tabulated in Table 3, while PLECS software is used to perform the simulations. Herein, to target a polluted grid with the presence of low-frequency harmonics, the grid voltage is assumed as follows:

$$v_g = 320[\cos(\omega t) + 0.1\cos(3\omega t) + 0.05\cos(5\omega t)]. \quad (37)$$

As for comparative analysis, two different case studies based on the availability of the input dc voltage source, i.e., $V_{\text{dc}} = 100$ V and $V_{\text{dc}} = 50$ V, are considered, while the rated injected power to the grid is assumed to be the same as $P_g = 2$ kW. As can be seen from Fig. 14(a) and (b), there is a clear reduction in rms values of the current stress profile on different circuit devices when the APD control is activated. This improvement is more visible when a higher value of the boost duty cycle or a lower value of the input dc voltage is adopted, as can be confirmed by Fig. 14(a) and (b). It should be noted that the rms currents of the involved components

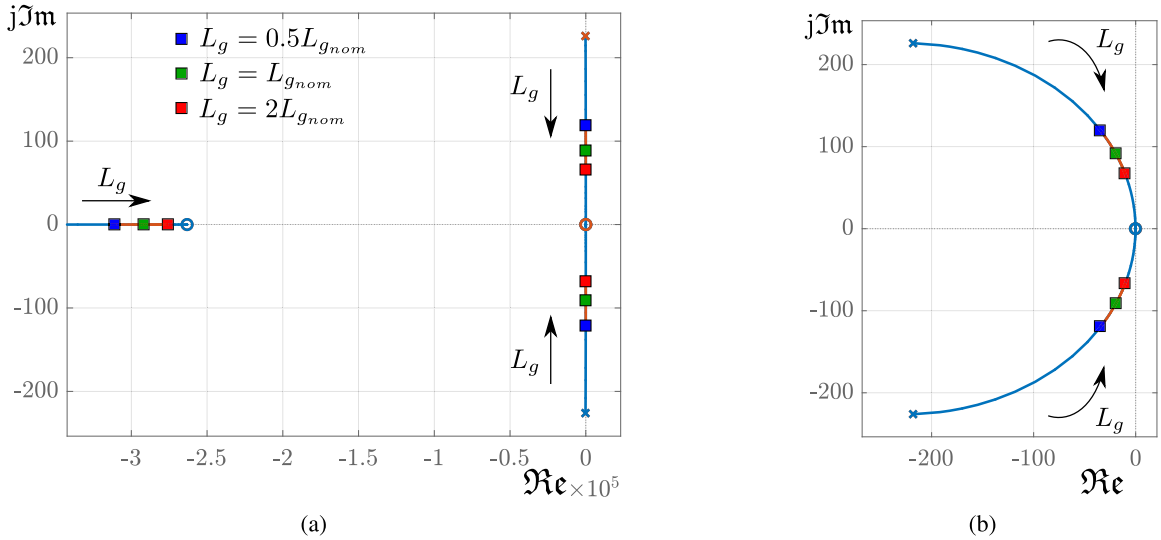

FIGURE 10. Root loci plot of the closed-loop poles under varying parameter L_g. (a) Overall view. (b) Zoomed-in view.

TABLE 4. Circuit-Characteristic-Based Comparison Among Different Available Topologies With APD Control

Topology	No. of Stages	No. of Levels	Cap. Voltage Rating	Cap. Value	L_{in} value	L_g value	Rated Power, f_{sw}	Reported Efficiency
Ref. [3]	2	3	450–600V	2×60 µF	NA	2×1 mH	1 kW, 20 kHz	89.5% @ 1kW
Ref. [6 ,Fig. 1a]	2+Buffer	3	400–700V	30 µF	NA	1 mH	2 kW, 30 kHz	97% @ 2 kW
Ref. [6, Fig. 1f]	2+Buffer	3	350V	75 µF	NA	1 mH	2 kW, 30 kHz	96.1% @ 2 kW
Ref. [10]	2	2	400V	30 µF	NA	2×2.2 mH	1 kW, 19 kHz	92% @ 1 kW
Ref. [13]	2	3	450V	430 µF	8 mH	2×7 mH	2.4 kW, 20 kHz	NA
Ref. [15]	1	2	250V	2×20 µF	20 µH	3 mH, 3.3 mH	180 W, 20–300 kHz	93% @ 180 W
Ref. [16]	2	2	550V	45 µF	230 µH	230 µH	3 kW, 100 kHz	95.6% @ 3 kW
Ref. [18]	1	2	400V	2×220 µF	2.75 mH	2×2 mH	180 W, 10 kHz	NA
Ref. [19]	2	3	600V	100 µF	3 mH	2.2 mH	2 kW, 20 kHz	96% @ 2 kW
Ref. [20]	1	3	450V	22 µF	30 µH	1.5 mH	400 W, 25 kHz	95% @ 400 W
S^5B5L Converter	1	5	250V	2×75 µF	190 µH	2×0.6 mH	2 kW, 100 kHz	95.2% @ 2 kW

TABLE 5. Components Used in the Experimental Prototype

Element	Type and Description
Power Switches	UJ4C075018K4S
Controller	DSP-TMS320F28379D
Gate Drivers	UCC21710
Isolated dc–dc Converters	MGJ2D121505SC
Voltage/Current Sensors	AMC3301

at $V_{dc} = 100$ V and $V_{dc} = 50$ V are not fully complying the power-balance theory when the APD control is OFF, i.e., the rms value of the dc input current in the first case is not half of the second case, as L_{in} tends to resonate with C_a and C_b due to the nature of the original circuit.

Since the proposed converter is a nonlinear dynamic system with time-variant coefficients in its state-space model, obtaining an accurate closed-form expression for the rms input current is not feasible [21]. However, a simulation-based sensitivity analysis has been performed to investigate the impact of the passive circuit components (L_{in} and C_a, C_b) on the rms input current values for both conventional and proposed control methods at $V_{dc} = 100$ V and $V_{dc} = 50$ V. As shown in Fig. 15, the rms input current is always lower when the APD control is enabled. In the case of conventional control, due to the resonant energy exchange between L_{in} and C_a, C_b, at certain passive components and D values, rms input current grows excessively. This phenomenon can also be described based on the equivalent resonant frequency of the dc input side of the converter. When the abovementioned resonant frequency is close to the grid power harmonics, a large low-frequency ripple on the passive components is expected, as shown in Fig. 15. Moreover, the resultant large ripple can lead to system instability in extreme cases (missing areas when the APD is OFF in Fig. 15). However, with the proposed APD control strategy, i_{in} is directly controlled by the PI controller $C_{dc}(s)$ to achieve a flat dc input current and suppress the resonance between C_a, C_b and L_{in}. It is worth noting that in this case, since $v_{L_{in}} = V_{dc} - v_C$, v_C is acting as an input disturbance for the PI controller $C_{dc}(s)$ [see Fig. 5(c)]. Considering the closed-loop tracking and input disturbance rejection performance of the PI controller $C_{dc}(s)$ shown in Fig. 9, the mentioned resonance is eliminated due to the significant disturbance rejection provided by $C_{dc}(s)$. Therefore, by using the proposed APD control strategy, not only the current stress on the passive and active components can be reduced, but also it improves the overall stability and reliability of the system.

Moreover, a loss analysis has been performed in PLECS to investigate the impact of the proposed APD control method on the power loss profile of the S^5B5L converter. The details of this analysis can be found in [21]. As a result, the reduction in

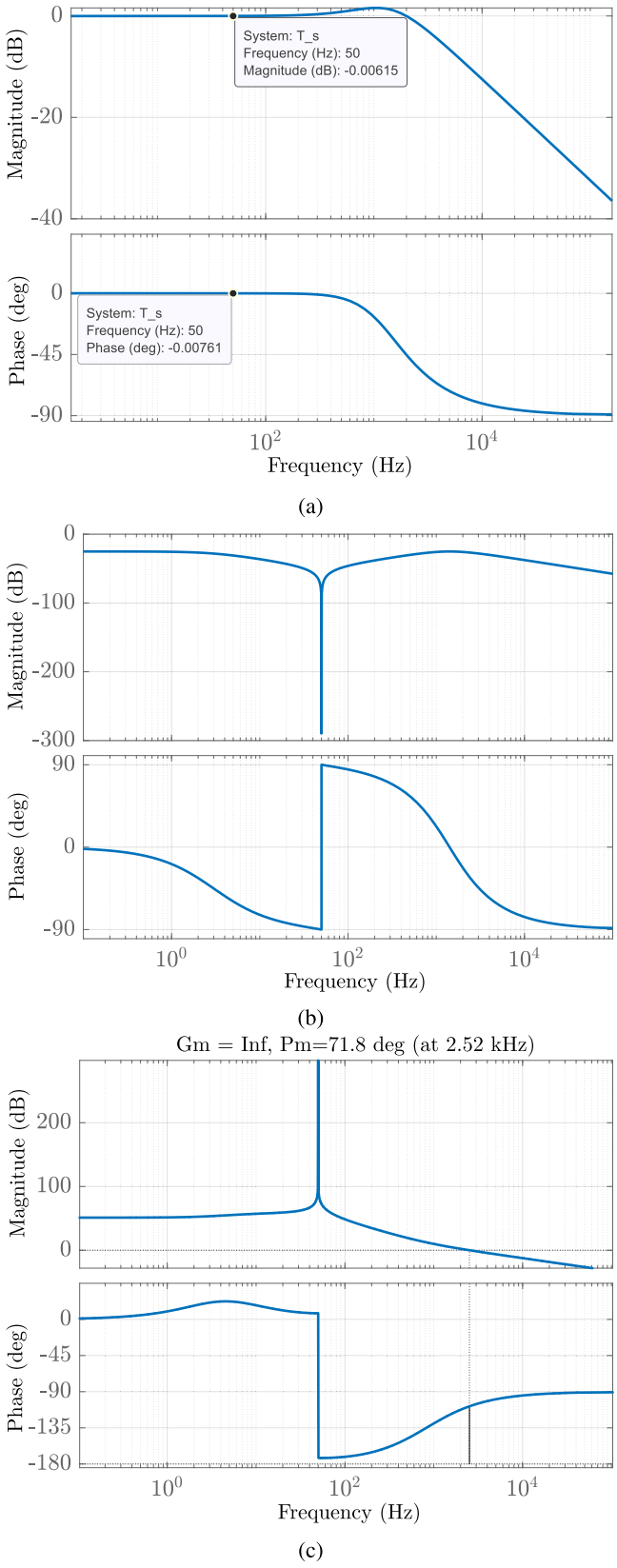

FIGURE 11. Bode plot of (a) closed-loop system: $i_g^\star$ to i_g, (b) i_g closed-loop input sensitivity against input disturbances, and (c) stability margins of the designed i_g control system.

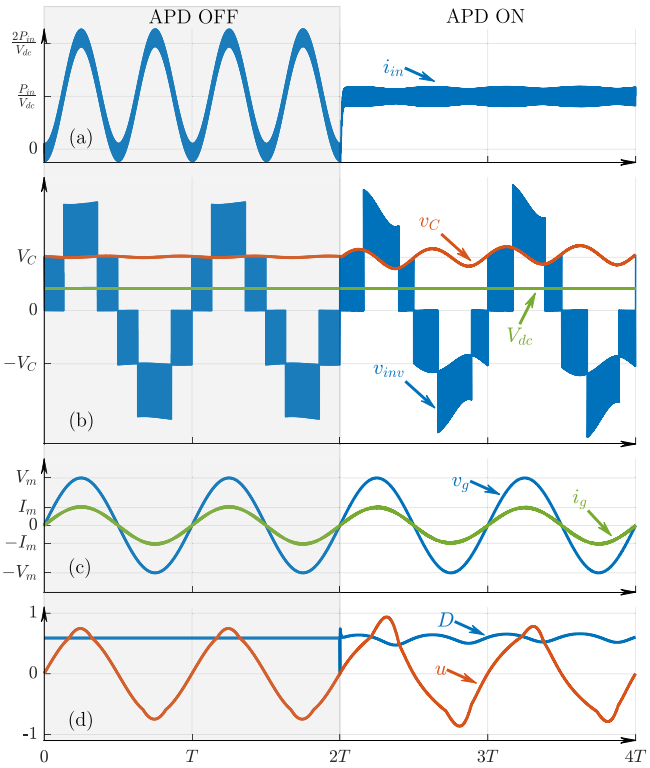

FIGURE 12. Typical key operating waveforms of the S^{5}B5L inverter under ideal grid-connected condition before and after enabling the proposed APD control scheme. (a) Input current (i_{in}). (b) Input dc voltage (V_{dc}), capacitor voltage (v_C), and inverter output voltage (v_{inv}). (c) Pure sinusoidal grid voltage (v_g) and grid current (i_g). (d) Boost duty cycle (D) and ac modulation reference (u).

rms values of the current stress in different circuit components with the activation of the APD control can clearly reduce the conduction losses of devices, as demonstrated in Fig. 16(a) and (b). Therefore, the major reduction of the losses is related to the input inductor, L_{in}, since the input current passing through it does not have any pulsating low-frequency content by applying the APD control. Furthermore, the conduction loss of the switch S_1 is also reduced, which is more significant for the higher range of boost duty cycle or lower input dc source voltage. Regarding this, it can be confirmed that the overall performance of the discussed S^{5}B5L grid-connected converter from the overall efficiency viewpoint is enhanced through applying an APD control, while the life span, reliability, and overall temperature of devices can also be improved.

B. COMPARISON OVER OTHER AVAILABLE TOPOLOGIES WITH APD CONTROL

The circuit features and characteristics of the discussed S^{5}B5L grid-connected converter over some other counterparts with APD control have been summarized in Table 4. The comparative items are the number of power conversion stages, the number of converter output voltage levels, the voltage rating of the capacitors and their capacitance, the reported value of the boost and filter inductors L_{in} and L_g, the rated

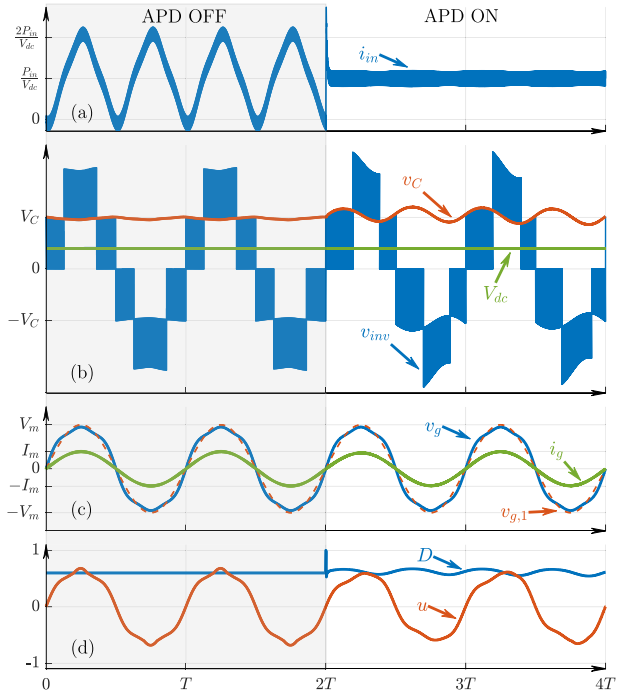

FIGURE 13. Typical key operating waveforms of the S^{5}B5L inverter under polluted grid-connected condition before and after enabling the proposed APD control scheme. (a) Input current (i_{in}). (b) Input dc voltage (V_{dc}), capacitor voltage (v_C), and inverter output voltage (v_{inv}). (c) Polluted grid voltage (v_g) with its fundamental harmonic ($v_{g,1}$) and grid current (i_g). (d) Boost duty cycle (D) and ac modulation reference (u).

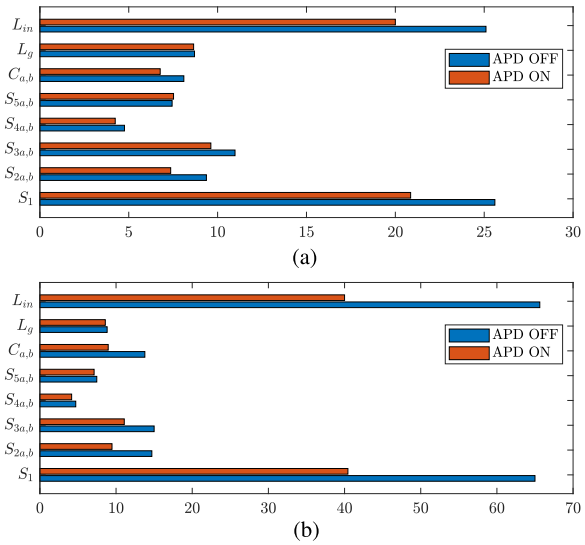

FIGURE 14. RMS currents using PLECS at $P_g = 2$ kW without and with APD control at (a) $V_{dc} = 100$ V and (b) $V_{dc} = 50$ V.

power and the switching frequency, and the reported overall efficiency at the rated power. As can be inspected, the recently proposed S^{5}B5L grid-connected converter is the only available topology that can generate a 5L output voltage with a single-stage integrated APD. The larger number of inverter output voltage levels leads to incorporating a smaller filter inductor L_g, while the voltage rating of the capacitors is only

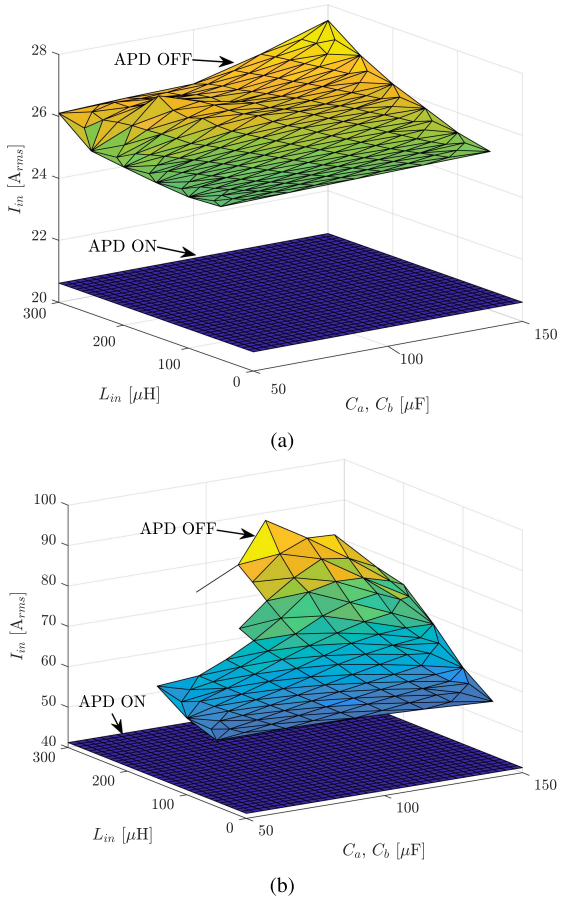

FIGURE 15. RMS input current using PLECS at $P_g = 2$ kW without and with APD control at (a) $V_{dc} = 100$ V and (b) $V_{dc} = 50$ V.

250 V, which is half of the inverter peak output voltage using a comparably small capacitance. Here, although the overall efficiency of the S^{5}B5L converter with APD control is less than some other reported counterparts, the applied switching frequency of the proposed method is almost five times larger than most other works in this comparison. Moreover, none of the reported systems has considered a polluted grid voltage in their integrated control strategy, while this scenario has been extensively addressed in the current work. It is worth mentioning that the reported efficiency for some of the works considered in this comparison does not include the boost stage efficiency.

VI. EXPERIMENTAL RESULTS

To validate the effectiveness of the APD control applied to the described S^{5}B5L converter, extensive experimental results from a 2-kW laboratory-built prototype shown in Fig. 17 under the grid-connected environment are presented in this section. The circuit specifications and closed-loop control parameters are outlined in Tables 3 and 5, while three dc power supplies (EA-PSI-9360-12) have been connected in parallel to provide a sufficient amount of input current and feed the converter. As for the grid-tied operation, a polluted grid voltage

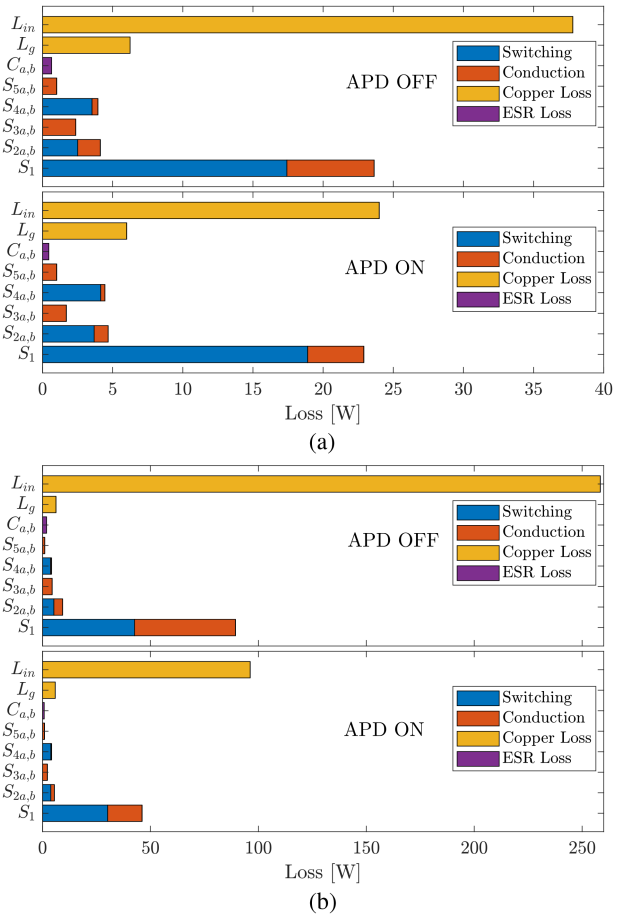

FIGURE 16. Loss breakdown using PLECS at $P_g = 2$ kW without and with APD control at (a) $V_{dc} = 100$ V and (b) $V_{dc} = 50$ V.

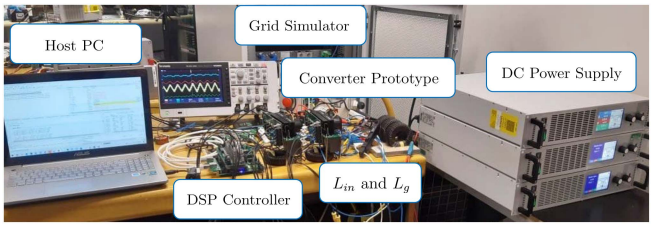

FIGURE 17. View of the experimental setup.

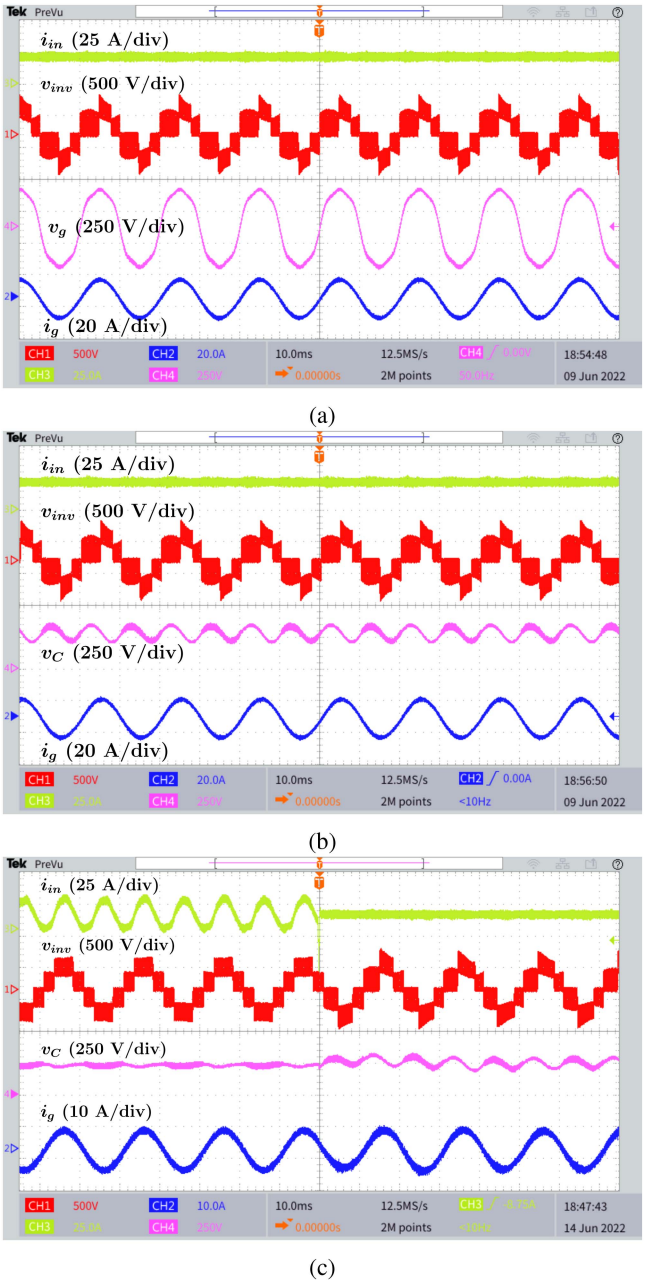

FIGURE 18. Experimental results under the polluted grid-connected condition at $V_{dc} = 100$ V and $C = 75$ μF. (a) Input current, inverter output voltage, grid voltage, and grid current at $P_g = 2$ kW. (b) Input current, inverter output voltage, capacitor voltage, and grid current at $P_g = 2$ kW. (c) Input current, inverter output voltage, capacitor voltage, and grid current at $P_g = 1$ kW before and after enabling the proposed APD control.

per (37) is emulated with a four-quadrant grid simulator (REGATRON TC30.528.43-ACS). A DSP (TMS320F28379D) has also been used to implement the proposed controller.

As for the first experimental test, the input dc voltage is set at 100 V, while based on the peak amplitude of the fundamental component of the grid voltage and with respect to Fig. 7, a voltage reference is selected as for $V_C^\star$ in the APD control loop. Hence, with respect to Fig. 5(c) and (d), the boost duty cycle D and the ac modulation reference u are attained and passed to the PS-PWM stage described in [21] to provide the required gate switching pulses. Fig. 18(a) and (b) shows the details of this experimental test during a steady-state condition. As can be seen, by applying the APD control, the input current is free from any double-line frequency and only contains the high-frequency content caused by the switching action. The average value of the input current is around 20 A with around 13 A as the peak value of the injected grid current. Here, the 5L inverter output voltage in the presence of a polluted grid voltage has been generated, while the voltage across both capacitors is balanced at 250 V with a double-line frequency ripple. The distortion in the 5L

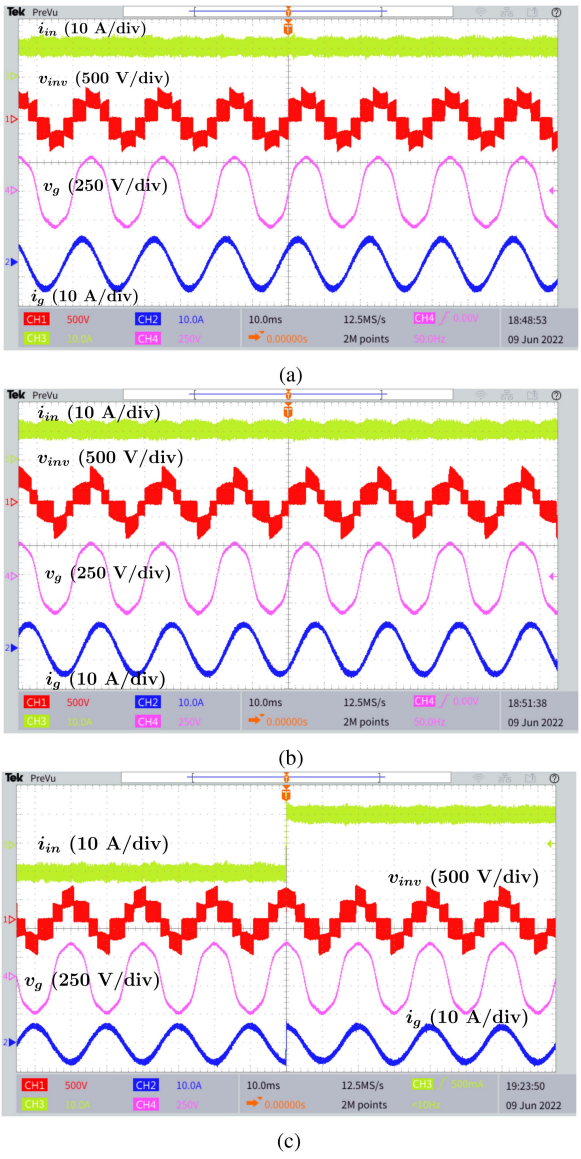

FIGURE 19. Experimental results under polluted grid-connected condition, $C = 75$ μF, and $V_{dc} = 100$ V. (a) Input current, the inverter output voltage, the grid voltage, and the grid current at $P_g = 1$ kW and $Q_g = +1$ kVAr. (b) Input current, the inverter output voltage, the grid voltage, and the grid current at $P_g = 1$ kW and $Q_g = -1$ kVAr. (c) Input current, the inverter output voltage, the grid voltage, and the grid current showing bidirectional power flow operation from $P_g = -1$ kW to $P_g = +1$ kW.

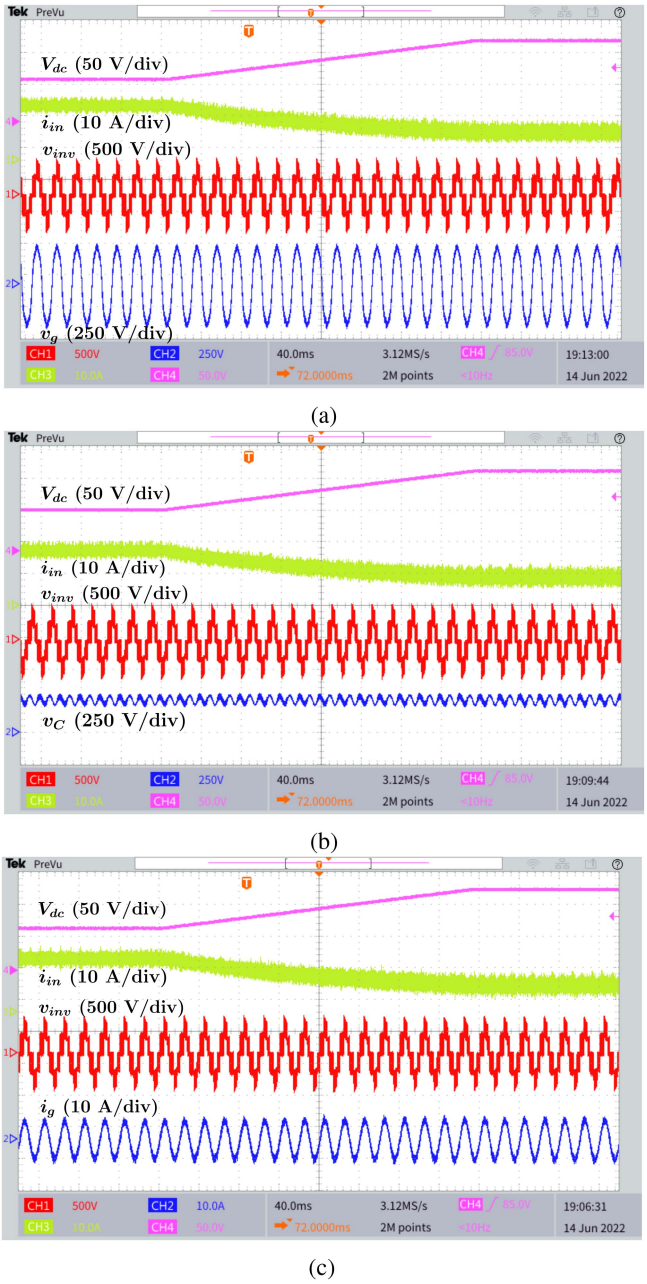

FIGURE 20. Experimental results under polluted grid-connected condition, $P_g = 1$ kW, $C = 75$ μF, and $V_{dc} = 60$ V to $V_{dc} = 120$ V. (a) Input dc voltage, the input current, the inverter output voltage, and the grid voltage. (b) Input dc voltage, the input current, the inverter output voltage, and the capacitor voltage. (c) Input dc voltage, the input current, inverter output voltage, and the grid current.

inverter output voltage is due to the small value of the capacitors as reported in [21], while the THD value of the injected grid current is less than 1% at 200 kHz apparent switching frequency at the ac side. The dynamic results before and after applying the APD at 1 kW injected grid power have also been demonstrated in Fig. 18(c). The APD action can clearly be seen through these results as the low-frequency ripple from the input current has been transferred to the voltages of the capacitors.

The respective reactive power support results under the leading and lagging power factor conditions, i.e., $P_g = 1$ kW and $Q_g = \pm 1$ kVAr, are shown in Fig. 19(a) and (b), respectively. As can be seen, under the APD control strategy, the input current is still free from low-frequency components in both reactive power compensation cases. The bidirectional power flow performance of the converter confirming absorbing power from the grid and injecting power into the grid under the grid-connected and APD control condition has also been shown in Fig. 19(c). Here, an electronic load is connected in parallel to the dc power supply to absorb the power

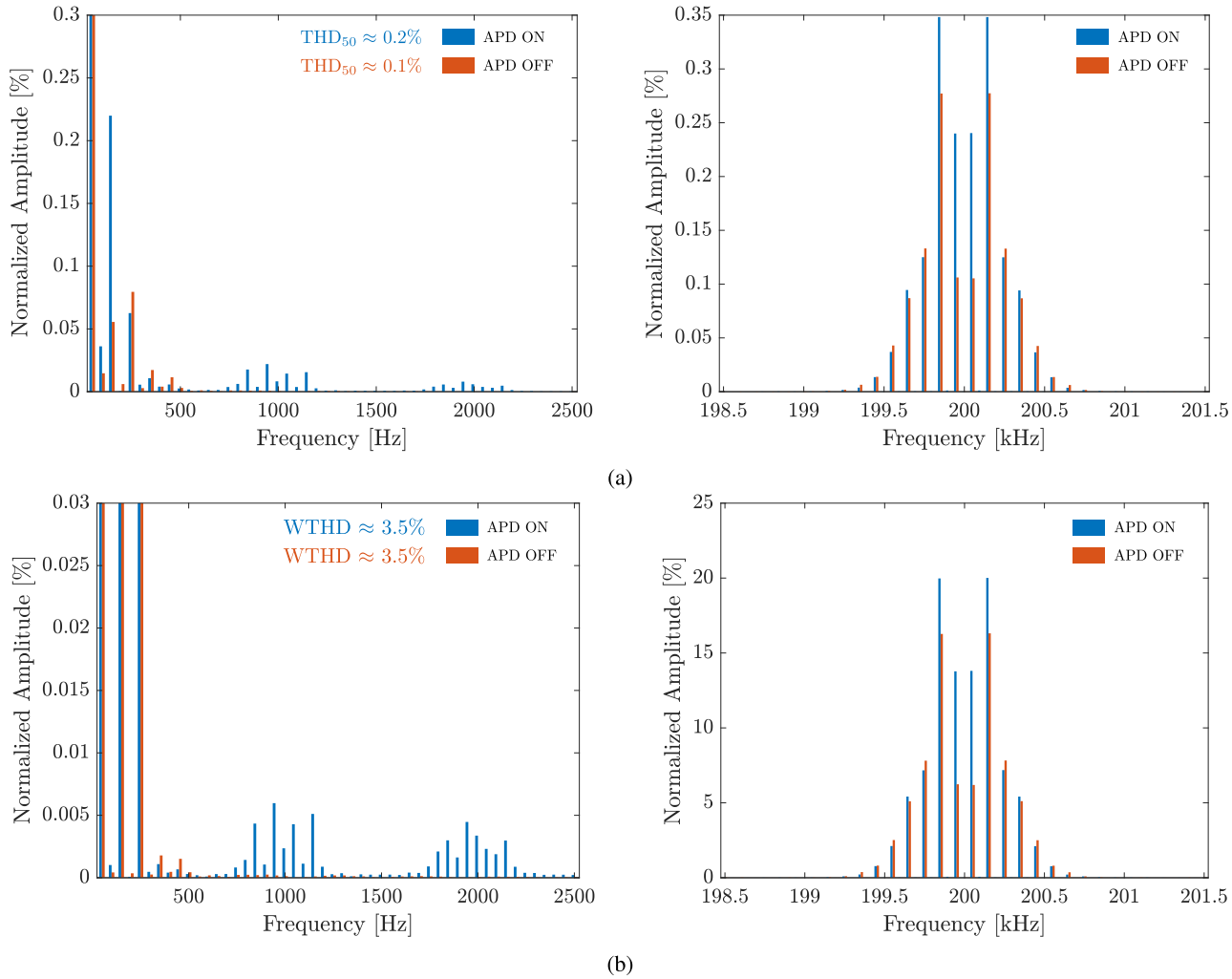

FIGURE 21. FFT analysis results of the inverter output at $C = 75$ μF, $P_g = 2$ kW (unity power factor), and polluted grid voltage. (a) i_g. (b) v_{inv}.

from the grid flowing in the reverse direction. As can be realized, all the output voltage levels have been generated, while the input current direction is changed from a negative value (absorbing power from the grid) to a positive value (injecting power into the grid).

To confirm the dynamic voltage conversion gain of the converter while meeting the peak grid voltage requirement, another dynamic test with a ramp change in the input dc voltage, i.e., from 60 to 120 V, and with the proposed APD control strategy is applied to the described S^5B5L converter. Details of this dynamic test while showing the input dc voltage, the input current, the 5L inverter output voltage, the polluted grid voltage, the voltage across the capacitors, and the injected grid current waveform at 1 kW are illustrated in Fig. 20(a)–(c). Here, even though the input dc voltage is getting changed with a ramp trend, the peak 5L output voltage of the inverter is kept fixed at around 500 V, i.e., two times the voltage across each of the capacitors, which is enough to inject the power to a grid with a maximum peak voltage of 320 V as for its fundamental harmonic.

One of the important aspects of any grid-connected power converter is its power quality. As can be seen throughout the experimental results, the proposed APD control strategy affects the inverter output voltage. This change can be observed in the frequency spectrum view of v_{inv} and i_g, as shown in Fig. 21. As can be seen in Fig. 21(a), the proposed APD control causes a slight increase in low-frequency harmonics of i_g. More precisely, THD values of i_g using conventional and proposed control methods are 0.1% and 0.2%, respectively. These values are well within the limits of the available standards (e.g., IEEE 519-2014). Moreover, Fig. 21(b) depicts the low- and high-frequency harmonics of v_{inv}. As can be seen, the difference in low-frequency harmonics is negligible, and the weighted THD values of v_{inv} for both conventional and the proposed APD control methods are practically identical. Therefore, a similar grid-interface filter can be used for both cases to achieve the same level of THD. It is worth mentioning that there is a large difference between the high-frequency harmonics of v_{inv} with conventional and the proposed controllers. However, these harmonic

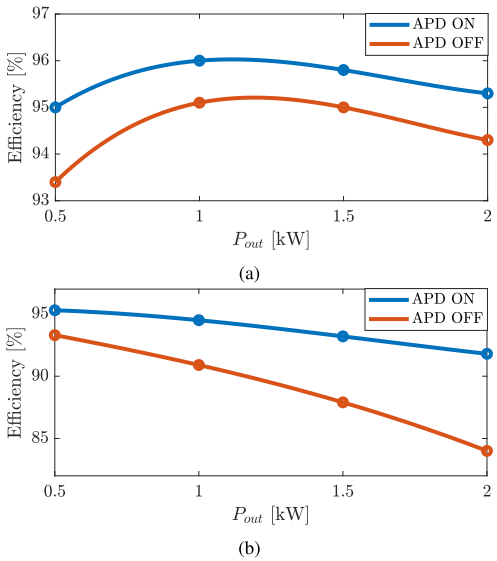

FIGURE 22. Efficiency comparison with and without APD control at $C = 75$ μF, unity power factor, and polluted grid voltage. (a) $V_{dc} = 100$ V. (b) $V_{dc} = 50$ V.

clusters are located at two-times switching frequency (i.e., at 200 kHz for the switching frequency of 100 kHz), where the grid-interface filter impedance is very high. Hence, the impact of high-frequency harmonics on the THD of i_g is not significant.

Finally, using a Yokogawa WT1806E precision power analyzer and the PLECS model of the converter, the overall dc-to-ac conversion efficiency of the S^{5}B5L converter at $V_{\rm dc} = 100$ V, and $V_{dc} = 50$ V under a wide range of the injected grid power with and without the APD control is measured and the results are shown in Fig. 22(a), and (b), respectively. As can be seen, the results confirm the expectation obtained from the simulation shown in Figs. 14 and 16, in which through applying the APD control, the overall efficiency of the system is improved by approximately 1% at $V_{\rm dc} = 100$ V and more than 5% at $V_{\rm dc} = 50$ V, while the conduction losses of the switches and copper losses of the input boost inductor are reduced.

VII. CONCLUSION

This article presented a grid-connected system with an integrated APD capability based on the recently proposed S^{5}B5L converter. Leveraging the integrated capacitors in the S^{5}B5L converter, the APD functionality was achieved without adding any extra circuit components to the entire system. The topology was connected to a grid polluted with several low-frequency harmonics. A GVO-based synchronization mechanism was also designed and included to inject a pure sinusoidal grid current, decomposing the harmonic components of the grid voltage and providing a clean feedforward signal, including all the expected low-frequency harmonics. This allowed for developing a tailored control strategy based on the S^{5}B5L structure using a single PR controller for the grid current injection with a filtered feedforward term. A comparative study was also conducted to evaluate the effectiveness of the proposed control strategy applied to the S^{5}B5L converter from the current stress on devices and the power losses of the active/passive elements viewpoints. Moreover, a sensitivity analysis for the values of the passive components at different operating points was performed. Extensive closed-loop experimental results obtained from a 2-kW laboratory-based prototype under the grid-connected condition were presented to validate the theoretical analysis of this proposal. As evidenced by these experimental results, the proposed solution effectively eliminated the low-frequency harmonic content from the input power drawn from the dc source without enlarging the passive elements. Consequently, the conduction losses were reduced, and thus, the overall efficiency of the entire conversion system was improved.

REFERENCES

[1] G. Zhang, Z. Li, B. Zhang, and W. Halang, "Power electronics converters: Past, present and future," *Renewable Sustain. Energy Rev.*, vol. 81, no. 1, pp. 2028–2044, 2018.
[2] J. W. Zapata, S. Kouro, G. Carrasco, H. Renaudineau, and T. A. Meynard, "Analysis of partial power dc–dc converters for two-stage photovoltaic systems," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 591–603, Mar. 2019.
[3] I. Serban, "Power decoupling method for single-phase H-bridge inverters with no additional power electronics," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4805–4813, Aug. 2015.
[4] G. Fontes, C. Turpin, S. Astier, and T. A. Meynard, "Interactions between fuel cells and power converters: Influence of current harmonics on a fuel cell stack," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 670–678, Mar. 2007.
[5] H. Wang and F. Blaabjerg, "Reliability of capacitors for dc-link applications—An overview," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 1866–1873.
[6] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of ac and dc active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 15–25, Mar. 2016.
[7] C.-H. Chang and K.-H. Ho, "A transformer-less high-gain inverter with step-up/down and single energy-processing features," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4726–4738, Aug. 2021.
[8] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4690–4698, Nov. 2012.
[9] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4778–4794, Jul. 2016.
[10] Q.-C. Zhong, W.-L. Ming, W. Sheng, and Y. Zhao, "Beijing converters: Bridge converters with a capacitor added to reduce leakage currents, dc-bus voltage ripples, and total capacitance required," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 325–335, Jan. 2017.
[11] Z. Liao and R. C. Pilawa-Podgurski, "A high power density multilevel bipolar active single-phase buffer with full capacitor energy utilization and controlled power harmonics," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 13067–13079, Nov. 2021.
[12] Z. Liao, N. C. Brooks, and R. C. Pilawa-Podgurski, "Design constraints for series-stacked energy decoupling buffers in single-phase converters," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7305–7308, Sep. 2018.
[13] S. G. Jorge, J. A. Solsona, and C. A. Busada, "Nonlinear control of a two-stage single-phase dc–ac converter," *IEEE Trans. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 4, pp. 1038–1045, Oct. 2022.
[14] Y. Shen, M. D. Antonio, S. Chakraborty, A. Hasnain, and A. Khaligh, "Comparison of CCM- and CRM-based boost parallel active power decoupler for PV microinverter," *IEEE Trans. Power Electron.*, vol. 37, no. 8, pp. 9889–9906, Aug. 2022.

[15] J. Jiang, S. Pan, J. Gong, F. Liu, X. Zha, and Y. Zhuang, "A leakage current eliminated and power oscillation suppressed single-phase single-stage nonisolated photovoltaic grid-tied inverter and its improved control strategy," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6738–6749, Jun. 2021.
[16] Y. Xia, J. Roy, and R. Ayyanar, "A capacitance-minimized, doubly grounded transformer less photovoltaic inverter with inherent active-power decoupling," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5188–5201, Jul. 2017.
[17] H. F. Ahmed, M. S. El Moursi, B. Zahawi, and K. Al Hosani, "Single-phase photovoltaic inverters with common-ground and wide buck–boost voltage operation," *IEEE Trans. Ind. Informat.*, vol. 17, no. 12, pp. 8275–8287, Dec. 2021.
[18] P. Nandi and R. Adda, "An active power decoupling-integrated reduced-switch current-fed switched inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 11, no. 2, pp. 1929–1942, Apr. 2023.
[19] X. Xu, M. Su, Y. Sun, B. Guo, H. Wang, and G. Xu, "Four-switch single-phase common-ground PV inverter with active power decoupling," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 3223–3228, Mar. 2022.
[20] H. Tian, M. Chen, G. Liang, and X. Xiao, "A single-phase transformerless common-ground type PV inverter with active power decoupling," *IEEE Trans. Ind. Electron.*, vol. 70, no. 4, pp. 3762–3772, Apr. 2023.
[21] M. Farhangi et al., "A single-source single-stage switched-boost multilevel inverter: Operation, topological extensions, and experimental validation," *IEEE Trans. Power Electron.*, vol. 37, no. 9, pp. 11258–11271, Sep. 2022.
[22] R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, S. S. Lee, F. Blaabjerg, and Y. P. Siwakoti, "Common-ground grid-connected five-level transformerless inverter with integrated dynamic voltage boosting feature," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 10, no. 6, pp. 6661–6672, Dec. 2022.
[23] S. S. Lee, Y. Yang, Y. P. Siwakoti, and K.-B. Lee, "A novel boost cascaded multilevel inverter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 9, pp. 8072–8080, Sep. 2021.
[24] R. P. Aguilera, P. Acuna, G. Konstantinou, S. Vazquez, and J. I. Leon, "Basic control principles in power electronics: Analog and digital control design," in *Control of Power Electronic Converters and Systems*. New York, NY, USA: Academic, 2018, ch. 2, pp. 31–68.
[25] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 836–841, May 2006.
[26] M. Castilla, J. Miret, J. Matas, L. G. de Vicuna, and J. M. Guerrero, "Control design guidelines for single-phase grid-connected photovoltaic inverters with damped resonant harmonic compensators," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4492–4501, Nov. 2009.
[27] G. Goodwin, S. Graebe, and M. Salgado, *Control System Design*. Upper Saddle River, NJ, USA: Prentice-Hall, 2001.
[28] S. Vazquez, E. Zafra, R. P. Aguilera, T. Geyer, J. I. Leon, and L. G. Franquelo, "Prediction model with harmonic load current components for FCS-MPC of an uninterruptible power supply," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 322–331, Jan. 2022.

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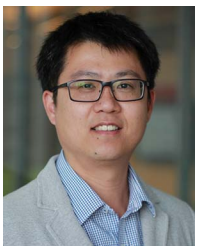

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