Single-Stage Grid-Connected Multilevel Converters: Topologies and Control Strategies

by **Majid Farhangi**

Thesis submitted in fulfilment of the requirements for the degree of
Doctor of Philosophy
under the supervision of
Prof. Dylan Lu
A/ Prof. Yam P. Siwakoti

School of Electrical and Data Engineering
Faculty of Engineering and IT
University of Technology Sydney
06/12/2023

Certificate of Authorship / Originality

I, Majid Farhangi, declare that this thesis is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the School of Electrical and Data Engineering at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis. This document has not been submitted for qualifications at any other academic institution.

This research is supported by the Australian Government Research Training Program.

Signature: Production Note: Signature removed prior to publication.

Date: December 7, 2023

Abstract

The global need for sustainable energy supplies is one of the major drivers in the power electronics industry. In this work, the main challenges and objectives for multilevel power converters in grid-connected applications have been elaborated. To address the identified requirements and challenges, a family of efficient multilevel converters with the single-stage dynamic voltage-boosting feature, reduced number of circuit components, modular structure, and bidirectional operation is presented. The aforementioned advantages make this converter a suitable candidate for renewable energy applications. Moreover, to further improve the performance of the proposed converter, an active power decoupling (APD) strategy for single-phase grid-connected inverters is presented to cancel out the double-line frequency ripple in the input current profile. This enables the converter to be employed in a broad range of grid-connected applications with improved efficiency without adding extra components to the circuit. The experimental results show more than 1% improvement in conversion efficiency over the whole power range, only by applying the proposed control strategy. Additionally, a flexible APD control strategy is applied to continuously adjust the tradeoff between the DC input current ripple and voltage stress on the circuit components, while retaining the power quality requirements of a standard grid-connected inverter. The voltage stress on the circuit components can be reduced by up to 17% with the proposed method compared to the conventional APD approaches. Furthermore, to address the scalability requirement of the single-stage DC-AC converters, a new transformerless grid-connected inverter with a common-grounded circuit architecture and single-stage dynamic voltage boosting gain is proposed. The key features of the presented inverter are the reduced current stress profile, modularity, uniform peak voltage stress on the switches, higher power handling capability, and bidirectional power flow operation. Through a modular design with a phase-shifted modulation, the injected grid current can be shared among the modules, while the size of the grid-interface filters can be reduced. The working principle and the generalized form of the converter are discussed, and some simulation and experimental

results are presented to validate its feasibility, achieving more than 95% efficiency in grid-connected mode at 120 V DC input voltage over a broad power range. Finally the conclusions and recommended future works are provided.

Dedication

To my wife, my family, and my friends

Acknowledgements

I would like to thank my wife, my family, my friends, and my colleagues who encouraged and helped me in this journey.

Also, I would like to express my gratitude to my supervisors Prof. Dylan Lu and Prof. Yam Siwakoti for their continuous support and guidance. In addition, I'm deeply thankful to Prof. Ricardo Aguilera for his valuable insights and support during my PhD studies.

Finally, I'm grateful to my dear friend, Dr. Reza Barzegarkhoo, who continuously helped me in this path, working and learning together.

Majid Farhangi
December 7, 2023
Sydney, Australia

List of Publications

Journal Papers:

- M. Farhangi, R. Barzegarkhoo, S. S. Lee, R. P. Aguilera, D. D. -C. Lu, and Y. P. Siwakoti, "An Interleaved Single-Stage Switched-Boost Common-Ground Multilevel Inverter: Design, Control, and Experimental Validation," in IEEE Trans. Ind. Appl., 2023. *(Under Review)*

- M. Farhangi, R. Barzegarkhoo, R. P. Aguilera, D. D. -C. Lu, M. Liserre and Y. P. Siwakoti, "A Single-Stage Switched-Boost Grid-Connected Five-Level Converter With Integrated Active Power Decoupling Under Polluted Grid Voltage Condition," in IEEE open j. Ind. Electron. Soc., vol. 4, pp. 328-345, 2023, doi: 10.1109/OJIES.2023.3305492.

- M. Farhangi, R. Barzegarkhoo, R. P. Aguilera, S. S. Lee, D. D. -C. Lu and Y. P. Siwakoti, "A Single-Source Single-Stage Switched-Boost Multilevel Inverter: Operation, Topological Extensions, and Experimental Validation," in IEEE Trans. Power Electron., vol. 37, no. 9, pp. 11258-11271, Sept. 2022, doi: 10.1109/TPEL.2022.3163762.

Conference Papers:

- M. Farhangi, R. Barzegarkhoo, R. P. Aguilera, Y. P. Siwakoti, D. D. -C. Lu, "A Flexible Active Power Decoupling Strategy for A Switched-Boost Single-Stage Grid-Connected Multilevel Inverter," 2023 IEEE Intl. Future Energy Electron. Conf. (IFEEC), Sydney, Australia, 2023.

- M. Farhangi, R. Barzegarkhoo, S. S. Lee, D. Lu and Y. Siwakoti, "An Interleaved Switched-Boost Common-Ground Five-Level Inverter," 2022 Intl. Power Electron. Conf. (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan, 2022, pp. 867-872, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807154.

- M. Farhangi, R. Barzegarkhoo, Y. P. Siwakoti, D. Lu and S. S. Lee, "A Novel Single-Source Single-Stage Switched-Boost Five-Level (S5B5L) Inverter With Dynamic Voltage Boosting Feature," 2021 IEEE Energy Convers. Congr. Expo. (ECCE), 2021, pp. 2557-2562, doi: 10.1109/ECCE47101.2021.9595174.

Related/Collaborative Publications:
Journal Papers:

- R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, M. Liserre and Y. P. Siwakoti, "New Family of Dual-Mode Active Neutral Point-Clamped Five-Level Converters," in IEEE Trans. Power Electron., doi: 10.1109/TPEL.2023.3283694.

- Y. Y. Syasegov, M. Farhangi, R. Barzegarkhoo, Y. P. Siwakoti, L. Li, D. D. -C. Lu, R. P. Aguilera and J. Pou, "A 5-Level HERIC Active-Clamped Inverter With Full Reactive Power Capability for Grid-Connected Applications," in IEEE open j. Ind. Electron. Soc., vol. 4, pp. 135-148, 2023, doi: 10.1109/OJIES.2023.3271637.

- Y. Y. Syasegov, M. Farhangi, R. Barzegarkhoo, L. Li, D. D. -C. Lu, R. P. Aguilera and Y. P. Siwakoti, "HERIC-Clamped and PN-NPC Inverters With Five-Level Output Voltage and Reduced Grid-Interfaced Filter Size," in IEEE open j. power electron., vol. 4, pp. 306-318, 2023, doi: 10.1109/OJPEL.2023.3265062.

- R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, F. Blaabjerg and Y. P. Siwakoti, "A Novel Active Neutral Point-Clamped Five-Level Inverter With Single-Stage-Integrated Dynamic Voltage Boosting Feature," in IEEE Trans. Power Electron., vol. 38, no. 6, pp. 7796-7809, June 2023, doi: 10.1109/TPEL.2023.3257959.

- S. S. Lee, S. Cao, R. Barzegarkhoo, M. Farhangi and Y. P. Siwakoti, "Single-Phase 5-Level Split-Midpoint Cross-Clamped (5L-SMCC) Inverter: An Alternative to the Two-Stage ANPC Topology," in Trans. Emerg. Sel. Topics Power Electron., vol. 11, no. 2, pp. 1995-2003, April 2023, doi: 10.1109/JESTPE.2023.3236012.

- R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, S. S. Lee, F. Blaabjerg and Y. P. Siwakoti, "Common-Ground Grid-Connected Five-Level Transformerless Inverter With Integrated Dynamic Voltage Boosting Feature," in IEEE Trans. Emerg. Sel. Topics Power Electron., vol. 10, no. 6, pp. 6661-6672, Dec. 2022.

- R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, Y. P. Siwakoti and J. Pou, "Nine-Level Nine-Switch Common-Ground Switched- Capacitor Inverter Suitable for High-Frequency AC-Microgrid Applications," in IEEE Trans. Power Electron., vol. 37, no. 5, pp. 6132-6143, May 2022, doi: 10.1109/TPEL.2021.3131847.

Conference Papers:

- R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, Y. P. Siwakoti and M. Liserre, "Active Neutral Point-Clamped Five-Level Inverter With Single-Stage Dynamic Voltage Boosting Capability," 2022 IEEE 13th Intl. Symp. on Power Electron. for Distributed Generation Systems (PEDG), Kiel, Germany, 2022, pp. 1-6, doi: 10.1109/PEDG54999.2022.9923158.

- R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera and Y. P. Siwakoti, "A Novel Seven-Level Switched-Boost Common-Ground Inverter With Single-Stage Dynamic Voltage Boosting Gain," 2022 Intl. Power Electron. Conf. (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan, 2022, pp. 873-877, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807006.

- M. Farhangi, Y. P. Siwakoti, R. Barzegarkhoo, S. U. Hasan, D. Lu and D. Rogers, "A Compact Design Using GaN Semiconductor Devices for a Flying Capacitor Five-Level Inverter," 2021 IEEE Energy Convers. Congr. Expo. (ECCE), 2021, pp. 2475-2479, doi: 10.1109/ECCE47101.2021.9595266.

- R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, Y. P. Siwakoti and S. S. Lee, "Switched-Boost Common-Ground Five-Level (SBCG5L) Grid-Connected Inverter With Single-Stage Dynamic Voltage Boosting Concept," 2021 IEEE Energy Convers. Congr. Expo. (ECCE), 2021, pp. 1014-1019, doi: 10.1109/ECCE47101.2021.9595581.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

The growth rate of renewable energy sources in the global energy market shows a clear trend and interest toward green power generation with a minimized carbon footprint. Australia has set ambitious targets to increase its share of renewable power and reduce its carbon footprint, similar to the efforts in Europe. The Australian government has established a goal to achieve 82% renewable electricity by 2030 [1,2]. Currently, Australia generates about 32% of its power from renewable sources, including wind, solar, and hydro [3]. In addition to this, Australia has committed to reducing its greenhouse gas emissions by 43% from 2005 levels by 2030 and aims to reach net zero emissions by 2050 [4].

To support the high renewable penetration in the existing electrical grids, the role of power electronic converters is inevitable. Power electronics is one of the critical enablers of integrating renewable sources in the electrical grid. Most renewable energy sources are not inherently compatible with the grid operating conditions and need a power converter as an interface. Normally, the power flow direction for renewable sources is from the source to load side (unidirectional power flow). Moreover, to address the intermittency issue of renewables, energy storage devices are crucial in modern grids. Integrating the battery energy storage systems into the grids, requires power converters with specific features such as bidirectional power flow capability, and continuous and ripple-free DC input current profile. In this case, a converter with built-in bidirectional power flow allows for efficient charging and discharging the energy-storing element (e.g., batteries, supercapacitors, etc.) according to the requested power reference commands. On the other hand, some energy-storage technologies such as fuel-cells are prone to accelerated degradation under fluctuating and changing currents [5]. Furthermore, low-frequency ripple currents in DC buses that are common in single-phase systems and unbalanced three-phase systems cause higher root-mean-square

(RMS) current values passing through the components, leading to increased operating temperatures and consequent potentially reduced lifetime of the batteries or DC-link capacitors.

Furthermore, the accelerating trend of modern electric vehicles (EVs) with improved range, superior performance, and energy efficiency opens an opportunity for developing better power converters complying with the strict and challenging automotive industry requirements in terms of reliability, electromagnetic compatibility (EMC), efficiency, compactness, and of course total cost of ownership. Moreover, in smart grids, EVs are considered as moving distributed energy-storage units. Therefore, they can be operated as grid-connected inverters and participate in the grid voltage and frequency regulation services through active and reactive power injection into the grid. More specifically, energy exchange from EV to grid (V2G) and from grid to EV (G2V) are important approaches to improve the power quality, power efficiency, and reduce the users' energy bills [6–8].

In most applications, a two-stage power conversion structure is necessary due to the requirements of the DC source and the load(s), as shown in Fig. 1.1(a). For instance, in a grid-connected PV inverter, a front-end boost DC-DC stage is followed by a DC-AC inverter, allows for Maximum Power Point Tracking (MPPT) under a wide range of irradiation and shading conditions while the grid voltage amplitude is met. Similarly, two-stage DC-AC power converters are broadly incorporated in many grid-connected applications such as battery energy storage systems. It should be noted that in some particular applications such as wind-based energy generation, the input source has an AC voltage waveform and, therefore, it requires a different power conversion architecture (e.g., a front-end AC-DC converter or a direct AC-AC converter).

One of the requirements for EV, fuel-cell, battery, and PV applications is a ripple-free and steady DC power. Therefore, due to the difference in the instantaneous power at the DC and AC ports, a power decoupling strategy is necessary. Conventionally, active or passive buffer circuits are used to address this issue in DC-AC converters. Thus, the buffer circuit needs to compensate and inject a suitable voltage or current to cancel this undesirable input ripple. However, including an additional buffer circuit to a DC-AC converter can increase the size, cost, complexity, and potentially the overall failure rate of the system. As a common practice, a two-stage structure is used in many grid-connected inverter units as shown in Fig. 1.1(a). The first DC-DC stage is responsible for achieving DC input voltage control as well as boosting the voltage to an appropriate level for the DC-AC stage. Moreover, the DC-DC stage in conjunction with the DC-link capacitor can serve as an Active Power Decoupling (APD) circuit to redirect the ripples from the DC port

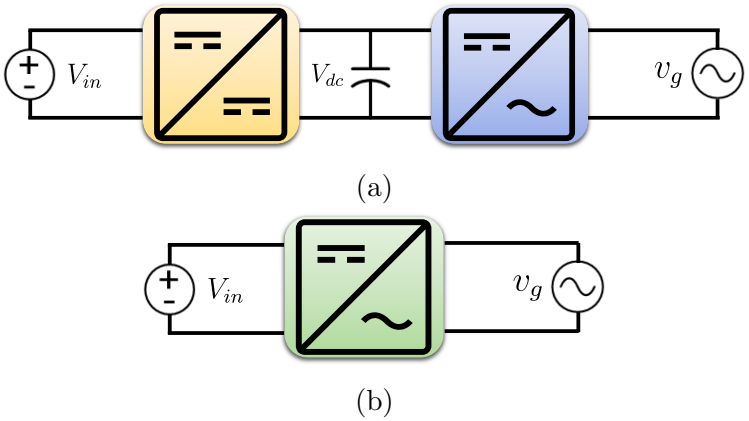


Fig. 1.1. DC-AC converter architectures: (a) conventional two-stage inverter with a dedicated boost stage, (b) single-stage inverter with integrated voltage boosting capability.

to the DC-link capacitor. However, the same level of functionality can be reached with some of the proposed single-stage DC-AC converters as shown in Fig. 1.1(b).

Power electronic converters with single power processing DC-AC stage have been recognized as efficient, compact, and attractive solutions during the latest years for the newly-developed renewable-energy (RE)-based systems [9]. This concept, as shown in Fig. 1.1(b), is motivated by targeting some shortcomings associated with the two-stage DC-AC converters such as lower overall efficiency, larger number of required components, lower feasible range of output voltage gain, higher manufacturing cost, and lower overall power density [10, 11]. The main research objectives and an overview of the report are presented in the next section.

1.1 Research Objectives

The main aim of this research is to propose improved DC-AC multilevel converter structures, modulation, and control strategies tailored for grid-connected applications with RE- and battery-based sources. More specifically, this work is moving toward the single-stage boost-based DC-AC converters with developed advanced capabilities such as dynamic voltage boosting gain, APD, bidirectional power flow, and full reactive power support.

The specific research objectives of this thesis are:

1. To propose and improve flexible single-stage multilevel converter structures complying with the application-specific requirements for both

single- and three-phase use cases

2. To develop integrated modulation and control strategies to enable the potential advanced features of the converters

3. To design control strategies with active power decoupling feature for single-stage multilevel converters as a critical requirement for PV, fuel cell, and battery operated systems

4. To investigate the possibility of power/current sharing within a multilevel converter with a modular architecture as an enabler for active thermal control techniques

5. To implement power converters with corresponding controllers to achieve bidirectional power flow feature for the battery-based systems such as EVs or battery energy storage systems

1.2 Thesis Overview

The rest of the thesis is structured as follows:

Chapter 2 provides a literature review on major aspects of power electronics converters with a focus on grid-connected applications. This includes an overview of the circuit topologies used in power converters, and various modulation and control approaches to be applied on power converters. Moreover, the identified gaps in the literature have been explained.

Chapter 3 aims to present a family of multilevel converters with the single-stage dynamic voltage-boosting feature, reduced number of circuit components, modular structure, bidirectional operation, continuous input current, and acceptable overall efficiency. The proposed structure is based on a three-level single-stage boost integrated inverter with an embedded quasi H-bridge (QHB) cell. These features allows using the proposed converters as an interface between the available varying low-voltage DC sources (e.g., battery or PV) and a standard AC grid. In addition, the proposed converters have the potential for integrating active power decoupling, that is investigated in the following chapters. The proposed topology directly addresses research objectives 1 and 5, and the proposed modulation to enhance the maximum voltage gain links to research objective 2.

Chapter 4 aims to implement an integrated active power decoupling technique using the proposed S^5B5L-VSI to eliminate the double-line frequency ripple at the DC port without any additional components. APD is particularly critical for single-phase EV chargers, battery- and RE-based applications, as it improves the power quality at the DC side and enhances the

overall power efficiency. This chapter addresses research objectives 2, 3, and 5 using the proposed APD control for bidirectional power flow control under distorted grid voltage conditions.

Chapter 5 extends the flexibility of conventional active power decoupling strategies and allows for a dynamically adjustable tradeoff between the double-line frequency ripple in the DC input current and capacitor voltage ripple. This can be used to reduce the voltage stress on the active and passive components or reducing the minimum capacitance requirement. This chapter links to research objectives 2, 3, and 5 by introducing a flexible active power decoupling control strategy with bidirectional power flow support.

Chapter 6 aims to implement a new concept of interleaved common-grounded switched-boost multilevel inverter (CGSB-MLI). It offers several important features including bidirectional power flow support, modularity, higher power handling capability through the interleaved circuit configuration, compatibility with PS-PWM technique, and uniform maximum voltage stress across the switches while retaining its single-stage dynamic voltage boosting. The common-grounded structure makes this converter an attractive candidate particularly for the applications where the negligible leakage current generation is a priority (e.g., PV sources). The presented topology in this chapter aligns with research objectives 1, 4, and 5, and its control strategy follows research objectives 2 and 4.

Finally, Chapter 7 summarizes the results and implications of this work, and provides recommended directions for the future works.

Chapter 2

Literature Review

DC-AC power converters are one of the essential building blocks in modern electricity grids and AC microgrids. In this chapter, an overview of the available circuit topologies and control approaches for DC-AC power converters has been presented. Firstly, suitable circuit topologies in the literature have been categorized and reviewed based on their features and characteristics. Next, conventional and advanced control strategies in this context have been summarized based on their structure. Finally, some of the identified research gaps and major design challenges in terms of topology and control methods have been explained.

2.1 DC-AC Converters

DC-AC converters can be categorized into three main groups based on their output characteristics:

- **Voltage-Source Converters:** The vast majority of the available DC-AC converters fall into this group due to easier implementation and component availability, especially for low- and medium-power converters. In this type, the output voltage of the converter is synthesized by connecting the circuit capacitors in different combinations to generate a switched voltage waveform (which can be filtered to obtain a smooth current waveform). Hence, the output of these converters behaves as a voltage source. Therefore, these converters are vulnerable to short-circuit faults, and over-current protection is essential to ensure a safe operation. Moreover, usually, all the power switches should be opened in case of a fault occurrence [12].

- **Current-Source Converters:** As opposed to voltage-source convert-

ers, in this group, the output current is synthesized by routing the current of an inductor to the output to generate a switched current waveform (which can be filtered to obtain a smooth voltage waveform). Hence, the output of these converters acts as a current source [13]. Consequently, they are vulnerable to open-circuit faults, and over-voltage protection is a key requirement [14]. The most important feature of this group of converters is their inherent immunity against short-circuit faults. However, their power density and efficiency are limited due to the required additional circuit components and magnetic elements compared to voltage-source converters [15].

- **Impedance-Source Converters:** Unlike voltage-source and current-source converters, impedance-source converters can handle both open-circuit and short-circuit fault conditions at their outputs for a short time. They also can offer voltage-boosting capabilities based on their unique structure [16–18]. In this type of converter, an impedance-source circuit based on arrangement of passive elements (i.e., inductors and capacitors) is followed by a switching circuit to generate a switched voltage waveform to be filtered at consequent stages [19].

Fig. 2.1 summarizes the main features of the above-mentioned DC-AC converter types.

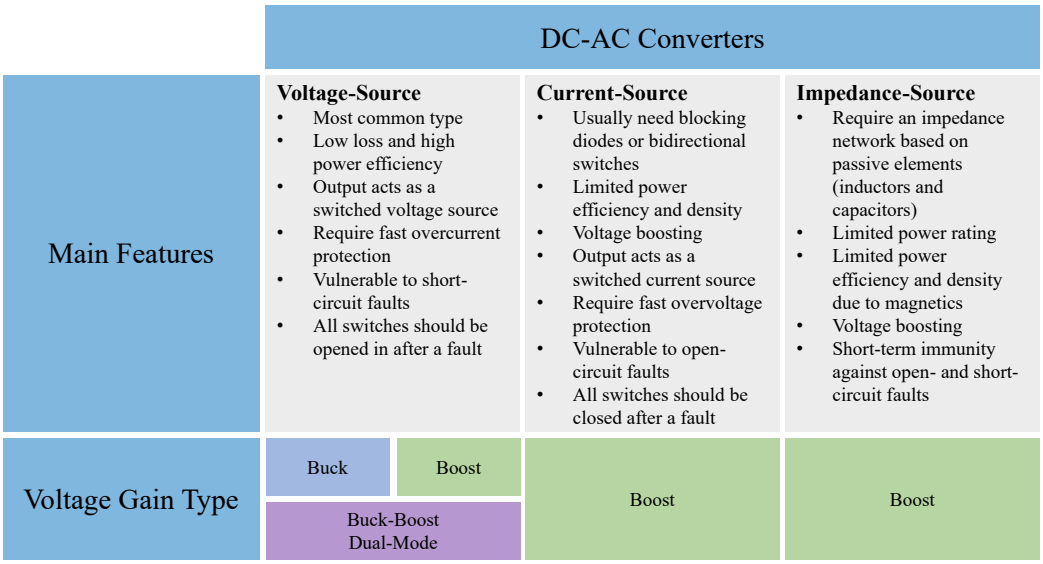


Fig. 2.1. DC-AC converter types.

To establish a reasonable boundary and scope for the work at hand, the rest of this work focuses on non-isolated voltage-source DC-AC converters, as

they are still the most popular type for industrial and residential applications.

2.1.1 DC-AC Converter Configurations

The voltage-source DC-AC converters can be categorized based on their circuit configuration as illustrated in Fig. 2.2. The most common configuration is based on the half-bridge structure that can be found in many converter topologies. The advantages of this configuration are the possibility of using commercially available modules and gate drivers, extensive design guidelines, and analysis tools to facilitate the design and testing process. The most widely-known DC-AC converter built based on the half-bridge configuration is the standard H-bridge converter. The next known circuit configuration is the midpoint clamp, which is formed by clamping the output to half of the DC-link voltage. The main benefit of this configuration is its ability to suppress the leakage current in grid-connected applications. However, it usually requires an active DC-link midpoint voltage balancing to ensure proper operation during line and load transients. Moreover, due to the large DC-link capacitors, the power density might be limited, especially in single-phase applications [20]. In some applications, such as transformerless PV inverters, reducing the leakage current is very important due to EMI and safety concerns [21]. One of the possible mitigation methods for the leakage current issue is generating a constant common-mode voltage (CMV) at all the switching states, which is the aim of constant CMV configurations. It should be noted that in this kind of configuration, the leakage current can be reduced significantly. However, due to some parasitic circuit elements and timing inaccuracies, still, the generated CMV is not perfectly constant, and some leakage current will be propagated [22]. The leakage current can be eliminated effectively by the common-ground type configurations, providing virtually zero CMV and almost zero leakage current. In this type, generating negative voltages is done with the help of capacitors connected to the output with the negative polarity [23–25]. It should be noted that the above-mentioned configurations can be combined to form a hybrid configuration converter.

In the following, some of the major three-level (3L) converter topologies are considered as conventional DC-AC converters. Additionally, a comparison has been conducted for the mentioned topologies.

2.1.2 Conventional 3L Converters

In this part, some well-known single-phase 3L DC-AC converters have been briefly introduced, along with their key features and setbacks. In addition,

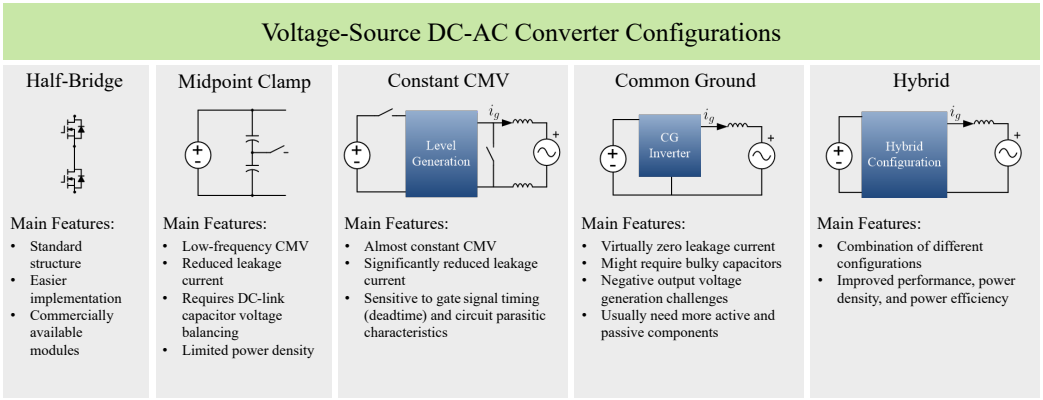


Fig. 2.2. DC-AC converter configurations.

a comparative study has been performed and the results are summarized in the end.

The introduced converters can be grouped into two categories based on their output voltage gain:

- **Buck-based converters:** These converters can only generate AC output voltages with an absolute value equal to or smaller than the DC input voltage. If the converter's output voltage can reach the DC-link voltage, it can be referred to as full DC-link voltage utilization (unity voltage gain).

- **Boost-based converters:** These converters can create AC output voltages with an absolute value greater than the DC input voltage. Conventionally, the maximum voltage gain of a boost converter is a fixed number (e.g., 2, 3, etc.) [26]. However, in some of the topologies available in the literature, the maximum voltage gain can be changed dynamically and continuously (i.e., by changing a duty cycle) [16, 23].

Considering the wide range of the DC input voltage in various practical applications (PV inverters, battery energy storage systems, etc.), often a boost DC-DC stage is required to implement a complete DC-AC power converter. This extra boost DC-DC stage can also help to achieve additional features, such as continuous input current, active power decoupling, and dynamic voltage-boosting gain [23, 24]. Therefore, for the buck-based converters, an extra boost DC-DC stage is essential for variable low-voltage DC sources (e.g., batteries or PV panels) for grid-connected converters. Hence, the overall DC-AC converter consists of two power conversion stages (two-stage converter structure). The same structure can be implemented with the boost-based converters with a fixed maximum voltage gain to keep the same

output voltage waveform and power quality over a wide range of input DC voltages. Having two consequent power processing stages might cause additional losses and increase the size and cost of the overall power conversion system.

On the other hand, boost-based converters with a dynamic voltage-boosting gain can eliminate the need for an extra DC-DC stage in this case. Consequently, even for a wide-varying DC input voltage, a single-stage power converter can be used. This enables potential improvements in power density, efficiency, and total cost for the whole power conversion platform [27, 28].

Fig. 2.3 shows the conventional 3L topologies considered in this part. It should be noted that a single-phase grid-connected condition with an L-type grid-interface filter has been assumed for all of the topologies for a fair comparison. The simplest and most common topology is an H-bridge consisting of four switches, two filter inductors, and one DC-link capacitor, as shown in Fig. 2.3(a). Although this topology offers a unity voltage gain (in linear modulation range) and uniform maximum voltage stress (MVS) across all devices, it suffers from an excessive high-frequency CMV, which in turn causes unwanted leakage currents. This topology is compatible with phase-shifted (PS) modulation, which can facilitate or improve the power loss distribution among the power devices and opens an opportunity for implementing sequential-based control methods [29].

Neutral-point-clamped (NPC) [30] and active NPC (ANPC) [31] are two well-known multilevel topologies that use the midpoint clamp configuration, as shown in Figs. 2.3(b) and 2.3(c), respectively. Both topologies support bidirectional power flow. However, in the NPC topology, power losses are distributed unequally among the power switches, and some of the transitions between the switching states must be avoided to prevent shoot-through due to the circuit topology [30]. Nonetheless, these drawbacks have been resolved in the ANPC converter, as the power losses can be shared equally among all the switches.

Another conventional topology is the T-Type structure [32], which is built based on the half-bridge and midpoint clamp configurations, as depicted in Fig. 2.3(d). In this topology, the MVS across the switches and the power losses in the switches are not equal. Moreover, it needs a bidirectional switch for the neutral-point clamping, which can be realized using several techniques [33–35].

Furthermore, HERIC [36], H5 [37], and PN-NPC [38] are based on the constant CMV configuration, as shown in Figs. 2.3(e), 2.3(f), and 2.3(g), respectively. These topologies are specifically designed to reduce the leakage current propagation in transformerless grid-connected inverters. All three provide a unity voltage gain with a bidirectional power flow capability.

Next, SSI [39] and quasi-Z-source [16] converters are two boost-based converters with a dynamic voltage-boosting gain. The SSI topology proposed in [39], as depicted in Fig. 2.3(h), offers a bidirectional power flow capability and uniform MVS across all circuit components with six switches, one capacitor, and three inductors. But it suffers from high-frequency CMV and excessive leakage current issues. Similarly, the quasi-Z-source topology presented in [16], as shown in Fig. 2.3(i), consists of four switches, one diode, four inductors, and two capacitors. Unlike the SSI in [39], it cannot handle reverse power flow (from AC to DC) due to the presence of the diode in its structure. Nevertheless, both of these topologies can be employed as a single-stage DC-AC power conversion system.

Table 2.1 summarizes the main features and characteristics of the mentioned conventional 3L voltage-source converters. It includes the basic configuration, number of active and passive devices, MVS and its uniformity across power devices, voltage gain, compatibility for phase-shifted (PS) modulation, CMV type and expected leakage current, and bidirectional power flow capability.

Table 2.1
Conventional 3L voltage-source DC-AC converters

Type of Converter	Configuration	No. of Devices					MVS Across Devices (p.u.)/ Uniform MVS		Voltage Gain	PS Modulation	CMV (Type)(p.u.)/ Leakage Current	Bidirectional Power Flow
		S	G	D	L	C	Switches	Capacitors				
H-Bridge	HB	4	4	0	2	1	1 / YES	1 / YES	1	YES	0.5 (HF) / High	YES
NPC [30]	MC	4	4	2	1	2	1 / YES	1 / YES	0.5	NO	0.5 (LF) / Low	YES
ANPC [31]	HB+MC	6	6	0	1	2	1 / YES	1 / YES	0.5	NO	0.5 (LF) / Low	YES
T-Type [32]	HB+MC	4	3	0	1	2	1 / YES	1 / YES	0.5	NO	0.5 (LF) / Low	YES
HERIC [36]	HB+CCMV	6	5	0	2	1	1 / YES	1 / YES	1	YES	0.5 (Const.) / Low	YES
H5 [37]	HB+CCMV	5	5	0	2	1	1 / YES	1 / YES	1	NO	0.5 (Const.) / Low	YES
PN-NPC [38]	MC+CCMV	8	8	0	2	2	1 / NO	0.5 / YES	1	NO	0.5 (Const.) / Low	YES
SSI [39]	HB	6	6	0	3	1	1 / YES	1 / YES	$D/(1-D)$	YES	0.5 (HF) / High	YES
quasi-Z Source [16]	HB	4	4	1	4	2	1 / YES	1 / NO	$1/(1-2D_{st})$	YES	0.5 (HF) / High	NO

HB: Half-bridge MC: Midpoint clamp CCMV: Constant CMV CG: Common Ground LF: Low-frequency HF: High-frequency D_{st}: Shoot-through duty cycle

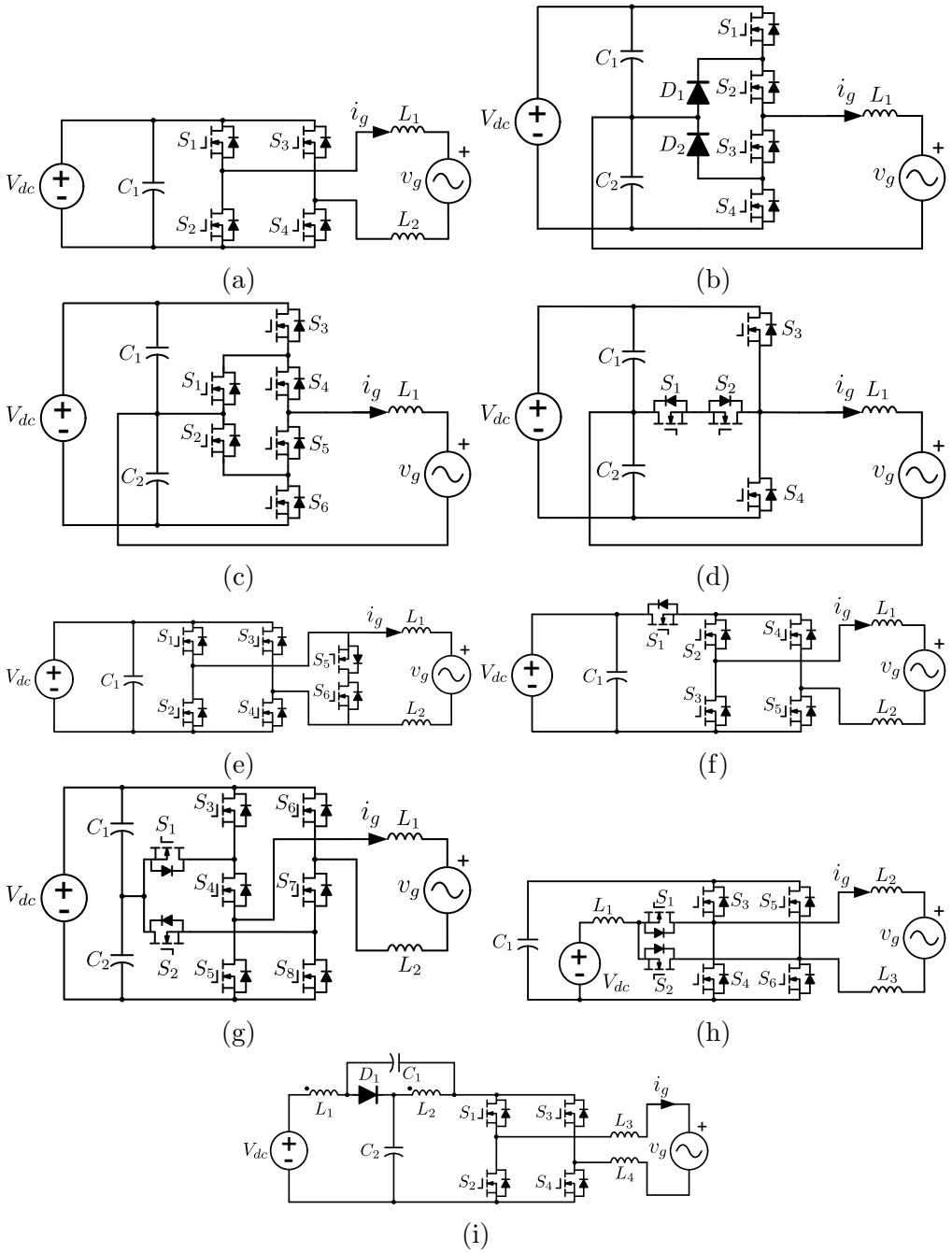


Fig. 2.3. Conventional 3L inverter topologies: (a) H-bridge; (b) NPC [30]; (c) ANPC [31]; (d) T-Type [32]; (e) HERIC [36]; (f) H5 [37]; (g) PN-NPC [38]; (h) SSI [39]; (i) qZ-source [16].

2.1.3 Extension Techniques

All the basic configurations and structures that have been mentioned above are only able to generate a 3L voltage at their output. However, it is more desirable to have a larger number of output voltage levels to improve the power quality, reduce total harmonic distortion (THD), and reduce the output filter size [40, 41]. Moreover, the maximum output voltage, current, and power of the converters are bounded to the limitations of their active and passive components. One of the basic possible solutions to extend the voltage range of a converter is using several series-connected switches instead of one switch. However, this approach needs fast and accurate voltage balancing of the series-connected switches, which increases the complexity of the power circuit and the gate drivers [42–44]. Similarly, paralleled switches can be used to increase the current rating of a converter, though the static and dynamic current balancing must be ensured for an effective implementation [45]. It is worth mentioning that with the series-connected and paralleled switches approaches, the number of output voltage levels will not be increased. Hence, the output filter size cannot be reduced using these two extension techniques. Fig. 2.4 summarizes the available extension techniques for DC-AC converters.

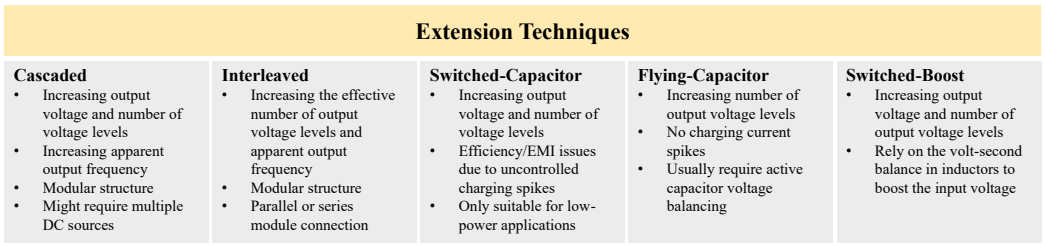


Fig. 2.4. An overview of the available extension techniques for DC-AC converters.

2.1.3.1 Cascaded Technique

Alternatively, cascaded and interleaved extension techniques can be employed to increase the number of output voltage levels, apparent output frequency, and maximum voltage ratings of a converter. In the cascaded method, similar cells are connected in series to synthesize a larger total output voltage. Some cascaded converters might require multiple isolated DC sources to operate, such as conventional cascaded H-bridge (CHB) topology [46], as shown in Fig. 2.5(a). It should be noted that some of the cascaded structures require only one DC source. For instance, a modular multilevel converter (MMC) [47] can be operated with only one DC source. An MMC can be formed based on many submodule structures. Among them, the half-bridge and full-bridge

submodule topologies are the most common choices. As an exmaple, an MMC with full-bridge submodules is depicted in Fig. 2.5(b). There are also some hybrid variants of CHB converters that can be operated with only one DC source without using HF isolation [48,49], or with the help of HF-isolated DC-DC converters [50].

Moreover, differential converters also use a special case of cascaded technique to create more voltage levels and achieve a higher DC-link voltage utilization. A simple H-bridge converter (see Fig. 2.3) can be considered as one of the simplest differential DC-AC converters, formed by the differential connection of two half-bridge cells. Another example of this type of converters is presented in [51], which synthesizes an AC output waveform using two differentially-connected boost converters.

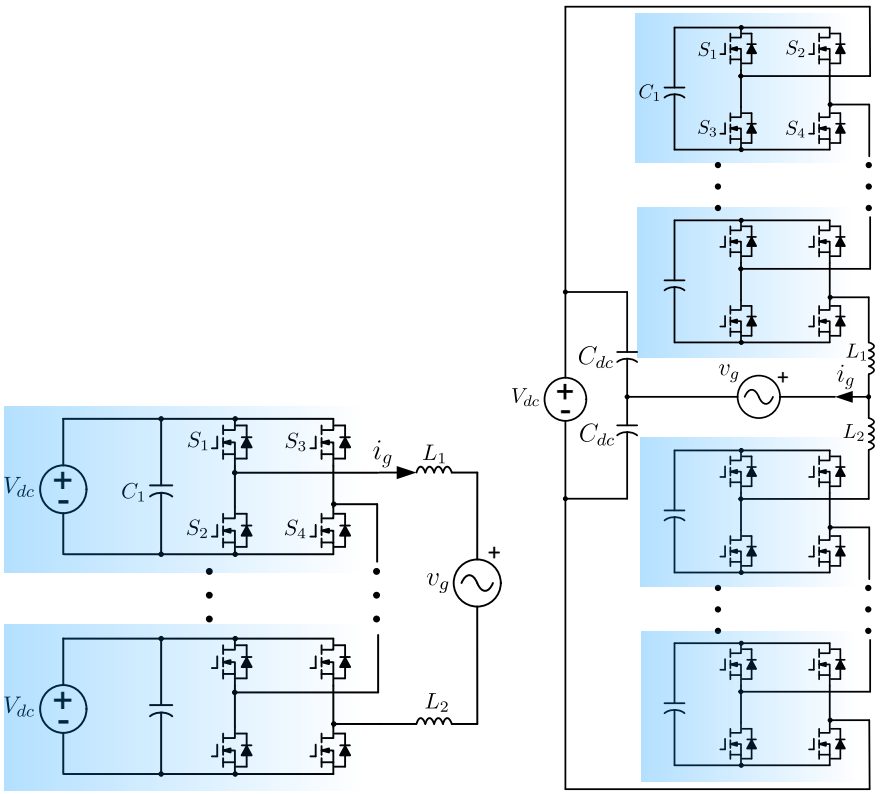


Fig. 2.5. Conventional multilevel converters based on cascading technique: (a) CHB [46]; (b) MMC [47].

2.1.3.2 Interleaved Technique

The interleaved technique helps achieve a larger apparent output switching frequency (or reduced switching frequency for a given apparent frequency) in series (cascaded) and paralleled converter units. In fact, the carriers used for modulation can be shifted in time with a particular phase shift in the interleaved method. Through this technique, the effective number of output voltage levels can be increased. In addition, a series connection enables increasing the maximum output voltage, and a parallel connection allows for a larger current handling capability of the converter. Consequently, using this technique, scalable and modular structures can be formed. Fig. 2.6 shows some examples of interleaved converters with parallel connections.

2.1.3.3 Switched-Capacitor Technique

The number of output voltage levels and voltage gain of a converter can be extended using the switched-capacitor (SC) techniques. In this type of extension, one or more SC cells are added to achieve the required voltage levels by series and/or parallel connection of the involved capacitors in the SC cells. The main benefit of this technique is its flexibility and simplicity in reaching a larger voltage gain and a higher number of voltage levels using fewer active and passive devices. However, the capacitors are charged through voltage sources with low-impedance charging paths, resulting in large charging current spikes, EMI, and reliability issues [53].

2.1.3.4 Flying-Capacitor Technique

This technique is based on the addition and subtraction of a capacitor voltage in the output current loop of a converter. It is important to emphasize that both the charging and discharging paths of a flying capacitor are usually through inductive loops. Therefore, the charging of the flying capacitor is smooth without any inrush spikes. Moreover, the voltages of the flying capacitors might need to be balanced and controlled, actively or passively, for a safe and stable operation under transients of the input source or the load sides [54, 55].

2.1.3.5 Switched-Boost Technique

Obtaining a dynamic voltage-boosting gain is a key feature in realizing single-stage DC-AC converters for wide-varying DC sources. Switched-boost techniques are based on the volt-second balance of an inductor to boost the DC input voltage with the desired gain controlled by the boost duty cycle. The

working principle of switched-boost circuits is closely related to the conventional synchronous boost converter. However, in this case, the boost circuit is merged with the level-generation circuits to reduce the component count and improve the overall performance of the system [23, 24].

2.1.4 Comparative Study

In this part, a few examples of notable multilevel converter topologies with hybrid configurations are presented in Figs. 2.7 and 2.8. Moreover, a topology comparison has been conducted and summarized, as shown in Table 2.2.

The topologies are organized into the following three main groups:

- Buck-Based
- Boost-Based
- Dual-Mode-Based

The selected buck-based converters are depicted in Fig. 2.7. Here, all the topologies can generate a five-level (5L) output voltage waveform. In addition, some of the notable boost-based converters are shown in Fig. 2.8. Furthermore, dual-mode converters have been included in this study as an emerging concept realized in recently published works such as [56,57]. Fig. 2.9 shows a 5L dual-mode converter with midpoint clamp configuration and two operating modes: 1) in the buck mode, the voltage gain is 0.5 and the circuit is working based on the flying capacitor technique; 2) in the boost mode, it provides a unity voltage gain based on a switched-capacitor technique [57]. A comparative study has been conducted for the mentioned topologies, and the results are summarized in Table 2.2. In this study, topologies with different combinations of configurations and extension techniques have been considered. Moreover, the comparative parameters are the number of output voltage levels, the number of circuit components, MVS across switches and capacitors and its uniformness, voltage gain, single-stage power conversion capability for wide-varying DC sources, active capacitor voltage balancing requirement, modulation type, the type of CMV and leakage current, and bidirectional power flow handling capability.

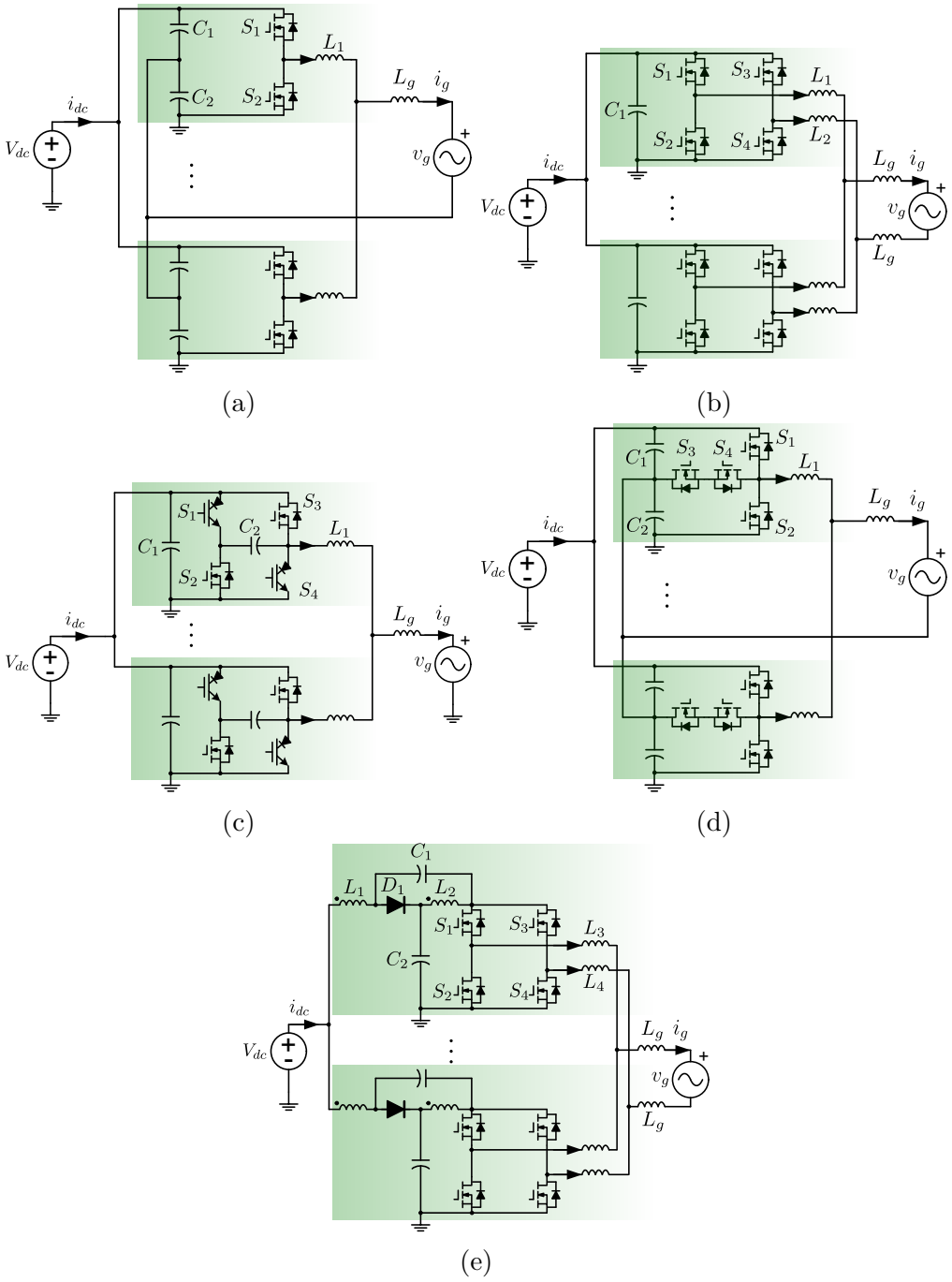


Fig. 2.6. Examples of single-phase interleaved DC-AC converters based on: (a) conventional half-bridge topology; (b) conventional H-bridge topology; (c) Siwakoti-H topology [52]; (d) T-type topology; (e) quasi Z-source topology [16].

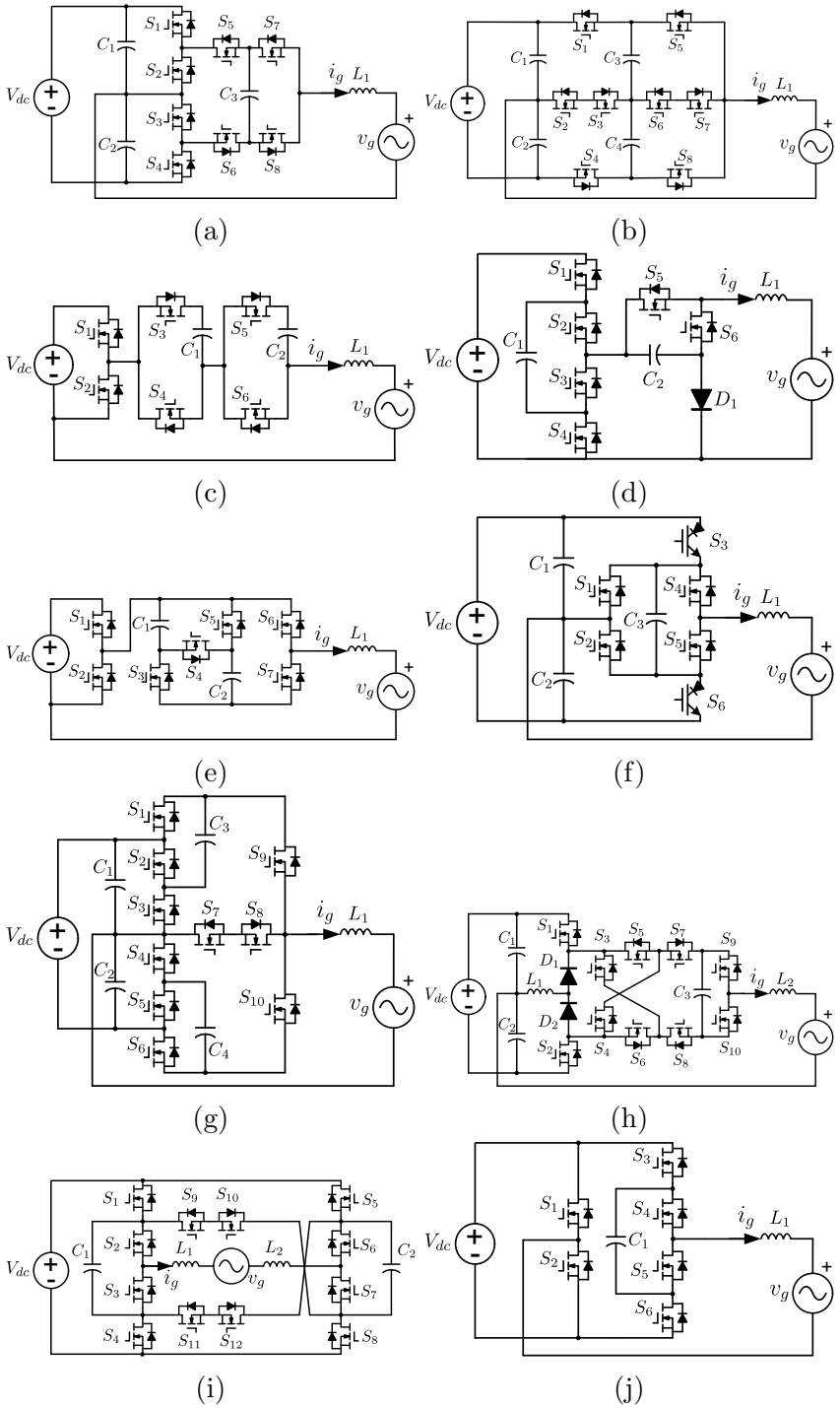


Fig. 2.7. Buck-based multilevel converters: (a) Hybrid ANPC [58]; (b) SMC [59]; (c) Hybrid CG [60]; (d) Hybrid CG [25]; (e) Hybrid CG [61]; (f) ABNPC [62]; (g) Hybrid T-Type [26]; (h) Hybrid MC [63]; (i) Hybrid FC [64]; (j) PUC5 [65].

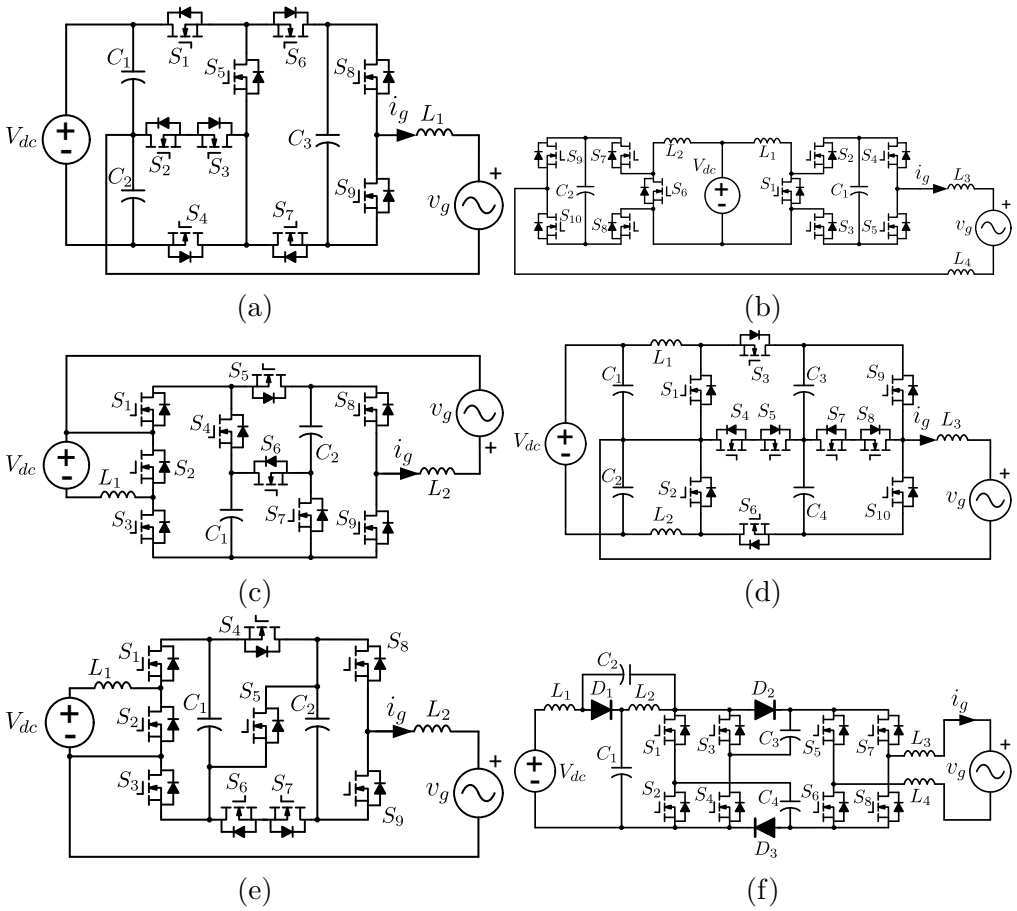


Fig. 2.8. Boost-based multilevel converters: (a) Hybrid ANPC [66]; (b) Hybrid SB [67]; (c) Hybrid SB [68]; (d) Hybrid SB [27]; (e) Hybrid SB [24]; (f) Hybrid qZ-Source [69].

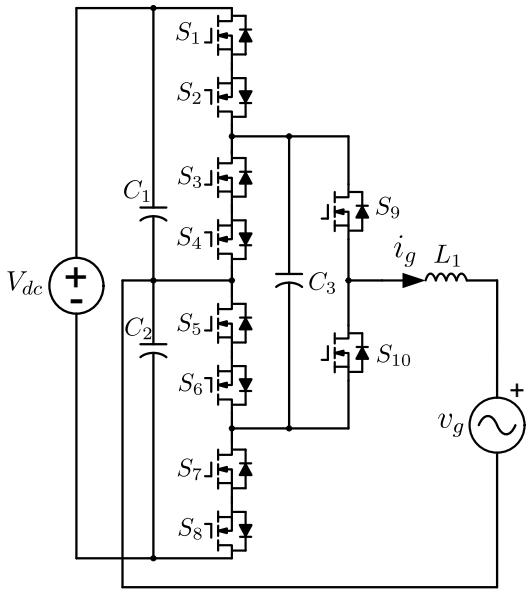


Fig. 2.9. Dual-mode 5L converter [57].

Table 2.2
Comparative study summary for the selected multilevel topologies

Type of Converter	Configuration	Extension Method	No. of Levels	No. of Devices					MVS Across Devices (p.u.)/ Uniform MVS		Voltage Gain	Single-Stage Power Conversion Capability	Active Balancing Requirement/ Modulation	CMV (p.u.)/ Leakage Current	Bidirectional Power Flow
				S	G	D	L	C	Switches	Capacitors					
Hybrid ANPC [58]	MC	FC	5	8	8	0	1	3	1 / NO	1 / NO	0.5	NO	YES / LS, Hybrid	0.5 (LF) / Low	YES
SMC [59]	HB+MC	FC	5	8	8	0	1	4	0.5 / YES	1 / NO	0.5	NO	YES / LS, PS	0.5 (LF) / Low	YES
Hybrid CG [60]	HB+CG	FC	5	6	6	0	1	2	1 / NO	0.5 / YES	1	NO	NO / PS, Hybrid	≈ 0 / ≈ 0	YES
Hybrid CG [25]	HB+CG	SC+FC	5	6	6	1	1	2	1 / NO	1 / NO	1	NO	YES / LS	≈ 0 / ≈ 0	YES
Hybrid CG [61]	HB+CG	SC	5	7	7	0	1	2	1 / NO	0.5 / YES	1	NO	NO / LS	≈ 0 / ≈ 0	YES
ABNPC [62]	HB+MC	SC	5	6	6	2	1	3	1 / NO	1 / NO	1	NO	YES / LS	0.5 (LF) / Low	NO
Hybrid T-Type [26]	HB+MC	SC	5	10	9	0	1	4	1.5 / NO	1 YES	1	NO	YES / LS	0.5 (LF) / Low	YES
Hybrid MC [63]	HB+MC	SC	5	10	10	2	2	3	0.5 / YES	0.5 / YES	1	NO	YES / LS, Hybrid	0.5 (LF) / Low	NO
Hybrid FC [64]	CCMV	FC	5	12	10	0	2	2	1 / NO	0.25 / YES	1	NO	YES / PS, Hybrid	0.5 (Const.) / Low	YES
PUC5 [65]	HB	FC	5	6	6	0	2	1	1 / NO	0.5 / YES	1	NO	YES / PS, Hybrid	0.5 (HF) / High	YES
Hybrid ANPC [66]	MC	SC+FC	7	9	8	0	1	3	0.67 / NO	0.67 / NO	1.5	NO	YES / LS	≈ 0 / ≈ 0	YES
Hybrid SB [67]	HB	SB+CAS	5	10	10	0	4	2	0.5 / YES	0.5 / YES	$2D/(1-D)$	YES	NO / PS, Hybrid	0.25 (HF) / Moderate	YES
Hybrid SB [68]	HB+CCMV	SC+SB	5	9	9	0	2	2	0.5 / YES	0.5 / YES	$2D/(1-D)$	YES	NO / LS	-0.5 / ≈ 0	YES
Hybrid SB [27]	HB+MC	SB	5	10	8	0	3	4	1 / NO	0.5 / NO	$D/(1-D)$	YES	NO / PS, Hybrid	≈ 0 / ≈ 0	YES
Hybrid SB [24]	HB+CG	SB+FC	5	9	8	0	2	2	1 / NO	1 / NO	$(1+D)/2(1-D)$	YES	NO / LS	≈ 0 / ≈ 0	YES
Hybrid qZ-Source [69]	HB	SC	7	8	8	3	4	4	1 / NO	1 / NO	$3/(1-2D_{st})$	YES	NO / LS	0.5 (HF) / High	NO
Dual-Mode [57]	HB+MC	SC+FC	5	10	6	0	1	3	1 / NO	1 / NO	1 (boost), 0.5 (buck)	NO	YES / LS, Hybrid	0.5 (LF) / Low	YES

HB: Half-bridge MC: Midpoint clamp CCMV: Constant CMV CG: Common Ground FC: Flying Capacitor SC: Switched Capacitor SB: Switched Boost CAS: Cascaded PS: Phase-Shifted LS: Level-Shifted
LF: Low-frequency HF: High-frequency D_{st}: Shoot-through duty cycle

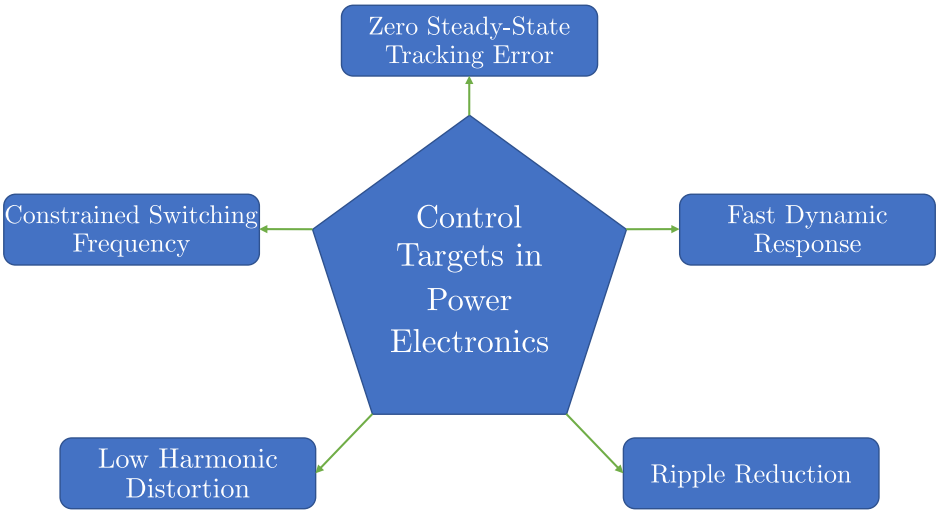


Fig. 2.10. Major control targets in power electronics converters.

2.2 Control and Modulation

This section focuses on the control aspect of DC-AC converters. More specifically, the common control targets, controller types, and modulators in power converters have been reviewed.

2.2.1 Control Targets

Most of power electronics converters require a closed-loop control system to achieve their intended purpose in practice. In the context of smart grids and grid-connected converters, the general control objectives can be categorized into five groups as depicted in Fig. 2.10. These objectives are summarized as follows:

- Zero Steady-State Tracking Error

  The main objective of the control system is tracking the reference as closely as possible within the limitations enforced by the plant or other applicable constraints. Hence, a zero tracking error (deviation of the controlled parameter from its reference) is desired. In DC systems with constant references and disturbances, normally proportional-integral (PI) or proportional-integral-derivative (PID) controllers are the preferred candidates due to their maturity, well-known behavior and design methods. These controllers can achieve a zero tracking error with constant references. However, in AC systems, they can cause considerable phase and amplitude errors due to the time-varying sinusoidal nature of

the references and disturbances. This tracking error can, in turn, cause issues such as power quality and non-ideal power factor problems [70].

- Fast Dynamic Response

  Power electronics converters can be found as a critical part of many systems, such as EVs, renewable distributed energy resources (DERs), battery energy storage units, industrial machines, etc. Therefore, to achieve the required response time in the overall system, the involved power converters must be able to follow the given commands and references accurately and quickly. For instance, in EV charging stations, specialized power converters are required to compensate for large charging load transients in a safe and swift manner to maintain the grid stability and power quality [71, 72].

- Ripple Reduction

  In many practical applications, it is desired to reduce the ripple on the critical voltages/currents to improve the power quality and power efficiency of the system. Furthermore, ripple reduction techniques allow using smaller passive components in power circuits, leading to more compact and potentially more affordable systems for broader applications [73, 74]. Moreover, undesired ripples can accelerate the degradation of some components, including batteries, fuel cells, capacitors, or even power semiconductors [75, 76].

- Low Harmonic Distortion

  Harmonic distortion is one of the well-known unwanted phenomena in AC and DC power circuits and systems. Ideally, in AC systems, the voltages and currents are expected to have a pure sinusoidal shape at the fundamental frequency only. Similarly, in DC systems, only DC voltages and currents should be present in the ideal case. Any additional oscillating component might cause some issues in the system itself or in the neighboring systems. For example, harmonics can increase the power losses in AC transformers and motors [77, 78].

- Constrained Switching Frequency

  Operating a power converter with a fixed switching frequency or varying switching frequency within a limited range helps to optimize the design parameters of the hardware and controllers. Moreover, it simplifies the power loss estimation process, especially for switching loss calculations. In addition, a constrained switching frequency results in predictable and almost constant voltage/current spectra in the frequency domain.

This can facilitate the filter design for the converter's input and output power ports [79].

As can be seen, some of the above-mentioned targets might not be compatible with each other. For instance, achieving low harmonic distortion might require a slower dynamic response. One of the challenging parts of the controller and modulator design process for power converters is to find and decide about these tradeoffs based on the application's requirements.

2.2.2 Controller Types

In most practical applications, power electronics converters need a controller unit to realize the intended goals by moving the operating points to the desired values within a closed-loop configuration. One of the possible approaches for categorizing the controllers for power converters is based on the presence of a modulator in the system [80]:

- **Controllers with External Modulator:** In this type, the controller generates a continuous control input (usually duty cycles) to regulate the desired outputs based on the averaged model of the power conversion system. Therefore, this control input belongs to a continuous control set (CCS). Because direct implementation of a continuous signal with a switching-based power converter is not feasible, a modulator is converting the duty cycles generated by the controller to the gate switching signals. A modulator normally is operating based on comparing a carrier signal (usually a triangular or a sawtooth waveform) with the modulation reference input. The main benefit of using a modulator is achieving a fixed or constrained switching frequency with a known spectrum in the frequency domain.

- **Controllers without Modulator:** It is possible to control a power converter directly without adding a modulator to the system. In this case, the control input is the gate signals (states of the power switches), which belongs to a finite control set (FCS). In this approach, an instantaneous dynamic model of the converter is used to design the controller. Therefore, a better dynamic response can be achieved compared to the average models. However, the spectra of the generated voltages are spread within a wide range of frequencies.

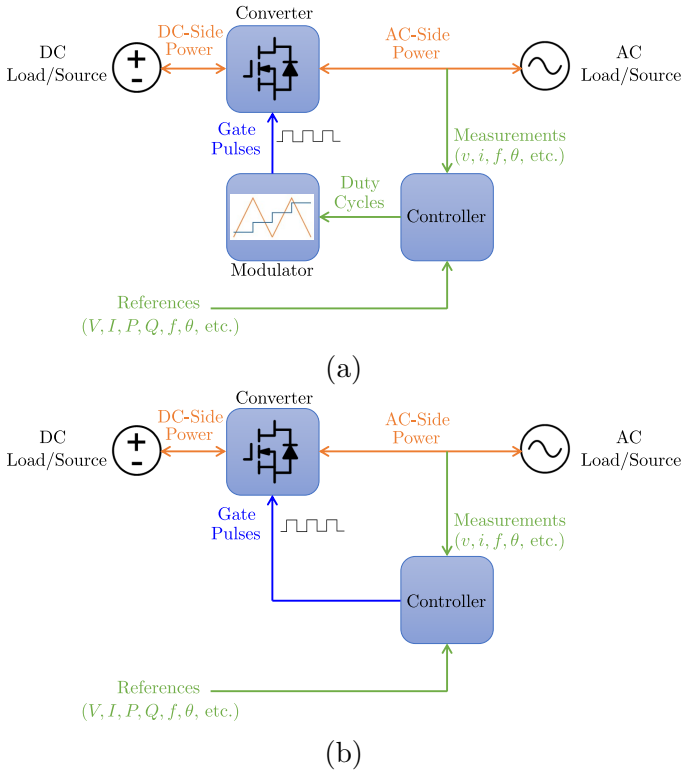


Fig. 2.11. Controller types: (a) controller with an external modulator; (b) controller without modulator.

2.2.3 Modulators

As mentioned above, a continuous control input needs to be translated into the switching pulses to be applied to a switching power converter using a modulator to synthesize a required converter output voltage. Many modulation methods have been proposed in the literature for different goals and applications. Among all, pulse-width modulation (PWM) is the most commonly used modulation technique in power converters. More specifically, PWM methods can be classified into three major groups:

2.2.3.1 Carrier-Based PWM

In this category, the modulation reference input is compared to a carrier signal and the result of the comparison is used to trigger the switches in a power converter. There are several variants of carrier-based PWM methods available in the literature, including sinusoidal PWM (SPWM) [81], trapezoidal PWM [82], zero-sequence PWM [83], and spread-spectrum PWM [84]. Among them, SPWM is the simplest method that is used in many low- and medium-power applications due to its acceptable performance and low computational cost. Zero-sequence PWMs are well-known for reducing the DC-link voltage requirement in three-phase systems by synthesizing a zero-sequence voltage in each phase [83]. In addition, spread-spectrum PWMs are developed to spread the high-frequency (switching) harmonics over a narrow frequency band to suppress the conducted and radiated emissions and mitigate EMI-related issues [84]. Furthermore, multi-carrier-based PWMs can be employed for controlling multilevel converters. The carrier-based PWM methods for multilevel converters can be categorized into three main groups:

- **Level-Shifted-PWM (LS-PWM):** In an LS-PWM, the modulation reference is compared to a set of vertically shifted carriers, as shown in Fig. 2.12(a). In LS-PWM, the apparent output frequency is equal to the carrier frequency. However, the average frequency of every switch over a fundamental cycle is lower than the carrier frequency in this type of modulation. Moreover, each power switch might present a different commutation frequency, which leads to an uneven power loss distribution. Generally, all multilevel converters can be controlled with the LS-PWM method [85, 86].

- **Phase-Shifted-PWM (PS-PWM):** On the other hand, in PS-PWM, the modulation reference is compared to a set of horizontally shifted (shifted in time or phase), as indicated in Fig. 2.12(b). In this modulation, the apparent output frequency is a multiple of the carrier frequency. In addition, the average frequency of every switch is equal

to the carrier frequency. It should be noted that using PS-PWM is only possible for some particular converters with redundant switching states, at least for one output voltage level. Consequently, it cannot be applied to every multilevel converter [87].

- **Hybrid PWM:** By combining the LS-PWM and PS-PWM methods, hybrid modulation methods can be designed and tailored for a wider range of multilevel converters with less redundant switching states. An example of a hybrid modulation is shown in Fig. 2.12(c). Since hybrid modulation methods are based on a combination of PS-PWM and LS-PWM, the characteristics of the modulator and the resultant spectrum of the unfiltered output voltage are highly dependent on the modulator's internal configuration [88].

2.2.3.2 Space-Vector PWM (SVM)

This modulation is created for three-phase two-level (2L) and multilevel converters. In the SVM method, the redundant switching states in the vicinity of the desired output voltage reference vector in the abc or $\alpha\beta$ frames are used to synthesize the requested output voltage. To do so, each identified (selected) switching state is applied to the converter for a specific (calculated) fraction of the sampling time [89, 90]. The selection criteria for the switching states depend on the objectives of the modulation. These objectives can be reducing power losses, CMV, or output ripples [91]. The SVM concept also can be extended to be applied to multi-phase systems, as presented in [92, 93]. An important point here is that although SVM and carrier-based PWM methods are using different approaches, it is possible to achieve exactly the same results as SVM by modifying the modulation references in carrier-based modulations [94].

2.2.3.3 Optimal PWM

To achieve good harmonic and dynamic performance in high-power converters with low switching frequencies, optimal PWM methods can be utilized. In this group of modulations, the number of switching commutations in a fundamental cycle is fixed, and the exact time for each commutation is determined through an optimization process. The main objective for such optimization is usually shaping the output voltage spectrum of the converter by controlling the low-frequency (LF) harmonics [95]. In addition, other objectives, such as voltage balancing and CMV reduction, can be incorporated into the

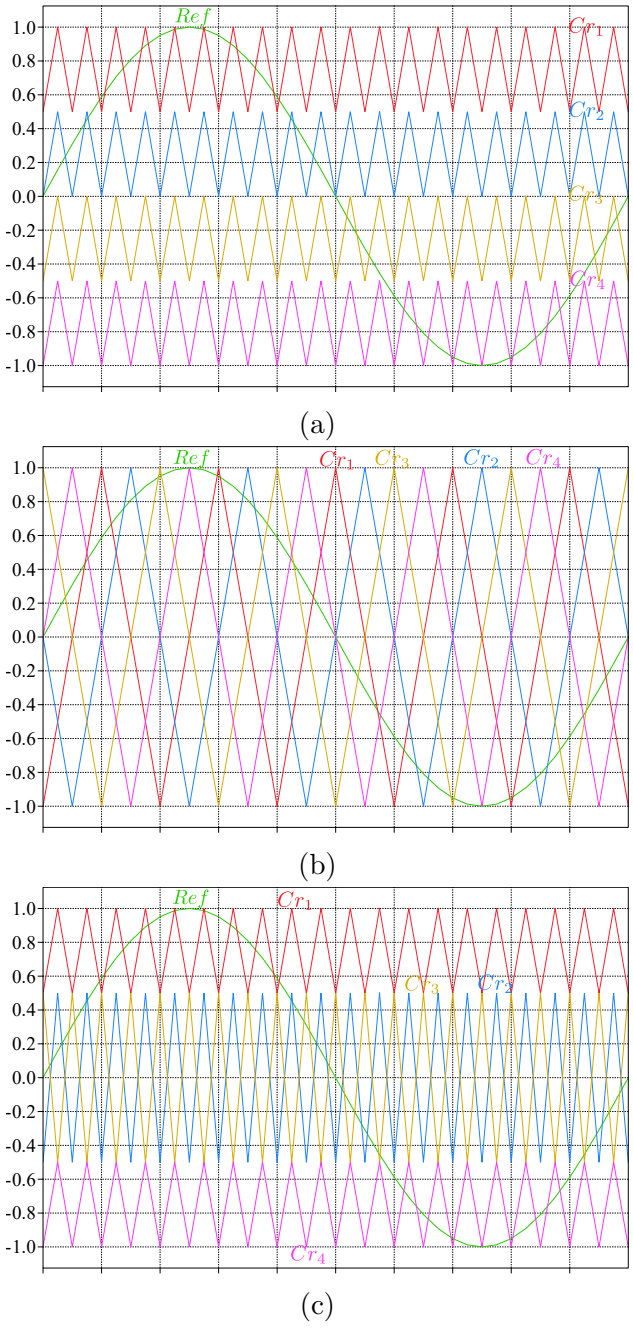


Fig. 2.12. Carrier-based PWM methods for multilevel converters: (a) LS-PWM; (b) PS-PWM; (c) Hybrid PWM.

optimization problem as well [95, 96]. The main benefit of using such modulation methods is having direct control over the voltage/current harmonics to ensure compliance with the grid codes [80]. Some of the variants of optimal PWM are selective harmonic elimination (SHE) [97, 98], selective harmonic mitigation (SHM) [99, 100], and optimal pulse pattern (OPP) [95, 96].

2.2.4 Control Strategies for Grid-Connected Inverters

In this part, a brief overview of the available control strategies for grid-connected inverters is presented. Looking from the design perspective, the grid-connected inverter controllers can be categorized into two major groups:

2.2.4.1 Frequency-Domain-Based Controllers

Frequency-domain-based controllers are designed based on the transfer function of the plant for single-input single-output (SISO) systems in the frequency domain. This group of controllers is the most common controller type used in many power electronics converters due to their robustness, predictable dynamic response, fixed switching frequency, acceptable performance, mature design techniques, and easy implementation in practice. It is worth mentioning that this type of controller needs an external modulator (e.g., PWM) to generate the required gate signals. For the control system design, the effects of the modulator can be neglected when the switching frequency is high enough. Therefore, a generic closed-loop control system can be formed as shown in Fig. 2.13. Here, $C(s)$ and $G_o(s)$ are the controller and plant transfer functions in the frequency domain, respectively. Additionally, r, u, and y are the reference (to be tracked), control input, and the system's output, respectively. Moreover, η_i is the input disturbance and η_o is the output disturbance in the system. Consequently, the output of the closed-loop system shown in Fig. 2.13 can be expressed as:

$$y(s) = T(s)r(s) + S(s)\eta_o(s) + S_i(s)\eta_i(s) \tag{2.1}$$

where $T(s)$ is the tracking transfer function, and $S(s)$ and $S_i(s)$ are the output and input sensitivity transfer functions which indicate the disturbance rejection performance of the controller. The expressions for the mentioned

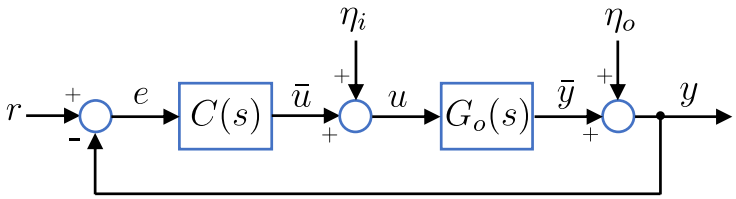


Fig. 2.13. A block diagram view of a generic closed-loop control system.

transfer functions are calculated below:

$$T(s) = \frac{C(s)G_o(s)}{1 + C(s)G_o(s)} \tag{2.2}$$

$$S(s) = \frac{1}{1 + C(s)G_o(s)} = 1 - T(s) \tag{2.3}$$

$$S_i(s) = \frac{G_o(s)}{1 + C(s)G_o(s)} = G_o(s)S(s) \tag{2.4}$$

As can be realized from (2.2)-(2.4), in an ideal closed-loop system, $T(s) = 1$ and $S(s) = 0$. However, in practice, this condition usually can be achieved only for a limited frequency range. It should be noted that for a given plant $G_o(s)$, the controller $C(s)$ affects $T(s)$, $S(s)$, and $S_i(s)$ transfer functions and they cannot be changed independently.

Since most of the modern power converters are based on digital controllers, the obtained controllers designed in frequency-domain assume a continuous-time domain, they must be transformed into a discrete-time form using discretization methods. Some of the well-known discretization methods are zero-order hold (ZOH), Tustin, forward Euler, and backward Euler [101].

2.2.4.1.1 PI Controller

The basic frequency-domain-based controller is the PI controller, which consists of a scalar gain and an integrator. The transfer function for a PI controller is given by:

$$C_{PI}(s) = K_p + \frac{K_i}{s} \tag{2.5}$$

To illustrate how the controller can be analytically design, a generic form of a first-order plant transfer function is considered as:

$$G_o(s) = \frac{K_o}{\tau_o s + 1} \tag{2.6}$$

As can be seen from (2.5), the total controller gain at DC (i.e., $s = 0$) is infinite. Therefore, using (2.2) and (2.5), it can be concluded that the

tracking error approaches zero, and perfect tracking can be achieved for DC references.

Considering (2.2), (2.5), and (2.6), the resultant closed-loop system can be expressed as a second-order system. Hence, by choosing the desired closed-loop system characteristics (i.e., natural frequency ω_n and damping factor ζ), the coefficients of a PI controller to govern a first-order plant can be expressed as follows [80]:

$$T_i = \frac{2\zeta}{\omega_n} - \frac{1}{\omega_n^2 \tau_o} \tag{2.7}$$

$$K_p = \frac{\omega_n^2 \tau_o}{K_o} T_i \tag{2.8}$$

$$K_i = \frac{K_p}{T_i} \tag{2.9}$$

Since the PI controller only can track DC references with zero steady-state error [i.e., $S(0) = 0$], it cannot be used for tracking AC references directly. However, in a synchronous reference frame (dq), AC signals will be translated to DC values, and PI controllers can be employed to control the injected active and reactive power into the grid. In this case, a phase-locked-loop (PLL) is required to extract the phase information for the $dq/\alpha\beta$ transformations. A simplified block diagram for such a controller is shown in Fig. 2.14(a).

2.2.4.1.2 Proportional-Resonant Controller

As mentioned before, PI controllers cannot perfectly track AC references due to their finite gain. This issue can be addressed by designing resonant-based controllers. In this case, the transfer function of the controller has a resonant frequency and infinite gain at the nominal fundamental frequency (ω_0). Therefore, perfect tracking and zero steady-state error can be achieved for AC references [101].

One of the possible approaches for designing a resonant controller is to transform a pre-designed PI controller to a resonant-based form as suggested in [102]. The resultant transfer function of such a proportional-resonant (PR) controller can be expressed as follows:

$$C_{PR}(s) = K_p + \frac{2K_i s}{s^2 + \omega_0^2} \tag{2.10}$$

where K_p and K_i are the coefficients of the pre-designed PI controller, and ω_0 is the resonant angular frequency of the PR controller.

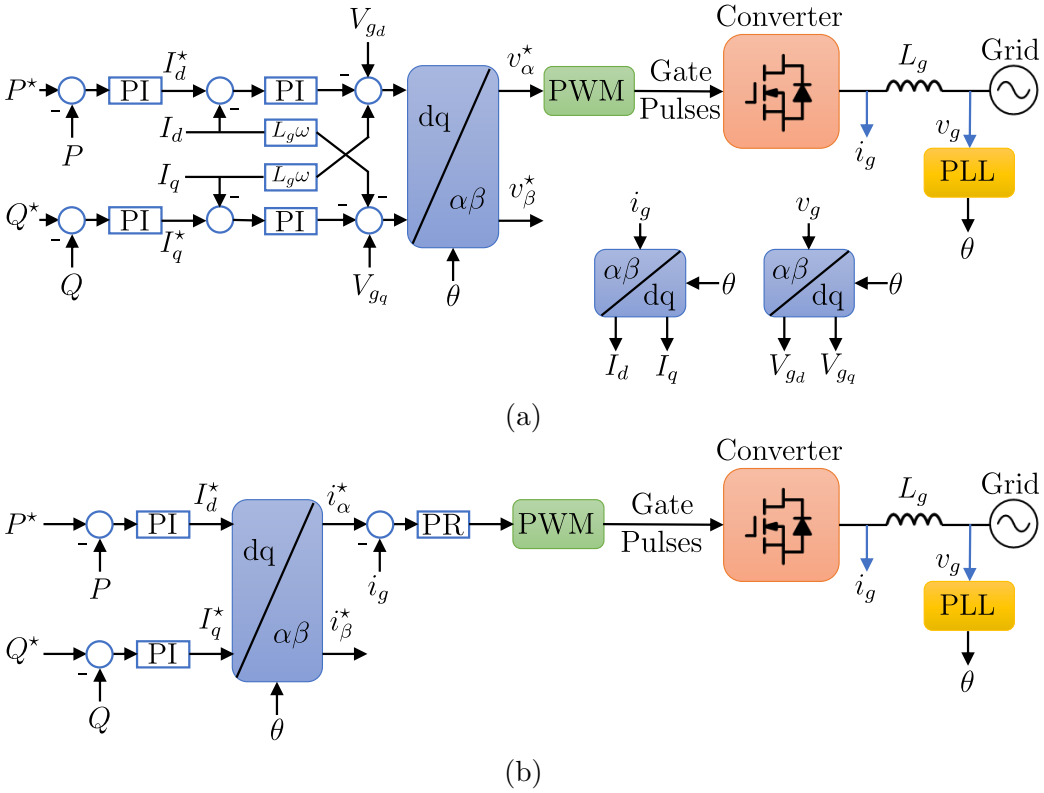


Fig. 2.14. Simplified block diagram view of conventional frequency-domain control strategies for grid-connected inverters: (a) PI controller; (b) PR controller.

As can be realized from (2.2), (2.10), and (2.6), the steady-state tracking error will be zero only for the references with the frequency of ω_0. Moreover, any disturbance at ω_0 in the closed-loop system will be perfectly rejected due to the infinite controller gain at its resonant frequency [70]. A simplified block diagram for such a controller is shown in Fig. 2.14(b).

2.2.4.2 Time-Domain-Based Controllers

In this category, the design and implementation procedure is based on a time-domain dynamic model of the system. The simplest controller in this group is the hysteresis controller. In this controller, the current is compared to its desired value (reference), and the control input is decided by the comparison result. In practice, an error band is considered to limit the switching frequency and prevent unnecessary commutations of the power switches [103]. The main benefits of this controller are its fast response time, robustness

against system parameter changes, and simple structure [103]. However, it has some drawbacks, such as variable switching frequency, noise sensitivity, and uncontrolled bandwidth [80]. There are some published works that tried to address the mentioned issues. For example, in [104], a fixed switching frequency is achieved through dynamic estimation and adjustment of the hysteresis bands.

One of the basic time-domain-based controllers is the state feedback controller (SFC). In this control strategy, the control inputs are determined as linear combinations of the error signals [101, 105]. Although this controller can achieve a fast dynamic response, including the control input and state constraints is not straightforward in this controller. Moreover, tuning the gain parameters is usually done using the pole placement approach. The pole placement method is based on placing the poles of the closed-loop transfer function at specific locations on the complex plane by normally selecting two dominant poles to achieve the desired behavior. However, using this method for systems with a large number of states might be complicated and not necessarily optimal [101].

To address the tuning issue of the SFC method, the linear quadratic regulator (LQR) method was introduced. Although the controller structure is similar to SFC, the method used to obtain the gain parameters is different. In fact, the LQR approach can deal with a larger number of states while the controller parameters can be obtained optimally by solving the algebraic Ricatti equations [101, 106].

Another type of model-based controller is the deadbeat controller, which tries to reach the reference in the next sampling time. Hence, deadbeat controllers usually have very quick response times, and their implementation is relatively simple. However, unrestricted control bandwidth makes these controllers sensitive to delays, errors, and uncertainties in the measurements and the models [107].

2.2.4.2.1 Model-Predictive Controller

Model-predictive control (MPC) is a nonlinear optimal control method in which the optimum set of control inputs is obtained subject to the system's model and control input and state constraints [46]. There are two main types of MPC-based controllers:

- FCS-MPC: In this type, the control inputs are directly the switching pulses or switching voltages in a power converter. Hence, the number of possible control inputs is finite, and a modulator is not required in this method. Consequently, the instantaneous model of the system

is used to predict the system's states in the next sampling times for each possible member of the input control set. Although it has a fast dynamic response and straightforward implementation, the switching frequency in this method is not constant due to the absence of the modulator [108, 109].

- CCS-MPC: To address the variable switching frequency in the FCS-MPC method, a modulator can be added to the control system, and the controller generates a continuous control input as the modulation reference signal. In this case, the average model of the system is used to predict the system's states in the next sampling times [29, 46].

It is important to note that there are other time-domain-based controllers that can be utilized in power electronic converters including bu not limited to sliding-mode controller (SMC), fuzzy logic controller, and neural-network-based controller [110,111]. However, those control approaches are not covered in this work due to scope and time constraints.

2.3 Design Challenges in Grid-Connected Inverters

The integration of renewable energy sources and energy storage units into smart grids require AC-DC and DC-DC power converters. Moreover, the interactions of EVs with the grids (e.g., V2G and G2V) can significantly impact the performance of smart grids. Considering AC grids as the major type of the current electricity networks, grid-connected inverters are one of the essential components in smart grids due to their vast applications. In the power electronics field, researchers focus on deriving new advantageous circuit topologies as well as control systems. However, for grid-connected inverters, there are particular challenges that need to be addressed to obtain a suitable power conversion system that meets the application requirements. In the following, some of the identified design challenges in grid-connected inverters in terms of circuit topology and control are provided.

2.3.1 Grid Filter Size and Power Quality

Most inverters for grid-connected applications are built based on conventional 3L topologies and SPWM methods to address the leakage current and CMV-related issues, reduce the total cost of the whole system, reduce the losses, and improve the power density of the converter while meeting the power

quality standards. In this regard, the output characteristics of a grid-tied inverter have a significant impact on its filtering requirement on the AC side. Generally, AC filters for grid-connected converters should have both differential and common-mode attenuation. The differential filtering mostly suppresses the high-frequency harmonics in the inverter's differential output voltage and improves the THD of the injected current into the grid. On the other hand, the main aim of common-mode filtering is to attenuate the leakage currents caused by the generated CMV [112].

In terms of injected current quality, grid codes require a maximum allowable THD value. For instance, the IEEE 519-2014 standard [113] mandates a THD value lower than 5%. Assuming a proper controller and a simple L-type grid-interface filter, the grid current quality mostly depends on the AC differential filter impedance, the apparent output frequency of the inverter, and the number of output voltage levels, as expressed below [40]:

$$\Delta i_g^{p-p} = \frac{V_{DC}}{(n-1)^2 f_{sw} L_g} \tag{2.11}$$

where, i_g^{p-p} is the peak-to-peak value of the high-frequency current ripple of i_g passing through L_g, n is the number of output voltage levels, f_{sw} is the apparent output frequency of the inverter, and V_{DC} is the total DC-link voltage of the inverter. As can be realized from (2.11), increasing the number of levels and/or the apparent output frequency of the inverter can reduce the size of the grid-interface filter significantly. Consequently, this leads to a more compact filter with smaller equivalent series resistance (ESR), resulting in a higher efficiency.

Another important aspect of grid-connected inverters is the generated CMV and leakage current. The maximum allowable root-mean-square (RMS) leakage current is restricted by several grid codes (e.g., VDE-AR-N 4105, IEC 60755, VDE 0100-410, and VDE 0100-721). The leakage current can be reduced or even virtually eliminated through various solutions based on circuit topology, modulation, and passive or active common-mode filters. Some of the proposed inverter topologies are specifically designed to minimize CMV variations and leakage currents. For instance, midpoint clamp-based [27,32,59] and NPC-based [20,62] topologies only exhibit an LF CMV, which in turn creates small leakage currents due to the relatively small values of the parasitic capacitances. Another group of topologies that generate a small leakage current is constant CMV configuration, which generates a constant CMV at any output voltage level [36, 37, 114]. Furthermore, common-grounded (CG) inverters generate virtually zero CMV and very small leakage currents [23–25]. It should be noted that a common-mode or split filter is still

required for the constant CMV inverters. However, common-mode filtering might be omitted for midpoint clamp-based and CG-based inverters.

2.3.2 Non-Ideal Grids and Voltage Harmonics

The grid voltage in real-life conditions might be distorted with LF harmonics due to unbalanced loads, unbalanced faults, and non-linear loads such as diode-bridge rectifiers. In this case, a grid-connected inverter should be able to still inject a sinusoidal current into the distorted grid to comply with the grid codes and prevent detrimental effects on the grid [113, 115]. This can create some challenges in terms of grid synchronization and also current reference generation. Conventionally, a PLL is used to synchronize the inverter with the grid voltage and extract the amplitude and phase information. This information is usually required for generating the grid current reference [116]. It should be noted that it is possible to synchronize the inverter with the grid without using a PLL [117]. Nevertheless, non-ideal grid conditions such as high grid impedance (weak grid), voltage harmonics, and unbalanced voltages in three-phase systems can negatively impact the performance of the synchronization method and power quality of the system [118–120].

2.3.3 Scalability and Modular Structure

One of the desired practical features for industrial inverters for smart grids is having a modular structure. This helps to reach the required voltage/current/power levels without redesigning the whole system. Moreover, is more economical to use similar modules to build a wide range of different inverter systems. In this case, the whole manufacturing process for the modules can be extensively optimized [46]. In addition, a modular structure facilitates maintenance and repair procedures in large inverters. Cascading and paralleling converters are commonly used to achieve modular systems. In a cascaded approach, the power level can be increased by increasing the total output voltage through the series connection of the modules [46, 47]. However, this approach might require multiple DC sources and compensation for unbalanced DC voltages [121, 122]. Similarly, the parallel connection of the modules can be used to increase the power by upscaling the total current rating of the inverter [123].

On the other hand, the interleaving technique allows for increasing the effective number of output voltage levels by using the PS-PWM technique. This method can be applied to both cascaded and paralleled modular configurations [121, 123].

Another aspect of inverters with modular structures is the capability to operate under unbalanced voltage/current/power conditions. Through a proper control strategy, this feature can be leveraged to implement active thermal control methods and improve the reliability and lifetime of the whole inverter [124, 125].

2.3.4 Power Decoupling

The so-called power decoupling approaches, i.e., active (APD), or passive (PPD) are mandatory tasks for such a single-phase grid-tied system. Through the PPD solutions, the physical size of the passive elements, i.e., input boost inductor or DC-link electrolyte capacitor of the inverter stage, might be large and heavy, which in turn sacrifices the power density and reliability of the entire system [126–128]. On the contrary, the idea of APD control is to divert the LF ripple content of the input current of the front-end DC-DC bidirectional boost converter to another energy storage element, i.e., the DC-link capacitor voltage of the inverter stage [28, 129, 130]. Alternatively, an APD control can be implemented using a dedicated buffer converter inserted between the DC source and the inverter stage [131, 132], or integrated into the DC-DC front-end bidirectional boost converter [133]. In both cases, the size of the energy storage elements can be kept low, while a good trade-off between the overall efficiency and power density can be achieved. Nonetheless, the major drawback of implementing an APD is the requirement of another power processing stage, i.e., the dedicated DC-DC front-end boost converter or an additional/external buffer converter. This further hinders overall efficiency improvement of the whole system and can cause reliability and low power density issues [127, 128, 134].

Conversely, single-stage boost-integrated inverters have been recently put forward in which they can boost the DC input voltage and synthesize an AC voltage at the output simultaneously. As shown in Fig. 2.15, with the integration of an APD control, an efficient energy conversion process for both PV and EV grid-connected applications is achievable. The single-stage 2L converters proposed in [135–138], the single-stage three-level (3L) buck-boost inverter presented in [139], and the single-stage common-grounded 3L boost inverter proposed in [140] are some of the recently rehearsed ideas with the possibility of an integrated APD control. Even though they are using a low number of semiconductors, the output voltage of these single-stage inverters is only 2L or 3L, and their voltage boosting ability is limited within a certain range, while bidirectional power flow performance is not possible due to the presence of the diode in their circuit design. Moreover, within a single-stage control design, the presence of grid voltage harmonics, which is usual in many

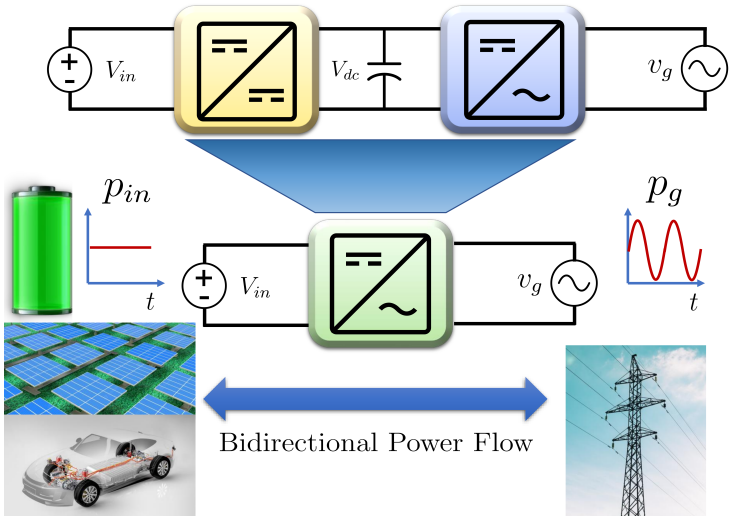


Fig. 2.15. The differences in energy conversion process between the conventional two-stage and boost-integrated single-stage DC-AC power converter architectures with APD control capability.

real applications, has not been adequately explored yet.

2.3.5 Single-Stage Dynamic Voltage Boosting and Bidirectional Power Flow

Power electronic converters with single power processing DC-AC stage have been recognized as efficient, compact, and attractive solutions during the latest years for the newly-developed renewable-energy (RE)-based systems [9]. This concept is motivated by targeting some shortcomings associated with the two-stage DC-AC converters, such as lower overall efficiency, larger number of required components, lower feasible range of output voltage gain, higher manufacturing cost, and lower overall power density [10, 11]. Considering the dynamic voltage gain of the commercially available two-stage DC-AC power conversion systems, the above-mentioned setbacks can be improved through the integration of the front-end DC-DC boost stage with a two or three-level (3L) voltage source inverter (VSI) [141–143].

The evolution process of these types of converters has been initiated by developing some single and three-phase circuit configurations such as the Z-source/quasi Z-source inverters (ZS/qZSIs) [19, 144], and the so-called split-source VSIs (SS-VSIs) [39, 145–149]. The inverter output voltage of the ZS/qZSIs [19,144] and SS-VSIs presented in [145,146] is a 2L waveform, while through the adjustment of the boost duty cycle, a flexible (dynamic) output

voltage gain can be achieved. In [145,146], some power diodes instead of active power switches are employed, which inhibits the bidirectional power flow operation, e.g., power conversion from the DC power source to the grid/load and vice versa. The improved versions of SS-VSIs presented in [147,148] only provide a 2L waveform but with a bidirectional power flow capability and the same overall voltage conversion gain as presented in [145,146]. The presented SS-VSIs in [149] and [39] are other recently developed topologies in this context, which can generate a 3L output voltage waveform with a bidirectional power flow feature using six and five power switches, respectively.

Alternatively, similar to [149] and [39], the SS-VSIs presented in [150,151] achieve single-stage power conversion as well, which helps to improve the power density and overall efficiency of the converter. However, all these SS-VSIs only offer a 2L or three-level (3L) output voltage waveform which results in a large AC filter or a degraded power quality. The low number of inverter output voltage levels, variable high-frequency CMV [152] with severe leakage current propagation issue for grid-connected PV applications, limited maximum practical output voltage gain [146], and significant voltage stresses across switches in the higher range of demanded boost gain are some associated shortcomings of these single-stage VSIs, which imbibe further attention for the future research development in this spot.

Hence, in the case of grid-tied inverters, a dedicated front-end DC-DC boost stage is usually needed to smooth the input current of such converters and to provide a dynamic voltage gain for the whole system. A 3L-CG-based VSI with virtually no leakage current propagation issue and dynamic output voltage gain has been recently introduced in [153, 154]. In this design, a single DC source is integrated into a single-stage DC-AC circuit configuration using five switches. By using only switches and the absence of diodes, such design broadens its applications since bidirectional power flow operation is made possible. This single-stage dynamic-boost CG-based VSI has further been developed in [155,156] to generate a 5L output voltage waveform, which results in reduced output filter size and better performance in terms of THD. The conceptualized approach in both [155] and [156] is based on maintaining the basic CG feature to alleviate the leakage current propagation issue using a dual T-type cell and two floating capacitors, but at the expense of additional power switches.

Furthermore, a dynamic voltage-boosting gain facilitates handling DC sources with wide-varying voltages (e.g., PV panels under changing irradiances), maximizing the modulation reference to generate the maximum number of voltage levels at the AC side and improving the power quality of the inverter. In addition, for battery-based systems, a bidirectional power flow is essential to charge and discharge the battery when required and handle its

voltage variations accordingly.

2.3.6 Research Gaps

Based on the conducted literature review, the following gaps have been identified:

- Only a few single-stage boost multilevel inverter topologies capable of generating more than three voltage levels have been found in the literature that can support APD feature. They are either SC-based topologies that suffer from the inrush charging currents, or MC-based that need extra voltage sensors for the DC-link voltage balancing and large DC-link capacitors in single-phase applications.

- The number, size, and cost of the required components of the available single-stage boost multilevel inverter topologies with integrated APD capability limit their utilization for cost-sensitive and residential applications. There is a potential for topologies with fewer components and similar functionalities and performance.

- No APD control strategy for single-stage 5L inverters has been found in the literature. The available solutions are only based on 2L or 3L topologies. Having a higher number of output voltage levels can potentially reduce the AC output filter size and improve the power efficiency and density.

- No APD control strategy for single-stage multilevel converters has been found that can maintain a flat DC input current and high AC power quality and low THD under distorted grid voltage with low-frequency harmonics. This is particularly important for practical applications, where the grid voltage is not purely sinusoidal and contains some harmonics.

- No APD control strategy for single-stage multilevel grid-connected converters has been found in the literature that can dynamically adjust the tradeoff between the voltage stress and the DC input current ripple without directly sensing or controlling the instantaneous capacitor voltage.

- The potential of interleaved multilevel converter structures as fully-modular grid-connected solutions has not been adequately studied in the literature and an in-depth and analytical analysis of the high-frequency input and output ripples is a critical yet mostly overlooked aspect in this category of multilevel converters.

Chapter 3

A Single-Source Single-Stage Switched-Boost Multilevel Inverter

This chapter presents a novel single-source single-stage switched-boost multilevel inverter with several derived extended topologies. Moreover, a modified non-linear PS-PWM is used to improve the dynamic voltage gain. This allows using wide-varying low-voltage DC sources such as batteries, fuel-cells, or PV panels interfaced to standard AC grids within a single power processing stage.

3.1 Introduction

Motivated by the importance of single-stage boost DC-AC converters with a multilevel output voltage waveform and reduced CMV/stress on devices, a new single-source single-stage switched-boost 5L (S^5B5L)-VSI is presented in this work. The proposed topology is comprised of nine power switches, a single inductor, and two self-balanced capacitors and offers the following features:

- Extended circuit capability with large dynamic voltage conversion gain over a wide range of DC input voltage variations.
- Lower number of required passive elements with a relatively small size in comparison to the recently developed boost-integrated inverters, which results in a compact design with high power density.
- Bidirectional power flow capability.

- Uniform and reduced value of the maximum voltage stress across all the switches.
- Reduced value of the CMV per each output voltage level, which is equal to one-quarter of the maximum inverter output voltage in a per-unit scale.
- Continuous and spike-free input current, which further enhances the range of its possible applications.
- Ability to be modulated with a hybrid PS-PWM technique. This enables the converter to double the effective switching frequency in the 5L inverter output voltage spectrum leading to higher quality output power with lower overall THD and filter-interface size.
- CG-based feature of the three-phase 3L circuit extension effectively eliminates the leakage current which is highly desirable in RE-based applications.

In the following sections, working principle, theoretical analysis, and simulation and experimental results of the proposed converter are provided.

3.2 Proposed S^{5}B5L-VSI

The overall structure of the proposed S^{5}B5L-VSI is illustrated in Fig. 3.1. As can be seen, the proposed topology is comprised of a single DC source with a fixed DC voltage, V_{dc}, that can be provided through any type of RE-based sources such as PV arrays or fuel cells, a single input inductor, L_{in}, and nine power switches configured as two differentially-connected quasi H-bridge (QHB) cells. Each of these QHB cells needs a floating capacitor, e.g., C_a, and C_b. A simple L-type filter split in two parts as $L_g/2$ in live and neutral sides of the grid is used as the grid interface. To convert V_{dc} to a boosted voltage across the capacitor of each QHB cell, S_1 is triggered by a high-frequency pulse with a DC (constant) duty cycle. Similar to the SS-VSIs, the voltage across both capacitors is balanced at the boosted voltage, $V_{C_a} = V_{C_b} = V_C = \frac{V_{dc}}{1-D}$, where D is the DC duty cycle of the switch S_1.

Considering V_C as the steady-state boosted voltage across the capacitors, three possible output voltage levels, e.g., $+V_C$, $-V_C$, and zero can be converted by each of the upper and lower sides of the proposed inverter. The 3L output voltages of the upper and lower QHB cells are named as v_a and v_b, respectively. Having taken the QHB cell A of the proposed S^{5}B5L-VSI with different switching status of the switch S_1, the list of ON switching states as

well as the status of L_{in} (charging or discharging) to generate a 3L output voltage waveform for v_a is tabulated in Table 3.1. As can be observed, L_{in} is regularly charged and discharged during the zero and $+V_{C_a}$ output voltage levels, while it has to be always charged during the conversion of $-V_{C_a}$ to the output voltage.

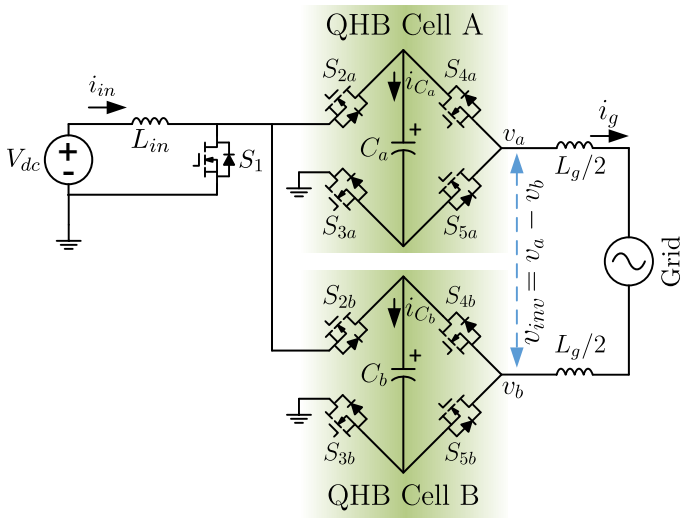


Fig. 3.1. The proposed S^{5}B5L-VSI.

Table 3.1
Switching states and corresponding output voltage generation in a QHB cell of S^{5}B5L-VSI.

Switching States	ON-State Switches	Input Inductor Status	v_a
1	S_1, S_{3a}, S_{4a}	Charging	$+V_{C_a}$
2	S_{2a}, S_{3a}, S_{4a}	Discharging	$+V_{C_a}$
3	S_1, S_{3a}, S_{5a}	Charging	0
4	S_{2a}, S_{3a}, S_{5a}	Discharging	0
5	S_1, S_{2a}, S_{5a}	Charging	$-V_{C_a}$

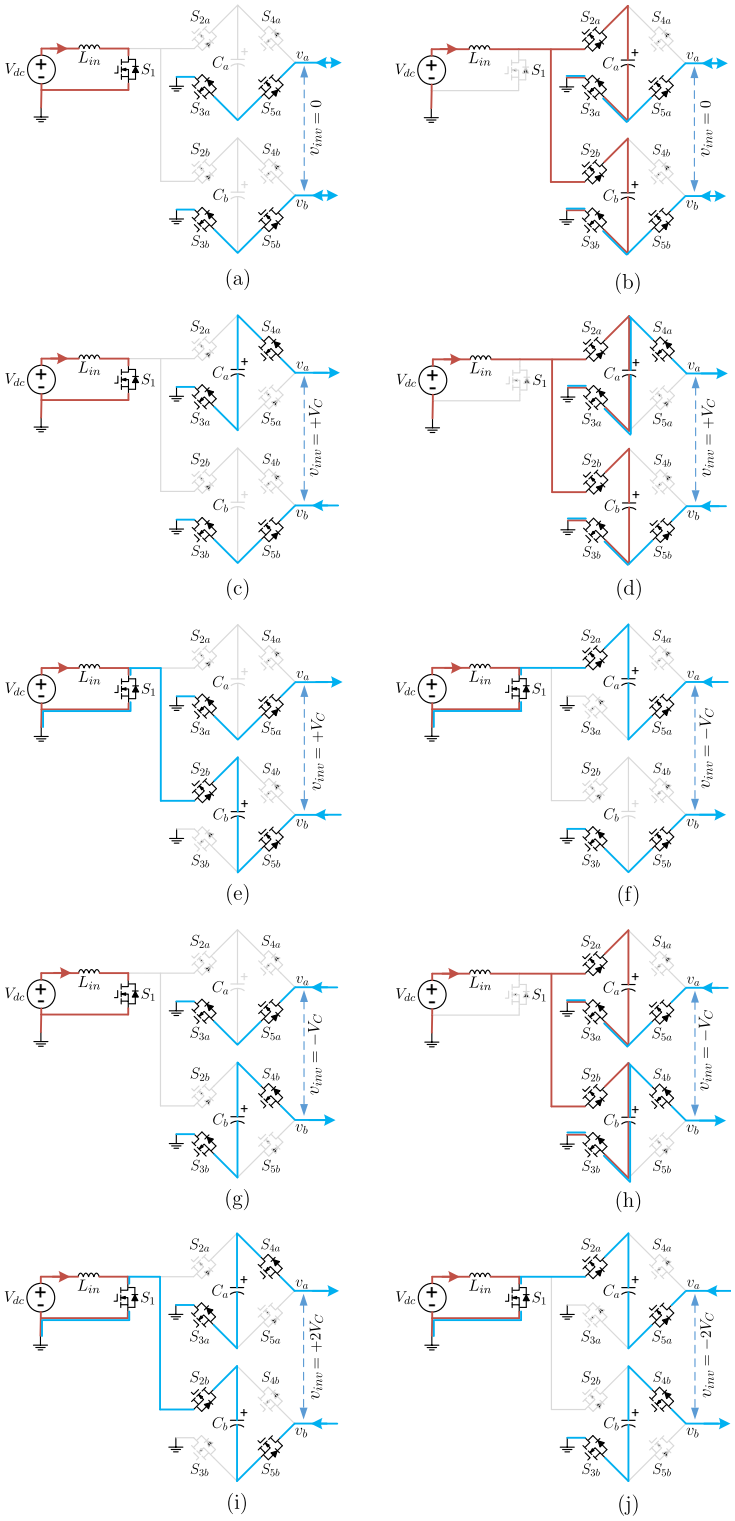


Fig. 3.2. Current flowing paths of the proposed S^{5}B5L-VSI at (a) $v_{inv} = 0$ (L_{in}: Charging), (b) $v_{inv} = 0$ (L_{in}: Discharging), (c),(e) $v_{inv} = +V_C$ (L_{in}: Charging), (d) $v_{inv} = +V_C$ (L_{in}: Discharging), (f),(g) $v_{inv} = -V_C$ (L_{in}: Charging), (h) $v_{inv} = -V_C$ (L_{in}: Discharging), (i) $v_{inv} = +2V_C$ (L_{in}: Charging), (j) $v_{inv} = -2V_C$ (L_{in}: Charging).

Table 3.2
Working principle of the proposed S^{5}B5L-VSI

Switching States	v_a	v_b	v_{inv}	v_{CM}
1	$+V_{C_a}$	$-V_{C_b}$	$V_{C_a} + V_{C_b} = 2V_C$	0
2	$+V_{C_a}$	0	$V_{C_a} = V_C$	$+V_C/2$
3	0	$-V_{C_b}$	$V_{C_b} = V_C$	$-V_C/2$
4	0	0	0	0
5	0	$+V_{C_b}$	$-V_{C_b} = -V_C$	$+V_C/2$
6	$-V_{C_a}$	0	$-V_{C_a} = -V_C$	$-V_C/2$
7	$-V_{C_a}$	$+V_{C_b}$	$-V_{C_a} - V_{C_b} = -2V_C$	0

The working principle of the entire system is shown in Table 3.2, while the current flowing paths of the proposed inverter at unity power factor in each of the switching states are shown in Fig. 3.2. Here, the charging/discharging currents of the boost inductor are highlighted in red, and the grid currents are shown with blue lines. It is worth mentioning that during the discharging period of L_{in}, the two capacitors will be connected in parallel with four power switches in the path. Although these switching states might cause additional current stress on the power components, the amplitude of the potential current spike in this case is limited through the path resistance, $4R_{ds(on)} + 2r_C$, where r_C is the ESR of the capacitors. Moreover, the high operating frequency limits the maximum instantaneous voltage difference between the two capacitors. Therefore, the circuit operation is not impacted significantly by the parallel connection of the capacitors in some of the switching states. It also is evident in the simulation and experimental results.

The instantaneous output voltage of the proposed inverter is $v_{inv} = v_a - v_b$. Hence, the possible values of the inverter output voltage can be listed as follows:

$$v_{inv} \in \{-2V_C, -V_C, 0, +V_C, +2V_C\}. \tag{3.1}$$

Similar to the performance of one QHB cell with the switch S_1, L_{in} can be charged or discharged when the converter is generating $-V_C$, 0, and $+V_C$ voltage levels. However, this is not possible for the case when $v_{inv} = \pm 2V_C$, since the switch S_1 has to remain in the ON state. In Table 3.2, the CMV instantaneous value, $v_{CM} = \frac{v_a + v_b}{2}$, has also been included, in which its peak value is varied within one-quarter of the peak inverter output voltage. This

can significantly alleviate the leakage current concern associated with some applications like grid-tied PV-integrated systems. Considering the split L-type filter used in the live and the neutral side of the grid, and regarding the high switching operation of the proposed converter, the impedance of the common-mode resonant path appearing between the grid and the DC input source can be increased sufficiently. Hence, with such an alleviated CMV and large common-mode impedance, the leakage current of the proposed topology can be reduced to an acceptable range [157].

The modulation scheme of the proposed S^{5}B5L-VSI is based on a modified PS-PWM technique to attain the maximum output voltage conversion gain for the fundamental component of the inverter output voltage. This type of modulation with the resultant gate switching pulses and the output voltage of each QHB cell are illustrated in Fig. 3.3. Here, an absolute function of a piece-wise sinusoidal reference, $d(t)$, is defined to be compared with two phase-shifted triangular carriers named as A_a and A_b. During a positive half-cycle, A_a and A_b are used to handle the upper and lower QHB cell switches, respectively. Conversely, in a negative half-cycle, this process is reversed. Therefore, A_a and A_b are used to commute the lower and upper QHB cell switches, respectively. Particularly, the switch S_1 is triggered with a constant DC duty cycle, D. This PWM pulse is achieved by comparing D with A_b. Moreover, the triggering pulses of S_{2a} and S_{2b} are obtained by comparing $d(t)$ and D with the carriers as they are involved in both voltage boosting and AC output voltage generation processes. The gate pulses of the rest of the switches are generated by comparing $d(t)$ with the carriers. As mentioned earlier, to generate output voltage levels $v_{inv} = \pm 2V_C$, switch S_1 must be ON. Hence, the maximum fundamental component of the proposed S^{5}B5L-VSI output voltage is expressed as follows:

$$V_{\max} = \left(\frac{1+D}{1-D}\right) V_{dc}. \tag{3.2}$$

From (3.2), the fundamental component of the desired output voltage can be found as:

$$v^{\star}_{ab}(t) = mV_{\max}\sin(\omega t) = V_{\max}u(t) \tag{3.3}$$

where, $m \in [0, 1]$ is the modulation index, ω is the fundamental angular frequency of the output voltage, and $u(t) \in [-1, 1]$ is the inverter voltage control signal in per-unit scale. Therefore, taking (3.2) and (3.3) into account,

$d(t)$ can be expressed via:

$$d(t) = \begin{cases} (1+D)\dfrac{u(t)}{2}, & u(t) \in [-\dfrac{2D}{1+D}, \dfrac{2D}{1+D}] \\ (1+D)u(t) - D, & u(t) \in (\dfrac{2D}{1+D}, 1] \\ (1+D)u(t) + D, & u(t) \in [-1, -\dfrac{2D}{1+D}). \end{cases} \tag{3.4}$$

The transition times, t_1-t_4, indicated in Fig. 3.3 can be defined as:

$$\begin{aligned} &d(t) > D, \ \forall t \in [t_1, t_2] \\ &d(t) < -D, \ \forall t \in [t_3, t_4]. \end{aligned} \tag{3.5}$$

Considering the steady-state operation, and with respect to (3.4)-(3.5), and Fig. 3.3, the transition switching time of t_1 over a full fundamental cycle, T, can be expressed as:

$$t_1 = \frac{1}{\omega} \arcsin\left(\frac{2D}{m(1+D)}\right). \tag{3.6}$$

From (3.6), other values of the switching transition times mentioned in (3.5) can be obtained, accordingly. As can be realized by (3.4) and Fig. 3.3, the AC reference of $d(t)$ has different amplitude characteristics over a full fundamental cycle. If the first function of this piece-wise waveform is used, the maximum value of the modulation index, m, has to be saturated at a lower value. This limitation comes from the fact that the switch S_1 must be ON when $v_{inv} = \pm 2V_C$. The major benefit of the modified version of the PS-PWM technique is the enhanced value of the output voltage gain, which is equal to:

$$G = m\left(\frac{1+D}{1-D}\right). \tag{3.7}$$

This feature is an extra benefit of the proposed structure rather than an inherent merit of the PS-PWM technique, which is related to the output voltage waveform with doubled effective switching frequency and enhanced capacitor voltage balancing. Considering the working principle of the proposed S^5B5L-VSI, the current and voltage stresses of the switches have been summarized in Table 3.3. Here, $i_{c,\max}$ is the maximum value of the current passing through each of the integrated capacitors, and I_m is the maximum

Table 3.3
Voltage and current stresses of the proposed S^{5}B5L-VSI

Switches	Maximum Voltage Stress	Maximum Current Stress
S_1	$\frac{V_{dc}}{1-D}$	$\approx 2i_{c,\max}$
S_{2a}, S_{2b}	$\frac{V_{dc}}{1-D}$	$\approx i_{c,\max}$
S_{3a}, S_{3b}	$\frac{V_{dc}}{1-D}$	$\approx i_{c,\max}$
S_{4a}, S_{4b}	$\frac{V_{dc}}{1-D}$	I_m
S_{5a}, S_{5b}	$\frac{V_{dc}}{1-D}$	I_m

value of the injected grid current. Considering the symmetrical structure of the proposed structure, $i_{c,\max}$ can be calculated as follows:

$$i_{c,\max} = \frac{i_{in,\max}}{2} = \frac{P_{in}}{2V_{dc}} + \frac{\Delta i_{LF,in}}{4} + \frac{\Delta i_{HF,in}}{4} \tag{3.8}$$

where, P_{in} is the average input power, $\Delta i_{LF,in}$ and $\Delta i_{HF,in}$ are the peak-peak low-frequency and high-frequency ripple components of i_{in}. The ripple components are studied in detail in Section 3.4. Furthermore, the maximum voltage stress of all the switches are uniform and equal to $v_{inv,\max}/2$ (0.5 in a per-unit scale). Also, excluding the switch S_1, the current stresses of four switches S_{2a}, S_{2b}, S_{3a}, and S_{3b} are equal to the current passing through the capacitors, $i_{c,\max}$. Through the remaining switches, circulates the injected grid current only. Hence, their maximum current stress is equal to I_m.

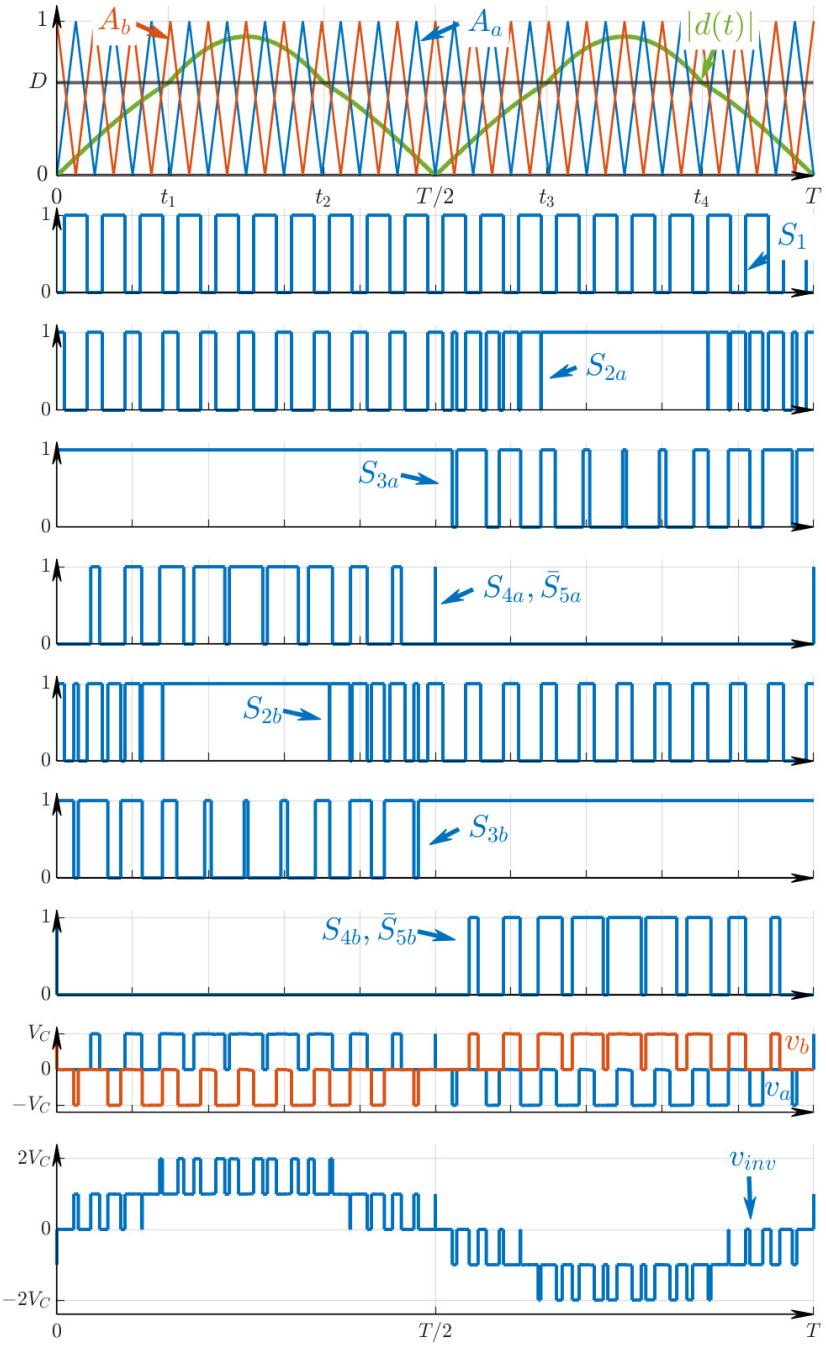


Fig. 3.3. Modified PS-PWM technique applied to the proposed S^{5}B5L-VSI with the gate switching pulses.

3.3 Topological Extensions

Through the described concept of the proposed S^5B5L-VSI, some topological extensions of the proposed inverter are presented in this section.

3.3.1 Three-Phase 3L Extension of the Proposed Topology

As shown in Fig. 3.4, the three-phase design of the proposed topology is formed based on three QHB cells. Similar to the basic concept, each of these QHB cells can make a 3L output voltage with respect to the ground, while the phase-to-phase voltages possess a 5L waveform with an integrated dynamic voltage-boosting feature. The total number of required semiconductor devices is 13 and the converter has been connected to the grid through three identical L-type filters. Compared with recently developed three-phase systems such as [150], the proposed topology offers a bidirectional power flow feature, and CG operation as well, while saving two switches as compared with [150]. Similar to the proposed S^5B5L-VSI, the switch S_1 is commuted based on a constant DC duty cycle, D, while the rest of the switches are triggered based on AC duty cycles, as explained in Section 3.2. Hence, the peak per-phase voltage of the converter is equal to $V_C = \frac{V_{dc}}{1-D}$, which is the boosted voltage across the involved capacitors of each phase.

The three-phase circuit extension of the proposed single-stage switched-boost VSI can be further compared with a two-stage bidirectional boost converter followed by a back-end 3L T-Type neutral point-clamped (NPC)-VSI or an Active NPC (ANPC)-VSI. These standard VSIs suffer from half DC-link voltage utilization. Hence, in the case of having a front-end DC-DC boost converter, their overall voltage conversion gain is limited to $\frac{0.5}{1-D}$. In contrast, the three-phase extension of the proposed topology offers a single-stage design with a voltage conversion gain of $\frac{D}{1-D}$. Moreover, the three-phase T-type NPC-VSI needs 14 power switches with non-uniform voltage stress and a relatively low value of the leakage current. Similarly, three-phase ANPC-VSI needs 20 power switches with non-uniform voltage stress. In contrast, the proposed topology needs 13 power switches and offers a CG feature per phase leading to a completely nullified leakage current value.

In general, any other 3L static-gain VSI needs a similar front-end DC-DC converter per phase to be cascaded as a three-phase circuit architecture, which could increase the size and overall cost of the entire system. Conversely, the proposed topology requires only a single boost inductor with three identical QHB cells to realize this feature.

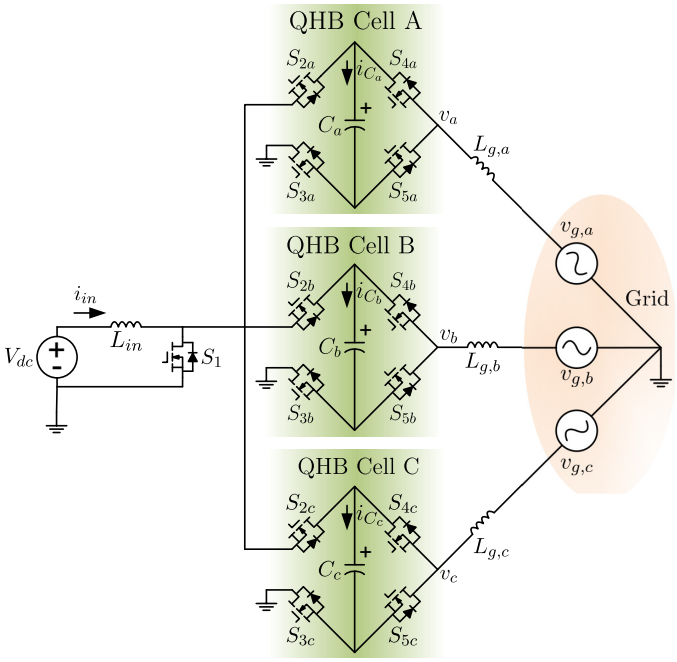


Fig. 3.4. Three-phase 3L extension of the proposed S^{5}B5L-VSI.

3.3.2 Extended 9L-FC-Based Variant of the Proposed Topology

Increasing the number of inverter output voltage levels is of interest for RE-based applications to further improve the quality of the injected grid current with a reduced output filter size. Each of the 3L output voltage waveforms (v_a and v_b) of the proposed S^{5}B5L-VSI can be enhanced to 5L when an extra FC cell is added at their output [158]. This extra FC cell includes two power switches and a floating capacitor. Following the same approach as given in the proposed S^{5}B5L-VSI, with the differential connection of upper and lower cells, a new variant of the proposed topology with nine output voltage levels is formed as shown in Fig. 3.5. The list of ON switching states of one module of this extended structure with the relevant status of L_{in}, FC condition, and its instantaneous output voltage are shown in Table 3.4. Here, the FC status is changed only in the middle output voltage levels in both half-cycles whilst the maximum output voltage of v_a and v_b is still equal to $V_C = \frac{V_{dc}}{1-D}$. Similar to the conventional FC-based VSIs, the FC voltages, $V_{C_{2a}}$ and $V_{C_{2b}}$ of this 9L variant of the proposed topology are balanced at the half value of $V_{C_{1a}}$ or $V_{C_{1b}}$ through the grid/load current without requiring an extra active balancing strategy. Hence, all the integrated capacitors are self-balanced.

Table 3.4
The list of ON switching states and the FC status of the 5L-CG-based VSI integrated into the 9L-FC-based variant of the proposed topology (↑: Charging, ↓: Discharging)

Switching States	ON-State Switches	FC Status	Inductor Status	v_a
1	S_1, S_{3a}, S_{4a}, S_{7a}	–	↑	$+V_{C_{1a}}$
2	S_{2a}, S_{3a}, S_{4a}, S_{5a}	–	↓	$+V_{C_{1a}}$
3	S_1, S_{3a}, S_{4a}, S_{6a}	↑	↑	$+0.5V_{C_{1a}}$
4	S_{2a}, S_{3a}, S_{4a}, S_{6a}	↑	↓	$+0.5V_{C_{1a}}$
5	S_1, S_{3a}, S_{5a}, S_{7a}	–	↑	0
6	S_{2a}, S_{3a}, S_{5a}, S_{7a}	–	↓	0
7	S_1, S_{3a}, S_{5a}, S_{6a}	↓	↑	$-0.5V_{C_{1a}}$
8	S_{2a}, S_{3a}, S_{5a}, S_{6a}	↓	↓	$-0.5V_{C_{1a}}$
9	S_1, S_{2a}, S_{5a}, S_{7a}	–	↓	$-V_{C_{1a}}$

The working principle of this 9L-FC-based variant of the proposed topology is summarized in Table 3.5. Here, the balanced voltage across both capacitors in QHB cells is the same and equal to the boosted voltage, i.e., $V_C = V_{C_{1a}} = V_{C_{1b}}$. It should be mentioned that except the $\pm 2V_C$ output voltage levels, all the middle levels can be generated through at least two redundant states.

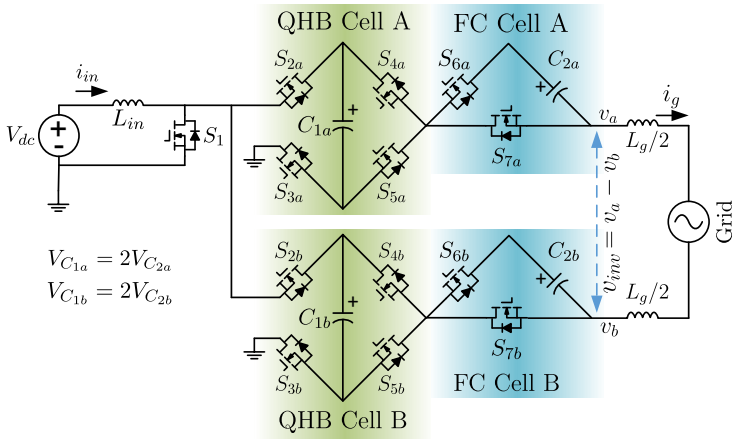


Fig. 3.5. The 9L circuit extension of the proposed topology.

Table 3.5
Switching state and corresponding output voltage of the 9L-FC-based variant of the proposed topology considering $V_{C_{1a}} = V_{C_{1b}} = V_C$

Switching States	v_a	v_b	v_{inv}
1	$+V_C$	$-V_C$	$2V_C$
2	$+V_C$	$-0.5V_C$	$1.5V_C$
3	$+0.5V_C$	$-V_C$	$1.5V_C$
4	$+V_C$	0	V_C
5	0	$-V_C$	V_C
6	0	$-0.5V_C$	$0.5V_C$
7	$+0.5V_C$	0	$0.5V_C$
8	0	0	0
9	$+V_C$	$+V_C$	0
10	$-V_C$	$-V_C$	0
11	$-0.5V_C$	0	$-0.5V_C$
12	$-V_C$	$+0.5V_C$	$-0.5V_C$
13	$-V_C$	0	$-V_C$
14	0	$+V_C$	$-V_C$
15	$-V_C$	$+0.5V_C$	$-1.5V_C$
16	$-0.5V_C$	$+V_C$	$-1.5V_C$
17	$-V_C$	$-V_C$	$-2V_C$

3.4 Passive Elements Design Guidelines and Power Loss Analysis

To further investigate the characteristics and circuit features of the proposed S^{5}B5L-VSI, some guidelines related to the passive elements design associated with the power loss analysis are presented in the following subsections.

3.4.1 Passive Elements Design Guidelines

The required value of L_{in} in the proposed S^{5}B5L-VSI directly depends on the input current, i_{in}, and its associated permissible ripple at different values of the integrated SB module duty cycle [159]. Similar to any single-phase grid-tied TL-inverter, i_{in} contains both low- (double-line) and high- (switching) frequency ripples. The low-frequency ripple of i_{in} can also be related to double-line ripple component of the steady state ripple voltage across C_a, and

C_b. To estimate the low-frequency ripples of these variables, an ac equivalent circuit of the proposed converter using its averaged model is extracted [160]. Therefore, considering the peak value of the injected grid current at the unity power factor condition, the following expressions as for the low-frequency ripple values of v_C and i_{in} in the steady-state can be obtained:

$$\Delta v_{LF,C} = \frac{2V_m I_m}{V_{dc}} \frac{2\omega L_{in}}{|1 - \frac{8L_{in}C\omega^2}{(1-D)^2}|} \tag{3.9}$$

$$\Delta i_{LF,in} = \frac{2V_m I_m}{V_{dc}(1-D)} \frac{1}{|1 - \frac{8L_{in}C\omega^2}{(1-D)^2}|} \tag{3.10}$$

where C is the capacitance of C_a and C_b, V_m and I_m are the peak values of the grid voltage and current, respectively.

On the other hand, the high-frequency ripple component of v_C and i_{in} in the steady-state can also be developed as follows, respectively [159]:

$$\Delta v_{HF,C} = \frac{D(1-D)i_{in,\max}}{2Cf_{sw}} \tag{3.11}$$

$$\Delta i_{HF,in} = \frac{DV_{dc}}{L_{in}f_{sw}} \tag{3.12}$$

where f_{sw} represents the switching frequency of the proposed converter and $i_{in,\max}$ is introduced in (3.8).

To better reflect the above-mentioned design guidance principles as for the single-phase operation of the proposed S^5B5L-VSI aiming to inject 3 kW power to the standard 50-Hz grid, a 400 V peak fundamental AC voltage is considered for the 5L output voltage of the inverter. Hence, regarding (3.2), the relationship between D and the DC input voltage, V_{dc} can be found as follows:

$$D = \frac{400 - V_{dc}}{400 + V_{dc}}. \tag{3.13}$$

Replacing (3.13) into (3.9)-(3.12) and concerning a 100 kHz switching frequency for a compact SiC-based design, the relationship between V_{dc}, L_{in}, and the required capacitance of the capacitors is obtained as Fig 3.6(a) and Fig 3.6(b), for a 3 kW and a 5 kW system, respectively. Here, it is assumed to have an identical capacitance for both C_a, and C_b, while a 10% allowable low-frequency ripple for their balanced voltage has been considered. From Fig 3.6(a), it can be seen that for the low available DC input voltage, the capacitors can be chosen with less than 100 μF capacitance, and the value of L_{in} can be designed around 100 μH to 200 μH range for a 3 kW grid-connected condition. Similarly, as shown in Fig 3.6(b) for a 5 kW system,

the capacitors can be chosen with less than 100 μF capacitance, and the value of L_{in} can be designed around 80 μH to 100 μH. Regarding this and as opposed to many recently-developed single-stage boost-integrated or SC-based multilevel inverters topologies, film capacitors with long lifespan and reliable performance can be adopted in the design, while the overall weight and size of the system can be kept low with such a small value of the passive components. Considering Fig. 3.6 and as for higher values of the DC input voltage, the involved capacitors can still be chosen small, while to have a continuous input current performance, which is crucial for grid-tied PV applications, larger values of L_{in} can be used.

In addition, the required passive elements values can be expressed in a per-unit (p.u.) frame for an easier comparison to other systems. To do this, a base voltage of $V_{base} = 220$ V RMS has been considered. Therefore, the base current for 3 kW and 5 kW systems can be calculated as $I_{base,3kW} = 3kVA/V_{base} \approx 13.64$ A RMS and $I_{base,5kW} = 5kVA/V_{base} \approx 22.73$ A RMS, respectively. Next, the base impedances can be obtained as $Z_{base,3kW} = V_{base}/I_{base,3kW} \approx 16.13\ \Omega$ and $Z_{base,5kW} = V_{base}/I_{base,5kW} \approx 9.68\ \Omega$. Considering a standard 50 Hz grid fundamental frequency, the impedances of the passive elements can be calculated and their p.u. values can be expressed as $Z_{p.u.} = Z/Z_{base}$. Therefore, the selected p.u. impedances for a 3 kW system are $Z_{C_a}, Z_{C_b} > 1.97$ p.u. and 0.0019 p.u.$< Z_{L_{in}} <$ 0.0039 p.u.. Similarly, for a 5 kW system the p.u. impedances can be selected as $Z_{C_a}, Z_{C_b} > 1.97$ p.u. and 0.0016 p.u.$< Z_{L_{in}} <$ 0.0019 p.u.. Furthermore, inductance and capacitance base values can be defined as:

$$L_{base} = \frac{V_{base}^2}{\omega S_{base}} \tag{3.14}$$

$$C_{base} = \frac{S_{base}}{\omega V_{base}^2} \tag{3.15}$$

where S_{base} is the base apparent power. Therefore the passive element values can be expressed in p.u. values. For a 3 kW system are $C_a, C_b < 0.507$ p.u. and 0.0019 p.u.$< L_{in} <$ 0.0039 p.u.. Similarly, for a 5 kW system the p.u. impedances can be selected as $C_a, C_b < 0.507$ p.u. and 0.0016 p.u.$< L_{in} <$ 0.0019 p.u..

It should be noted that a comprehensive comparison has been performed based on the core module (QHB) of the S^5B5L-VSI under the same operating conditions and switching frequency. This comparison can be found in Subsection 6.5 of this thesis.

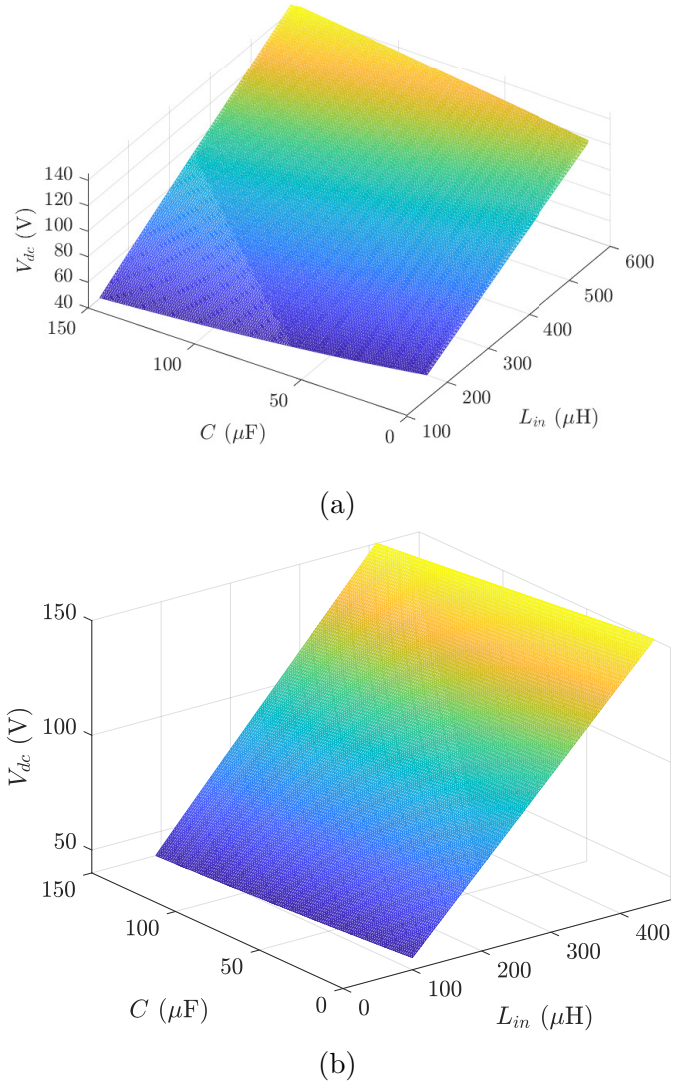


Fig. 3.6. Boundary values of input inductor and module capacitors for 10% ripple on the capacitor voltages at: (a) $P = 3$ kW; (b) $P = 5$ kW.

3.4.2 Power Loss Analysis

The power losses of the proposed S^{5}B5L-VSI include the switching and conduction losses of the power switches, the losses of the input and filter inductors, and the conduction losses of the capacitors. The switching losses of the power switches are comprised of the turn-on and turn-off losses expressed

Table 3.6
Instantaneous switching frequency of the gate signals of the proposed S^5B5L-VSI.

$d(t)$	$[0, D)$	$[D, 1]$	$(-D, 0)$	$[-1, -D]$
f_{S_1}	f_{sw}	f_{sw}	f_{sw}	f_{sw}
$f_{S_{2a}}$	f_{sw}	f_{sw}	$2f_{sw}$	0
$f_{S_{2b}}$	$2f_{sw}$	0	f_{sw}	f_{sw}
$f_{S_{3a}}$	0	0	f_{sw}	f_{sw}
$f_{S_{3b}}$	f_{sw}	f_{sw}	0	0
$f_{S_{4a}}, f_{S_{5a}}$	f_{sw}	f_{sw}	0	0
$f_{S_{4b}}, f_{S_{5b}}$	0	0	f_{sw}	f_{sw}

as [161]:

$$P_{S_i,on} = \frac{1}{T}\int_0^T E_{on}\big(v_{S_i,on}(t), i_{S_i,on}(t)\big) f_{S_i}(t)\, dt \tag{3.16}$$

$$P_{S_i,off} = \frac{1}{T}\int_0^T E_{off}\big(v_{S_i,off}(t), i_{S_i,off}(t)\big) f_{S_i}(t)\, dt \tag{3.17}$$

where $P_{S_i,on}$ and $E_{on}\big(v_{S_i,on}(t), i_{S_i,on}(t)\big)$ are the average turn-on power loss, and the turn-on switching energy of the ith switch, respectively. Moreover, $f_{S_i}(t)$ is the instantaneous switching frequency of the ith switch, and T is the fundamental period of the grid voltage. Similarly, $P_{S_i,off}$, and $E_{off}\big(v_{S_i,off}(t), i_{S_i,off}(t)\big)$ are the average turn-off power loss and turn-off switching energy of the ith switch, respectively. Additionally, $v_{S_i,on}(t), i_{S_i,on}(t)$ and $v_{S_i,off}(t), i_{S_i,off}(t)$ are the switch voltage and current at turn-on and turn-off instants, respectively. The values of the switching transition voltages and currents are shown in Table 3.7. Moreover, due to the inherent capacitor voltage balancing feature of the proposed topology, the voltage of both capacitors are considered to be equal in this section ($v_{C_a} = v_{C_b} = v_C$). The details of switching energies can be found in the MOSFET datasheet or in thermal models provided by the manufacturers. Considering the modified PS-PWM described in Section 3.2, the instantaneous switching frequency of each switch over a fundamental period, T, is summarized in Table 3.6.

The conduction losses of the power switches can be calculated as:

$$P_{S_i,cond} = \frac{1}{T}\int_0^T v_{S_i}(t) i_{S_i}(t)\, dt \tag{3.18}$$

where $P_{S_i,cond}$ is the average conduction power loss of the ith switch, and $v_{S_i}(t)$ and $i_{S_i}(t)$ are the switch voltage and current, respectively.

Table 3.7
Turn-on and turn-off voltages and currents of the switches in the proposed S^{5}B5L-VSI.

$v_{S_i,on}, v_{S_i,off} \approx \langle v_C \rangle$ $i_{S_1,on}$=$\langle i_{in} \rangle - \Delta i_{HF,in}/2$ $i_{S_1,off}$=$\langle i_{in} \rangle + \Delta i_{HF,in}/2$			
v_a	0	$+V_C$	$-V_C$
$i_{S_{2a},on}$	$-i_{S_1,off}$	$-i_{S_1,off}$	$-\langle i_g \rangle$
$i_{S_{2a},off}$	$-i_{S_1,on}$	$-i_{S_1,on}$	$-\langle i_g \rangle$
$i_{S_{3a},on}, i_{S_{3a},off}$	$\langle i_g \rangle$	$\langle i_g \rangle$	–
$i_{S_{4a},on}, i_{S_{4a},off}$	–	$\langle i_g \rangle$	–
$i_{S_{5a},on}, i_{S_{5a},off}$	$-\langle i_g \rangle$	–	$-\langle i_g \rangle$
v_b	0	$+V_C$	$-V_C$
$i_{S_{2b},on}$	$-i_{S_1,off}$	$-i_{S_1,off}$	$\langle i_g \rangle$
$i_{S_{2b},off}$	$-i_{S_1,on}$	$-i_{S_1,on}$	$\langle i_g \rangle$
$i_{S_{3b},on}, i_{S_{3b},off}$	$-\langle i_g \rangle$	$-\langle i_g \rangle$	–
$i_{S_{4b},on}, i_{S_{4b},off}$	–	$-\langle i_g \rangle$	–
$i_{S_{5b},on}, i_{S_{5b},off}$	$\langle i_g \rangle$	–	$\langle i_g \rangle$

The losses associated with L_{in} and L_g can be expressed as [157]:

$$P_{L_g} = I_{g,rms}^2 r_{L_g} + k_1 f_{sw}^{\alpha_1} B_g^{\beta_1} W_1 \times 10^{-3} \tag{3.19}$$

$$P_{L_{in}} = I_{in,rms}^2 r_{L_{in}} + k_2 f_{sw}^{\alpha_2} B_{in}^{\beta_2} W_2 \times 10^{-3} \tag{3.20}$$

where $I_{g,rms}$ and $I_{in,rms}$ are the grid and input RMS currents, r_{L_g} and $r_{L_{in}}$ are the ESR of L_g and L_{in}, B_g and B_{in} are the magnetic flux density of L_g and L_{in}, k_1,α_1,β_1 and k_2,α_2,β_2 are the core loss coefficients of the inductors, and W_1,W_2 are the core weights in grams. Here, at the rated output power, the dominant components of the i_g and i_{in} in the frequency spectrum are concentrated at the low-frequency side (i.e., DC-300 Hz). Therefore, the core losses are small compared to the conduction losses.

The conduction losses associated with the capacitors can be obtained as follows:

$$P_C = P_{C_a} + P_{C_b} = 2I_{C,rms}^2 r_C \tag{3.21}$$

where $I_{C,rms}$ is the RMS current of C_a or C_b, r_C is the ESR of the capacitors. It should be noted that due to the symmetrical structure of the proposed converter and the modified PS-PWM technique, the RMS currents of both capacitors are equal.

Finally, the total power loss can be calculated as:

$$P_{loss} = \sum_{i}(P_{S_i,on} + P_{S_i,off} + P_{S_i,cond}) + P_{L_g} + P_{L_{in}} + P_C \tag{3.22}$$

The governing differential equations of the proposed inverter have been derived using the averaging technique as below:

$$\begin{aligned} \frac{d\langle i_{in}\rangle}{dt} &= \frac{D-1}{L_{in}}\langle v_C\rangle + \frac{V_{dc}}{Lin} \\ \frac{d\langle v_C\rangle}{dt} &= \frac{1-D}{2C}\langle i_{in}\rangle - \frac{u(t)}{2C}\langle i_g\rangle \\ \frac{d\langle i_g\rangle}{dt} &= \frac{(1+D)u(t)}{L_g}\langle v_C\rangle - \frac{v_g(t)}{L_g} \end{aligned} \tag{3.23}$$

where $< \cdot >$ is used to denote the average values of the respective variables in a switching period. Considering the non-linear governing equations of the proposed S^{5}B5L-VSI, a simulation-based numerical method using PLECS software has been chosen for estimating the power losses more accurately. The detailed calculated loss breakdown can be found in Section 3.7.

3.5 Comparative Study

To show the main differences and circuit potentiality of the proposed S^{5}B5L-VSI with respect to some recently proposed single-stage SB and SC-based VSIs, a comparative study is conducted in this section. As stated earlier, one of the main features of the proposed S^{5}B5L-VSI introduced in Fig. 3.1 is the higher dynamic voltage boosting capability over a wide range of DC duty cycles. Fig. 3.7 highlights this feature by presenting the voltage conversion gain versus the DC duty cycle, D, for several VSIs. The relationship between the overall voltage conversion gain and the DC duty cycle of different well-known single-phase boost-based structures such as single-stage 3L-ZS/qZSI [19], single-stage 3L-SS-VSIs [39, 145–149], the cascaded-boost 5L-VSI [67], and the two-stage 5L-active neutral-point-clamped (ANPC) inverter with a front-end DC-DC boost converter have been highlighted in Fig. 3.7. As can be seen, although ZS/qZSIs offer a higher gain compared to the proposed S^{5}B5L-VSI, they have a theoretical 50% duty cycle limitation and can generate only 2L or 3L output voltage waveforms. In contrast, the proposed S^{5}B5L-VSI with its modified PS-PWM switching scheme has a comparable gain at the higher range of DC duty cycles. It needs only a single

inductor and two self-balanced capacitors with a voltage rating equal to half of the inverter output voltage, while this voltage stress on integrated passive elements of ZS/qZSIs is significantly higher. Because of this low voltage stress on passive elements and due to the larger number of output voltage levels generation with a PS-PWM technique, relatively smaller passive elements are needed for the proposed S^5B5L-VSI. Furthermore, the magnetic element design challenges, excessive gain sensitivity to the shoot-through duty cycle, and steep power efficiency drop at higher voltage gains are the major drawbacks of ZS/qZSIs [162, 163].

Table 3.8 compares the required circuit components and the overall performance of different recently introduced single-source 5L-VSIs with the proposed S^5B5L-VSI. Here, the 5L-VSIs presented in [157,164–166] are all based on SC-technique with static voltage conversion gain, while the rest of the considered topologies are based on single-stage dynamic voltage conversion gain. In this table, the circuit characteristics of the standard 5L-ANPC inverter followed by a front-end bidirectional DC-DC boost converter as a two-stage system have also been included. The comparative items in this table are the number of required active and passive devices (switches (S), gate drivers (G), diodes (D), capacitors (C), and inductors (L)), the value of the voltage conversion gain, the maximum per-unit value of the blocking voltage across the switches, the nature of DC input current drawn from the DC source, capacitor voltage self-balancing, bidirectional operation, circuit extension capability, type of PWM technique, and the reported efficiency at the rated power. As can be realized from Table 3.8, the proposed S^5B5L-VSI offers many benefits in terms of the reduced number of switching devices, uniform maximum voltage stresses across the switches, bidirectional power flow operation, and the extension capability with the PS-PWM technique. The importance of the PS-PWM technique shows its main feature in increasing the apparent switching frequency. Therefore, at the same carrier frequency, the apparent output switching frequency of the 5L converters modulated with the PS-PWM technique is two times larger than the ones triggered with the LS-PWM technique. Although the recently developed 5L-CG-based VSI in [158] requires fewer switches compared with the proposed topology, its maximum output voltage gain is half of the proposed S^5B5L-VSI. Hence, it needs some power switches with a larger blocking voltage. These features make the proposed topology and its extended circuit configurations an attractive choice for many RE-based grid-connected applications.

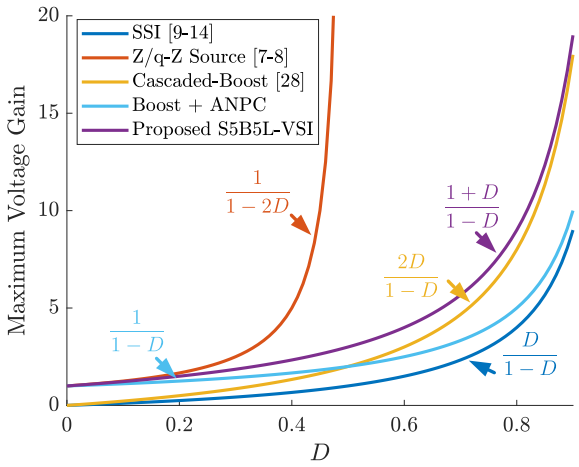


Fig. 3.7. Comparative output voltage gain curves of SSI, Z/q-Z source, cascaded boost, double-stage boost+ANPC, and the proposed inverter.

Table 3.8
A comparison between the proposed S^5B5L-VSI and the other single-source single-phase 5L-based VSIs.

Type of Converter	No. of Components				Voltage Gain	Voltage Stress Max. (p.u.) /Uniform	Input Current Nature	Bidirectional/ Caps Self Balancing	Extension Capability/ Modulation	Reported Efficiency
	S(G)	D	C	L						
CGSC-VSI [164]	8 (8)	1	2	0	2	1/NO	Discontinuous	NO/YES	NO/LS	NA
SC-VSI [165]	10(9)	0	1	0	2	1/NO	Discontinuous	YES/YES	NO/LS	NA
ABNPC-VSI [166]	8 (8)	0	3	0	1	1/NO	Discontinuous	YES/YES	NO/LS	98.3%@3kW
ABNPC-VSI [167]	12 (11)	0	4	2	2	1.5/NO	Semi-Continuous	YES/YES	NO/LS	97.5%@160W
CG-VSI [155]	10 (8)	0	2	1	$\frac{2D}{1-D}$	1/NO	Semi-Continuous	NO/NO	NO/LS	98%@1kW
CG-VSI [156]	14 (10)	0	2	1	$\frac{2D}{1-D}$	1/NO	Semi-Continuous	YES/YES	NO/LS	NA
CG-VSI [158]	7 (7)	0	2	1	$\frac{D}{1-D}$	1/NO	Continuous	NG/YES	NO/LS	95%@1kW
CG-VSI [168]	9 (8)	0	2	1	$\frac{D}{1-D}$	1/NO	Continuous	NG/YES	NO/LS	96%@1.5kW
Cascaded-Boost-VSI [67]	10 (10)	0	2	2	$\frac{2D}{1-D}$	0.5/YES	Continuous	YES/YES	NG/PS	97.3%@1kW
Boost with ANPC-VSI	10 (10)	0	4	1	$\frac{1}{1-D}$	2/YES	Continuous	YES/YES	NO/PS	NA
Proposed S^5B5L-VSI	9 (9)	0	2	1	$\frac{(1+D)}{1-D}$	0.5/YES	Continuous	YES/YES	YES/PS	96.1%@3kW

NG: Not Given NA: Not Available LS: Level-Shifted PS: Phase-Shifted G: Gate Drivers

3.6 Control Strategy

In this section, a closed-loop control strategy is presented to govern the system to inject active and reactive power into a standard grid under an ideal and harmonic-free grid voltage condition. This is achieved by obtaining the AC reference u from the output of a PR controller tuned at the expected grid fundamental frequency, as shown in Fig. 3.8. Here, a simple PLL is used to detect the fundamental phase and amplitude of the grid voltage, i.e., ωt and V_m. Then through the current reference generation stage and the desired active and reactive power references, $P_g^\star$ and $Q_g^\star$, a grid current reference, $i_g^\star$, is generated. As for an available DC input voltage, an appropriate value of boost duty cycle D is also defined based on the peak grid voltage, (3.3), and (3.2) to inject the power into the grid. In Fig. 3.8, $G_{ac}(s)$ is a first-order system plant based on the ESR and inductance of the grid-interface filter, describing the relationship between grid current, i_g, and the voltage across the grid-interface filter, v_{L_g}, in the frequency domain. Moreover, in this control strategy, the grid voltage, v_g, acts as an input disturbance for the PR controller, which can be rejected by the PR controller tuned at the fundamental frequency of the grid [80]. Through this control design, the injected current is controlled; however, the input current contains a dominant double-line frequency ripple component that can be alleviated using available power decoupling methods. This issue will be thoroughly investigated in the subsequent chapters of this thesis.

3.7 Simulation and Experimental Results

To further evaluate the performance of the proposed S^5B5L-VSI topology (Fig. 3.1) and its three-phase circuit extension (Fig. 3.4), simulation and experimental results are presented in this section. The simulation results are conducted in PLECS environment, while the experimental results are captured based on a 3 kW laboratory-built prototype shown in Fig. 3.9. The passive elements of the proposed topology in both the simulation and experimental studies are chosen based on the design guidelines presented in Section 3.4. The simulation parameters and the prototype specifications are tabulated in Table 3.9. The verification results are discussed in the following subsections. It should be noted that in both simulation and experimental case studies, the operation of the proposed converter has been studied over a large input voltage variation (more than 50%), to emulate real-life conditions such as partial shading in PV systems, or battery state of charge and temperature variations.

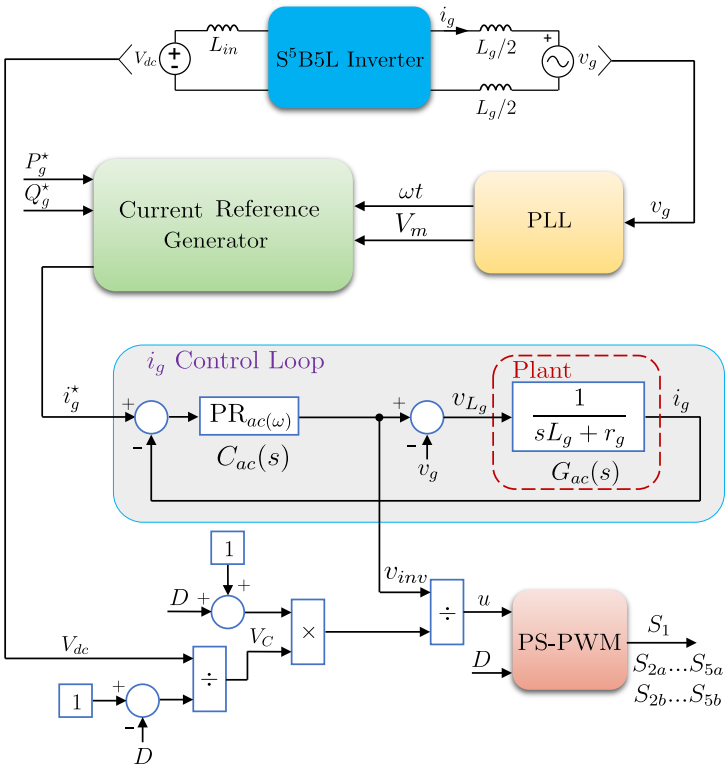


Fig. 3.8. Control block diagram for the proposed S^{5}B5L-VSI.

Table 3.9
Parameters used for the experimental prototype

Element	Type and Description
Power Switches	UJ4C075018K4S (750 V, 18 mΩ)
Controller	DSP-TMS320F28379D (TI LaunchPad 379D)
Switching Frequency	100 kHz
C_a, C_b, r_C	75 µF (0.380 p.u.), 3 mΩ (Film)
L_{in}, $r_{L_{in}}$	0.15 mH (0.0029 p.u.), 16 mΩ
L_g, r_{L_g}	0.6 mH (0.0117 p.u.), 28 mΩ
Gate Drivers	UCC21710 (with Overcurrent Protection)
Isolated DC-DC Converters	MGJ2D121505SC (12V In, +15V,-5V Out)

3.7.1 Simulation Results

A grid-connected system is chosen to perform the simulation, where the grid voltage amplitude and frequency are 311 V peak, and 50 Hz, respectively.

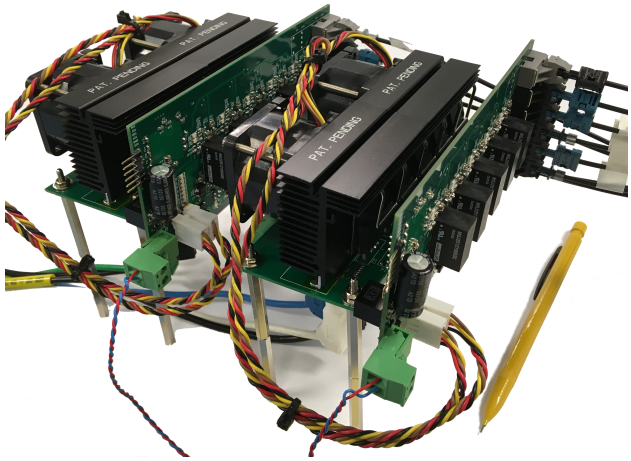


Fig. 3.9. A picture of the 3 kW experimental prototype.

Since the capacitors of the proposed S^5B5L-VSI are self-balanced, a simple PR controller is used to govern the system for injecting the power to the grid with a zero steady-state error [169], as shown in Fig. 3.8. Regarding this, a reference current with the peak value of 10 A is set for the simulations, which results in a 1.5 kW injected power into the grid. The gate switching pulses are provided based on the described PS-PWM technique with a 100 kHz switching frequency.

Fig. 3.10(a)-(f) show the details of the simulation results for two different values of D, and V_{dc}. In the first scenario, the input voltage is set at 100 V. Hence, to meet the grid peak amplitude requirement, a DC duty cycle of D = 0.55 is considered. The resultant 5L inverter output voltage waveform, the injected grid current, input current, voltage stress across the switches, capacitor voltages, current stress of the switches, and the current passing through the capacitors are shown in Fig. 3.10(a)-(c). Regarding the symmetry of the proposed S^5B5L-VSI, only the voltage and current stresses of one of the integrated QHB cells, i.e., QHB cell A, have been shown in these results. Conversely, to show the voltage-boosting capability of the proposed S^5B5L-VSI, another test with the input voltage of 55 V, and DC duty cycle of D = 0.75 is conducted. The related simulation waveforms of this case study have also been illustrated in Fig. 3.10(d)-(f). As can be observed from both above-mentioned case studies, due to the dynamic voltage conversion gain of the proposed topology, the maximum output voltage of the inverter is 400 V and the capacitor voltages are balanced at 200 V. The maximum voltage stress of the switches are equal to half of the maximum inverter output voltage, which is in agreement with the theory. The maximum current stress

belongs to the Switch S_1, which should handle approximately twice the current passing through each capacitor. The input current waveforms in both case studies confirm the fact that the grid-tied operation of the converter is feasible without inducing any large discontinuous inrush spike.

Regarding the capacitance mismatch between the two capacitors, a series of simulations have been conducted to investigate the effect of unequal capacitance due to the manufacturing tolerance on the performance of the proposed converter. Considering a $\pm 20\%$ tolerance for the capacitor values, as a worst-case scenario, the capacitance of C_a has been set to $1.2C$ and C_b has been set to $0.8C$. Compared to the ideal case with equal capacitor values, the RMS current passing through C_a was changed from 11.97 A to 11.94 A and the RMS current of C_b was changed from 11.97 A to 12.05 A. Moreover, the output current waveform and output power quality was unchanged.

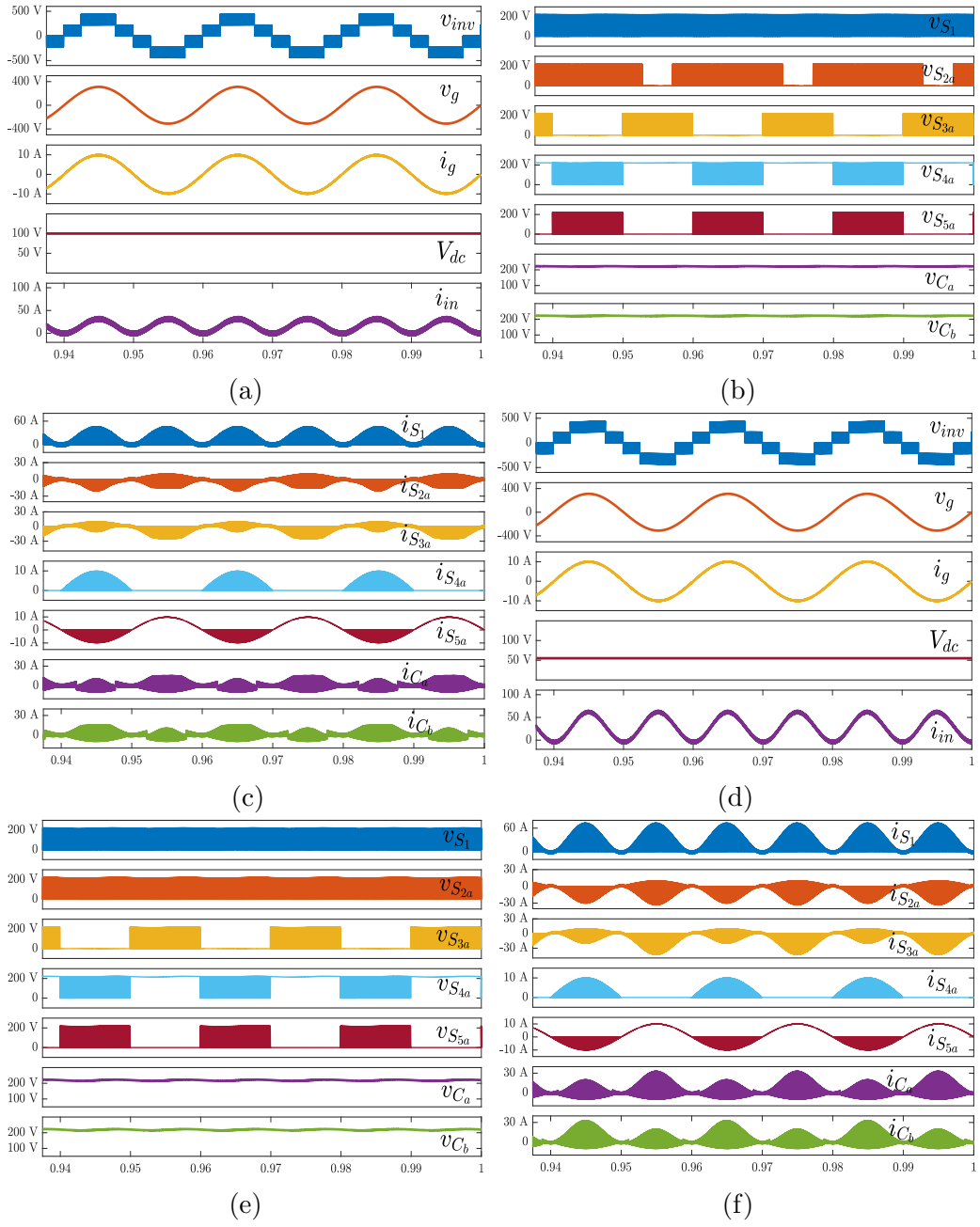


Fig. 3.10. Simulation results using PLECS: (a) the 5L output voltage of the proposed S^{5}B5L-inverter, grid-voltage, grid current, input voltage, and input current at $D = 0.55$; (b) the voltage stress of the switches and the voltage across the capacitors at $D = 0.55$; (c) the current stress profile of the switches at $D = 0.55$; (d) the 5L output voltage of the proposed S^{5}B5L-inverter, grid-voltage, grid current, input voltage, and input current at $D = 0.75$; (e) the voltage stress of the switches and the voltage across the capacitors at $D = 0.75$; (f) the current stress profile of switches at $D = 0.75$.

3.7.2 Experimental Results

For the experimental verification, two different cases studies for an open-loop RL load and a closed-loop grid-tied operation are considered. The experimental results are taken for both single and three-phase variants of the proposed topology (Fig. 3.1 and Fig. 3.4). The input DC power supply is provided through a PV emulator (EA-PSI-9750-12). A DSP (TMS320F28379D) is utilized to generate the required PWM pulses at 100 kHz. A four-quadrant grid-simulator (REGATRON TC30.528.43-ACS) is also used to perform the closed-loop grid-connected tests, where the grid peak voltage and frequency are adjusted at 320 V and 50-Hz, respectively.

As per the single-phase open-loop design, the results of different case studies have been provided in Fig. 3.11(a)-(f). In the first test, the converter operates at 1 kW with the input voltage set at 50 V. Considering the voltage boosting capability of the proposed topology and regarding the described PS-PWM process, the values of D and m are set at 0.8 and 0.87, respectively. The 5L inverter output voltage, the voltage across both integrated capacitors, the input current, and the load current are shown in Fig. 3.11(a), which reflects the feasible performance of the proposed topology in the higher range of voltage boosting operation. Fig. 3.11(b) and (c) show the same set of waveforms at $V_{dc} = 50$ V, when a step change in m (from 0.61 to 0.87) and D (from 0.6 to 0.7) is applied. The results again reflect the correct converter operation during such dynamic tests.

Due to the maximum current limitation of the DC power supply in the lab, the performance of the proposed topology operating at 3 kW was verified for low voltage boosting DC duty cycle ranges. As shown in Fig. 3.11(d), the DC input voltage is set at 100 V, while D and m are set at 0.65 and 0.73, respectively. The peak of the load current is around 18 A and the peak output voltage of the proposed inverter is around 570 V. As expected, the input current waveform is continuous with 100 Hz double-line frequency content. Fig. 3.11(e) also shows the dynamic results of the proposed converter when the load has suddenly changed from 0.5 kW to 1.5 kW power. In this case, the DC input voltage is set at 120 V. Finally, the experimental results of this case study related to the voltage stress waveforms of different switches at the rated 3 kW power with $V_{dc} = 100$ V, $D = 0.65$, and $m = 0.73$ have been shown in Fig. 3.11(f), which are in agreement with the theory and the simulation.

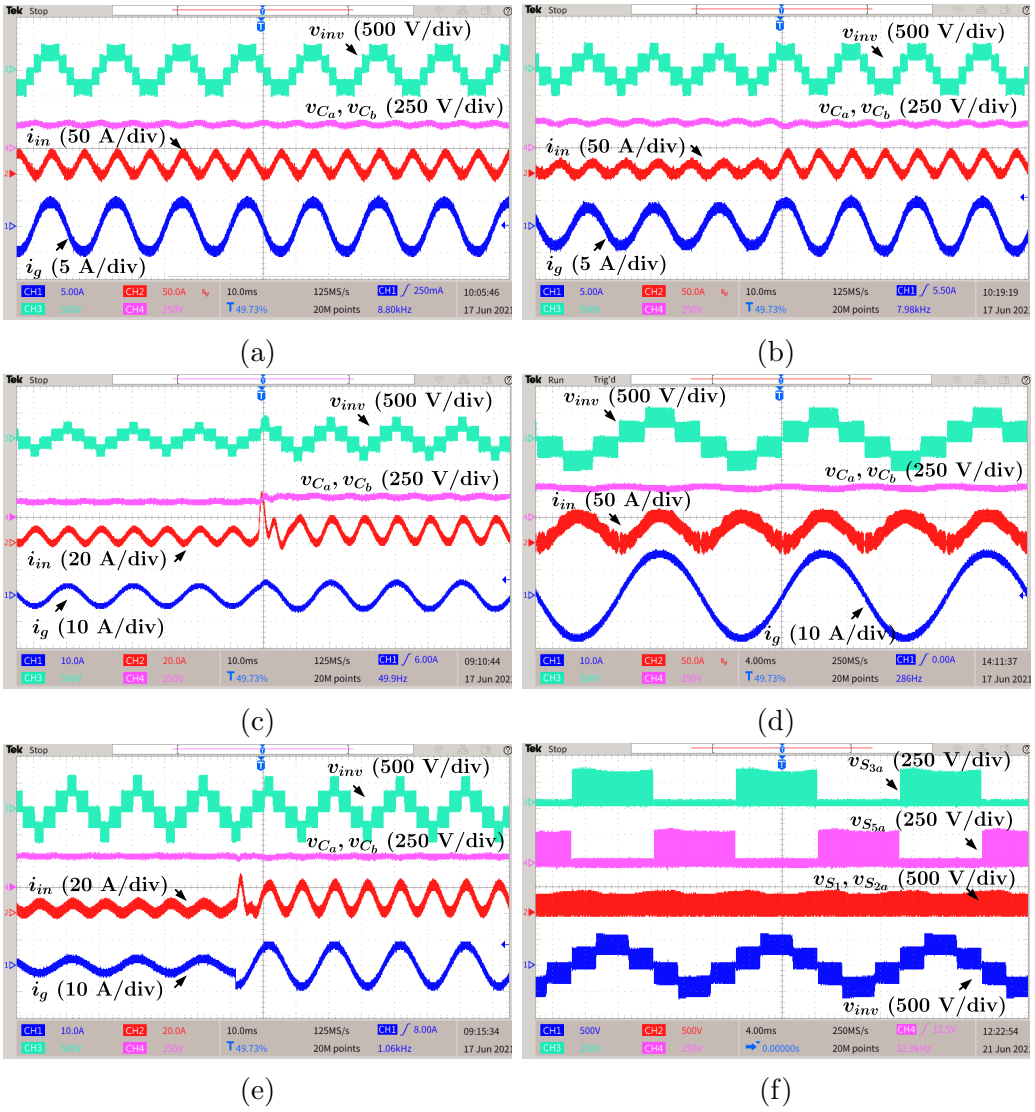


Fig. 3.11. Experimental results showing from top to bottom: 5L proposed inverter output voltage, the voltage across the capacitors, input current, and the load current: (a) at 1 kW output power, $D = 0.8$, $m = 0.87$, and $V_{dc} = 50$ V; (b) at $D = 0.8$, and $V_{dc} = 50$ V under the step change in m from 0.61 to 0.87; (c) at $V_{dc} = 50$ V, and step change in D from 0.6 to 0.7; (d) at 3 kW output power, $D = 0.65$, $m = 0.73$, and $V_{dc} = 100$ V; (e) at $V_{dc} = 120$ V, $D = 0.65$, $m = 0.73$, and step change in the load value from 0.5 kW to 1.5 kW output power; and (f) the blocking voltages across S_{3a}, S_{3b} (green trace), S_{5a}, S_{5b} (pink trace), and S_{2a}, S_{2a}, and S_1 (red trace) at $D = 0.65$, $m = 0.73$, and $V_{dc} = 100$ V.

The closed-loop grid-tied performance of the proposed S^{5}B5L-VSI using a PR controller associated with the modified PS-PWM technique is shown in Fig. 3.12(a)-(c). Here, the applied DC input voltage, the 5L inverter output voltage, the grid voltage, v_g, and the injected grid current, i_g, waveforms have been shown from top to bottom, respectively. To confirm the enhanced output voltage gain potentiality of the proposed S^{5}B5L-VSI, the results are taken within three different case studies of $V_{dc} = 90$ V with $D = 0.6$, $V_{dc} = 55$ V with $D = 0.75$, and $V_{dc} = 40$ V with $D = 0.85$ as shown in Fig. 3.12(a)-(c), respectively. Here, the small fluctuation in the DC input voltage is due to the inherent characteristic of the used PV emulator since its input-output internal capacitor is low. Also, because of the limitation of the used PV emulator in terms of output current, the results are taken at different ranges of the injected output power i.e., 2 kW, 1 kW, and 500 W for the cases of $D = 0.6$, $D = 0.75$, and $D = 0.85$, respectively. As can be realized from these results, the peak value of the inverter output voltage in all the cases is in accordance with the described relationship in (3.3) and Fig. 3.6 since the converter can meet the peak amplitude requirement of the grid voltage even with a low value of the DC input voltage. It is worth mentioning that regarding Fig. 3.7, to get the same output voltage gain with the same values of D through the normal PS-PWM technique presented in [67], the provided DC-link voltage should be larger to meet the peak amplitude requirement of the grid voltage.

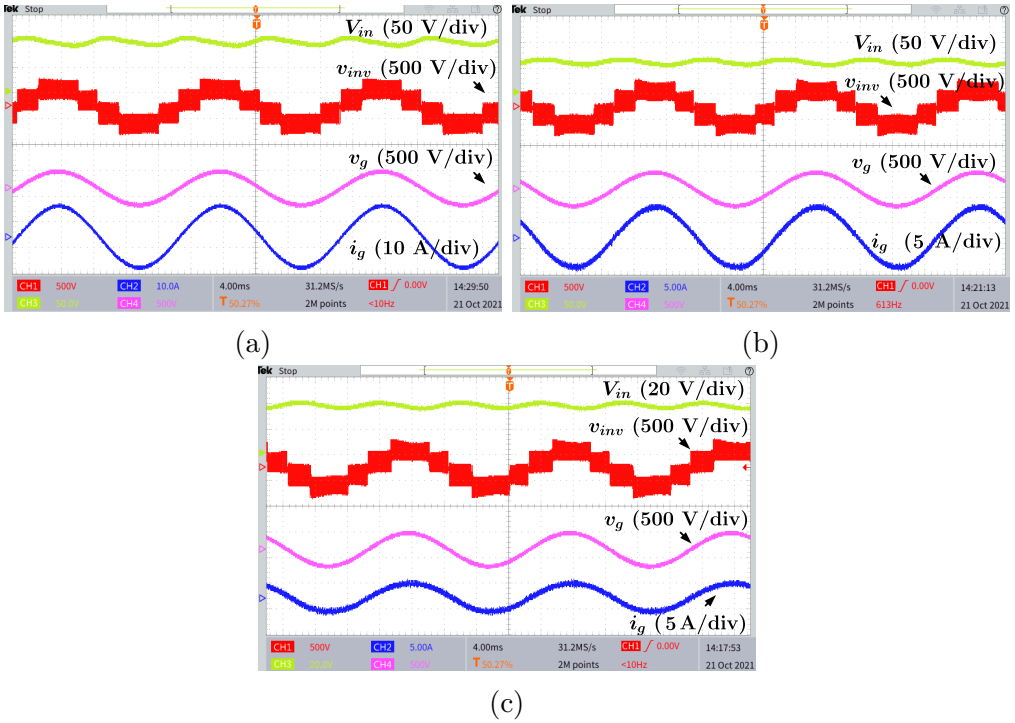


Fig. 3.12. Experimental waveforms of the proposed topology at (a) V_{dc} = 90 V and D = 0.6, (b) V_{dc} = 55 V and D = 0.75, (c) V_{dc} = 40 V and D = 0.85.

To confirm the correct performance of the proposed S^{5}B5L-VSI in reactive power support mode, the experimental results shown in Fig. 3.13(a)-(b) can be considered. Here, the DC input voltage and the value of D are set at 90 V, and 0.7, respectively. The results are taken for both leading (P = 1 kW, Q = 1 kVAr) and lagging (P = 1 kW, Q = -1 kVAr) power factors, while the input current is continuous and all the desired 5L output voltage waveform of the inverter with a quality sinusoidal injected current have been generated. In the following, Fig. 3.13(c) shows the bidirectional operation of the converter when the power flow direction changes from P = -1 kW to P = +1 kW. Consequently, the average input current is negative when the power is flowing from the grid to the DC source, and it is positive when the power flows from the DC source to the grid. Herein, an electronic load has been connected in parallel with the PV emulator to absorb the reverse power at the DC side. In both operational modes, the converter can generate all the desired 5L output voltage with a continuous input current and a sinusoidal waveform for the injected grid current.

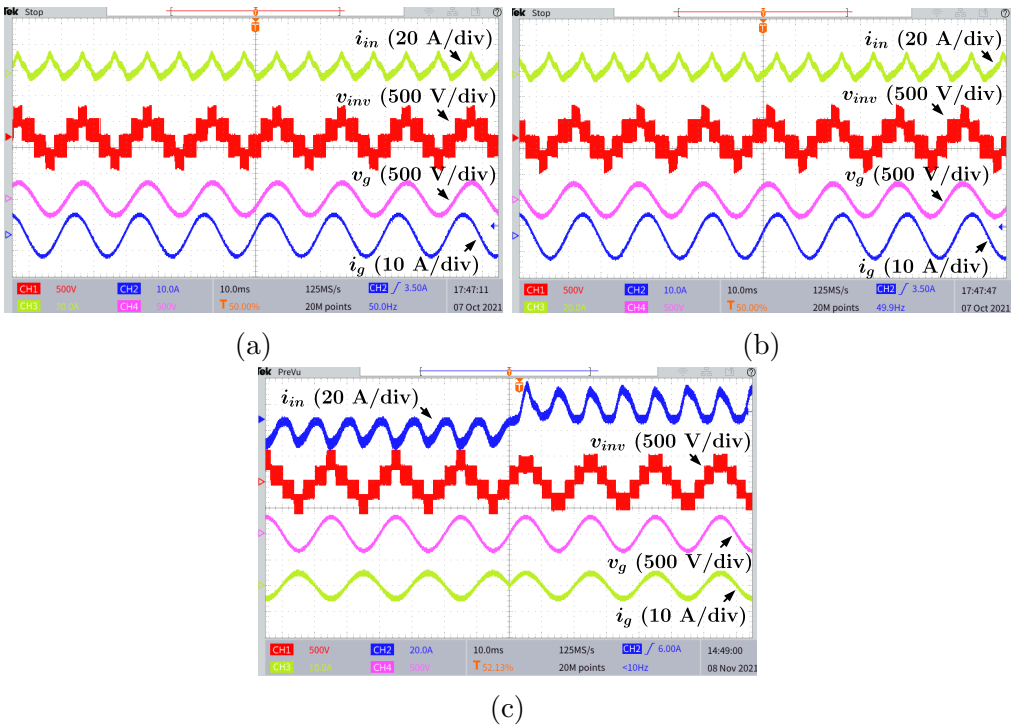


Fig. 3.13. Experimental waveforms of the proposed topology at V_{dc} = 90 V (a) leading power factor (P = 1 kW, Q = 1 kVAr), (b) lagging power factor (P = 1 kW, Q = -1 kVAr), and (c) bidirectional operation (P = -1 kW to P = +1 kW).

Furthermore, Fig. 3.14(a)-(c) show the related three-phase experimental results of the proposed topology. In this case, the DC input voltage is set at 100 V. To reach 400 V peak at each phase output voltage, D and m are set at 0.75 and 0.73, respectively. Fig. 3.14(a) shows the 3L phase-to-ground output voltage of the inverter and the DC input voltage waveform, while the 5L phase-to-phase output voltages and the DC input voltage are shown in Fig. 3.14(b). The input current waveform with an average value of 32 A, and the related three-phase currents for a 3.2 kW load are also shown in Fig. 3.14(c).

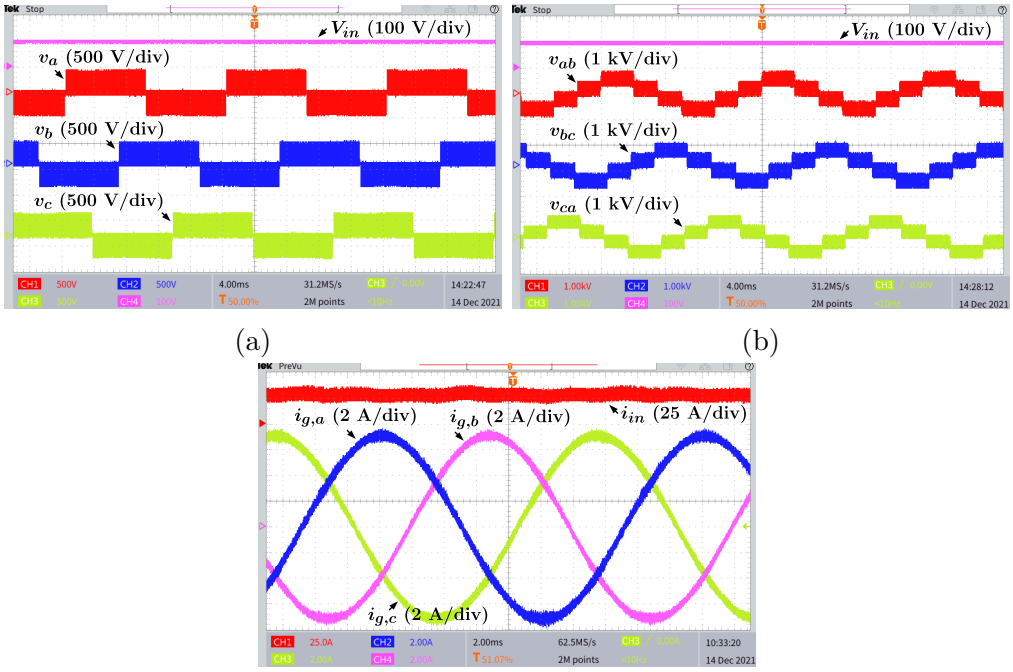


Fig. 3.14. Experimental waveforms of the three-phase extension of the proposed topology at $V_{dc} = 100$ V. (a) 3L phase-to-ground output voltages and DC input voltage, (b) 5L phase-to-phase voltages and DC input voltage, and (c) load current of each phase at 3.2 kW output power and input current.

Finally, the trends of calculated and measured efficiency for the single-phase design of the proposed S^{5}B5L-VSI from 500 W to 3 kW tested power are illustrated in Fig. 3.15(a), where the DC input voltage is set at 100 V, and D is equal to 0.7. As for the calculated results, the detailed thermal model of the power switches is used in PLECS, while a Voltech PM3000A Universal Power Analyzer is utilized to measure the overall efficiency of the proposed converter in practice. The results show more than 96.5% overall efficiency over a wide range of the output power changes. The details of loss breakdown results for the involved semiconductor devices and passive elements at 3 kW output power are also illustrated in Fig. 3.15(b). Considering the grid-tied experimental results presented in Fig. 3.12(a)-(c), the FFT analysis of the proposed S^{5}B5L-VSI is illustrated in Fig. 3.15(c). Here, the measured THD values of the inverter output voltage and the load/grid current are 0.31% and 0.38%, respectively. As can be realized in Fig. 3.15(c), due to applying the improved PS-PWM technique, the mass of harmonic clusters is around twice the switching frequency, which further helps the converter to maintain

a high power quality compatible with the IEEE 519-2014 standard [113].

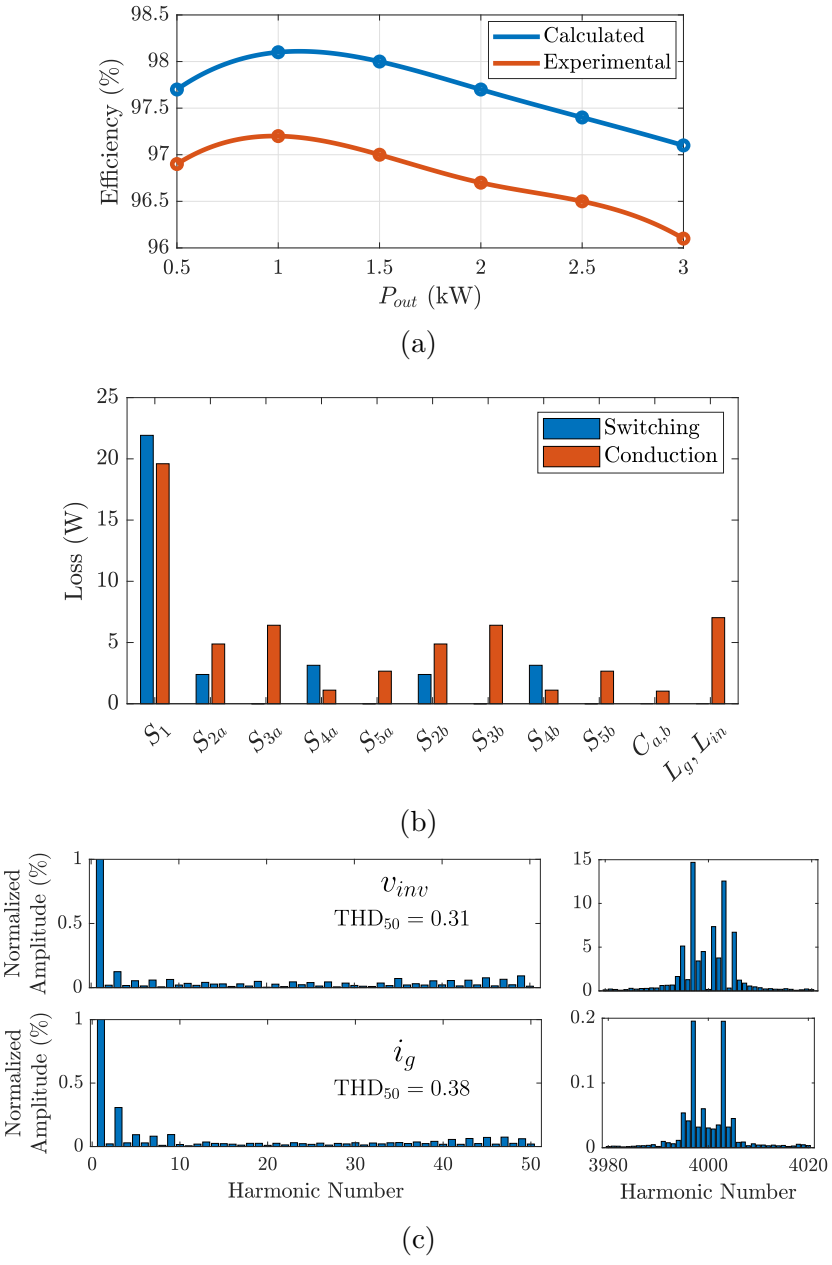


Fig. 3.15. Converter performance: (a) Calculated and measured efficiency of the proposed S^{5}B5L-VSI, (b) PLECS loss breakdown results at $P = 3$ kW and $V_{dc} = 100$ V, (c) experimental inverter output voltage and grid current harmonics at $P = 3$ kW, and $V_{dc} = 100$ V.

3.8 Conclusion

A 5L switched-boost inverter with the single-stage dynamic voltage boosting feature using a single DC power supply is introduced in this chapter. The proposed topology is comprised of nine active power switches with a single inductor and two self-balanced capacitors. Compared to existing topologies, bidirectional power flow capability, reduced number of switching devices, reduced per-unit voltage stress across the switches, reduced CMV per each output voltage level, improved overall voltage conversion gain, and the circuit extension ability are the major benefits of the proposed converter. Furthermore, dynamic voltage boosting feature, continuous and spike-free input current, and modularity make the proposed converter an attractive candidate for many grid-connected applications. The operation and working principle of the proposed topology with its extra topological derivations have been discussed. Design guidelines, power loss analysis, and comparative study have been also provided. Finally, the performance and feasibility of the proposed inverter for both single and three-phase configurations have been verified by several simulation and laboratory experimental results. The measured peak efficiency of the proposed converter is around 97% at 1 kW, while the tested results up to 3 kW output power show more than 96.1% efficiency in practice.

As identified in the analysis and experimental results, a significant double-line frequency ripple is present in the input current profile. Similar to many available single-phase DC-AC converters, this issue might restrict the applicability of such converters in some cases including PV, fuel-cell, or battery systems. It is worth mentioning that this particular challenge has been studied in detail in the following chapters.

Chapter 4

A Single-Stage Switched-Boost Grid-Connected Five-Level Converter With Integrated Active Power Decoupling Under Distorted Grid Voltage Condition

This chapter introduces an APD method for the proposed S^5B5L converter to improve the performance and efficiency of the overall system through eliminating the low-frequency ripples in the DC input current. Furthermore, a distorted grid voltage condition is considered to reflect a realistic operating environment.

4.1 Introduction

The proposed S^5B5L topology offers several attractive features in terms of the number of semiconductor devices, improved dynamic voltage conversion gain, low value of the required passive elements, bidirectional power flow performance, and continuous input current profile. Despite these advantages, this topology still presents a double-line frequency ripple in the DC input current that can affect the overall efficiency.

The aim of this work is to further enhance the circuit performance of the S^5B5L converter with an integrated APD capability in the presence of grid voltage harmonics for applications that require constant and ripple-free DC

current (e.g., PV, battery, fuel-cell systems, etc.). As for the APD control, two simple proportional-integrator (PI) controllers are used for the DC-link side, while only a single proportional-resonant (PR) controller is employed to govern the converter to inject the required current to the grid at the AC side. A general method based on a grid voltage observer (GVO) technique has also been applied to synchronize the system with the fundamental component and obtain a filtered version of the grid voltage with low-frequency harmonics. The main features/contributions of the work at hand are:

- To the best of the authors' knowledge, integration of APD into a single-stage switched-boost (SB) 5L converter without introducing additional circuit components has not been fully studied yet. This chapter aims to add APD capability to the S^5B5L converter, which is one of the promising types of available SB-based 5L converters in the literature. The same solution can also be applied to other types of SB-based converters as long as their input current before integration of APD contains only low-frequency ripple contents.

- Increasing the overall efficiency of the previously proposed S^5B5L converter over a wide range of input DC voltage/power levels by reducing the current stress profile of the passive/active elements. This is achieved without changing the size of passive elements of the original circuit or adding any extra components.

- Implementing a closed-loop grid current controller under a distorted grid voltage by only using a single PR controller, as opposed to the conventional multi-resonant-based architecture, thus, simplifying the overall control system design process.

- Investigating the system performance under a polluted grid voltage with a straightforward GVO-based solution with inherent filtering capabilities. This improves the robustness of the system against high-frequency measurement noises, and reduces the controller complexity using a feed-forward technique.

To this end, the proposed closed-loop control strategy is introduced and analyzed in the following sections.

4.2 Closed-Loop Control Strategy Applied to the S^{5}B5L Converter Without APD Under Distorted Grid Voltage

According to the working principle of the S^{5}B5L grid-connected converter, two control inputs, i.e., the boost duty cycle $D \in (0, 1)$ and the AC modulation reference $u \in [-1, 1]$, must be generated by the closed-loop control strategy and sent to the PS-PWM stage to provide the required gate switching pulses. Hence, considering (4.1) as the average voltage across each of the involved capacitors, the inverter output voltage and its maximum fundamental value are expressed as (4.2) and (4.3), respectively.

$$V_c = \frac{V_{dc}}{1 - D} \tag{4.1}$$

$$v_{inv} = v_{max} u \tag{4.2}$$

$$v_{max} = (1 + D) V_c. \tag{4.3}$$

The aim of the standard closed-loop control technique implemented in the previous chapter is to govern the system to inject active and reactive power to a standard grid without applying the APD control under an ideal and harmonic-free grid voltage condition. However, in this chapter, a more realistic case with a distorted grid voltage with low-frequency harmonics has been considered and the control strategy has been modified accordingly. This is achieved by obtaining the AC reference u from the output of multiple PR controllers tuned at the expected grid voltage harmonic frequencies, as shown in Fig. 4.1. Here, a simple PLL is used to detect the fundamental phase and amplitude of the grid voltage, i.e., ωt and V_m. Additionally, the grid current, i_g, is measured with a current sensor. Then through the current reference generation stage and the desired active and reactive power references, $P_g^\star$ and $Q_g^\star$, a grid current reference, $i_g^\star$, is generated as follows:

$$i_g^\star = \frac{2P_g^\star}{V_m} \cos(\omega t) + \frac{2Q_g^\star}{V_m} \sin(\omega t). \tag{4.4}$$

As for an available DC input voltage, an appropriate value of boost duty cycle D is also defined based on the peak grid voltage and (4.3) to inject the power into the grid. In Fig. 4.1, $G_{ac}(s)$ is a first-order system plant based on the ESR and inductance of the grid-interface filter, describing the relationship between grid current, i_g, and the voltage across the grid-interface filter, v_{L_g}, in the frequency domain. Moreover, in this control strategy, the grid voltage, v_g, acts as an input disturbance for the PR controllers, which can be rejected

by multiple PR controllers tuned at the fundamental frequency and expected harmonics of the grid voltage. [80,170,171]. Through this control design, the injected current is controlled; however, the input current contains a dominant double-line frequency ripple component leading to excessive conduction losses of the input DC inductors and semiconductors.

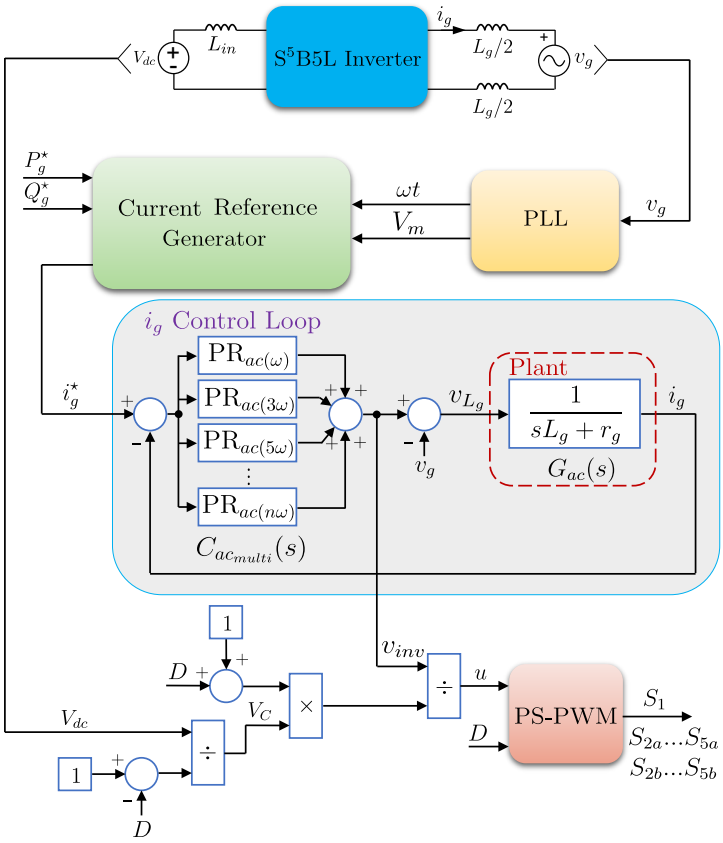


Fig. 4.1. Multi-PR control strategy for the S^{5}B5L-VSI under distorted grid voltage without APD functionality.

4.3 Proposed Control Strategy with APD Under Distorted Grid Voltage

As opposed to the control solution without APD functionality, the proposed closed-loop control strategy applied to the S^{5}B5L grid-connected converter includes an integrated APD control strategy that is able to operate under a grid voltage polluted with low-frequency harmonics. Hence, to derive an

expression for the injected grid power, p_g, it is necessary to define the grid voltage in the presence of the low-frequency harmonics, and the injected grid current, i.e.:

$$v_g = \sum_{h \in H} V_{g,h} \cos(h\omega t + \phi_h) \tag{4.5}$$

$$i_g = I_m \cos(\omega t + \phi) \tag{4.6}$$

where h, $V_{g,h}$, ϕ_h, ω, I_m, and ϕ are the harmonic order, the amplitude and phase of the h^{th} harmonic of the grid voltage, the grid fundamental angular frequency, the peak value of the injected current, and the phase angle of the injected grid current with respect to the fundamental harmonic of the grid voltage, respectively. Moreover, $H = \{1, 3, 5, ..., M\}$ is the measured harmonics, M is the highest harmonic order considered, and $\phi_1 = 0$. Hence, the expression for the instantaneous grid power, p_g, can be derived as follows:

$$\begin{aligned} p_g &= v_g i_g \\ &= \sum_{h \in H} \frac{V_{g,h} I_m}{2} [\cos((h-1)\omega t + \phi_h - \phi) \\ &\quad + \cos((h+1)\omega t + \phi_h + \phi)]. \end{aligned} \tag{4.7}$$

From (4.7), it can be deduced that p_g in the single-phase grid-tied application consists of a dc, $p_{g,dc}$, and a low-frequency ripple, $p_{g,r}$, term as:

$$\begin{aligned} p_{g,dc} &= \frac{V_m I_m}{2} \cos(\phi) \\ p_{g,r} &= p_g - p_{g,dc} \end{aligned} \tag{4.8}$$

where V_m is the fundamental amplitude of the grid voltage, i.e., $V_m = V_{g,1}$.

On the other hand, according to the concept of APD control strategy, the input DC source power, p_{in}, has to be free from any low-frequency ripple/pulsating content. Hence, the ripple AC power, $p_{g,r}$, must be provided by the integrated energy storage elements, e.g., the boost inductor, L_{in} or the capacitors C_a or C_b in the described S^5B5L converter. Considering that the aim of an APD control strategy is to cancel out any low-frequency ripple from the input current, $p_{g,r}$ is provided through the contribution of the capacitors in the S^5B5L grid-connected converter. Therefore, considering p_C as the required instantaneous power of the involved capacitors, it follows that:

$$p_g(t) = p_{in}(t) + p_C(t) \tag{4.9}$$

$$p_C(t) = p_{C_a}(t) + p_{C_b}(t) = p_{g,r}(t). \tag{4.10}$$

Hence, considering identical capacitance, C, for both integrated capacitors, the instantaneous capacitor voltages that include a low-frequency AC ripple term, are expressed as follows:

$$v_C^2(t) = \frac{1}{C}\int p_{g,r}(t)dt \tag{4.11}$$

$$\begin{aligned} v_C^2(t) &= \frac{V_m I_m}{2C}\frac{\sin(2\omega t+\phi)}{2\omega} \\ &+\frac{I_m}{2C}\sum_{h\in H, h\neq 1} V_{g,h}\Bigg(\frac{\sin((h-1)\omega t+\phi_h-\phi)}{(h-1)\omega} \\ &\qquad + \frac{\sin((h+1)\omega t+\phi_h+\phi)}{(h+1)\omega}\Bigg) + K \end{aligned} \tag{4.12}$$

$$\tilde{v}_C^2 = v_C^2 - K \tag{4.13}$$

where K is the integration constant value related to the average capacitor voltage requirement of each of the involved capacitors to meet the peak grid voltage value as per (4.3).

Considering the above discussion, the overall control block diagram consists of four sections as shown in Fig. 4.2, where the aim of APD control is fulfilled by controlling i_{in} free from any low-frequency ripple component, v_C with the required average value, and the injected grid current, i_g, following a sinusoidal reference current. Hence, $i_{in}^\star$, $V_C^\star$, and $i_g^\star$, are defined as the references for the input current, the average capacitor voltages, and the injected grid current, respectively. Here, the GVO or PLL mechanism shown in Fig. 4.2(a) is in charge of grid synchronization and extracting the fundamental component of a distorted grid voltage to define the required references. In this work, a GVO is designed as an alternative solution instead of a conventional PLL. The added benefit of using GVO instead of a PLL is its inherent filtering ability against high-frequency noises in the grid voltage measurement. Figs. 4.2(b) and (c) also indicate the requirement of the APD control for the DC input current and capacitor voltages, while Figs. 4.2(d) and (e) show the details of the controller to inject the desired active and reactive power to the grid at the AC side and its modulator, respectively. Herein, as for V_C and i_{in} control loops, two PI controllers, i.e., $C_C(s)$ and $C_{dc}(s)$ in Figs. 4.2(b) and (c), are needed, where the first-order transfer functions, $G_C(s)$ and $G_{dc}(s)$, are considered to design the aforementioned controllers.

Regarding the capacitor voltage control loop, the plant transfer function, $G_C(s)$ has been derived based on the relationship between the capacitor power and the squared value of the capacitor voltage in the frequency domain,

i.e., $P_C(s) = sCV_C^2(s)$. It should be noted that since both C_a and C_b have the same voltage due to the switching states of the S^5B5L converter (see Fig. 3.2), $G_C(s)$ is derived based on the total equivalent capacitance, i.e., C_a and C_b in parallel. Similarly, the plant transfer functions for the DC input current and grid current control loops are obtained based on the relationship between the current and the voltage across an L-type filter considering its parasitic ESR. As for the injected grid current control loop shown in Fig. 4.2(d), a single PR controller, $C_{ac}(s)$, is designed based on $G_{ac}(s)$. Here, r_C, r_{in}, and r_g are denoted as the ESR of the involved capacitors, the input inductor, and the output filter inductors, respectively. Moreover, the grid current, i_g, is measured with a current sensor.

It should be noted that the feed-forward term used in the grid current controller is obtained from the GVO; hence, it can be considered as a filtered replica of the grid voltage measurement, while including all the expected low-frequency harmonics. Consequently, the calculated inverter voltage is free from any high-frequency noises. By considering a ZOH discretization, the required parameters of the PI and PR controllers for the input current, capacitors voltages, and the injected grid current control are obtained in the z-domain for digital implementation. As indicated in Fig. 4.2(b), to extract the DC component (average) of v_C, a low pass filter (LPF) is required. In the next subsections, the mechanism of the GVO and the reference design for the three main control loops are described in detail.

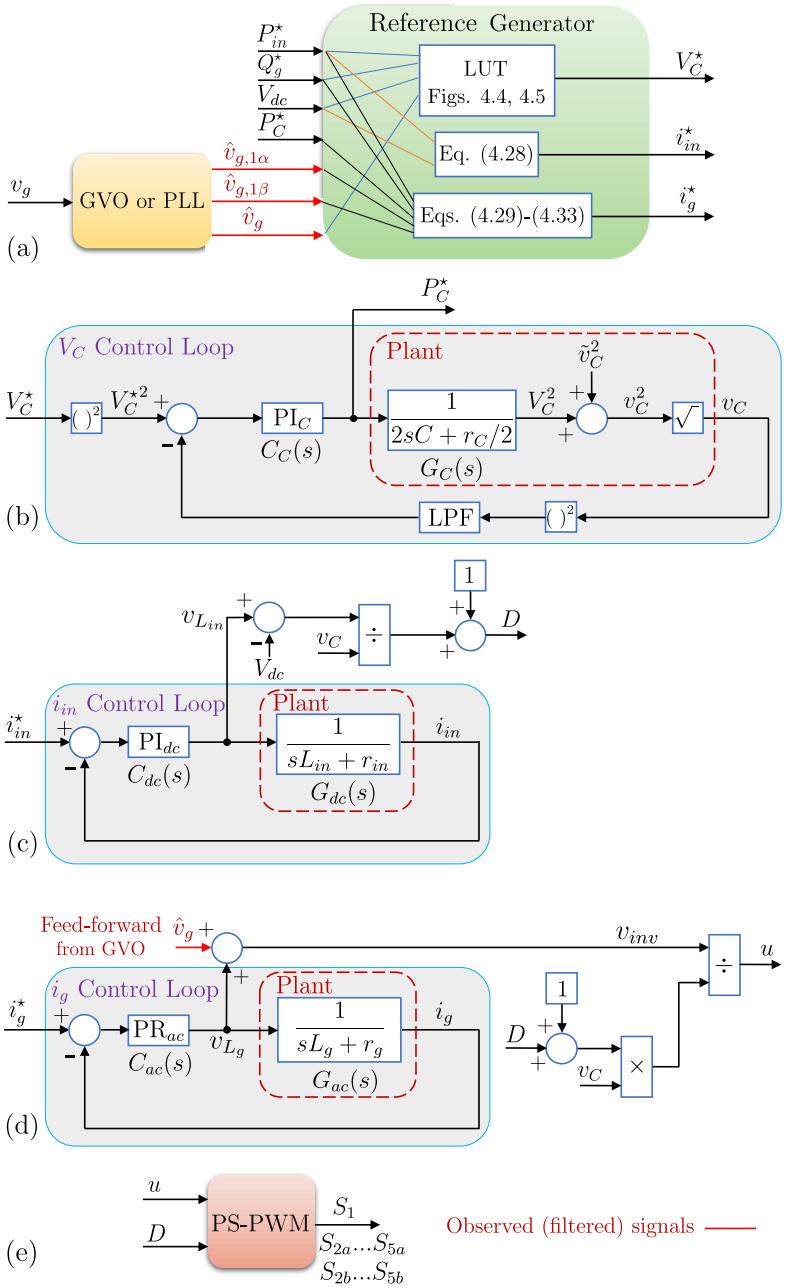


Fig. 4.2. Proposed control strategy with APD: (a) grid synchronization and reference generation; (b) capacitor voltage controller; (c) DC input current controller; (d) grid current controller; (e) modulator.

4.3.1 GVO Mechanism

In the general case of having a polluted grid voltage with several low-frequency harmonics, the fundamental component of the grid voltage is required to be extracted for the current reference generation. Moreover, obtaining a noise-free version of the measured grid voltage is also relevant since it is used as a feed-forward term in the i_g control loop. Conventionally, a PLL can be employed for this purpose; however, the whole PLL structure must be replicated for each harmonic component to reconstruct a clean sample of the grid voltage. A more suitable and straightforward alternative for extracting this information is to develop a generalized GVO mechanism. As this is an observer-based synchronization strategy, this single structure can be used not only to decompose the grid voltage in each harmonic component but also to reduce the high-frequency noise of the instantaneous grid voltage. Hence, the measured grid voltage in the stationary reference frame can be expressed as a summation of its harmonic contents:

$$v_{g_{\alpha\beta}} = \sum_{h \in H} v_{g,h_{\alpha\beta}} \tag{4.14}$$

where, $v_{g_{\alpha\beta}} \in \mathbb{R}^2$ and $v_{g,h_{\alpha\beta}} \in \mathbb{R}^2$ are the grid voltage and its harmonic component vectors in a stationary reference frame, respectively. Therefore, $v_{g,h_{\alpha\beta}}$ can be written as:

$$v_{g,h_{\alpha\beta}} = \begin{bmatrix} v_{g,h_\alpha} \\ v_{g,h_\beta} \end{bmatrix} = \begin{bmatrix} V_{g,h}\cos(h\omega t + \phi_h) \\ V_{g,h}\sin(h\omega t + \phi_h) \end{bmatrix}. \tag{4.15}$$

Assuming the steady-state condition or slowly changing harmonic content of the grid voltage, the derivative of each grid voltage harmonic can be derived as follows:

$$\frac{dv_{g,h_{\alpha\beta}}}{dt} = \frac{d}{dt}\begin{bmatrix} v_{g,h_\alpha} \\ v_{g,h_\beta} \end{bmatrix} = Jh\omega v_{g,h_{\alpha\beta}} \tag{4.16}$$

where

$$J = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}. \tag{4.17}$$

A continuous-time state-space system model can be constructed based on (4.14)-(4.16) with the grid voltage harmonics in a stationary reference frame as the system states, x, and the grid voltage as the system output, y:

$$x = \begin{bmatrix} v_{g,1_{\alpha\beta}} & v_{g,3_{\alpha\beta}} & \dots & v_{g,M_{\alpha\beta}} \end{bmatrix}^T \tag{4.18}$$

$$y = v_{g_\alpha} = \sum_{h \in H} v_{g,h_\alpha}. \tag{4.19}$$

This leads to the following continuous-time state space model:

$$\frac{dx}{dt} = A_c x + \varpi \tag{4.20}$$

$$y = C_c x + \nu \tag{4.21}$$

where

$$A_c = \begin{bmatrix} J\omega & O_2 & O_2 & \dots & O_2 \\ O_2 & J3\omega & O_2 & \dots & O_2 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ O_2 & O_2 & O_2 & \dots & JM\omega \end{bmatrix}, \tag{4.22}$$

$$C_c = \begin{bmatrix} 1 & 0 & 1 & 0 & \dots & 1 & 0 \end{bmatrix}, \tag{4.23}$$

and O_2 is a zero matrix of dimension 2×2. Moreover, ϖ and ν are the process and measurement noises, respectively.

This dynamic model can be discretized using the ZOH method. Therefore, the following discrete state-space model is formed:

$$\begin{aligned} x_{k+1} &= Ax_k + \varpi_k \\ y_k &= C_c x_k + \nu_k \end{aligned} \tag{4.24}$$

where A is the resultant state dynamics matrix after discretization. Here, it is important to emphasize that the pair (A, C_c) is observable. Therefore, based on the derived discrete state-space model in (4.24), an observer can be designed either through a pole placement or a steady-state Kalman filter approach. The pole placement method is based on placing the poles of the closed-loop transfer function at specific locations on the complex plane by normally selecting two dominant poles to achieve the desired behavior. However, using this method for systems with a large number of states might be complicated and not necessarily optimal. On the contrary, the Kalman filter approach can deal with a larger number of states while the observer parameters can be obtained optimally [101]. In this work, the latter is chosen due to the large number of states. Thus, the GVO is designed to estimate the instantaneous amplitude of each harmonic of the measured grid voltage as:

$$\begin{aligned} \hat{x}_{k+1} &= A\hat{x}_k + G_o(y_k - \hat{y}_k) \\ \hat{y}_k &= C_c\hat{x}_k \end{aligned} \tag{4.25}$$

where G_o, $\hat{x}_{k+1}$, and $\hat{x}_k$ are the observer gain matrix and estimated states at time step k and $k+1$, respectively. Similarly, $\hat{y}_k$ is the estimated output (i.e., grid voltage) at time instant k.

The observer gain matrix, G_o, can be calculated based on the known system and noise parameters, i.e., discrete state-space model in (4.24), by solving the following discrete-time algebraic Ricatti equation as explained in [101, 172]:

$$G_o = APC_c^T(C_cPC_c^T + R_f)^{-1} \tag{4.26}$$

$$P = APA^T - G_oC_cPA^T + Q_f \tag{4.27}$$

where P is the estimate covariance matrix, R_f is the measurement noise covariance matrix, and Q_f is the process noise covariance matrix. In this work, as there is only one measurement used for the observer, R_f possesses only a scaler value that depends on the grid voltage sensor noise, i.e., a noisier sensor translates to a higher value of R_f. The value of R_f should be equal to the covariance of the voltage sensor, which can be easily obtained by recording a large number of measurements with constant voltage at the sensor's input and calculating the covariance of the recorded values. In addition, Q_f represents the process noise that can be caused by model errors or uncertainties. Here, Q_f is considered as:

$$Q_f = q_fI_n \tag{4.28}$$

where I_n is the identity matrix with the same dimensions as A, and $q_f > 0$ is a number indicating model errors. Therefore, a larger q_f means the model is not trusted, and the observer relies more on the sensor information. Conversely, a smaller q_f implies an accurate state-space model, and the observer relies more on the model predictions. Consequently, the value of q_f can be used to set the observer bandwidth [172]. Knowing R_f and Q_f, matrices P and G_o can be calculated using (4.26)-(4.27). It should be noted that the observer gain, G_o, is a constant matrix (time-invariant). Hence, it can be calculated offline to reduce the computational overhead of the observer. Here, the function *idare* in MATLAB is used to solve (4.26)-(4.27) and obtain G_o.

Therefore, following the above procedure, as indicated in Fig. 4.2(a), the GVO gets the measured grid voltage as per (4.5), and outputs the estimated value of the grid voltage, $\hat{v}_g$. This helps to reject high-frequency measurement noises effectively. Consequently, to define the grid current reference, $i_g^\star$, as for the next stage of the control system shown in Fig. 4.2(a), the fundamental value of the observed grid voltage in the stationary ($\alpha\beta$) reference frame, i.e., $\hat{v}_{g,1\alpha\beta}$ is extracted through the GVO stage.

4.3.2 Reference Design

As per Fig. 4.2(a), the reference generator stage receives six inputs, i.e., $P^{\star}_{in}$, $Q^{\star}_{g}$, V_{dc}, $P^{\star}_{C}$, and $v_{g,1_{\alpha\beta}}$, which are the intended reference values of the input active power, grid reactive power, the input DC voltage of the converter, the required capacitors power reference, and the observed fundamental value of the grid voltage extracted from the described GVO mechanism, respectively. Through these, the references $i^{\star}_{in}$, $V^{\star}_{C}$, and $i^{\star}_{g}$ are generated to govern the system as per Fig. 4.2(b)-(d). Moreover, the active and reactive grid power references, $P^{\star}_{in}$ and $Q^{\star}_{g}$, are external references, which represent the power level being transferred from/to the power supply to/from the grid and required reactive power compensation level, which in turn determine the desired power factor. Consequently, the required references are expressed as follows:

$$i^{\star}_{in} = \frac{P^{\star}_{in}}{V_{dc}} \tag{4.29}$$

$$P^{\star}_{g} = P^{\star}_{in} + P^{\star}_{C} \tag{4.30}$$

$$i^{\star}_{g} = \frac{2P^{\star}_{g}}{\hat{V}_{m}}\cos(\omega t) + \frac{2Q^{\star}_{g}}{\hat{V}_{m}}\sin(\omega t) \tag{4.31}$$

where

$$\hat{V}_{m} = \sqrt{\hat{v}^{2}_{g,1_{\alpha}} + \hat{v}^{2}_{g,1_{\beta}}} \tag{4.32}$$

$$\cos(\omega t) = \frac{\hat{v}_{g,1_{\alpha}}}{\hat{V}_{m}} \tag{4.33}$$

$$\sin(\omega t) = \frac{\hat{v}_{g,1_{\beta}}}{\hat{V}_{m}}. \tag{4.34}$$

It should be noted that an MPPT functionality can be added to the proposed APD solution for PV-based applications. In this case, an MPPT controller is required to decide the PV voltage reference, $V^{\star}_{dc}$, and a PV voltage controller (e.g., a PI controller) follows the reference by generating the input current reference, $i^{\star}_{in}$, accordingly. Since the proposed APD control scheme expects the input power reference, $P^{\star}_{in}$, it is obtained by multiplying $i^{\star}_{in}$ and V_{dc}. Fig. 4.3 illustrates such a control scheme.

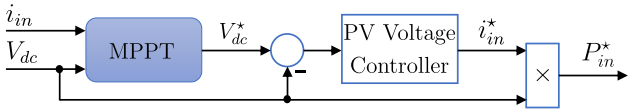


Fig. 4.3. Additional MPPT controller providing the input power reference, $P^{\star}_{in}$, to the proposed APD control strategy.

Regarding the grid-tied operation of the S^{5}B5L converter, the average capacitor voltage, V_C, should be set high enough to meet the grid voltage at any time instant. Hence, considering (4.2) and (4.3), the following relation must be satisfied:

$$v_{max} > v_g > -v_{max}. \tag{4.35}$$

On the other hand, assuming the steady-state condition, by substituting $v_C = \frac{V_{dc}}{1-D}$ into (4.3), an alternative expression for v_{max} can be derived as follows:

$$v_{max} = 2v_C - V_{dc}. \tag{4.36}$$

Therefore, (4.35) can be rewritten as:

$$2v_C - V_{dc} > v_g > -(2v_C - V_{dc}). \tag{4.37}$$

The derived inequality in (4.37) can be further expanded by substituting (4.12) into the expression. Consequently, by knowing the operating conditions, i.e., the grid voltage, the amplitude of the injected grid current, the DC input voltage, and the power factor, a minimum value of K in (4.12) can be found. Hence, there exists a minimum average capacitor voltage that can satisfy (4.37), which is chosen as the reference value, $V_C^\star$, for the capacitor voltage loop control as depicted in Fig. 4.2(c). In this work, due to the nonlinear behavior of the involved equations, this calculation has been performed offline using numerical and iterative methods and the value of the minimum average capacitor voltage has been stored in a lookup table (LUT) for a given range of operating conditions. The resultant values of $V_C^\star$ are shown in Figs. 4.4 and 4.5 for $C = 75$ μF. Fig. 4.4 depicts the minimum average capacitor voltage at unity power factor and for different power levels and the DC input voltages. In addition, Fig. 4.5 shows the variation of this minimum average capacitor voltage at $V_{dc} = 100$ V, and different power factors and power levels.

Moreover, to quantify the voltage stress on the circuit power components (i.e., switches and capacitors), the peak capacitor voltage for different power levels and DC input voltages has been numerically calculated and depicted in Fig. 4.6. In addition, to analyze the impact of the power factor on the voltage stress on the circuit components, a similar analysis has been performed for a wide range of power levels and power factors, as shown in Fig. 4.7. Based on the results of the above analyses, it can be observed that the worst-case scenario in terms of voltage stress happens at higher DC input voltages, higher power levels, and lower values of ϕ.

It should be noted that wider operating ranges are possible by increasing the capacitance or the average capacitor voltage. Based on the selected

components and the limitations of the available hardware prototype and laboratory equipment, the maximum power of 2 kW is considered in this work.

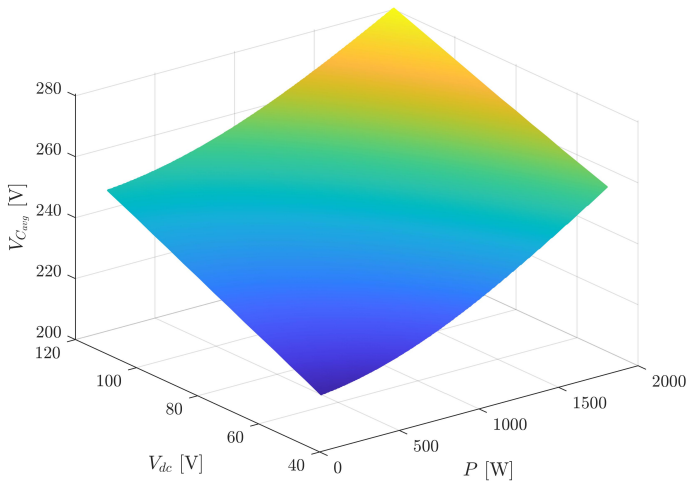


Fig. 4.4. Minimum required average capacitor voltage (V_C) for a given grid-tied operating condition and $C = 75$ µF.

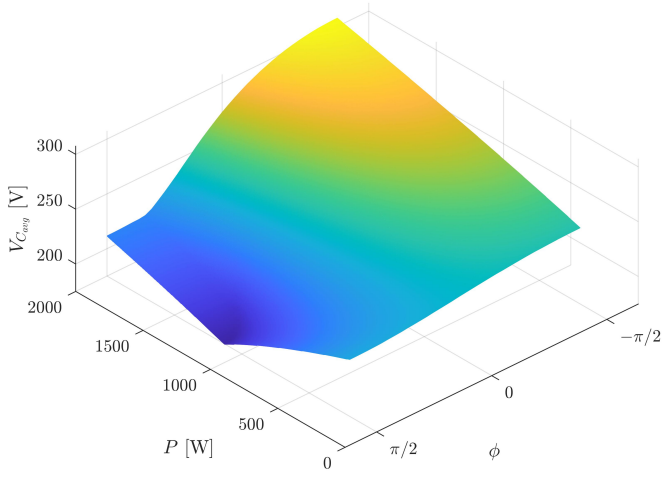


Fig. 4.5. Minimum required average capacitor voltage (V_C) for a given ϕ and grid-tied operating condition at $V_{dc} = 100$ V and $C = 75$ µF.

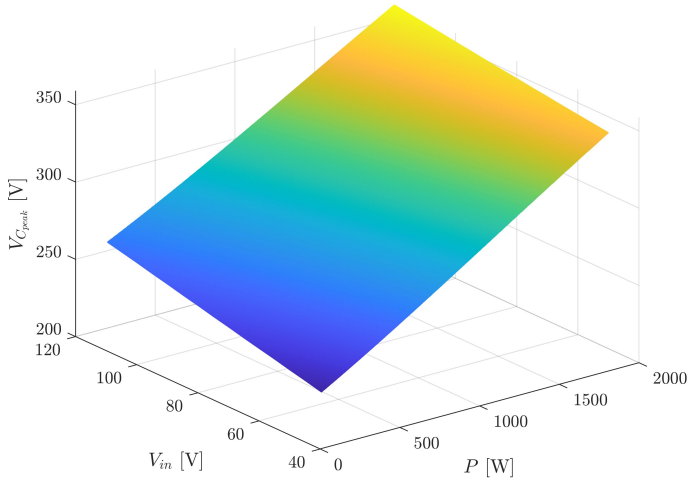


Fig. 4.6. Minimum required peak capacitor voltage (V_C) for a given grid-tied operating condition and $C = 75$ µF.

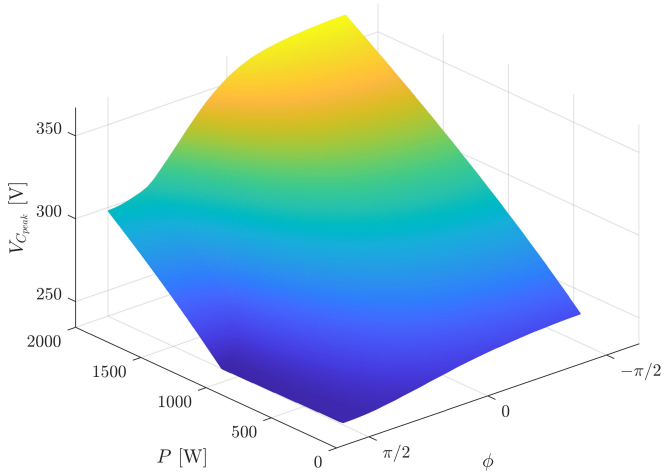
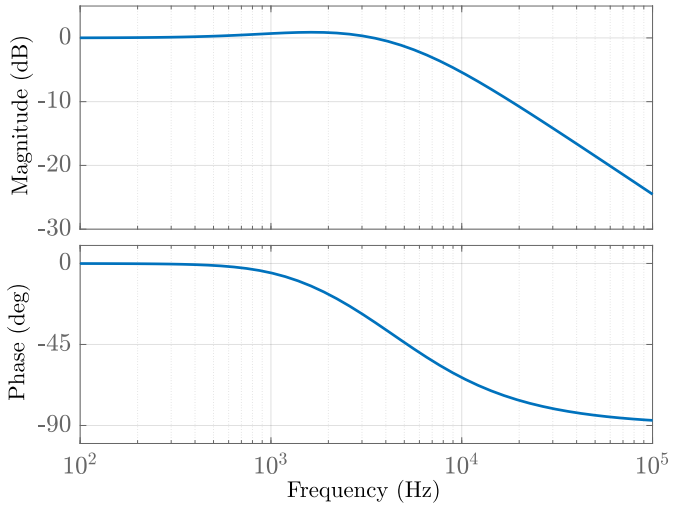


Fig. 4.7. Minimum required peak capacitor voltage (V_C) for a given ϕ and grid-tied operating condition at $V_{dc} = 100$ V and $C = 75$ µF.

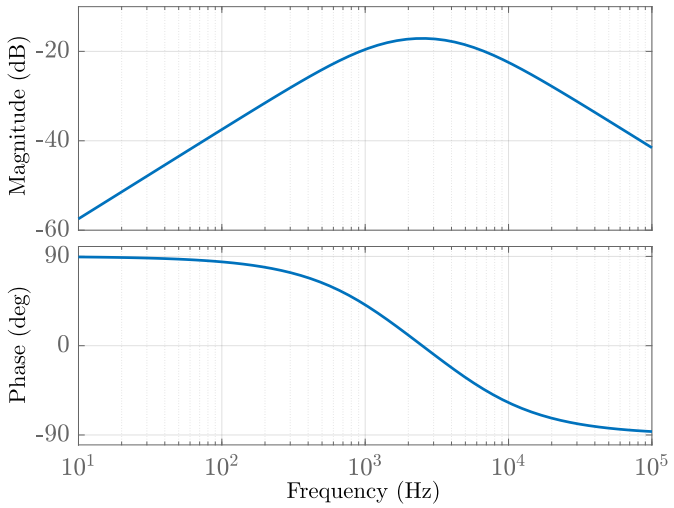
4.3.3 Stability and Sensitivity Analysis

To ensure the stable operation and robust performance of the proposed control strategy, a detailed stability and sensitivity analysis has been conducted

in this section. This analysis is based on the explained closed-loop system in Section 2.2.4.1. The circuit/controller parameters are outlined in Table 4.1. Firstly, the tracking performance and the control input disturbance rejection of the DC input current controller are depicted and verified in Fig. 4.8. As shown in Fig. 4.8(a), the controller can track DC references accurately without any steady-state error. Moreover, Fig. 4.8(b) indicates that control input disturbances are always rejected with more than 17 dB attenuation in the worst case.



(a)

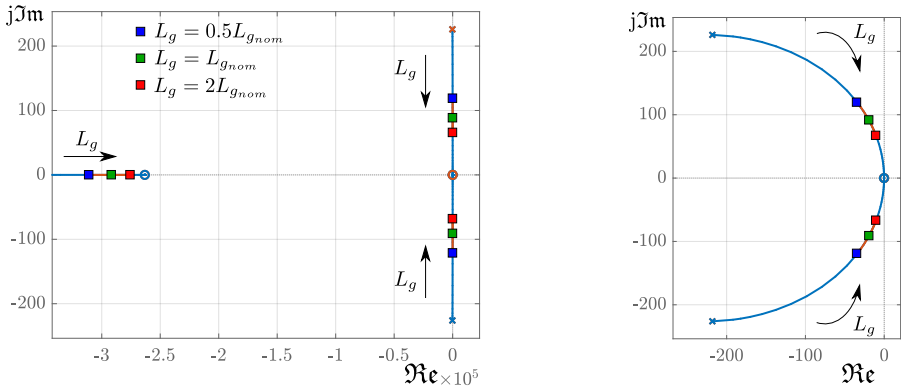


(b)

Fig. 4.8. Bode plot of: (a) closed-loop system: $i_{in}^{\star}$ to i_{in}; (b) i_{in} closed-loop input sensitivity against input disturbances.

Table 4.1
Controller parameters used for simulation and experimental prototype

Parameter	Value
Switching Frequency	100 kHz
$L_{g_{nom}}$	1.2 mH (0.0147 p.u.)
C_a,C_b, r_C	75 µF (0.603 p.u.), 3 mΩ (Film)
L_{in}, r_{in}	0.19 mH (0.0023 p.u.), 60 mΩ
L_g, r_g	1.2 mH (0.0147 p.u.), 80 mΩ
ω	$2\pi \times 50$ rad/s
$C_C(s)$	$0.007 + \frac{0.1}{s}$
$C_{dc}(s)$	$7.103 + \frac{46881}{s}$
$C_{ac}(s)$	$30.079 + \frac{263190s}{s^2+\omega^2}$



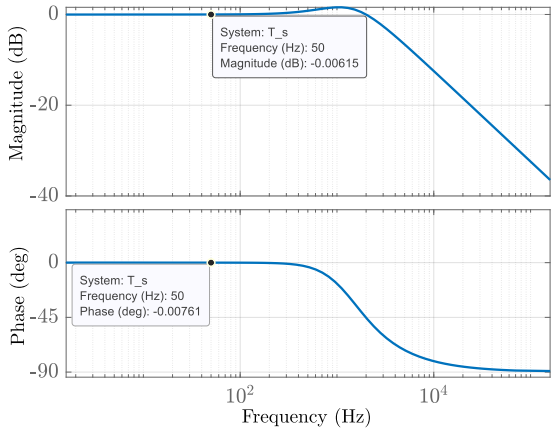
(a) (b)

Fig. 4.9. Root loci plot of the closed-loop poles under varying parameter L_g: (a) Overall view; (b) zoomed-in view.

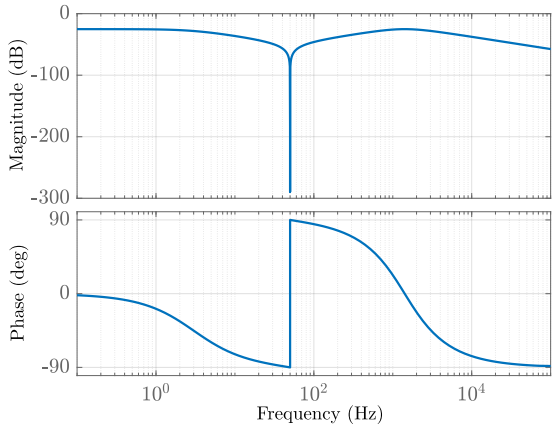
Next, regarding the uncertain value of L_g, a sensitivity analysis based on the root locus method is performed to show the stability of the controller over a wide range of L_g. Fig. 4.9 illustrates the root loci plot of the closed-loop poles for the grid current controller with the variable parameter L_g. As can be seen, over the whole range of possible values of L_g (i.e., from 0 to $+\infty$), all the poles have a negative real part. Additionally, the location of the poles over the range $[0.5L_{g_{nom}}, 2L_{g_{nom}}]$ are shown in red in Fig. 4.9, in which all the real parts are negative. Furthermore, the gain and phase margins of the grid current controller are obtained and depicted in Fig. 4.10(c), in which the gain margin is infinite and the phase margin is 71.8°. Therefore, the stable

operation of the grid current controller is guaranteed.

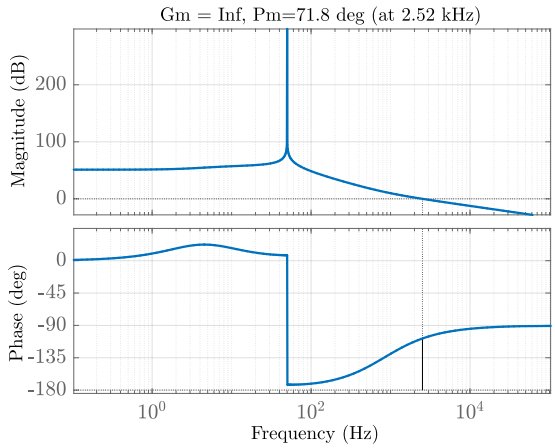
Then, the tracking performance and the control input disturbance rejection of the grid current controller are depicted and verified in Figs. 4.10(a) and 4.10(b), respectively. As shown in Fig. 4.10(a), the controller can track AC references at fundamental grid frequency (50 Hz) accurately without any steady-state error. Moreover, Fig. 4.10(b) indicates that control input disturbances are always rejected with more than 25 dB attenuation in the worst case. It should be noted that any disturbance at the fundamental grid frequency will be rejected perfectly, as shown in Fig. 4.10(b).



(a)



(b)



(c)

Fig. 4.10. Bode plot of: (a) closed-loop system: $i_g^\star$ to i_g; (b) i_g closed-loop input sensitivity against input disturbances; (c) stability margins of the designed i_g control system.

4.4 Comparative Study

As early discussed, applying the APD control to the S^{5}B5L converter can enhance the overall efficiency of the whole conversion system by reducing the current stress profile of the switches, and the input inductor. In the following sub-sections, the performance of the S^{5}B5L converter with and without APD control and a case-to-case comparison over other available solutions/converters are presented.

4.4.1 Performance Investigation of the S^{5}B5L Converter With and Without APD

Figs. 4.11 and 4.12 show typical key waveforms of the S^{5}B5L converter over four fundamental grid cycles, T, connected to a grid with an ideal sinusoidal and polluted voltage, respectively. During the first two cycles, the APD control is OFF; therefore, the input current i_{in} has a dominant double-line frequency ripple. After this, the APD control strategy is activated, and therefore the low-frequency ripple components of i_{in} is diverted to v_c. The variation of the boost duty cycle, D, and the AC modulation reference, u, is due to applying the APD control and the presence of the harmonics in the grid voltage. It is worth mentioning that although the 5L waveform of the inverter output voltage is affected by the APD control, the injected grid current, i_g, still has a low THD due to the closed-loop current control. It should be noted that with the proposed APD control, the maximum AC modulation reference, u, still can vary within its full range (i.e., $[-1, 1]$). However, the maximum inverter voltage, v_{max}, is time-variant under the proposed APD control strategy due to the varying boost duty cycle.

In the following, a comparative study in terms of current stress and power loss distribution on devices of the above-mentioned S^{5}B5L grid-connected converter is conducted to further highlight the performance of the converter with and without APD control strategy. The circuit/controller specifications for this comparative study have been tabulated in Table 4.1, while PLECS software is used to perform the simulations. Herein, to target a polluted grid with the presence of low-frequency harmonics, the grid voltage is assumed as follows:

$$v_g = 320[\cos(\omega t) + 0.1\cos(3\omega t) + 0.05\cos(5\omega t)]. \tag{4.38}$$

As for comparative analysis, two different case studies based on the availability of the DC input voltage source, i.e., $V_{dc} = 100$ V and $V_{dc} = 50$ V, are considered, while the rated injected power to the grid is assumed to be the same as $P_g = 2$ kW. As can be seen from Figs. 4.13(a) and (b), there is a

clear reduction in RMS values of the current stress profile on different circuit devices when the APD control is activated. This improvement is more visible when a higher value of the boost duty cycle or a lower value of the DC input voltage is adopted, as can be confirmed by Figs. 4.13(a) and (b). It should be noted that the RMS currents of the involved components at $V_{dc} = 100$ V and $V_{dc} = 50$ V are not fully complying the power-balance theory when the APD control is OFF, i.e., the RMS value of the DC input current in the first case is not half of the second case, as L_{in} tends to resonate with C_a, C_b due to the nature of the original circuit.

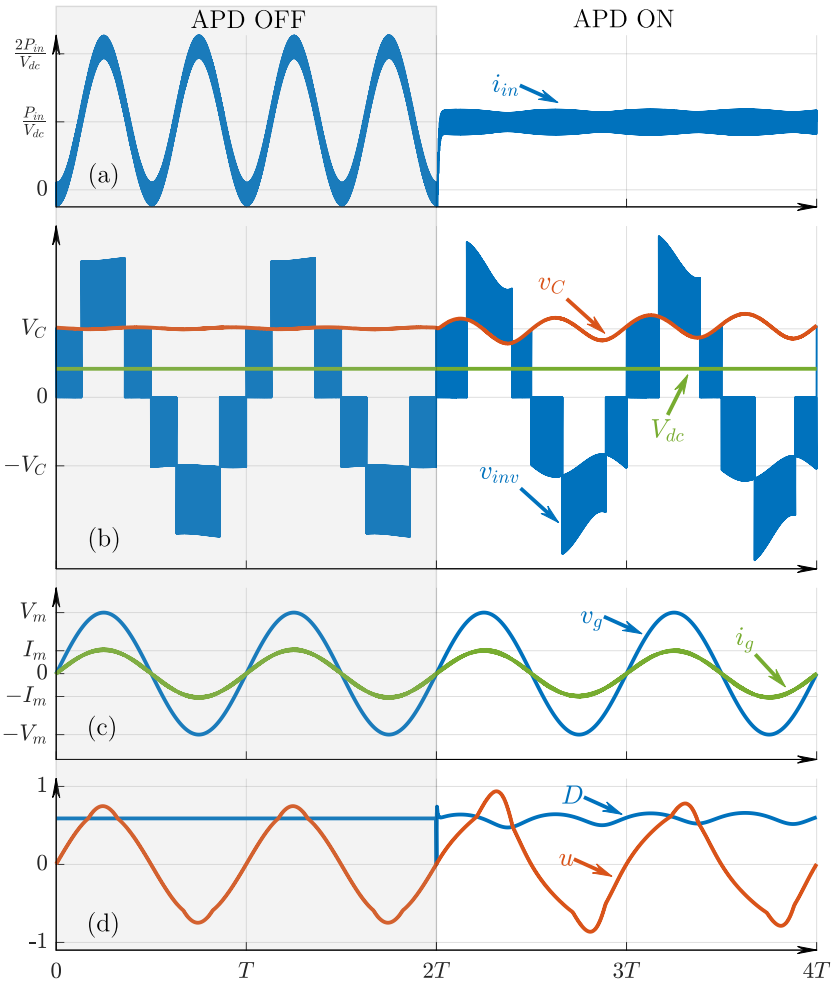


Fig. 4.11. Typical key operating waveforms of the S^{5}B5L inverter under ideal grid-connected condition before and after enabling the proposed APD control scheme: (a) input current (i_{in}); (b) DC input voltage (V_{dc}), capacitor voltage (v_C), and inverter output voltage (v_{inv}); (c) pure sinusoidal grid voltage (v_g), and grid current (i_g); (d) boost duty cycle (D), and AC modulation reference (u).

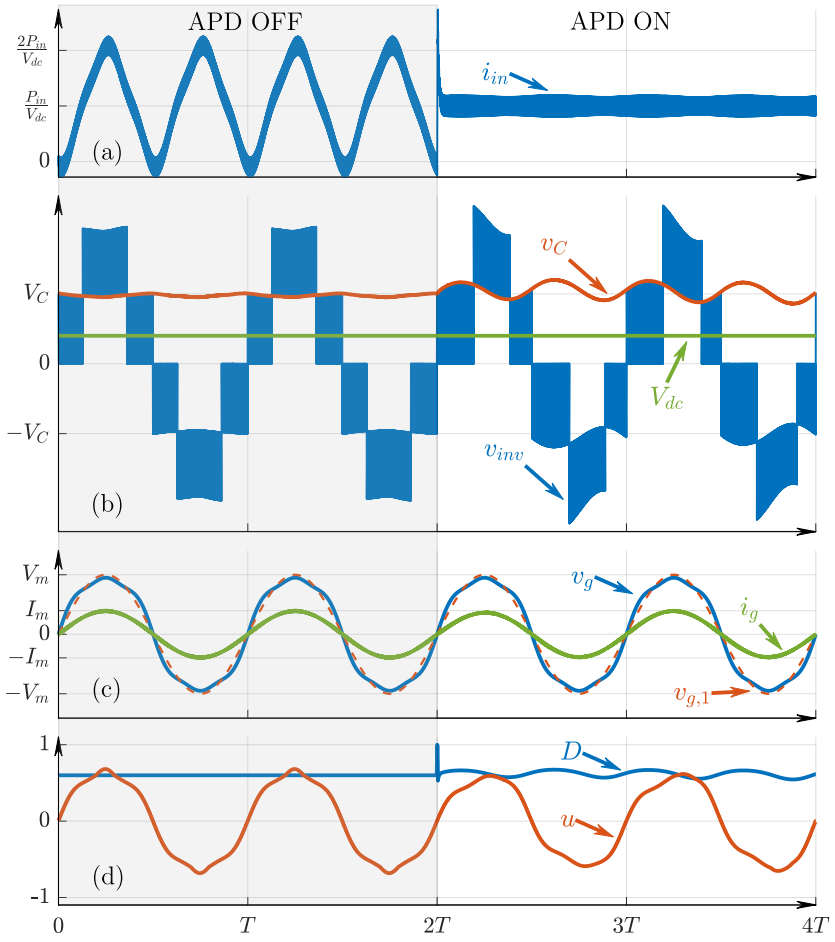


Fig. 4.12. Typical key operating waveforms of the S^{5}B5L inverter under polluted grid-connected condition before and after enabling the proposed APD control scheme: (a) input current (i_{in}); (b) DC input voltage (V_{dc}), capacitor voltage (v_C), and inverter output voltage (v_{inv}); (c) polluted grid voltage (v_g) with its fundamental harmonic ($v_{g,1}$), and grid current (i_g); (d) boost duty cycle (D), and AC modulation reference (u).

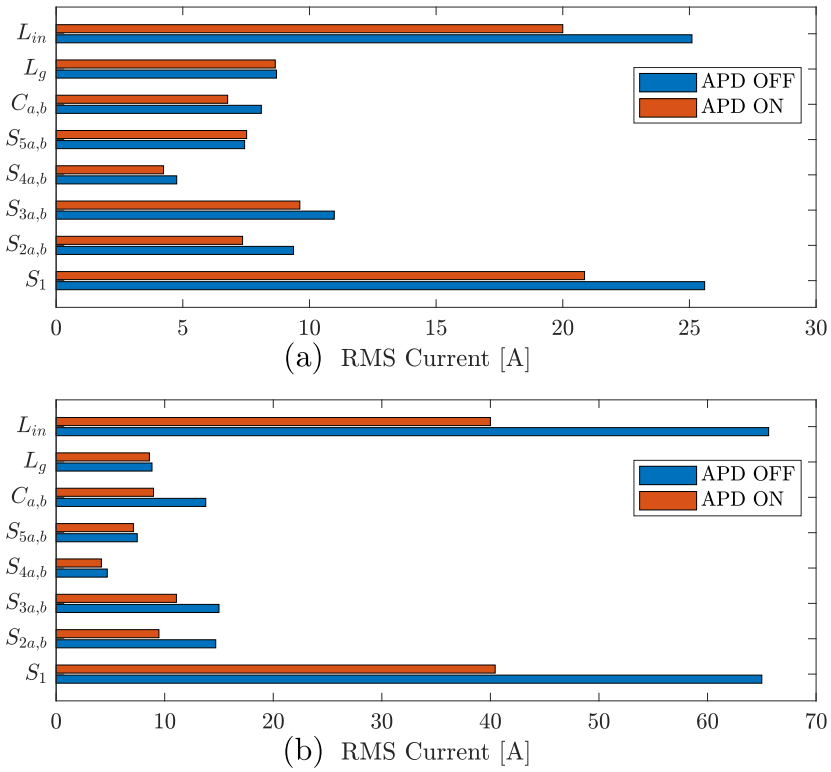
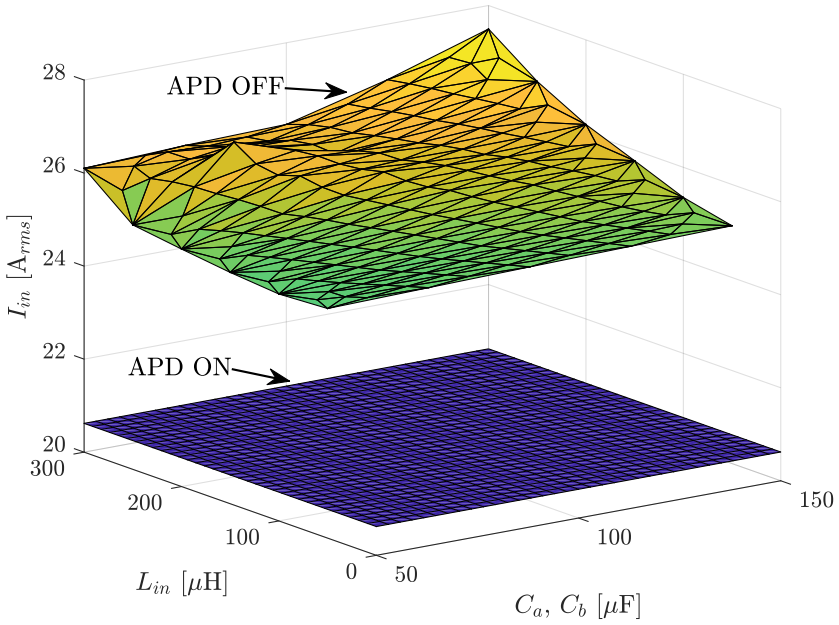


Fig. 4.13. RMS currents using PLECS at $P_g = 2$ kW without and with APD control at: (a) $V_{dc} = 100$ V; (b) $V_{dc} = 50$ V.

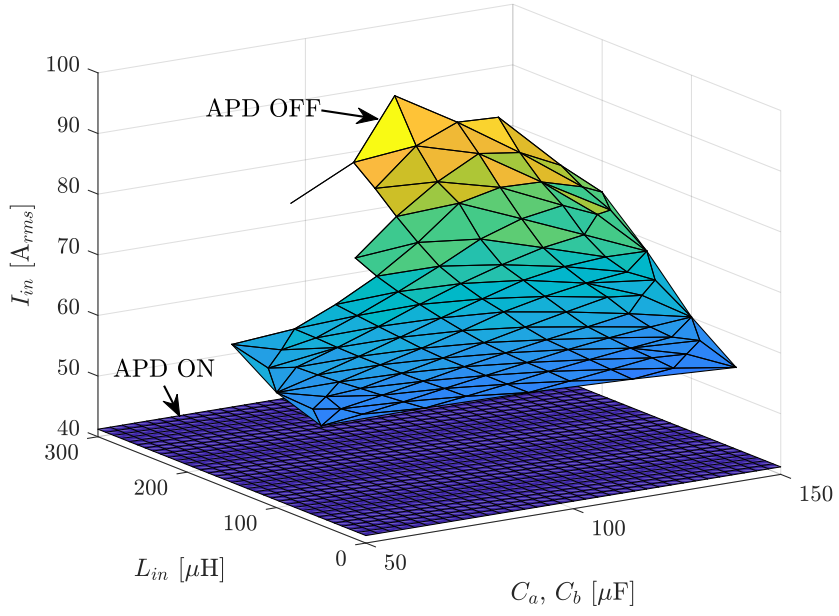
Since the proposed converter is a nonlinear dynamic system with time-variant coefficients in its state-space model, obtaining an accurate closed-form expression for the RMS input current is not feasible [173]. However, a simulation-based sensitivity analysis has been performed to investigate the impact of the passive circuit components (L_{in} and C_a,C_b) on the RMS input current values for both multi-PR and proposed control methods at $V_{dc} = 100$V and $V_{dc} = 50$V. As shown in Fig. 4.14, the RMS input current is always lower when the APD control is enabled. In the case of multi-PR control, due to the resonant energy exchange between L_{in} and C_a,C_b, at certain passive components and D values, RMS input current grows excessively. This phenomenon also can be described based on the equivalent resonant frequency of the DC input side of the converter. When the above-mentioned resonant frequency is close to the grid power harmonics, a large low-frequency ripple on the passive components is expected, as shown in Fig. 4.14. Moreover, the resultant large ripple can lead to system instability in extreme cases (missing areas when the APD is OFF in Fig. 4.14). However, with the proposed APD control strategy, i_{in} is directly controlled by the PI controller

$C_{dc}(s)$ to achieve a flat DC input current and suppress the resonance between C_a, C_b and L_{in}. It is worth noting that in this case, since $v_{L_{in}} = V_{dc} - v_C$, v_C is acting as an input disturbance for the PI controller $C_{dc}(s)$ [see Fig. 4.2(c)]. Considering the closed-loop tracking and input disturbance rejection performance of the PI controller $C_{dc}(s)$ shown in Fig. 4.8, the mentioned resonance is eliminated due to the significant disturbance rejection provided by $C_{dc}(s)$. Therefore, by using the proposed APD control strategy, not only the current stress on the passive and active components can be reduced, but also it improves the overall stability and reliability of the system.

Moreover, a loss analysis has been performed in PLECS to investigate the impact of the proposed APD control method on the power loss profile of S^5B5L converter. The details of this analysis can be found in Chapter 3. As a result, the reduction in RMS values of the current stress in different circuit components with the activation of the APD control can clearly reduce the conduction losses of devices as demonstrated in Figs. 4.15(a) and (b). Therefore, the major reduction of the losses is related to the input inductor, L_{in}, since the input current passing through it does not have any pulsating low-frequency content by applying the APD control. Furthermore, the conduction loss of the switch S_1 is also reduced, which is more significant for the higher range of boost duty cycle or lower DC input voltage. Regarding this, it can be confirmed that the overall performance of the discussed S^5B5L grid-connected converter from the overall efficiency viewpoint is enhanced through applying an APD control, while the life-span, reliability, and overall temperature of devices can also be improved.



(a)



(b)

Fig. 4.14. RMS input current using PLECS at $P_g = 2$ kW without and with APD control at: (a) $V_{dc} = 100$ V; (b) $V_{dc} = 50$ V.

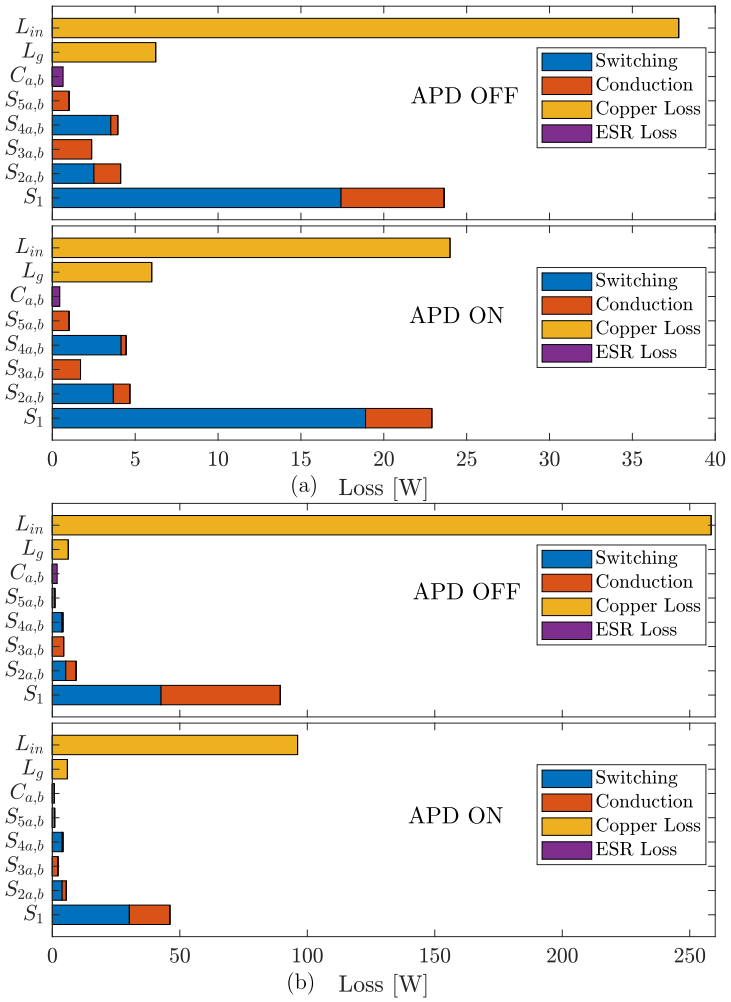


Fig. 4.15. Loss breakdown using PLECS at $P_g = 2$ kW without and with APD control at: (a) $V_{dc} = 100$ V; (b) $V_{dc} = 50$ V.

In addition, as another practical example, the proposed control strategy has been integrated in a grid-connected PV system with an additional MPPT controller (see Fig. 4.3). The simulated results of such a configuration have been shown in Fig. 4.16. A similar approach can be followed to control the DC input voltage in the case batteries during constant-voltage phase of the charging process.

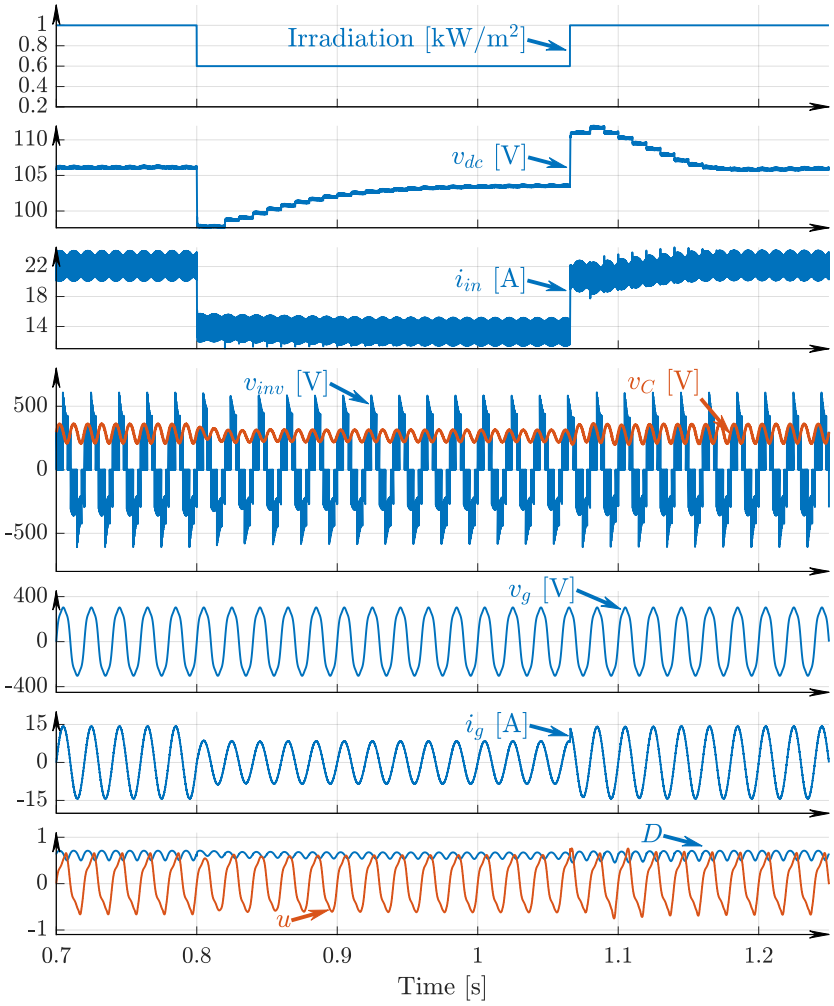


Fig. 4.16. Simulation results of a 2 kW grid-connected PV system with the proposed APD control and MPPT functionality.

4.4.2 A Comparison over Other Available Topologies with APD Control

The circuit features and characteristics of the discussed S^{5}B5L grid-connected converter over some other counterparts with APD control have been summarized in Table 4.2. The comparative items are the number of power conversion stages, the number of converter output voltage levels, the voltage rating of the capacitors and their capacitance, the reported value of the boost and filter inductors L_{in}, and L_g, the rated power and the switching frequency, and the reported overall efficiency at the rated power. As it can be inspected, the recently proposed S^{5}B5L grid-connected converter is the only available

topology that can generate a 5L output voltage with a single-stage integrated APD. The larger number of inverter output voltage levels leads to incorporating a smaller filter inductor L_g, while the voltage rating of the capacitors is only 250 V, which is half of the inverter peak output voltage using a comparably small capacitance. Here, although the overall efficiency of the S^5B5L converter with APD control is less than some other reported counterparts, the applied switching frequency of the proposed method is almost five times larger than most other works in this comparison. Moreover, none of the reported systems has considered a polluted grid voltage in their integrated control strategy, while this scenario has been extensively addressed in the current work. It is worth mentioning that the reported efficiency for some of the works considered in this comparison does not include the boost stage efficiency.

Table 4.2
A circuit characteristics-based comparison among different available topologies with APD control

Topology	No. of Stages	No. of Levels	Cap. Voltage Rating	Cap. Value	L_{in} value	L_g value	Rated Power, f_{sw}	Reported Efficiency
Ref. [128]	2	3	450V-600V	2×60µF	NA	2×1mH	1kW, 20kHz	89.5% @ 1kW
Ref. [130] (Fig. 1a)	2+Buffer	3	400V-700V	30µF	NA	1mH	2kW, 30kHz	97% @ 2kW
Ref. [130] (Fig. 1f)	2+Buffer	3	350V	75µF	NA	1mH	2kW, 30kHz	96.1% @ 2kW
Ref. [28]	2	2	400V	30µF	NA	2×2.2mH	1kW, 19kHz	92% @ 1kW
Ref. [133]	2	3	450V	430µF	8mH	2×7mH	2.4kW, 20kHz	NA
Ref. [135]	1	2	250V	2×20µF	20µH	3mH, 3.3mH	180W, 20kHz-300kHz	93% @ 180W
Ref. [136]	2	2	550V	45µF	230µH	230µH	3kW, 100kHz	95.6% @ 3kW
Ref. [138]	1	2	400V	2×220µF	2.75mH	2×2mH	180W, 10kHz	NA
Ref. [139]	2	3	600V	100µF	3mH	2.2mH	2kW, 20kHz	96% @ 2kW
Ref. [140]	1	3	450V	22µF	30µH	1.5mH	400W, 25kHz	95% @ 400W
S^5B5L Converter	1	5	250V	2×75µF	190µH	2×0.6mH	2kW, 100kHz	95.2% @ 2kW

Table 4.3
Components used in the experimental prototype

Element	Type and Description
Power Switches	UJ4C075018K4S (750 V, 18 mΩ)
Controller	DSP-TMS320F28379D
Gate Drivers	UCC21710
Isolated DC-DC Converters	MGJ2D121505SC
Voltage/Current Sensors	AMC3301

4.5 Experimental Results

To validate the effectiveness of the APD control applied to the described S^5B5L converter, extensive experimental results from a 2 kW laboratory-built prototype shown in Fig. 4.17 under the grid-connected environment are presented in this section. The circuit specifications and closed-loop control parameters are outlined in Table 4.1 and Table 4.3, while three DC power supplies (EA-PSI-9360-12) have been connected in parallel to provide a sufficient amount of input current and feed the converter. As for the grid-tied operation, a polluted grid voltage per (4.38) is emulated with a four-quadrant grid simulator (REGATRON TC30.528.43-ACS). A DSP (TMS320F28379D) has also been used to implement the proposed controller.

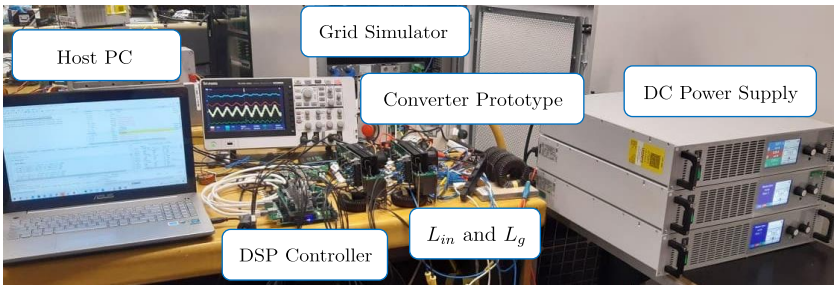


Fig. 4.17. A view of the experimental setup.

As for the first experimental test, the DC input voltage is set at 100 V, while based on the peak amplitude of the fundamental component of the grid voltage and with respect to Fig. 4.4, a voltage reference is selected as for the $V_C^\star$ in the APD control loop. Hence, with respect to Figs. 4.2(c) and (d), the boost duty cycle D and the AC modulation reference u are attained and passed to the PS-PWM stage described in [173] to provide the required gate switching pulses. Figs. 4.18(a) and (b) show the details of this experimental test during a steady-state condition. As can be seen, by applying the APD

control, the input current is free from any double-line frequency and only contains the high-frequency content caused by the switching action. The average value of the input current is around 20 A with around 13 A as the peak value of the injected grid current. Here, the 5L inverter output voltage in the presence of a polluted grid voltage has been generated, while the voltage across both capacitors is balanced at 250 V with a double-line frequency ripple. The distortion in the 5L inverter output voltage is due to the small value of the capacitors as reported in [173], while the THD value of the injected grid current is less than one percent at 200 kHz apparent switching frequency at the AC side. The dynamic results before and after applying the APD at 1 kW injected grid power have also been demonstrated in Fig. 4.18(c). The APD action can clearly be seen through these results as the low-frequency ripple from the input current has been transferred to the voltages of the capacitors.

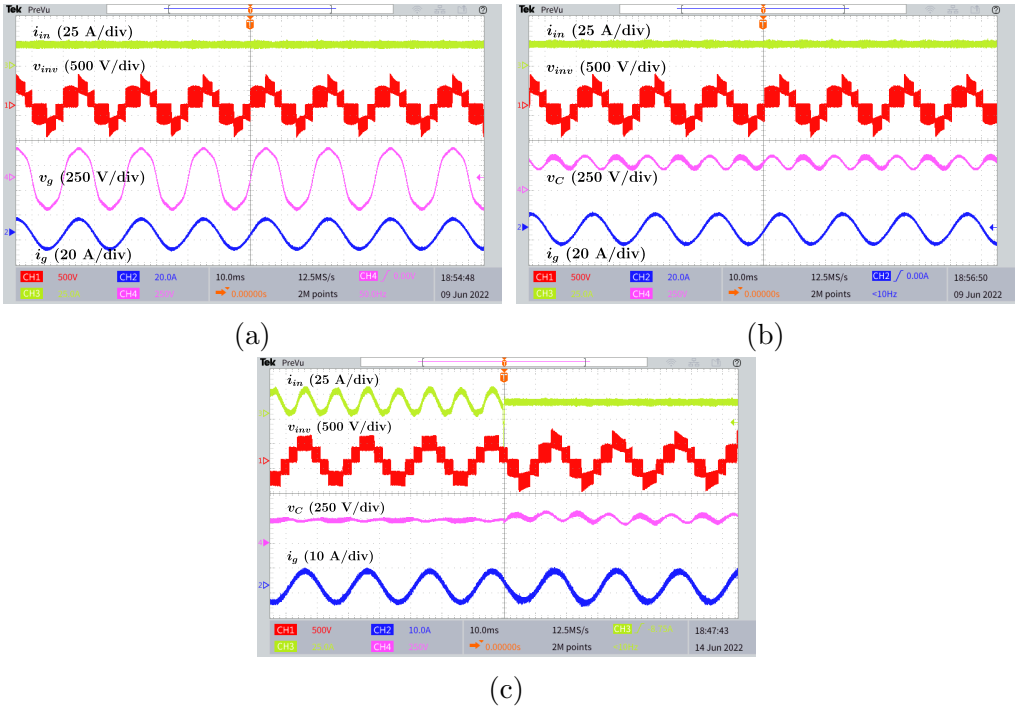


Fig. 4.18. Experimental results under the polluted grid-connected condition at $V_{dc} = 100$ V and $C = 75$ µF: (a) the input current, inverter output voltage, grid voltage, and grid current at $P_g = 2$ kW; (b) the input current, inverter output voltage, capacitor voltage, and grid current at $P_g = 2$ kW; (c) the input current, inverter output voltage, capacitor voltage, and grid current at $P_g = 1$ kW before and after enabling the proposed APD control.

The respective reactive power support results under the leading and lagging power factor conditions, i.e., $P_g = 1$ kW and $Q_g = \pm 1$ kVAr, are shown in Fig. 4.19(a) and (b), respectively. As can be seen, under the APD control strategy, the input current is still free from low-frequency components in both reactive power compensation cases. The bidirectional power flow performance of the converter confirming absorbing power from the grid and injecting power into the grid under the grid-connected and APD control condition has also been shown in Fig. 4.19(c). Here, an electronic load is connected in parallel to the DC power supply to absorb the power from the grid flowing in the reverse direction. As can be realized, all the output voltage levels have been generated, while the input current direction is changed from a negative value (absorbing power from the grid) to a positive value (injecting power into the grid).

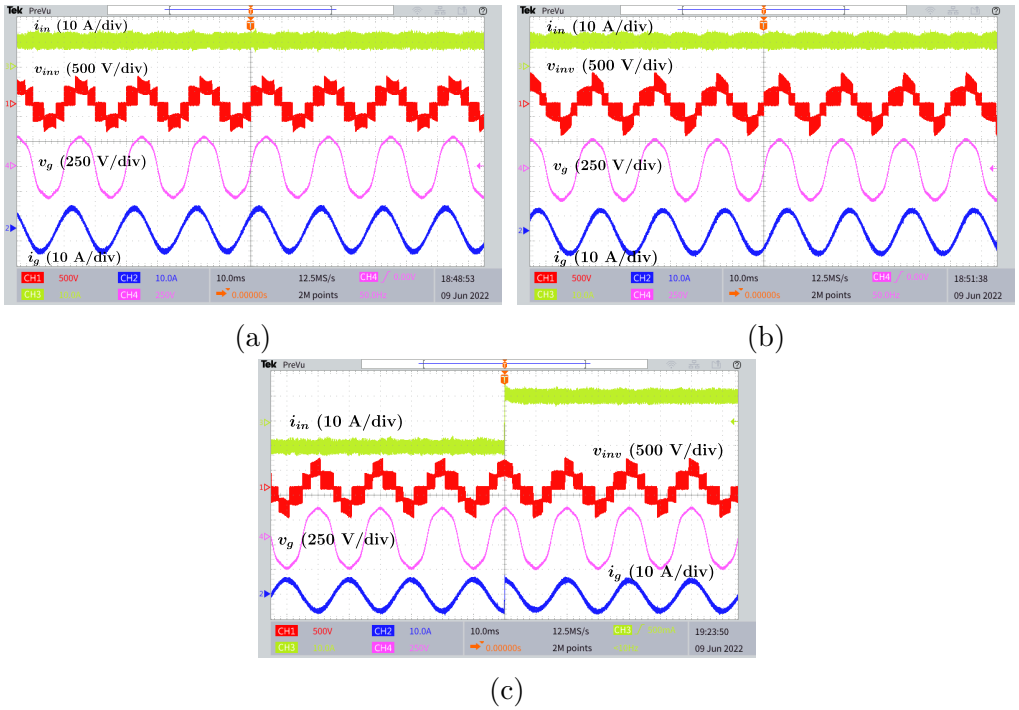


Fig. 4.19. Experimental results under polluted grid-connected condition, $C = 75$ µF, and $V_{dc} = 100$ V: (a) the input current, the inverter output voltage, the grid voltage, and the grid current at $P_g = 1$ kW, $Q_g = +1$ kVAr; (b) the input current, the inverter output voltage, the grid voltage, and the grid current at $P_g = 1$ kW, $Q_g = -1$ kVAr; (c) the input current, the inverter output voltage, the grid voltage, and the grid current showing bidirectional power flow operation from $P_g = -1$ kW to $P_g = +1$ kW.

To confirm the dynamic voltage conversion gain of the converter while meeting the peak grid voltage requirement, another dynamic test with a ramp change in the DC input voltage, i.e., from 60 V to 120 V, and with the proposed APD control strategy is applied to the described S^5B5L converter. Details of this dynamic test while showing the DC input voltage, the input current, the 5L inverter output voltage, the polluted grid voltage, the voltage across the capacitors, and the injected grid current waveform at 1 kW are illustrated in Fig. 4.20(a)-(c). Here, even though the DC input voltage is getting changed with a ramp trend, the peak 5L output voltage of the inverter is kept fixed at around 500 V, i.e., two times the voltage across each of the capacitors, which is enough to inject the power to a grid with a maximum peak voltage of 320 V as for its fundamental harmonic.

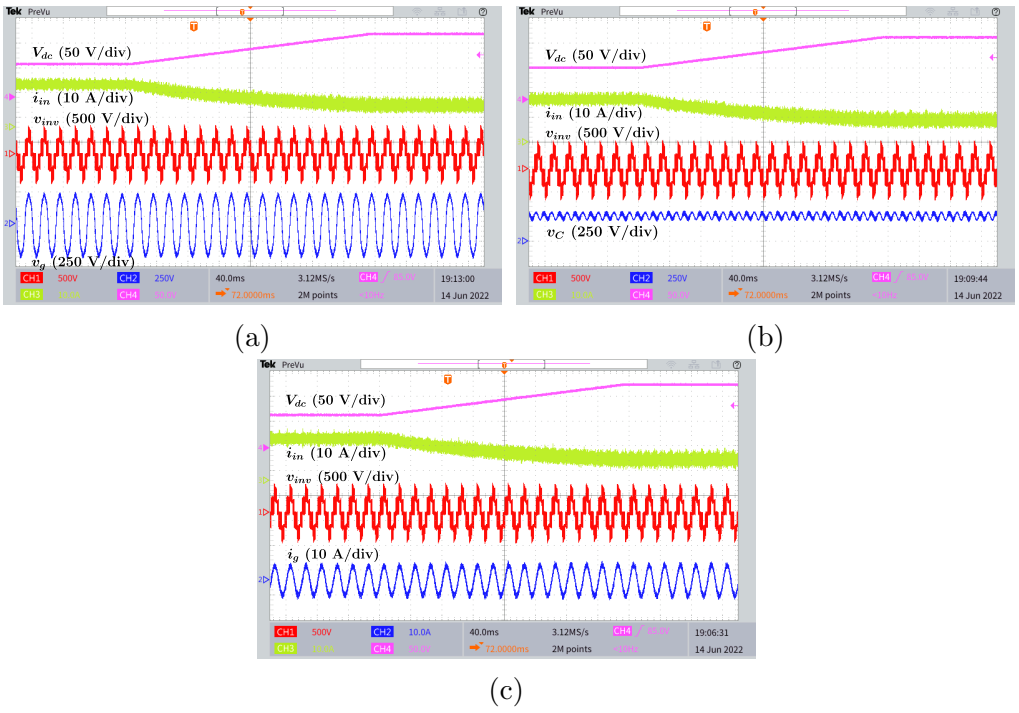
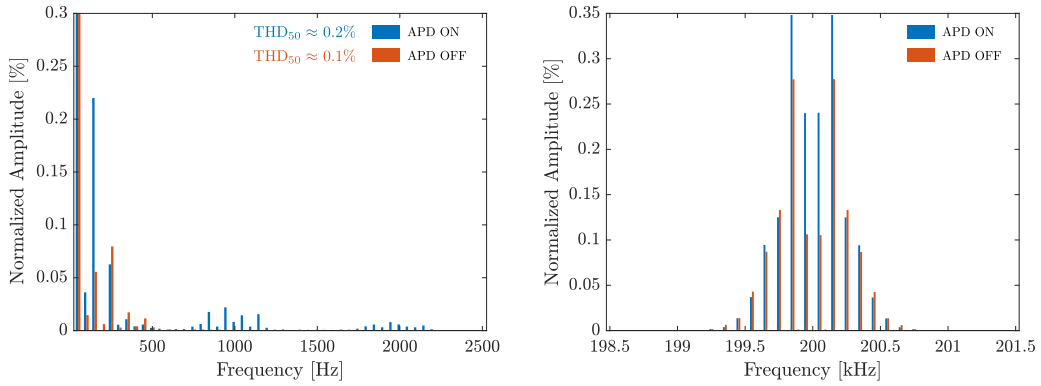


Fig. 4.20. Experimental results under polluted grid-connected condition, $P_g = 1$ kW, $C = 75$ µF, and $V_{dc} = 60$ V to $V_{dc} = 120$ V: (a) the DC input voltage, the input current, the inverter output voltage, and the grid voltage; (b) the DC input voltage, the input current, the inverter output voltage, and the capacitor voltage; (c) the DC input voltage, the input current, inverter output voltage, and the grid current.

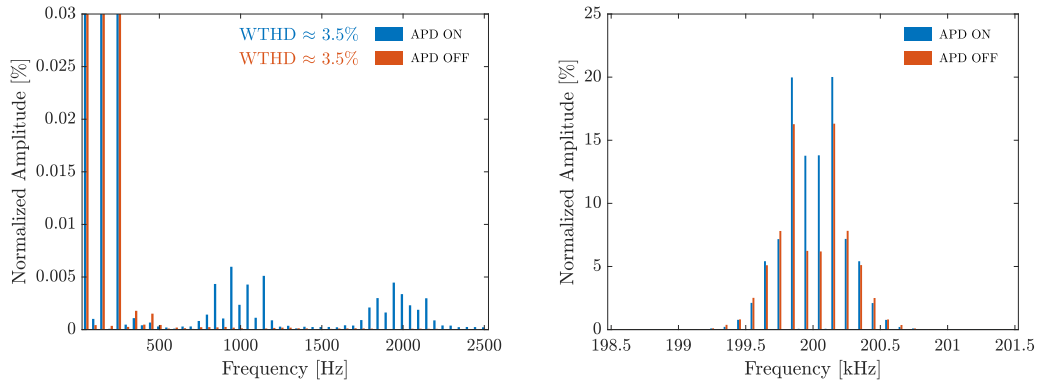
One of the important aspects of any grid-connected power converter is its power quality. As can be seen throughout the experimental results, the

proposed APD control strategy affects the inverter output voltage. This change can be observed in the frequency spectrum view of v_{inv} and i_g, as shown in Fig. 4.21. As can be seen in Fig. 4.21(a), the proposed APD control causes a slight increase in low-frequency harmonics of i_g. More precisely, THD values of i_g using multi-PR and proposed control methods are 0.1% and 0.2%, respectively. These values are well within the limits of the available standards (e.g., IEEE 519-2014). Moreover, Fig. 4.21(b) depicts the low- and high-frequency harmonics of v_{inv}. As can be seen, the difference in low-frequency harmonics is negligible, and the weighted THD (WTHD) values of v_{inv} for both multi-PR and the proposed APD control methods are practically identical. Therefore, a similar grid-interface filter can be used for both cases to achieve the same level of THD. It is worth mentioning that there is a large difference between the high-frequency harmonics of v_{inv} with multi-PR and the proposed controllers. However, these harmonic clusters are located at two-times switching frequency (i.e., at 200 kHz for the switching frequency of 100 kHz), where the grid-interface filter impedance is very high. Hence, the impact of high-frequency harmonics on the THD of i_g is not significant.

Finally, using a Yokogawa WT1806E precision power analyzer and the PLECS model of the converter, the overall DC-AC conversion efficiency of the S^5B5L converter at $V_{dc} = 100$ V, and $V_{dc} = 50$ V under a wide range of the injected grid power with and without the APD control is measured and the results are shown in Fig. 4.22(a), and (b), respectively. As can be seen, the results confirm the expectation obtained from the simulation shown in Figs. 4.13 and 4.15, in which through applying the APD control, the overall efficiency of the system is improved by approximately one percent at $V_{dc} = 100$ V and more than five percent at $V_{dc} = 50$ V, while the conduction losses of the switches and copper losses of the input boost inductor are reduced.

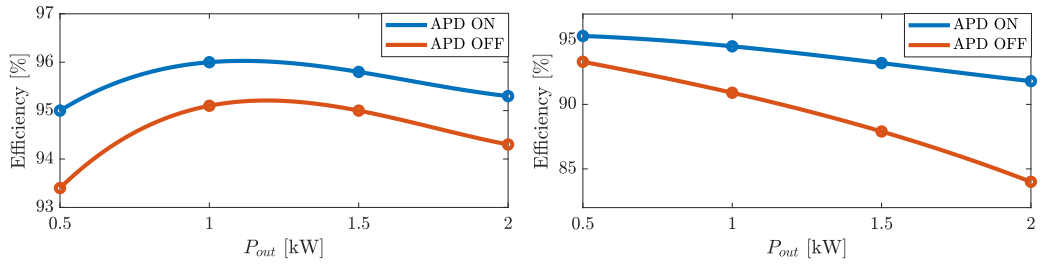


(a)



(b)

Fig. 4.21. FFT analysis results of the inverter output at $C = 75$ µF, $P_g = 2$ kW (unity power factor), and polluted grid voltage: (a) i_g; (b) v_{inv}.



(a) (b)

Fig. 4.22. Efficiency comparison with and without APD control at $C = 75$ µF, unity power factor, and polluted grid voltage: (a) $V_{dc} = 100$ V; (b) $V_{dc} = 50$ V.

4.6 Conclusion

This chapter has presented a grid-connected system with an integrated APD capability based on the recently proposed S^5B5L converter. Leveraging the integrated capacitors in S^5B5L converter, the APD functionality has been achieved without adding any extra circuit components to the entire system. The topology has been connected to a grid polluted with several low-frequency harmonics. A GVO-based synchronization mechanism has also been designed and included to inject a pure sinusoidal grid current, decomposing the harmonic components of the grid voltage, and providing a clean feed-forward signal, including all the expected low-frequency harmonics. This allows for developing a tailored control strategy based on the S^5B5L structure using a single PR controller for the grid current injection with a filtered feed-forward term. A comparative study has also been conducted to evaluate the effectiveness of the proposed control strategy applied to the S^5B5L converter from the current stress on devices and the power losses of the active/passive elements viewpoints. Moreover, a sensitivity analysis for the values of the passive components at different operating points has been performed. Extensive closed-loop experimental results obtained from a 2 kW laboratory-based prototype under the grid-connected condition are presented to validate the theoretical analysis of this proposal. As evidenced by these experimental results, the proposed solution effectively eliminated the low-frequency harmonic content from the input power drawn from the DC source without enlarging the passive elements. Consequently, the conduction losses are reduced, and thus, the overall efficiency of the entire conversion system is improved.

As a direction for future work, some of the limitations of the presented control strategy can be improved. For example, the LUTs used for average capacitor voltage reference can be replaced by closed-form mathematical expressions. Another limitation is increasing the voltage stress on the circuit elements such as capacitors and power switches, which can be potentially improved through converter topologies or control strategies. Finally, in the cases that the DC input source can provide some of the double-line frequency ripple power, there is an opportunity to adjust the trade-off between voltage stress and input current ripple. This case has been investigated in more detail in the following chapter.

Chapter 5

Flexible Active Power Decoupling for A Single-Stage Single-Phase Grid-Connected Inverter

In this chapter, the concept of APD is extended to a more general form. A flexible APD idea is presented to enable adjusting the inherent tradeoffs present in a conventional APD method. In the proposed method, the ripple factor can be varied based on the application requirements and targets, achieving a higher flexibility in controlling system's operating conditions.

5.1 Introduction

In the previous chapter, an integrated active power decoupling technique has been implemented with the proposed S^5B5L-VSI to eliminate the double-line frequency ripple at the DC port without any additional components. One of the limitations in complete elimination of double-line frequency ripples on the DC input current is the increased capacitor voltage ripple and increased voltage stress on the circuit components. To have a better control over these tradeoffs, a flexible APD (FAPD) approach is introduced. A qualitative comparison between the operating conditions without APD, with conventional APD, and with FAPD is depicted in Fig. 5.1. In the following section, the working principles of conventional APD and the proposed FAPD approaches are presented.

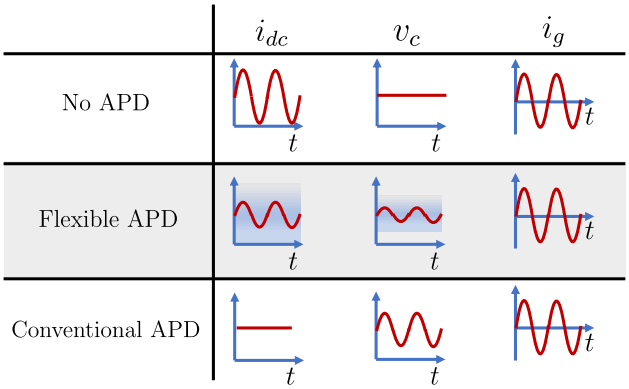


Fig. 5.1. A qualitative comparison based on the operating conditions without APD, with conventional APD, and with the proposed FAPD methods.

5.2 APD Working Principle

In this section, the general equations of an APD system are derived and presented step by step. Considering a sinusoidal grid voltage and injected grid current, the instantaneous grid power can be calculated as:

$$v_g = V_m \sin(\omega t) \tag{5.1}$$

$$p_g = v_g i_g = V_m \sin(\omega t) I_m \sin(\omega t + \phi) \tag{5.2}$$

where V_m, I_m, and ϕ are the peak grid voltage, peak grid current, and the phase shift between the grid voltage and current, respectively.

Knowing the fact that any converter has some internal losses, the total inverter input power is:

$$p_{inv} = p_g + p_{loss,inv} \tag{5.3}$$

where $p_{loss,inv}$ is the instantaneous inverter power loss. Assuming an acceptable efficiency of the power converter, the total inverter power can be approximated as:

$$p_{inv} = p_{inv,dc} + p_{inv,ac} = p_g = \frac{V_m I_m}{2} \cos(\phi) - \frac{V_m I_m}{2} \cos(2\omega t + \phi) \tag{5.4}$$

$$p_{inv,dc} = \frac{V_m I_m}{2} \cos(\phi) \tag{5.5}$$

$$p_{inv,ac} = -\frac{V_m I_m}{2}\cos(2\omega t + \phi) \tag{5.6}$$

where $p_{inv,dc}$ and $p_{inv,ac}$ are the DC and ripple components of the instantaneous inverter power. As can be seen from (5.4)-(5.6), the ripple power of the inverter has a double-line frequency and its amplitude is directly proportional to V_m and I_m. A buffer circuit can be utilized to compensate for this ripple power. The following equation shows the power balance of the whole system, including a buffer unit:

$$p_{in} = p_{inv} + p_{buf} + p_{loss,buf} \tag{5.7}$$

where p_in, p_{buf}, and $p_{loss,buf}$ are the input power, buffer circuit power and its losses, respectively. By neglecting the losses and substituting (5.4) into (5.7), the total input power can be calculated as:

$$p_{in} = p_{inv,dc} + p_{inv,ac} + p_{buf}. \tag{5.8}$$

Generally, the aim of a buffer circuit is to completely nullify the AC component of the inverter power. However, it can cause some restrictions in terms of the required passive element sizing and voltage/current stress of the active and passive components. In the next section, a dynamic and flexible approach is introduced to overcome the mentioned limitations.

5.3 FAPD Working Principle

As mentioned in the previous section, a buffer circuit is conventionally included to eliminate the AC ripple power of the single-phase inverters. To generalize this approach, an FAPD method is proposed and explained in this section.

Considering (5.8), the buffer can be used to cancel only a portion of the AC ripple:

$$p_{buf} = -\gamma p_{inv,ac} \tag{5.9}$$

where γ is the ripple compensation factor. Substituting (5.9) into (5.8) gives the resultant input power:

$$p_{in} = p_{inv,dc} + (1-\gamma)p_{inv,ac}. \tag{5.10}$$

Note that if γ=1, the buffer cancels the AC ripple completely, similar to the conventional buffer control methods. Assuming a constant voltage at the DC side (V_{in}), the input current can be calculated:

$$i_{in} = \frac{p_{in}}{V_{in}} = \frac{V_m I_m}{2V_{in}} \big[\cos(\phi) - (1-\gamma)\cos(2\omega t + \phi) \big]. \tag{5.11}$$

The proposed FAPD method can be implemented with a conventional two-stage system as well as some single-stage boost-based inverters with dynamic gain. Therefore, the FAPD method is formulated based on the proposed S^{5}B5L-VSI in the following.

The instantaneous power delivered or absorbed by the buffer circuit is equal to sum of the powers of its energy storing-elements (L_{in} and C_a,C_b):

$$p_{buf} = p_{L_{in}} + p_{C_t} \tag{5.12}$$

where $p_{L_{in}}$ and p_{C_t} are the instantaneous power of L_{in} and C_t, respectively. C_t is the equivalent capacitance of C_a and C_b in parallel connection ($C_t = C_a + C_b$).

The instantaneous power of the input inductor (L_{in}) can be expressed as:

$$p_{L_{in}} = v_{L_{in}} i_{in} = L_{in} i_{in} \frac{di_{in}}{dt} \tag{5.13}$$

where $v_{L_{in}}$ is the voltage across L_{in}. By substituting (5.11) into (5.13), $p_{L_{in}}$ can be derived:

$$p_{L_{in}} = 2\omega L_{in}(1-\gamma)\frac{V_m^2 I_m^2}{4V_{in}^2}\left[\cos(\phi)\sin(2\omega t+\phi) - \frac{1-\gamma}{2}\sin(4\omega t+2\phi) \right] \tag{5.14}$$

Similarly, the instantaneous power of C_t can be obtained:

$$p_{C_t} = v_{C_t} i_{C_t} = C_t v_{C_t} \frac{dv_{C_t}}{dt} = p_{buf} - p_{L_{in}} \tag{5.15}$$

where v_{C_t} is the voltage across C_a or C_b (it should be noted that the $V_{C_a} = V_{C_b}$ during the normal operation of S^{5}B5L-VSI).

$$p_{C_t} = \frac{\gamma V_m I_m}{2}\cos(2\omega t+\phi) - \omega L_{in}(1-\gamma)\frac{V_m^2 I_m^2}{4V_{in}^2}\left[\cos(\phi)\sin(2\omega t+\phi) - \frac{1-\gamma}{2}\sin(4\omega t+2\phi) \right] \tag{5.16}$$

The voltage across the equivalent buffer capacitance (v_{C_t}) can be calculated by combining (5.15) and (5.16). The resultant differential equation is a separable equation and its solution is:

$$v_{C_t} = \sqrt{A_1 \sin(2\omega t+\phi) + A_2 \cos(2\omega t+\phi) + A_3 \cos(4\omega t+2\phi) + c} \tag{5.17}$$

$$A_1 = \frac{\gamma V_m I_m}{2\omega C_t} \tag{5.18}$$

$$A_2 = \frac{L_{in}(1-\gamma)V_m^2 I_m^2}{2C_t V_{in}^2} \tag{5.19}$$

$$A_3 = \frac{-L_{in}(1-\gamma)^2 V_m^2 I_m^2}{8C_t V_{in}^2} \tag{5.20}$$

where c is the integration constant. Note that the average voltage (dc component) of C_a or C_b can be changed by using this constant.

5.4 Control Strategy

In this section, the proposed control strategy and its building blocks are illustrated and explained in detail. Fig. 5.2 depicts the overall structure of the controller and involved signals. The main block is based on a continuous control set model predictive controller (CCS-MPC). The reasons for choosing such a scheme are including excellent dynamic performance in transients, inherent noise rejection capability, bilinear nature of the system, and compatibility with PS-PWM method.

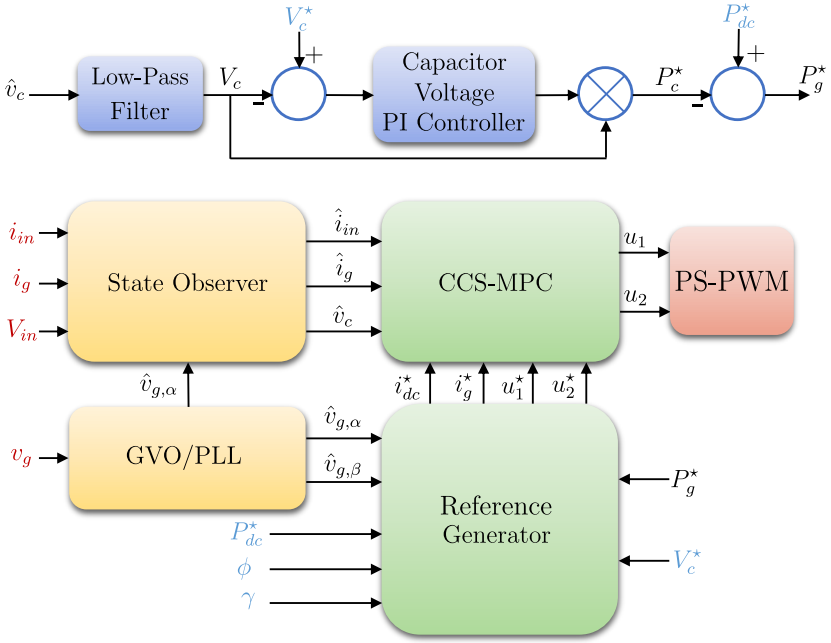


Fig. 5.2. Block diagram of the proposed control system.

5.4.1 System Modeling

The continuous-time average dynamic model of the proposed S^{5}B5L-VSI is derived as:

$$\begin{aligned}\frac{di_{in}(t)}{dt} &= \frac{u_1(t)-1}{L_{in}}v_C(t) + \frac{V_{in}}{L_{in}} \\ \frac{di_g(t)}{dt} &= \frac{-r_g}{L_g}i_g(t) + \frac{2u_2(t)}{L_g}v_C(t) - \frac{v_g(t)}{L_g} \\ \frac{dv_C(t)}{dt} &= \frac{1-u_1(t)}{2C}i_{in}(t) + \frac{u_2(t)}{2C}i_g(t)\end{aligned} \tag{5.21}$$

where $u_1(t) \in [0,1]$ is the boost duty cycle and $u_2(t) \in [-1,1]$ is the AC modulation reference, and L_g and r_g are the inductance and resistance of the grid-interface filter, respectively. Note that from here, C=C_t. Such a dynamic system can be represented using state-space equations in a discrete-time domain:

$$\mathbf{x}(k) \triangleq \begin{bmatrix} i_{in}(k) & i_g(k) & v_C(k) \end{bmatrix}^T \tag{5.22}$$

$$\mathbf{u}(k) \triangleq \begin{bmatrix} u_1(k) & u_2(k) \end{bmatrix}^T \tag{5.23}$$

$$\mathbf{x}(k+1) = \mathbf{A}\mathbf{x}(k) + \mathbf{B}(\mathbf{x}(k))\mathbf{u}(k) + \mathbf{g}(k) \tag{5.24}$$

$$\mathbf{y}(k) = \mathbf{C}\mathbf{x}(k) \tag{5.25}$$

$$\mathbf{A} = \begin{bmatrix} 1 & 0 & \frac{-T_s}{L_{in}} \\ 0 & 1-\frac{T_s r_g}{L_g} & 0 \\ \frac{-T_s}{2C} & 0 & 1 \end{bmatrix} \tag{5.26}$$

$$\mathbf{B}(k) = \begin{bmatrix} \frac{T_s}{L_{in}}v_C & 0 \\ 0 & \frac{2T_s}{L_g}v_C \\ \frac{-T_s}{2C}i_{in} & \frac{-T_s}{2C}i_g \end{bmatrix} \tag{5.27}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \tag{5.28}$$

$$\mathbf{g}(k) = \begin{bmatrix} \frac{T_s}{L_{in}} V_{in} & \frac{-T_s}{L_g} v_g & 0 \end{bmatrix}^T \tag{5.29}$$

where T_s is the sampling time of the control system.

There are a few important points that should be considered here:

- The controllability of the system is checked and verified.
- As can be seen from matrix $\mathbf{B}$, the system is bilinear. Therefore, this matrix must be updated at every sampling time.
- Although the system has three state variables, only two of them are direct measurements. The capacitor voltage will be estimated by a full-state observer.

5.4.2 Model Predictive Control

The CCS-MPC block with the prediction horizon of one is governed by the following equations:

First, the state error and control input error vectors are calculated:

$$\mathbf{e}(k) = \mathbf{x}(k) - \mathbf{x}^\star(k) \tag{5.30}$$

$$\boldsymbol{\delta}(k) = \mathbf{u}(k) - \mathbf{u}^\star(k) \tag{5.31}$$

Then, based on the obtained errors, a quadratic cost function can be formed:

$$J(k) = ||\mathbf{e}^T(k+1)\mathbf{Q}\mathbf{e}(k+1)||_2^2 + ||\boldsymbol{\delta}^T(k)\mathbf{R}\boldsymbol{\delta}(k)||_2^2 \tag{5.32}$$

$$\mathbf{Q} = \begin{bmatrix} \lambda_1 & \lambda_2 & \lambda_3 \end{bmatrix} \boldsymbol{I}_3 \tag{5.33}$$

$$\mathbf{R} = \begin{bmatrix} \sigma_1 & \sigma_2 \end{bmatrix} \boldsymbol{I}_2 \tag{5.34}$$

where $\boldsymbol{I}$ is the identity matrix, λ_i ($i \in [1, 2, 3]$) is the weighting factor for the state i, and σ_j ($j \in [1, 2]$) is the weighting factor for the steady-state condition of the control input j.

Therefore, the optimum control inputs can be found by minimizing the defined cost function:

$$\mathbf{u}^{opt}(k) = \arg\left\{ \min_{\mathbf{u}(k)} J(k) \right\} \tag{5.35}$$

Since the defined cost function has a quadratic form, the optimum control inputs can be calculated by solving the following partial derivative equation (PDE):

$$\frac{\partial J(k)}{\partial \mathbf{u}(k)} = 0 \tag{5.36}$$

The general solution for (5.36) can be expressed as:

$$\mathbf{u}^{opt}(k) = \begin{bmatrix} u_1^{opt}(k) & u_2^{opt}(k) \end{bmatrix}^T = -\mathbf{W}^{-1}\mathbf{F} \tag{5.37}$$

$$\mathbf{W} = \mathbf{B}^T\mathbf{Q}\mathbf{B} + \mathbf{R} \tag{5.38}$$

$$\mathbf{F} = \mathbf{B}^T\mathbf{Q}(\mathbf{A}\mathbf{x}(k) + \mathbf{g}(k) - \mathbf{x}^\star(k+1)) - \mathbf{R}\mathbf{u}^\star(k) \tag{5.39}$$

It is worth mentioning that in the above solution, the control input constraints are not considered. Hence, the calculated optimum control inputs might exceed their valid ranges. Therefore, a hard saturation is used to obtain a sub-optimal solution due to the limited computational power of the DSP controller.

$$u_x(k) = \begin{cases} 1 & \text{,if } u_x^{opt}(k) > 1 \\ u_x^{opt}(k) & \text{,if } -1 \leq u_x^{opt}(k) \leq 1 \\ -1 & \text{,otherwise} \end{cases}. \tag{5.40}$$

5.4.3 Grid Voltage Observer

In this work, a GVO is used to transform the measured instantaneous grid voltage to the $\alpha\beta$ frame and extract its amplitude. A state-space system is formed to create a dynamic model and obtain the stationary reference-frame components of the grid voltage. Assuming:

$$v_g = V_m \sin(\omega t) \tag{5.41}$$

where V_m and ω are the amplitude and angular frequency of the grid voltage. It should be noted that v_g is the grid voltage at the point of common coupling (PCC), which can be directly sensed by the controller using a voltage sensor.

Then, the following continuous-time state-space system model is formed to generate the orthogonal α and β signals:

$$\begin{bmatrix} \dot{v_{g,\alpha}} \\ \dot{v_{g,\beta}} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix} \begin{bmatrix} v_{g,\alpha} \\ v_{g,\beta} \end{bmatrix} \tag{5.42}$$

$$y = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} v_{g,\alpha} \\ v_{g,\beta} \end{bmatrix} \tag{5.43}$$

where y is the measured signal which is the actual grid voltage.

Finally, a Luenburger state observer is used to estimate $v_{g,\alpha}$ and $v_{g,\beta}$. The added benefit of using an observer is its noise filtering feature that reduces the impact of the grid voltage measurement noise on the system performance. Alternatively, a PLL can be used to obtain $v_{g,\alpha}$ and $v_{g,\beta}$ components.

5.4.4 Reference Design

After defining the foundation of the control strategy, the required references for the MPC block should be formulated and calculated. Therefore, in this part, the reference design for the proposed control system is presented.

First, $v_{g,\alpha}$ and $v_{g,\beta}$ are used to extract the grid voltage amplitude as follows:

$$\hat{V}_m = \sqrt{\hat{v}_{g,\alpha}^2 + \hat{v}_{g,\beta}^2} \tag{5.44}$$

$$\sin(\omega t) = \hat{v}_{g,\alpha}/\hat{V}_m \tag{5.45}$$

$$\cos(\omega t) = \hat{v}_{g,\beta}/\hat{V}_m \tag{5.46}$$

Next, the grid current amplitude reference can be calculated as:

$$I_m^\star = \frac{2P_g^\star}{\hat{V}_m} \tag{5.47}$$

where $P_g^\star$ is the grid power reference.

Considering an L-type grid interface filter, the inverter output voltage reference in steady-state is expressed as:

$$v_{inv}^\star = r_g I_m \sin(\omega t + \phi) + \omega L_g I_m \cos(\omega t + \phi) + \hat{v}_{g,\alpha} \tag{5.48}$$

where ϕ is the desired phase shift between v_g and v_g. L_g and r_g are the grid interface filter inductance and its parasitic series resistance, respectively.

In addition, the grid current and DC input current references in steady-state are obtained as:

$$i_g^\star = I_m^\star \sin(\omega t + \phi) \tag{5.49}$$

$$i_{in}^\star = \frac{\hat{V}_m I_m^\star}{2V_{in}} \big[\cos(\phi) - (1-\gamma)\cos(2\omega t + \phi) \big] \tag{5.50}$$

Furthermore, the steady-state references of the control inputs are designed as:

$$u_1^\star = 1 - \frac{V_{in}}{V_C^\star} \tag{5.51}$$

$$u_2^\star = \frac{v_{inv}^\star}{2\hat{v}_C} \tag{5.52}$$

where $V_C^\star$ and $\hat{v}_C$ are the average and estimated capacitor voltage. In the following, the state observer, which is used in this work, will be explained. It should be noted that in the proposed control strategy, unlike many available APD methods, the instantaneous capacitor voltage (ripple) has not been directly sensed or controlled. Instead, only the DC input and AC output currents are controller through the MPC block and the capacitor average voltage is controlled by a PI controller. To the best of the author's knowledge at the time of writing this thesis, there is no published work using the proposed approach.

5.4.5 State Observer

A full-state observer is used here to eliminate the need for direct capacitor voltage measurement and improve the system's robustness against the noise in measured state variables. A Luenburger observer is designed using the pole placement approach with the following parameters:

$$\zeta = 0.707, \omega_n = 2\pi \times 1000 rad/s \tag{5.53}$$

The main observer equation in discrete-time domain is:

$$\hat{\mathbf{x}}(k+1) = \mathbf{A}\hat{\mathbf{x}}(k) + \mathbf{B}(k)\mathbf{u}(k) + \mathbf{L}(\mathbf{y}(k) - \hat{\mathbf{y}}(k)) \tag{5.54}$$

where $\hat{\mathbf{x}}(k+1)$ is the estimated state vector for the next sampling time, $\mathbf{L}$ is the observer gain matrix, $\mathbf{y}(k)$ is the output state vector, and $\hat{\mathbf{y}}(k)$ is the estimated output state vector. As can be seen in the above equation, this observer is estimating the state variables in the next sampling time. Hence it is a prediction-based observer. This is an important feature that can be leveraged when combined with a digital controller. The reason behind is the control delay imposed by the DSP architecture. A prediction of one sampling time ahead is required to compensate for this delay and stable operation of the controller as indicated in (5.32).

5.4.6 Capacitor Voltage Controller

A simple proportional-integral (PI) controller is used to regulate the average voltage across the capacitors (C_a, C_b), as shown in Fig. 5.2. A low-pass filter with the cut-off frequency of 2ω is inserted to remove the double-line frequency ripple component of v_C.

$$P_C = V_C i_C = C V_C \frac{dV_C}{dt} \tag{5.55}$$

where V_C is the filtered (average) capacitor voltage. Transforming the above dynamic equation into the s-domain gives:

$$\frac{V_C}{P_C} = \frac{1}{sC}\frac{1}{V_C} \tag{5.56}$$

By defining a new control input, u_{PI}, a feed-forward approach is adopted:

$$u_{PI} = \frac{P_C}{V_C} \tag{5.57}$$

$$\frac{V_C}{u_{PI}} = \frac{1}{sC} \tag{5.58}$$

Therefore, a PI controller can be designed based on a first-order plant transfer function. The purpose of this PI controller is to generate a capacitor power reference:

$$P_C^\star = u_{PI} * V_C \tag{5.59}$$

$$P_g^\star = P_{in}^\star - P_C^\star \tag{5.60}$$

where $P_g^\star$, $P_{in}^\star$, and $P_C^\star$ are the average references for grid power, DC input power, and capacitor power, respectively.

5.4.7 Minimum Capacitor Voltage Reference Estimation

In this subsection, the minimum required average capacitor voltage for a given operating point is estimated. The motivation of such estimation is reducing the voltage stress across the power switches and capacitors. Consequently, it can lead to a reduced power losses, especially, switching loss of the semiconductors.

Considering (5.17)-(5.20), the ratio between the coefficients have been calculated as follows:

$$\frac{A_2}{A_1} = \frac{1-\gamma}{\gamma}\frac{L_{in}V_m I_m}{V_{in}^2} \tag{5.61}$$

$$\frac{A_3}{A_2} = \frac{\gamma - 1}{4} \tag{5.62}$$

For practical operating conditions of $V_m < 340$ V, $I_m < 30$ A, $V_{in} > 50$ V, and $\gamma > 0.3$, the coefficients can be approximated as:

$$\begin{aligned} A_2/A_1 &\approx 0 \\ A_3/A_1 &\approx 0 \end{aligned} \tag{5.63}$$

It should be noted that the above approximations can be inaccurate at some certain operating conditions such as smaller values of γ. Consequently, the estimated capacitor voltage is expressed as:

$$v_C \approx \sqrt{A_1 \sin(2\omega t + \phi) + c} \tag{5.64}$$

Regarding the high-frequency operation of the converter and small value of L_{in}, and using (5.21), the value of u_1 can be approximated as:

$$u_1(t) \approx \frac{v_C(t) - V_{in}}{v_C(t)} \tag{5.65}$$

Therefore, considering the improved modulation scheme and voltage gain from (3.7), the maximum inverter voltage is calculated:

$$v_{inv,\max}(t) = \frac{1 + u_1(t)}{1 - u_1(t)} V_{in} \approx 2v_C(t) - V_{in} \tag{5.66}$$

Knowing the relatively small impedance of the grid interface filter inductor (L_g) at the line frequency, it can be assumed that $v_{L_g} \approx 0$. As a result, the following equation can be derived:

$$v_{inv,\max} \approx v_g(\theta_i) \tag{5.67}$$

where θ_i is the fundamental angle at which $|v_g - v_{inv,max}|$ is minimized. Using (5.66) and (5.67), the minimum capacitor voltage can be expressed as:

$$\min(4v_C^2) \approx (v_g(\theta_i) + V_{in})^2 \tag{5.68}$$

Obtaining the precise value of θ_i using analytical methods needs a considerable computation power which exceeds the limits of a regular DSP controller such as C2000 series microcontrollers. Therefore, an intuitive estimation is used based on the capacitor voltage waveform shape:

$$\theta_i \approx \frac{\pi}{2} + (\frac{\pi}{4} - \frac{\phi}{2})\frac{A_1}{\bar{v}_C^2(t)} \tag{5.69}$$

By combining (5.64), (5.68), and (5.69), a simplified closed-form estimation of the minimum required capacitor voltage at a given operating conditions can be derived:

$$\bar{V}_{C,\min} \approx \frac{1}{2}\sqrt{\frac{\gamma V_m I_m}{\omega C} + (V_m \sin(\theta_i) + V_{in})^2} \tag{5.70}$$

5.5 Theoretical Analysis

In this section, the impact of the operating conditions on the system performance is studied. Such theoretical analysis is based on the derived equations in the previous sections. The results are visualized using 3D figures and color mapped surfaces. The amplitude of grid voltage (V_m) is set at 320 V peak and the grid frequency is 50 Hz. Moreover, the value of L_{in} and L_g are considered as 140 μH and 1.2 mH. Additionally, the losses are neglected and f_{sw} is 100 kHz. The chosen values for the inductors are based on the original S^{5}B5L-VSI design explained in Chapter 3. For the selected values of the capacitors, three representative values have been considered: $C = 75$ μF as a very small capacitor that can be realized by high-performance film- or ceramic type internal structures; $C = 150$ μF as a small electrolytic-type capacitor; and $C = 220$ μF as a larger electrolytic capacitor with a reduced voltage stress.

Fig. 5.3 show the minimum required average capacitor voltage which is estimated by (5.69)-(5.70) at $P_g = 3$ kW at different ripple factors, capacitor values, and DC input voltages. As can be seen, the required average capacitor voltage increases at lower values of C and larger values of γ. It is worth mentioning that all the following figures in this section are based on the minimum average capacitor voltages shown in Fig. 5.3. Figure 5.4 depicts the capacitor voltage ripple (peak-peak value) at $P_g = 3$ kW at different ripple factors, capacitor values, and DC input voltages. As can be seen, the capacitor voltage ripple increases at lower values of C and larger values of γ. The importance of this figure is in estimating the capacitor lifetime, especially in the case of using electrolytic capacitors. Similarly, Fig. 5.4 illustrates the capacitor peak voltage at $P_g = 3$ kW at different ripple factors, capacitor values, and DC input voltages. As expected, the capacitor peak voltage increases at lower values of C and larger values of γ. The capacitor peak voltage has a significant impact on the switching losses and component

selection in the proposed converter, since all the power switches must block this voltage.

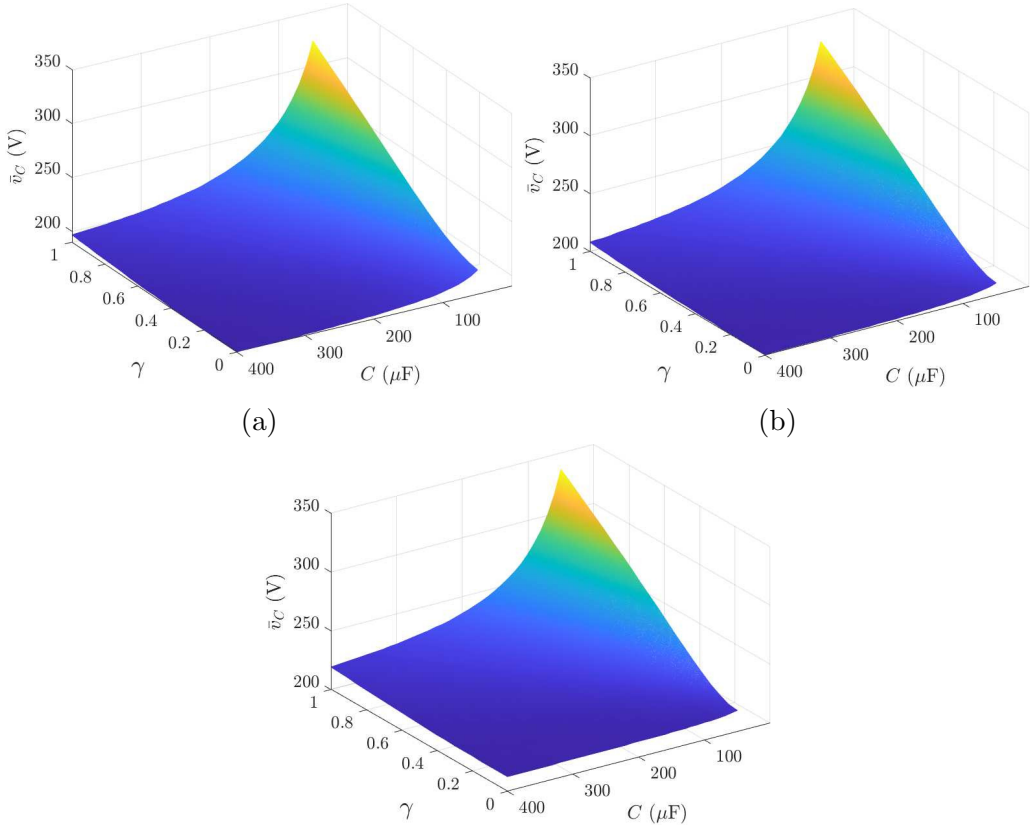


Fig. 5.3. Minimum required average capacitor voltage at different ripple factors and $P_g = 3$ kW at (a) $V_{in} = 50$ V, (b) $V_{in} = 75$ V, and (c) $V_{in} = 100$ V.

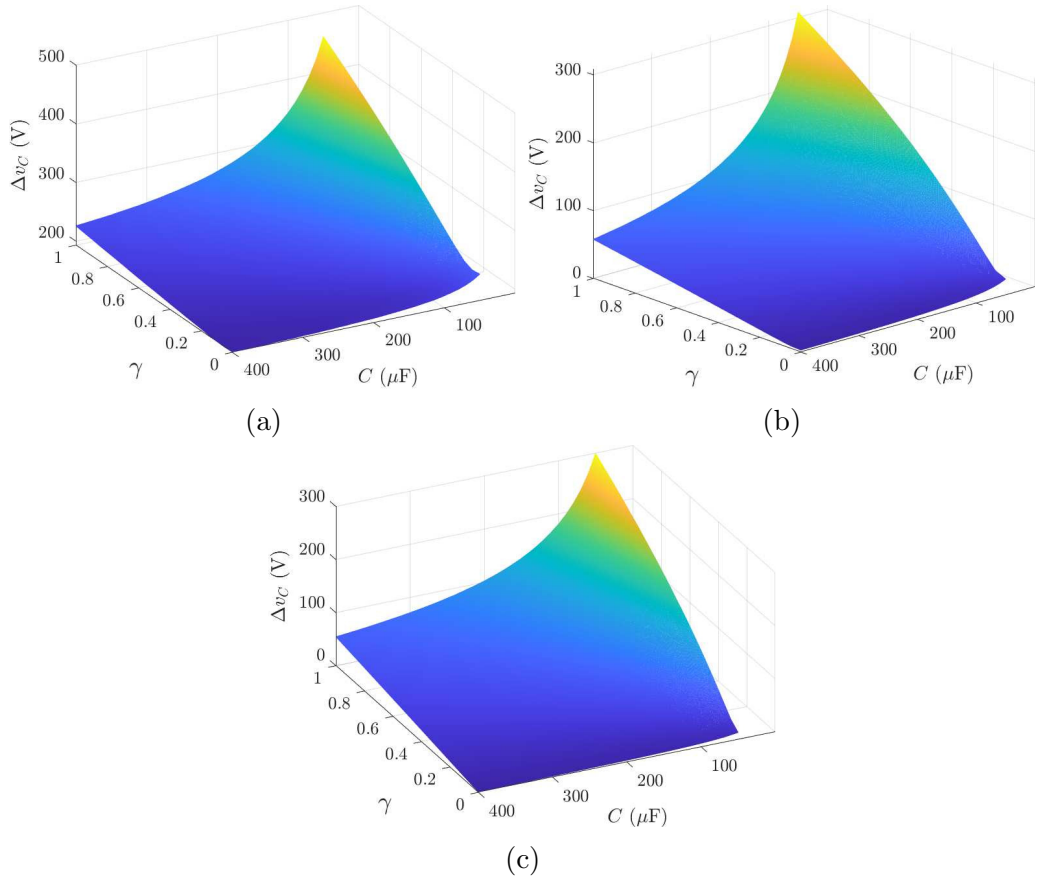


Fig. 5.4. Capacitor voltage ripple at different ripple factors and $P_g = 3$ kW at (a) $V_{in} = 50$ V, (b) $V_{in} = 75$ V, and (c) $V_{in} = 100$ V.

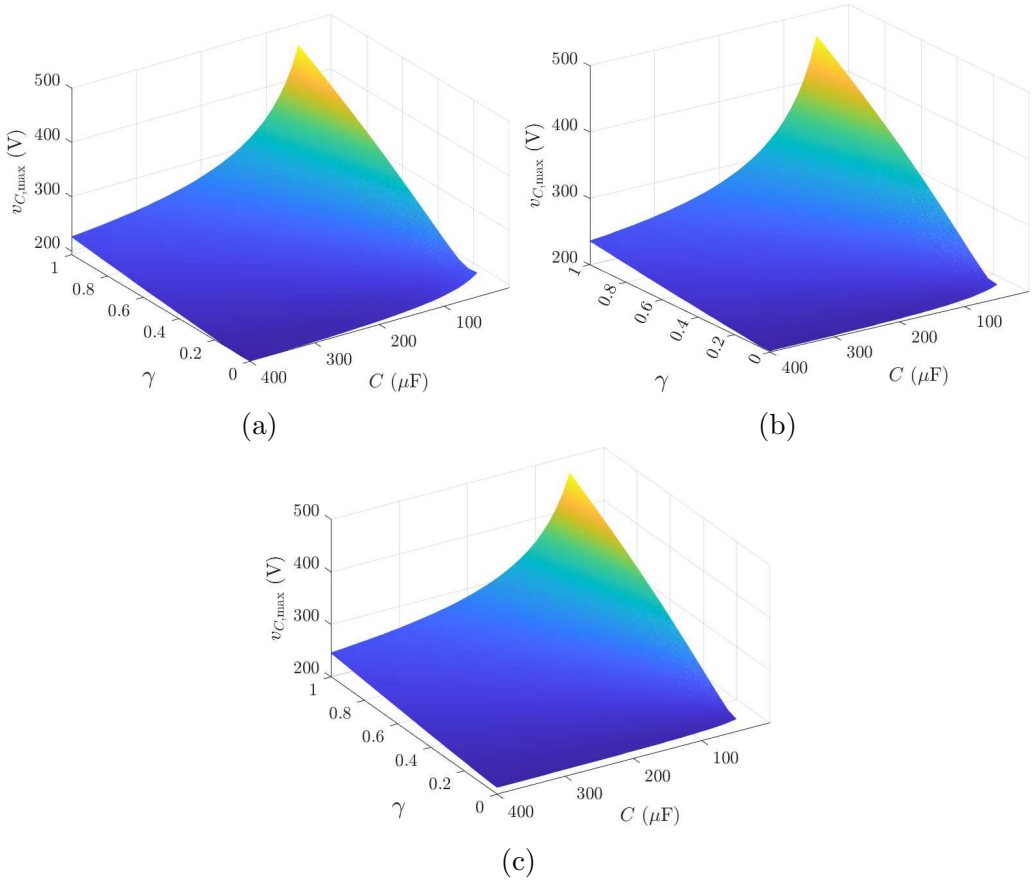


Fig. 5.5. Capacitor peak voltage at different ripple factors and $P_g = 3$ kW at (a) $V_{in} = 50$ V, (b) $V_{in} = 75$ V, and (c) $V_{in} = 100$ V.

Moreover, the influence of the grid power on the capacitor voltage is investigated in Figs. 5.6-5.8 at $V_{in} = 100$ V and different ripple factors and capacitor values. As shown in the mentioned figures, the required average voltage, ripple and peak voltage of the capacitor increases at higher powers and ripple factors. In addition, larger capacitance values lower the capacitor voltage as the energy storage capability is enhanced.

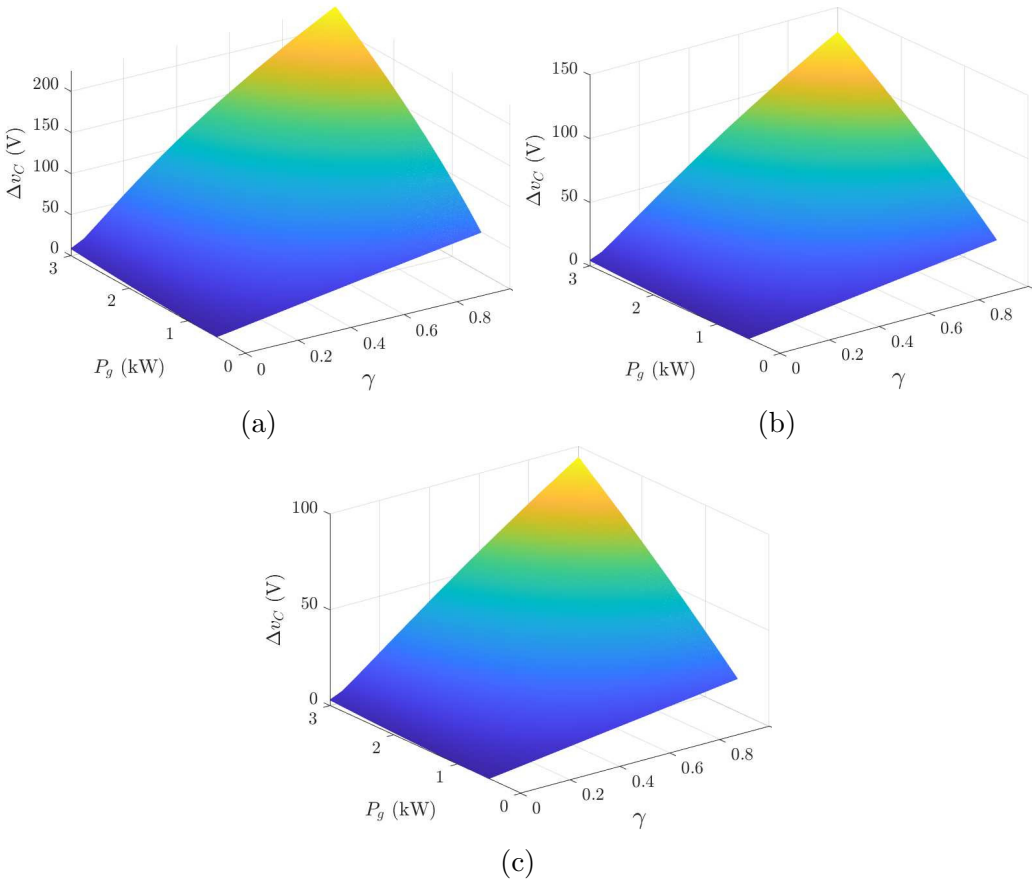


Fig. 5.6. Capacitor voltage ripple at different ripple factors at $V_{in} = 100$ V (a) $C = 75$ μF, (b) $C = 150$ μF, and (c) $C = 220$ μF.

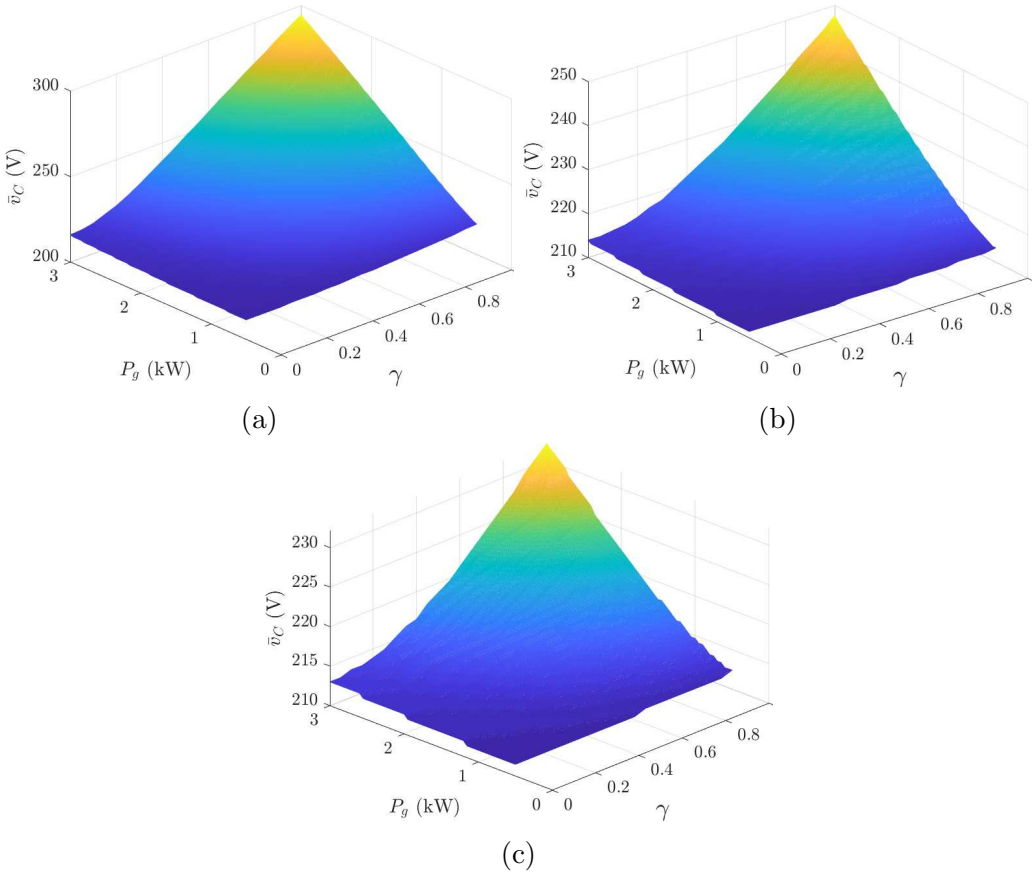


Fig. 5.7. Capacitor average voltage at different ripple factors at $V_{in} = 100$ V (a) $C = 75$ μF, (b) $C = 150$ μF, and (c) $C = 220$ μF.

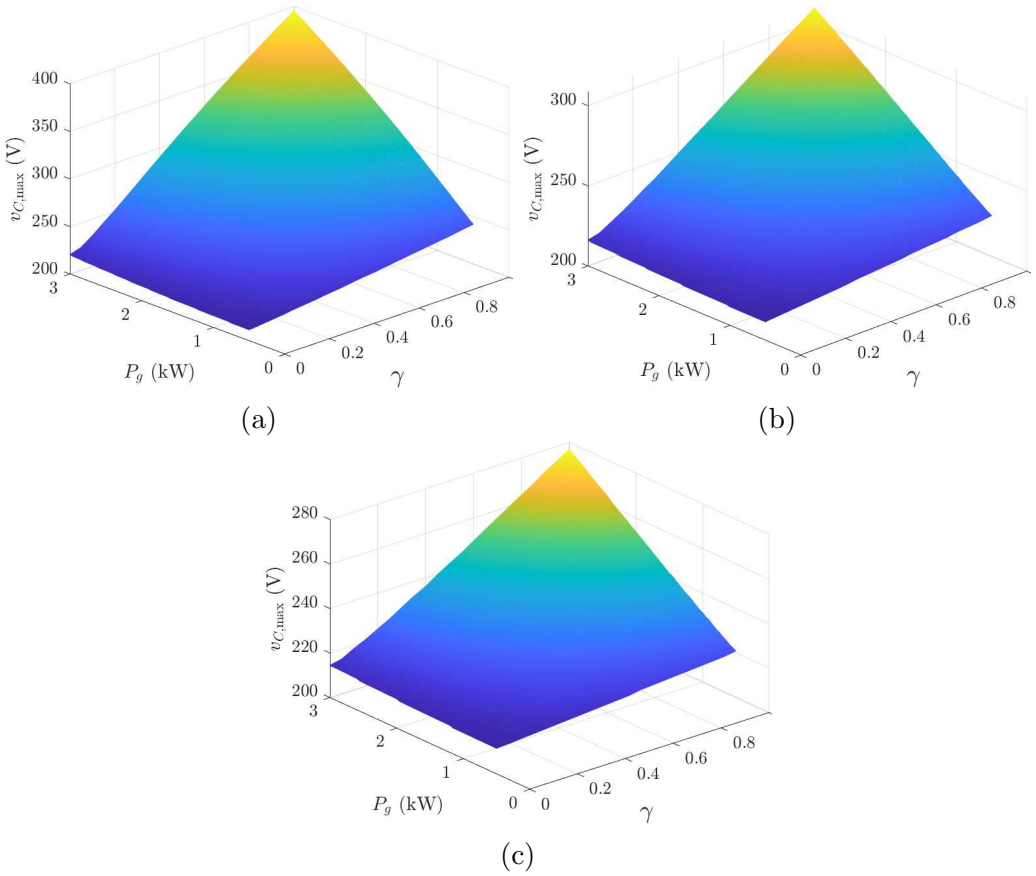


Fig. 5.8. Capacitor peak voltage at different ripple factors at $V_{in} = 100$ V (a) $C = 75$ μF, (b) $C = 150$ μF, and (c) $C = 220$ μF.

Furthermore, the impact of the power factor on the capacitor voltage is illustrated in Fig. 5.9 and Fig. 5.10 at $V_{in} = 100$ V, $S = 3$ kVA, and different ripple factors and capacitor values. Fig. 5.9 shows the capacitor ripple voltage at different operating conditions. Unlike the previous figures, the surfaces in this figure are not smooth and the gradients are not continuous. As a general trend, larger values of γ and smaller values of ϕ lead to an increased capacitor ripple voltage. Additionally, Fig. 5.10 depicts the capacitor peak voltage. Similar to Fig. 5.9, the gradient of the surfaces are not continuous. However, the trends are not the same. Here, the capacitor peak voltage is higher at larger ϕ values. In both figures, a higher capacitance value causes a lower ripple and peak voltage across the capacitors.

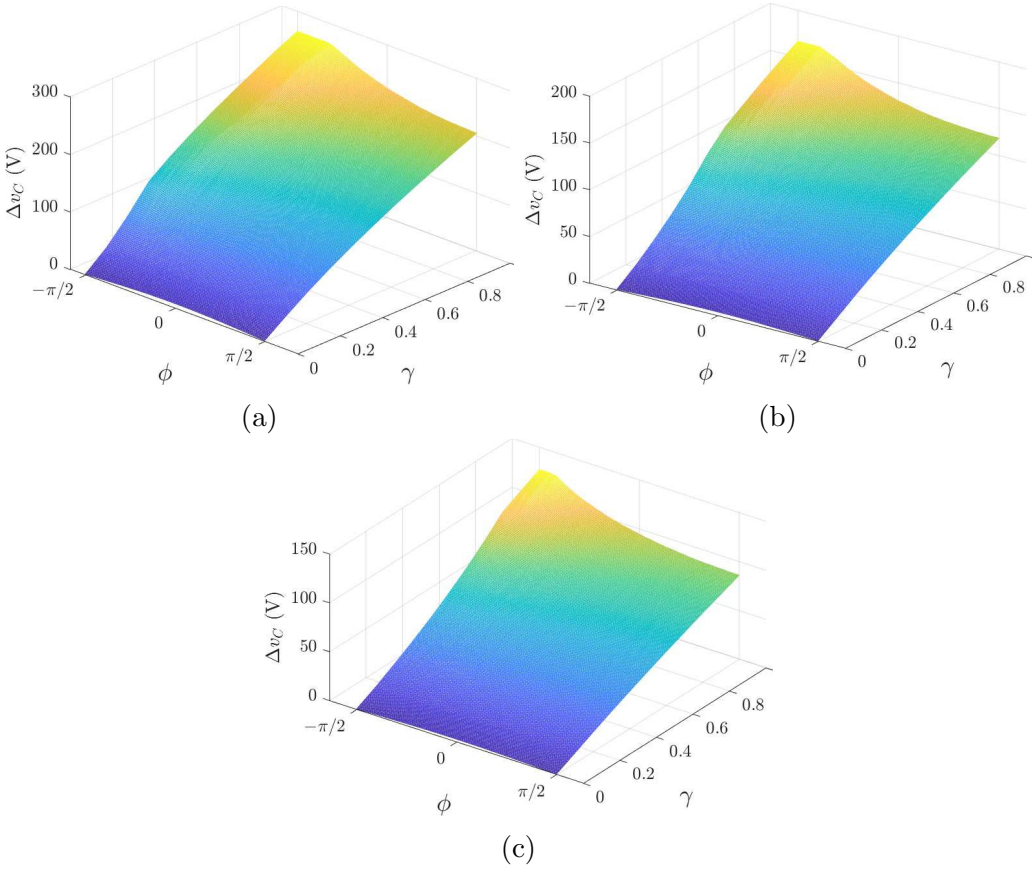


Fig. 5.9. Capacitor voltage ripple at different ripple factors and power factors, $S = 3$ kVA, $V_{in} = 100$ V (a) $C = 75$ µF, (b) $C = 150$ µF, and (c) $C = 220$ µF.

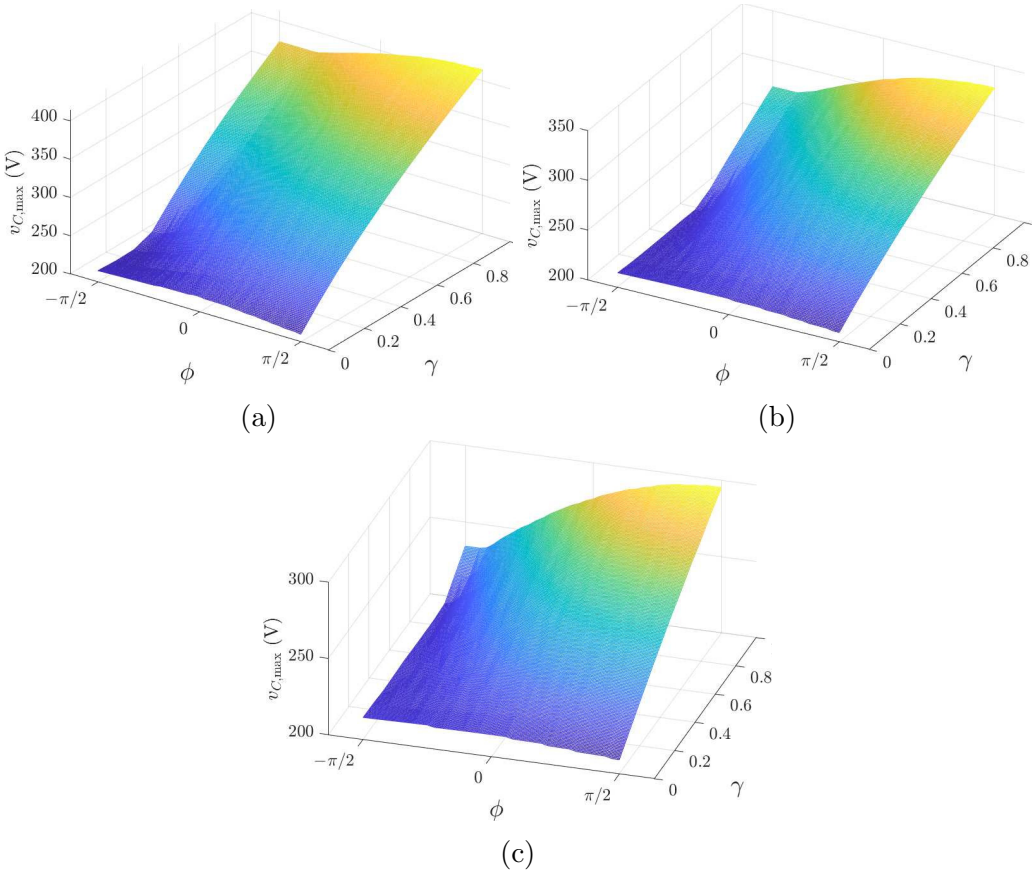


Fig. 5.10. Capacitor peak voltage at different ripple factors and power factors, $S = 3$ kVA, $V_{in} = 100$ V (a) $C = 75$ µF, (b) $C = 150$ µF, and (c) $C = 220$ µF.

As the last case study, the effect of the DC input voltage on the capacitor voltage is visualized in Fig. 5.11 and Fig. 5.12 at $P_g = 3$ kW, different ripple factors, DC input voltages, and capacitor values. Fig. 5.11 shows the capacitor ripple voltage at different operating conditions. Furthermore, Fig. 5.12 shows the capacitor peak voltage. As a general trend, larger values of γ lead to an increased capacitor ripple voltage. As can be seen, due to the dynamic voltage boosting capability of the proposed S^{5}B5L-VSI, the influence of the input voltage on the converter operation is not significant for the considered voltage range. This is a very important feature of the proposed converter and the implemented control strategy, especially for PV and battery energy storage applications.

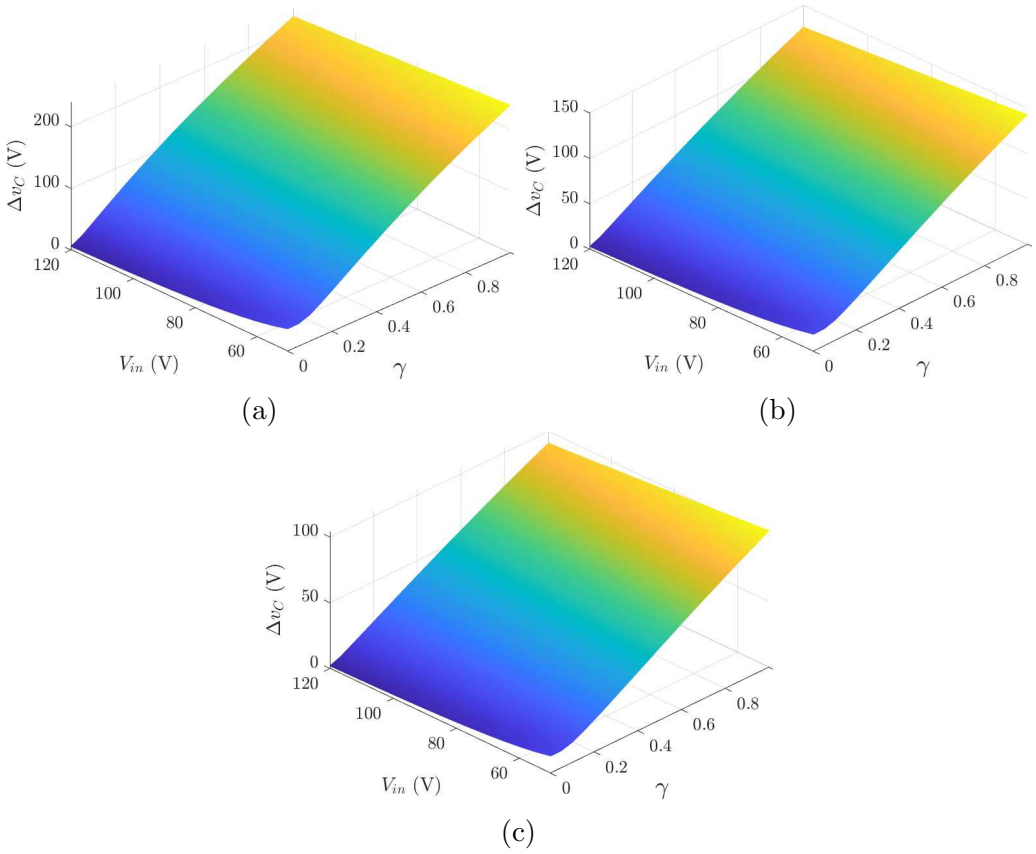


Fig. 5.11. Capacitor voltage ripple at different ripple factors and input voltages, P_g=3 kW (a) $C = 75$ µF, (b) $C = 150$ µF, and (c) $C = 220$ µF.

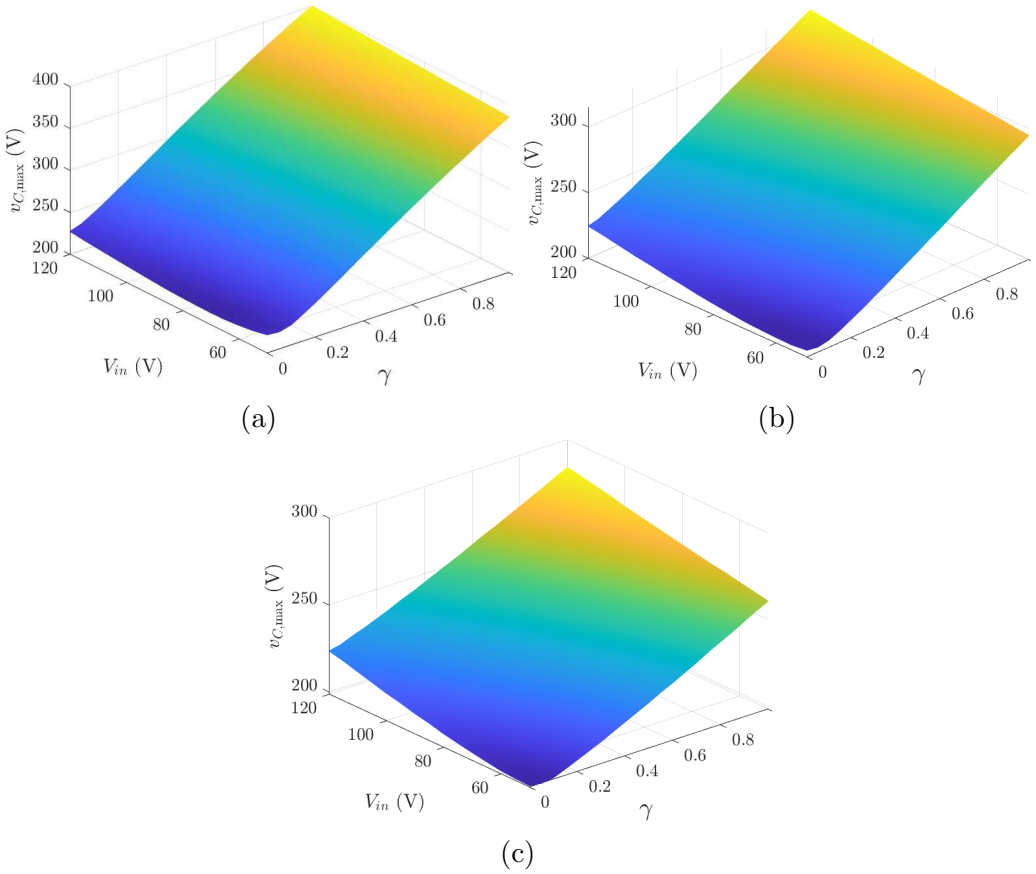


Fig. 5.12. Capacitor peak voltage at different ripple factors and input voltages, P_g=3 kW (a) $C = 75$ μF, (b) $C = 150$ μF, and (c) $C = 220$ μF.

As can be seen from Fig. 5.3 to Fig. 5.12, the worst-case scenario in terms of voltage stress on the power components happens at higher ripple factors (due to the higher power difference between the DC and AC sides), higher DC input voltages, lower capacitance values, higher powers, and lower ϕ values.

5.6 Sensitivity Analysis

This section investigates the impact of the grid impedance and its uncertain value on the performance of the presented control strategy. First, it should be noted that the controller can only measure the grid voltage at the PCC, where a voltage sensor is employed to directly sense the grid voltage. Such a configuration for a single-phase system is depicted in Fig. 5.13. Herein, the grid impedance has been considered as $L_{grid,L}$ and $r_{grid,L}$ for the active line and $L_{grid,N}$ and $r_{grid,N}$ for the neutral line. The mentioned grid impedances

with the ideal grid voltage, $v_{g,int}$, form the Thevenin equivalent circuit model of the grid. It is worth emphasizing that the grid-interface filter, L_g, is a part of the converter and it's values is considered to be known.

Since this work is not focusing on the weak grids, the converter's operation and power quality has been simulated under ideal case with zero total grid impedance (i.e., $L_{grid,L} + L_{grid,N} = 0$ and $r_{grid,L} + r_{grid,N} = 0$), and a significantly larger grid impedance (i.e., $L_{grid,L} + L_{grid,N} = 4m$H and $r_{grid,L} + r_{grid,N} = 50\text{m}\Omega$). In addition, two values (minimum and maximum) have been considered for the grid-interface filter, representing the manufacturing tolerances of the inductors. Table 5.1 summarizes the sensitivity analysis results in terms of AC power quality. The system parameters and component values are the same as in Section 5.5 and the converter is operated with FAPD at $V_{in} = 100$ V, $P_g = 3$ kW, $C = 75$ µF, and different γ values.

As indicated in the sensitivity analysis results, higher γ values lead to higher THD values which is one the tradeoffs of the proposed FAPD method. This issue stems from the increased high-frequency harmonic content in the inverter voltage due to the higher required capacitor average voltage. Moreover, the addition of the grid impedance does not have a significant impact on the grid-side power quality at relatively large values of L_g (in this analysis, when $L_g = 1.6$ mH).

Furthermore, to consider the impact of the imbalanced capacitor values due to existing component tolerances, three sets of simulations have been conducted with different capacitance imbalances and γ values. In this analysis, when there is no capacitance imbalance, both C_a and C_b experience the same current stress due to the symmetric circuit topology and modulation. However, in the case of ±20% capacitance mismatch, a slightly higher current passes through the smaller capacitor. Therefore, the difference in the RMS currents of two capacitors is less than 2%, as listed in Table 5.2.

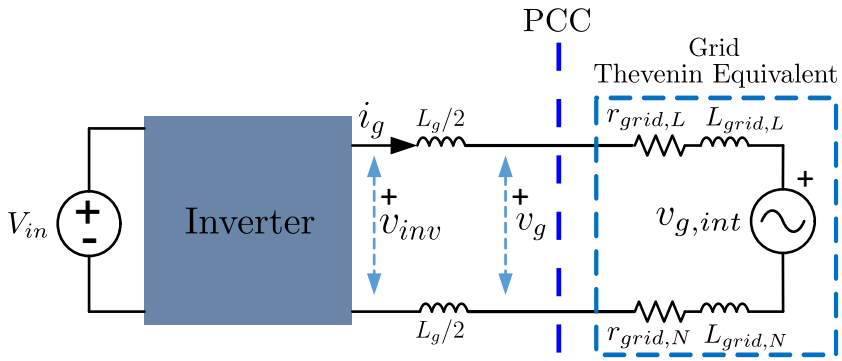


Fig. 5.13. Detailed diagram of the proposed grid-connected system.

Table 5.1
Sensitivity analysis results considering the grid impedance and grid-interface filter uncertainty

γ	L_g	$L_{grid,P} + L_{grid,N}$	THD_{i_g}
0	1.2 mH	0 mH	0.4 %
0.6	1.2 mH	0 mH	0.6 %
1	1.2 mH	0 mH	1 %
0	0.8 mH	4 mH	0.7 %
0.6	0.8 mH	4 mH	0.9 %
1	0.8 mH	4 mH	1.1 %
0	0.8 mH	0 mH	0.6 %
0.6	0.8 mH	0 mH	0.8 %
1	0.8 mH	0 mH	1.1 %
0	1.6 mH	4 mH	0.4 %
0.6	1.6 mH	4 mH	0.5 %
1	1.6 mH	4 mH	0.9 %
0	1.6 mH	0 mH	0.3 %
0.6	1.6 mH	0 mH	0.5 %
1	1.6 mH	0 mH	0.9 %

Table 5.2
Sensitivity analysis results considering the capacitance mismatch

γ	C_a	C_b	$I_{C_a,rms}$	$I_{C_b,rms}$
0	75 µF	75 µF	11.49 A	11.49 A
0	60 µF	90 µF	11.56 A	11.47 A
0.6	75 µF	75 µF	10.35 A	10.35 A
0.6	60 µF	90 µF	10.49 A	10.33 A
1	75 µF	75 µF	9.97 A	9.97 A
1	60 µF	90 µF	9.85 A	10.26 A

5.7 Simulation Results

In this section, the operation of the proposed control strategy for the the S^5B5L-VSI as a grid-tied bidirectional inverter is verified through simulation. The system parameters and component values are the same as in Section 5.5. As for the first scenario, Fig. 5.14 depicts the converter operation with FAPD at $V_{in} = 100$ V, $P_g = 1$ kW, $C = 75$ µF, and different γ values. As can be

seen, when $\gamma = 0$, FAPD is disabled, the capacitor ripple voltage is very small, and the input current fluctuates between 0 A to 20 A at double-line frequency. When $\gamma = 1$, the capacitor voltage has the maximum ripple and the DC input current is constant at 10 A with only high-frequency ripples caused by the switching action. This full APD operation mode is the same as conventional APD methods. However, when $\gamma = 0.6$, the capacitor ripple voltage decreases compared to the full APD mode. Moreover, the DC input current has the same average value, but with a larger 100 Hz imposed ripple. As shown here, the proposed control method can track the references without any undesirable transients and the tradeoff between the ripples on capacitor voltage and input current can be balanced using the γ parameter.

In the second scenario, the bidirectional operation of the system is simulated. Fig. 5.15 shows the key waveforms of the system with FAPD at $V_{in} = 100$ V, $\gamma = 0.6$, and P_g from +3 kW to -3 kW. Similar to the previous case, the transition is fast and without any significant overshoot or oscillations. This feature can be utilized effectively in the battery-based energy storage systems. Furthermore, Fig. 5.16 depicts the performance of the proposed method in reactive power support. In this case, $V_{in} = 100$ V, $\gamma = 0.6$, and $P_g = 1$ kW, and Q_g changes from +1 kVAr to -1 kVAr.

To highlight one of the possible applications of the proposed FAPD method, a grid-connected energy storage system is considered. Using the S^5B5L-VSI with a conventional APD method, the low-frequency ripple component of the capacitor voltages can grow excessively at higher power references, ultimately causing power quality issues. Such operating condition has been depicted in Fig. 5.17, where the grid power reference is increased for a short period of time. As can be seen in Fig. 5.17, although the dc input current is almost flat, the grid current is distorted at the higher demanded power. Conversely, using the proposed FAPD approach, the peak capacitor voltage is kept constant while a high-quality current waveform is preserved, as shown in Fig. 5.18. In this case, a lower ripple factor has been chosen based on the theoretical analysis results to keep the capacitor peak voltage constant. As a consequence, a fraction of the instantaneous ripple power is drawn from the dc input source. This approach can be useful for improving the peak power handling capability for short periods of time, especially with battery-based input sources. Since only a fraction of the ac ripple is present at the dc input side temporarily, the known disadvantages of the ac ripple drawn from the dc source, such as reduced efficiency and battery degradation, are less pronounced. As verified in this section, the proposed control method can track power references without any undesirable transients, and the tradeoff between the ripples on capacitor voltage and dc input current can be balanced using the γ parameter, based on the specific requirements of each particular

application.

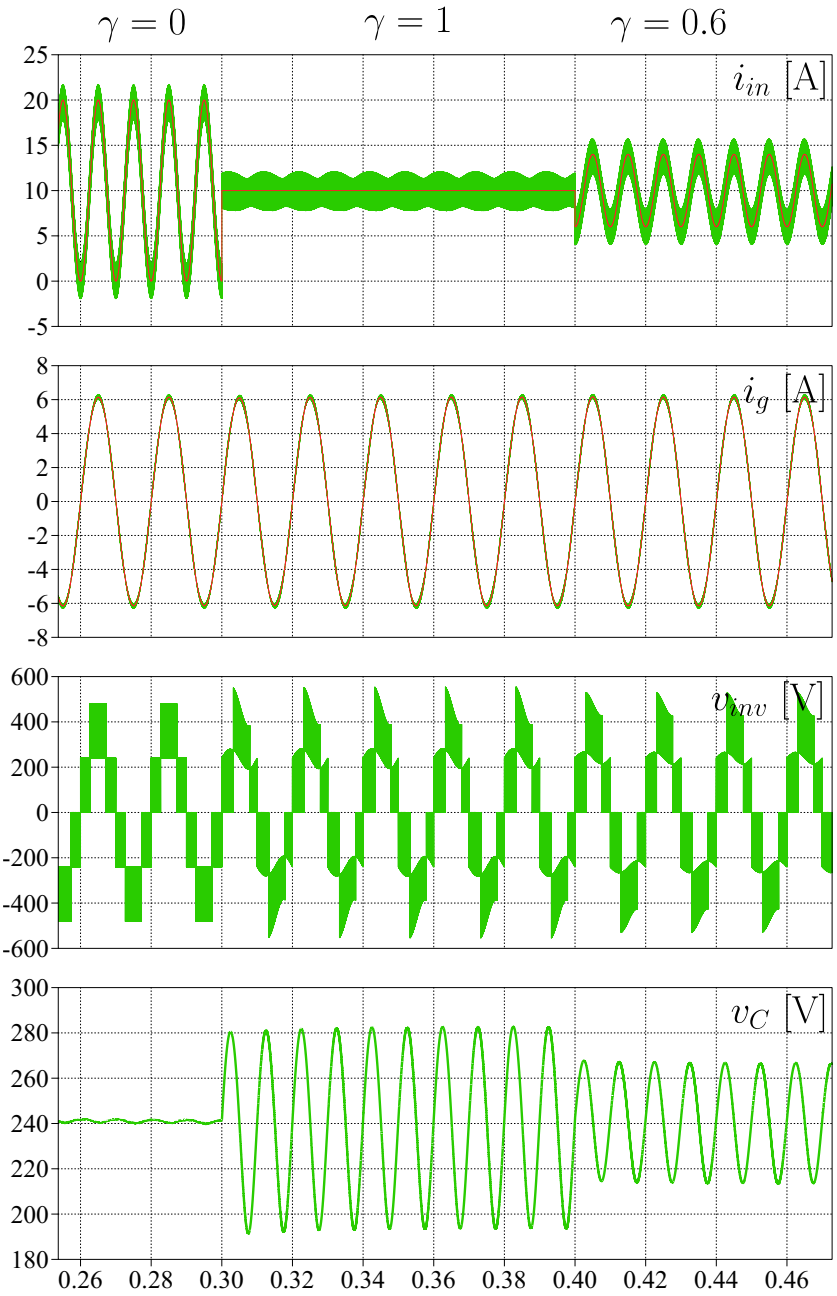


Fig. 5.14. Simulation results of the proposed S^5B5L-VSI with FAPD at V_{in}=100 V, P_g=1 kW, and different γ values.

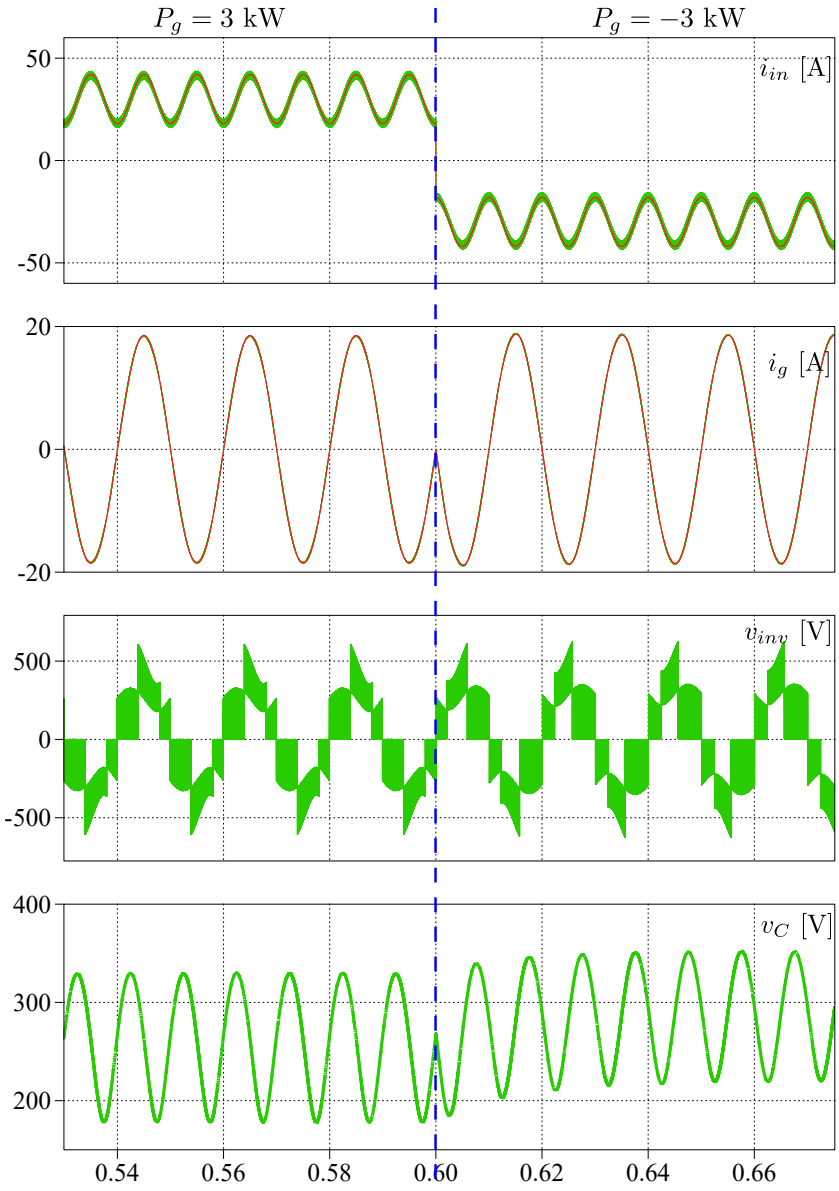


Fig. 5.15. Simulation results of the proposed S^{5}B5L-VSI with FAPD at V_{in}=100 V, $\gamma = 0.6$, and P_g from +3 kW to -3 kW.

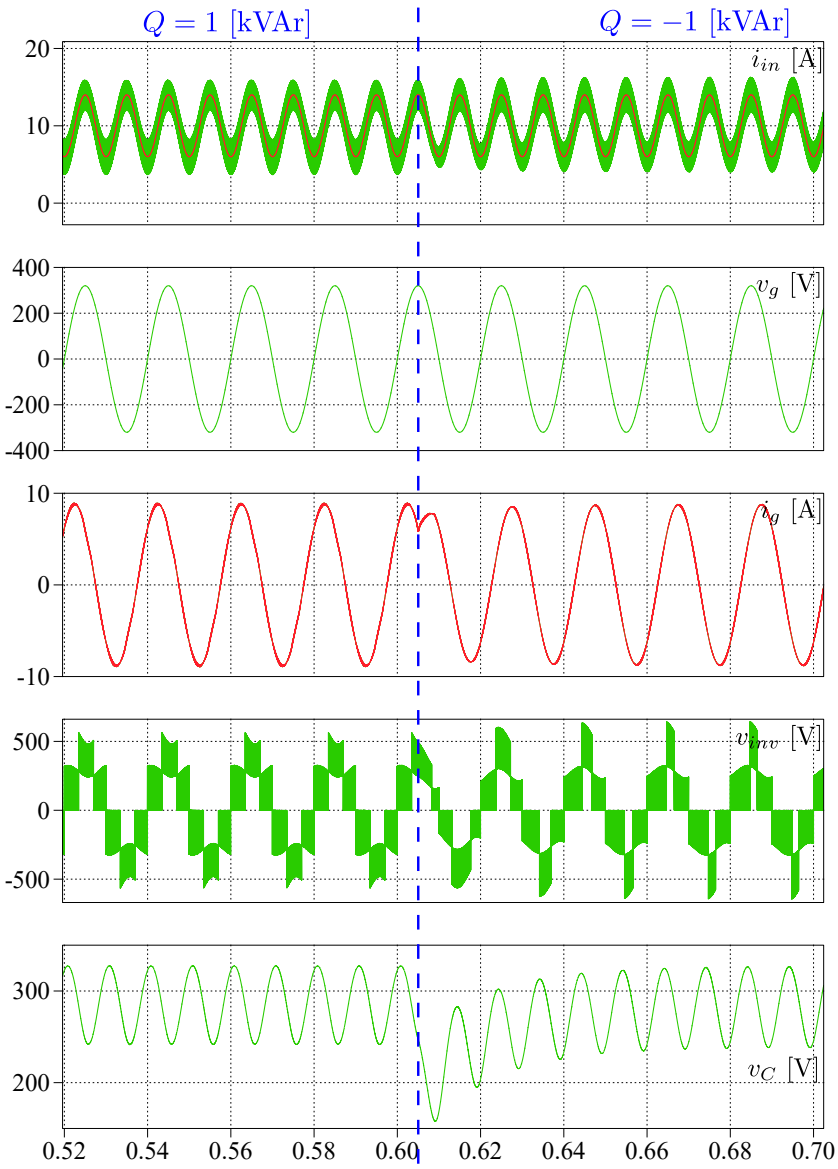


Fig. 5.16. Simulation results of the proposed S^{5}B5L-VSI with FAPD at V_{in}=100 V, $\gamma = 0.6$, and $P_g = 1$ kW, and Q_g from +1 kVAr to -1 kVAr.

5.8 Conclusion

A novel control strategy for FAPD has been introduced in this work. The mathematical derivation and the controller structure are presented in detail. Unlike the conventional APD methods, the proposed method can adjust the

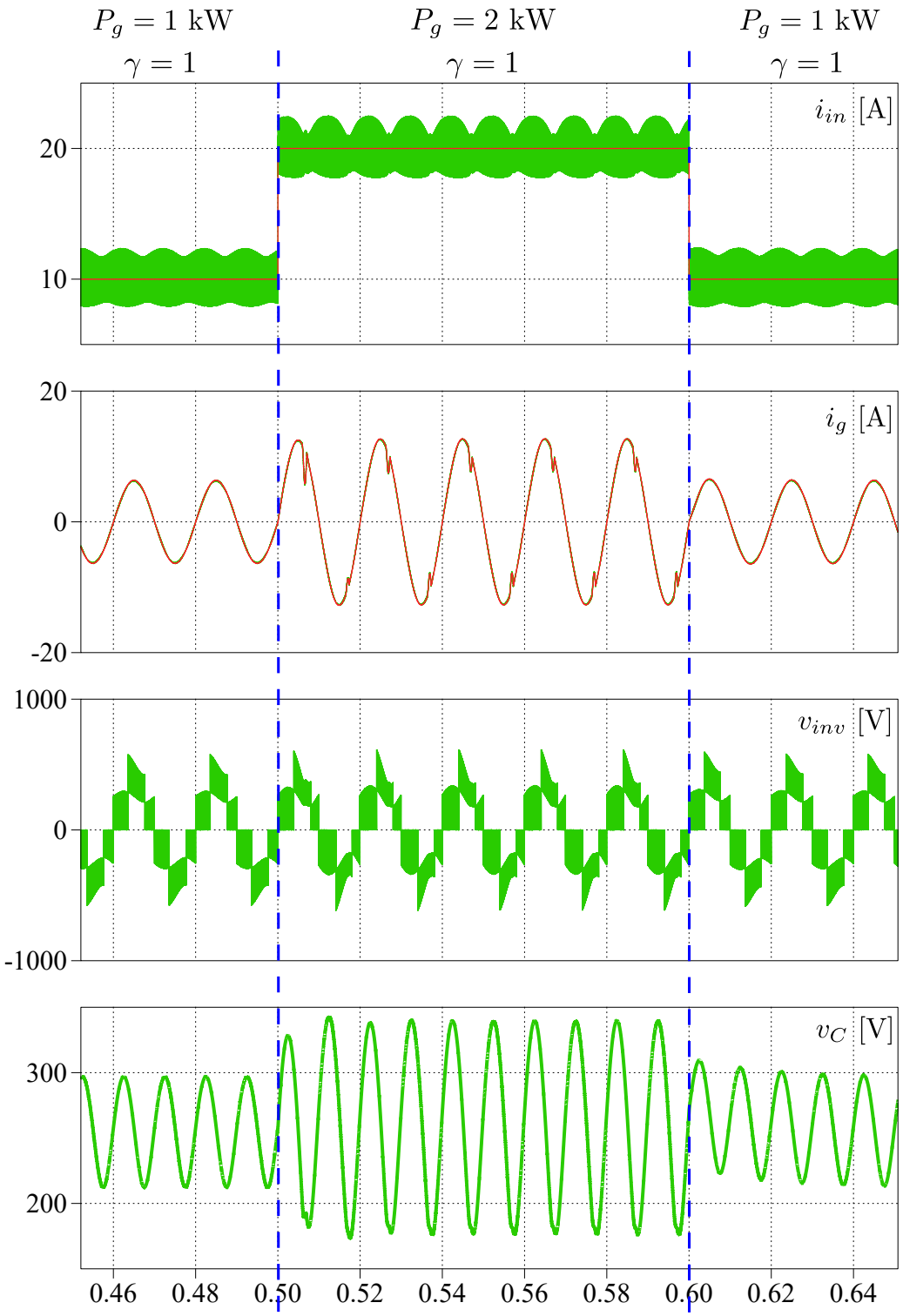


Fig. 5.17. Simulation results of the S^{5}B5L-VSI with conventional APD at $V_{in} = 100$ V, and pulsed transition from $P_g = 1$ kW to $P_g = 2$ kW.

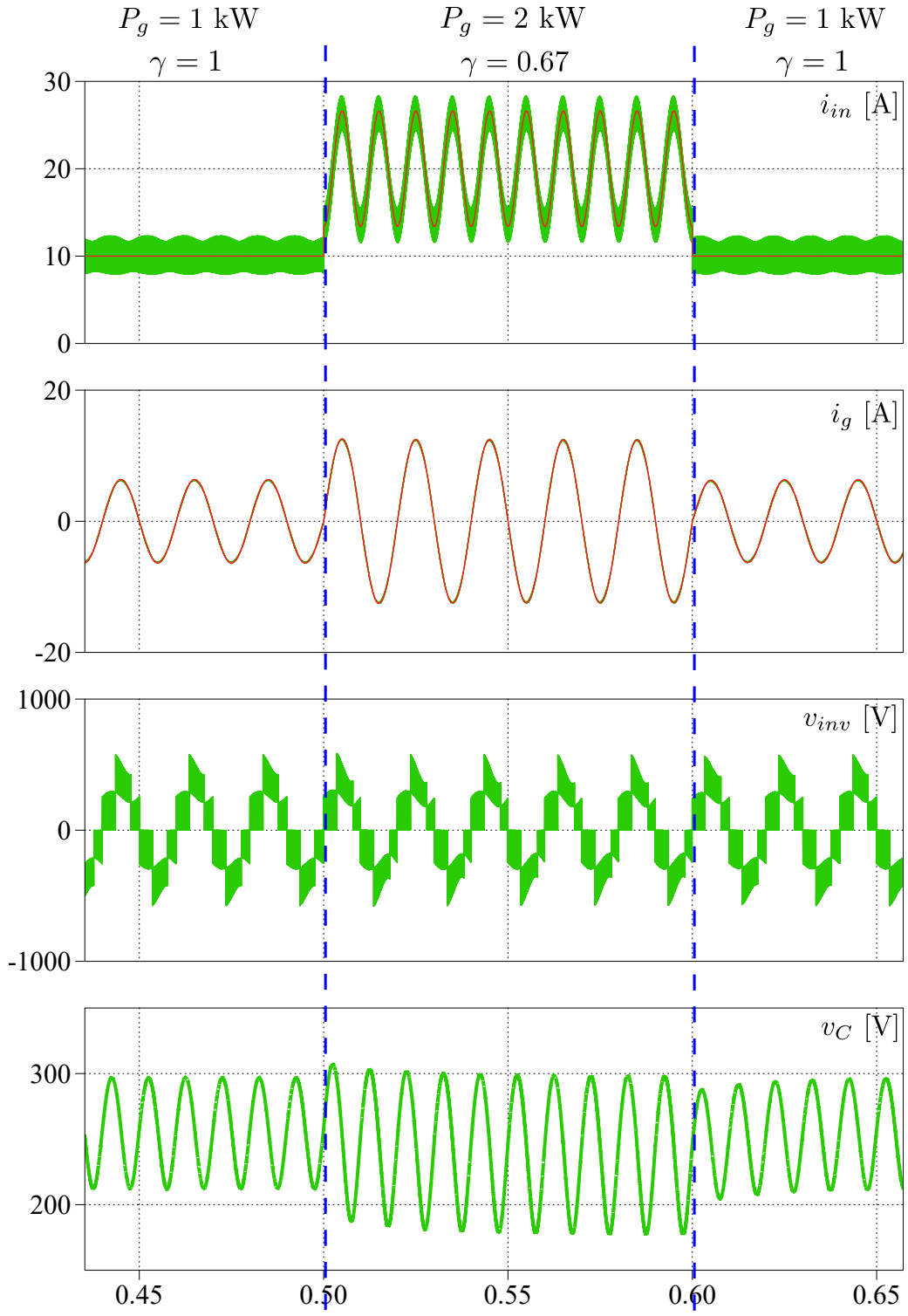


Fig. 5.18. Simulation results of the S^{5}B5L-VSI with the proposed FAPD at $V_{in} = 100$ V, and pulsed transition from $P_g = 1$ kW to $P_g = 2$ kW.

balance between the desired ripple at the DC and AC sides with a continuous variable. A model predictive controller is used as the core of the proposed method to improve the transient performance. The correct operation of the proposed controller is verified in the simulation. Due to the COVID-19 pandemic and unexpected lab shutdowns, this idea was verified at the simulation level at the time of writing this thesis. As part of the future works, the proposed idea will be further analyzed and verified through experiment.

Chapter 6

An Interleaved Single-Stage Switched-Boost Common-Ground Multilevel Inverter: Design, Control, and Experimental Validation

This chapter introduces an interleaved single-stage switched-boost common-ground inverter to realize a scalable and modular converter with numerous interesting features such as bidirectional power flow, dynamic voltage boosting gain, common-grounded structure, adjustable power sharing, etc.

6.1 Introduction

One of the limitations of the proposed S^5B5L-VSI is its high-frequency CMV and power scalability. To address these limitations, the concept of interleaved CGSB-based MLI is developed in this work, which extends and complements the work presented in [174]. The proposed interleaved CGSB-MLI offers several important features:

- Modularity and generalization capability to realize a large number of output voltage levels and scalable power rating.
- Independently controllable power sharing among the modules enabling Active Thermal Control (ATC) and fault-tolerance capability under grid-connected conditions.

- Single-stage DC-AC power conversion with dynamic voltage boosting and CG features.
- Bidirectional power flow operation and full reactive power support.
- Uniform MVS across all devices with a reduced current stress profile.
- Enhancement of the apparent inverter output switching frequency with a PS-PWM technique.
- Continuous and spike-free operation of the input current with a current ripple cancellation capability.
- Using smaller passive component values compared to the similar available solutions.

In the following, the working principles of the proposed interleaved CGSB-MLI and its modulation/control strategy over a derived 7L configuration are discussed.

6.2 Proposed Interleaved CGSB-MLI and Its Modulation/Control Strategy

This section discusses the working principle of the proposed generalized topology, followed by the modulation and control strategy for a 7L variant of the proposed interleaved CGSB-MLI.

6.2.1 Working Principle of the Proposed Generalized Topology

The proposed topology is developed using an interleaved connection of N CG-based QHB modules with a single DC source, V_{dc}, as illustrated in Fig. 6.1. The interleaved connection can work based on the input-parallel, output-parallel condition, while the resultant system is connected to the grid via split inductor filters of L_{g_x}. Here, $x \in \{1, 2, ..., N\}$ is the index per each module to realize $2N + 1$ number of output voltage levels as per v_{inv}. Regarding such configuration, the proposed overall system possesses a CG-based feature with the leakage current cancellation capability. Here, each of these CG-QHB modules needs an input boost inductor, L_{dc_x}, five power switches, and a floating capacitor, C_x. The working principle of such a CG-based QHB module has been presented in Chapter 3, where each of them can generate

a 3L-switched voltage at its output, v_x, with a continuous input current profile. Taking one CG-QHB module into account, the switching condition and the status of the input inductor per each module are listed in Table 3.1. Regarding such working principle and considering the switch S_{ix} as the ith switch in each of CG-QHB modules ($i \in \{1, 2, ..., 5\}$), the switch S_{1x} must be triggered with a constant boost duty cycle, D_x, which determines the boosted voltage across C_x in steady-state as follows:

$$V_{C_x} = \frac{V_{dc}}{1 - D_x}. \tag{6.1}$$

Here, the 3L output voltage in each of the CG-based QHB modules is realized with an AC modulation reference, d_x, as:

$$v_x = d_x v_{C_x} \tag{6.2}$$

where v_{C_x} is the instantaneous value of the capacitor voltage per module. Moreover, as per Table 3.1, the Switch S_{1x} must be ON for generating a negative voltage at the module output, i.e., $v_x = -v_{C_x}$. Consequently, this constraint limits the maximum fundamental component in each CG-QHB module's output voltage, which results in the following expression:

$$\hat{v}_{x_{fund.}} = D_x V_{C_x} = \frac{D_x}{1 - D_x} V_{dc}. \tag{6.3}$$

The above equation confirms that the proposed topology can work even when a low or wide-varying DC input voltage is available since the boost duty cycle can be properly tuned to meet the minimum grid peak voltage requirement for power injection. Taking advantage of the proposed interleaved configuration, and considering i_{g_x} as the output current per each CG-QHB module, the overall injected grid current can be denoted as:

$$i_g = i_{g_1} + i_{g_2} + \cdots + i_{g_N}. \tag{6.4}$$

The above-mentioned relationship can facilitate a large injected grid current handling capability, which can be propitious for ATC and fault-tolerant performance of the whole system. Moreover, due to the input-parallel output-parallel configuration of this interleaved-based topology, the maximum voltage stress across all the semiconductor devices is identical and equal to the boosted voltage of the involved capacitors.

Meanwhile, to realize the relationship between the resultant output voltage of the proposed interleaved CGSB-based MLI, the following expression for the total grid current, i_g, can be derived as:

$$L_g \frac{di_g}{dt} + r_g i_g = v_{inv} - v_g. \tag{6.5}$$

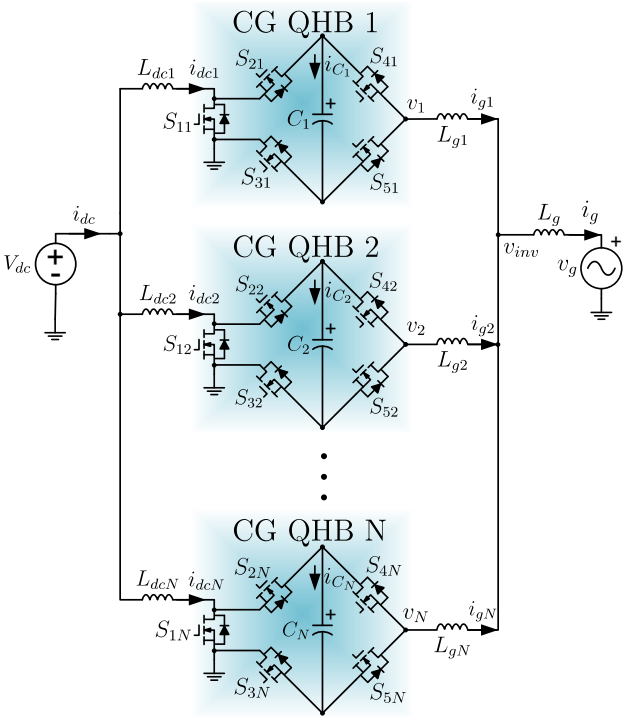


Fig. 6.1. The proposed interleaved CGSB-based MLI.

On the other hand, the AC currents for each of the CG-QHB modules can be expressed as:

$$\begin{aligned} L_{g_1}\frac{di_{g_1}}{dt} + r_{g_1}i_{g_1} &= v_1 - v_{inv} \\ L_{g_2}\frac{di_{g_2}}{dt} + r_{g_2}i_{g_2} &= v_2 - v_{inv} \\ &\vdots \\ L_{g_N}\frac{di_{g_N}}{dt} + r_{g_N}i_{g_N} &= v_N - v_{inv} \end{aligned} \tag{6.6}$$

where r_{g_x} is the ESR of the split filter inductors, and v_g is the grid voltage. Therefore, the overall switched-voltage of the proposed interleaved CGSB-MLI is obtained as:

$$v_{inv} = \frac{\sum_{k=1}^{N} \frac{v_k - r_{g_k} i_{g_k}}{L_{g_k}} + \frac{v_g + r_g i_g}{L_g}}{\sum_{k=1}^{N} \frac{1}{L_{g_k}} + \frac{1}{L_g}}. \tag{6.7}$$

Considering the same value as per each of the split inductors incorporated at the output of CG-QHB modules, the relationship of v_{inv} can be further

Table 6.1
Working principle of the proposed 7L variant of the proposed interleaved CGSB-based MLI with 3 CG-QHB modules (assuming $L_g \gg L_{g_x}/N$)

State	v_1	v_2	v_3	v_{inv}
1	$+v_{C_1}$	$+v_{C_2}$	$+v_{C_3}$	$\frac{+v_{C_1}+v_{C_2}+v_{C_3}}{3} = +V_C$
2	$+v_{C_1}$	$+v_{C_2}$	0	$\frac{+v_{C_1}+v_{C_2}}{3} = +2V_C/3$
3	$+v_{C_1}$	0	$+v_{C_3}$	$\frac{+v_{C_1}+v_{C_3}}{3} = +2V_C/3$
4	0	$+v_{C_2}$	$+v_{C_3}$	$\frac{+v_{C_2}+v_{C_3}}{3} = +2V_C/3$
5	$+v_{C_1}$	0	0	$\frac{+v_{C_1}}{3} = +V_C/3$
6	0	$+v_{C_2}$	0	$\frac{+v_{C_2}}{3} = +V_C/3$
7	0	0	$+v_{C_3}$	$\frac{+v_{C_3}}{3} = +V_C/3$
8	0	0	0	0
9	$-v_{C_1}$	0	0	$\frac{-v_{C_1}}{3} = -V_C/3$
10	0	$-v_{C_2}$	0	$\frac{-v_{C_2}}{3} = -V_C/3$
11	0	0	$-v_{C_3}$	$\frac{-v_{C_3}}{3} = -V_C/3$
12	$-v_{C_1}$	$-v_{C_2}$	0	$\frac{-v_{C_1}-v_{C_2}}{3} = -2V_C/3$
13	0	$-v_{C_2}$	$-v_{C_3}$	$\frac{-v_{C_2}-v_{C_3}}{3} = -2V_C/3$
14	$-v_{C_1}$	0	$-v_{C_3}$	$\frac{-v_{C_1}-v_{C_3}}{3} = -2V_C/3$
15	$-v_{C_1}$	$-v_{C_2}$	$-v_{C_3}$	$\frac{-v_{C_1}-v_{C_2}-v_{C_3}}{3} = -V_C$

simplified as:

$$v_{inv} = \frac{\frac{1}{L_{g_x}} \sum_{k=1}^{N} v_k + (\frac{r_g}{L_g} - \frac{r_{g_x}}{L_{g_x}}) i_g + \frac{v_g}{L_g}}{\frac{N}{L_{g_x}} + \frac{1}{L_g}}. \tag{6.8}$$

Assuming similar parameters for all the CG-QHB modules, and a relatively large grid-side filter inductor ($L_g \gg L_{g_x}/N$), the resultant inverter output voltage value can be approximated as:

$$v_{inv} \approx \frac{v_1 + v_2 + ...v_x}{N}. \tag{6.9}$$

It should be noted that the required number of interleaved modules, N, can be chosen based on the maximum required injected power and the power rating of each module.

6.2.2 Modulation/Control Strategy for A 7L Variant of the Proposed Converter

The proposed inverter can generate a $2N + 1$-level output voltage waveform using N CG-QHB modules with a PS-PWM technique. The PS value among the carriers is equal to $2\pi/N$, while the harmonic cluster of the AC output is at Nf_{sw} for a f_{sw} switching frequency. Taking three modules of the described CG-QHB into account, a 7L-CGSB-based inverter with an interleaved configuration is derived. The working principle of such a 7L-CGSB-based inverter is provided in Table 6.1. As can be realized, the middle levels of the resultant inverter output voltage, i.e., $\pm 2V_C/3$ and $\pm V_C/3$, are generated using three redundant switching states (RSSs). This can help the converter to be modulated with a PS-PWM scheme leading to enhancement in the apparent frequency of AC waveforms to three times the switching frequency. Details of such a PS-PWM strategy with the resultant gate switching pulses of the switches are shown in Fig. 6.2. To integrate all the RSSs into the modulation process and to enhance the apparent switching frequency of the 7L inverter output voltage, three PS carriers, i.e., C_{r1}, C_{r2}, and C_{r3}, with 120° phase displacement with respect to each other are needed as shown in Fig. 6.2. These PS carriers within the PS-PWM scheme need to be compared with both DC and AC modulation references as depicted in Fig. 6.2. Here, an identical/same value of the boost duty cycle D_x for all the CG-QHB modules and a sinusoidal AC modulation reference $d(t)$ as per (6.10) are considered.

$$d(t) = m \sin(\omega t) \tag{6.10}$$

where m is the modulation index, and ω is the angular frequency of the grid voltage. Here, due to the limitation of each of described CG-QHB modules in generating the negative output voltage level (discharging of L_{dc_x} during this level is not possible), the value of D_x must be within the following range:

$$0 \leq m \leq D_x. \tag{6.11}$$

Such limitation on the modulation index results in a slightly higher voltage stress on the power components. The impact of this limitation is investigated in more detail in Section 6.5. Utilizing the proposed converter in a full bridge differential configuration in a single-phase application (i.e., two sets of CG-QHB modules, one set synthesizes the active line and the other set generates the neutral line) can mitigate this limitation at the cost of increased CMV due to loss of CG feature. Moreover, in a three-phase application, common modulation and control techniques such a zero-sequence voltage injection can alleviate the voltage stress on the circuit components.

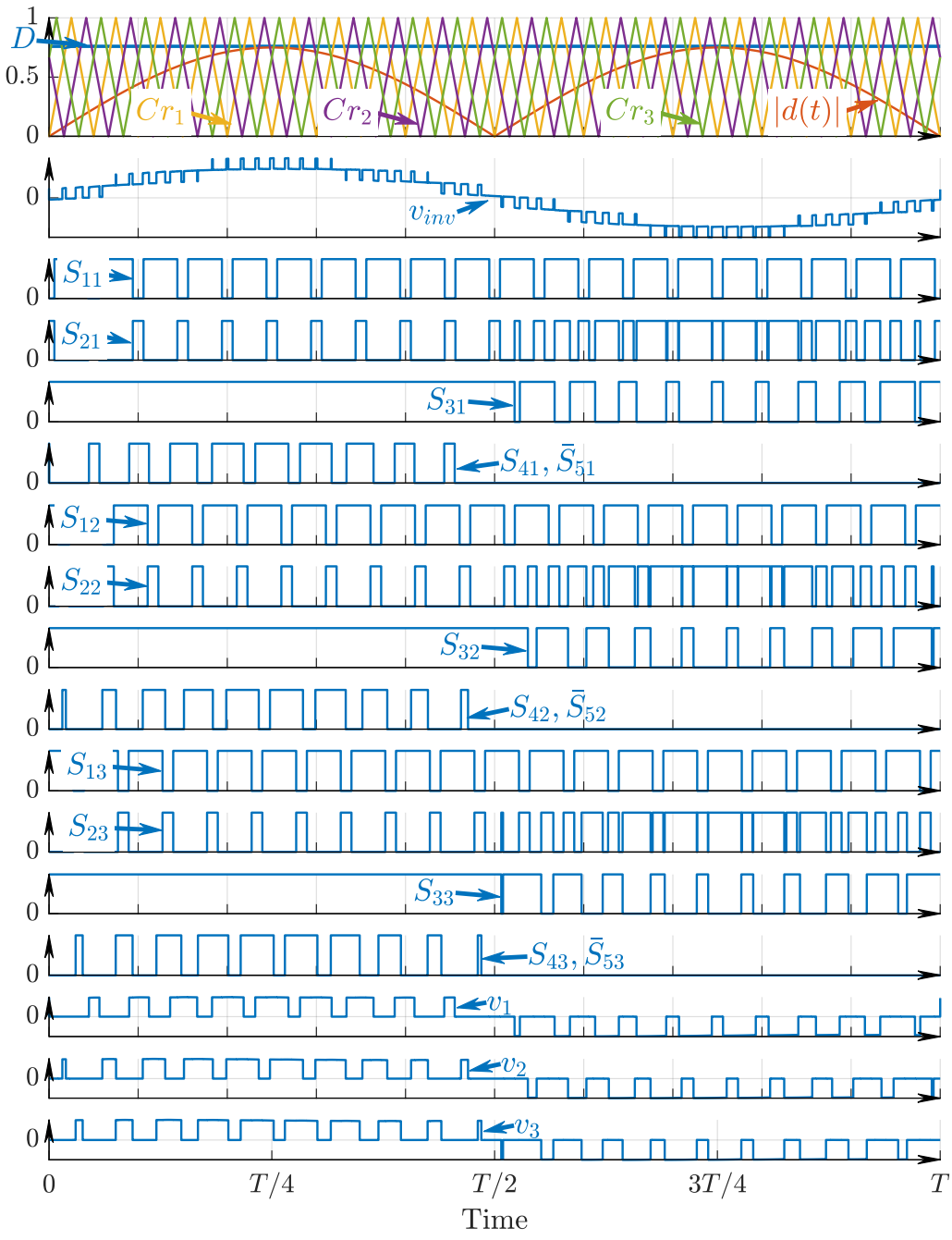


Fig. 6.2. Modulation waveforms and gate switching pulses of the 7L variant of the proposed interleaved CGSB-based MLI, where $D = D_x$.

Regarding such modulation strategy, a detailed diagram of the closed-loop system to inject the power to the grid via the proposed 7L-CGSB-based

inverter is illustrated in Fig. 6.3. The control procedure is based on a PR controller per each CG-QHB module, while considering the required active and reactive power, $P_g^\star$, and $Q_g^\star$, the sinusoidal current reference is defined as (6.12) for the whole interleaved system:

$$i_g^\star = \frac{2P_g^\star}{V_m}\cos(\omega t) + \frac{2Q_g^\star}{V_m}\sin(\omega t) \tag{6.12}$$

where V_m is the peak grid voltage, v_g. Here, any grid synchronization strategy, such as a PLL, can be used to extract the phase, ωt, and amplitude, V_m, of the grid voltage. To realize a controllable power sharing in the proposed inverter, the total grid current expressed in (6.12) must be distributed among the CG-QHB modules using a set of current weighting factors, λ_x. Therefore, the AC current reference for each CG-QHB module can be expressed as:

$$i_{g_x}^\star = \lambda_x i_g^\star \tag{6.13}$$

where

$$\sum_{x=1}^{3} \lambda_x = 1. \tag{6.14}$$

Hence, three PR controllers with the transfer function of $C_{ac}(s)$ are required to accurately track the module AC current references, $i_{g_x}^\star$, calculated in (6.13). Considering $G_{ac}(s)$ as the system plant, the procedure in Section 2.2.4.1 was followed to design the PR controllers represented by their transfer function, $G_{ac}(s)$. The overall view of the controller for the 7L variant of the proposed inverter is illustrated in Fig. 6.3.

Consequently, the PR controllers generate three AC reference signals d_1, d_2, and d_3, to synthesize a 3L-switched voltage per each module, i.e., v_1, v_2, and v_3, which in turn results in a 7L output voltage, v_{inv}, of the resultant system.

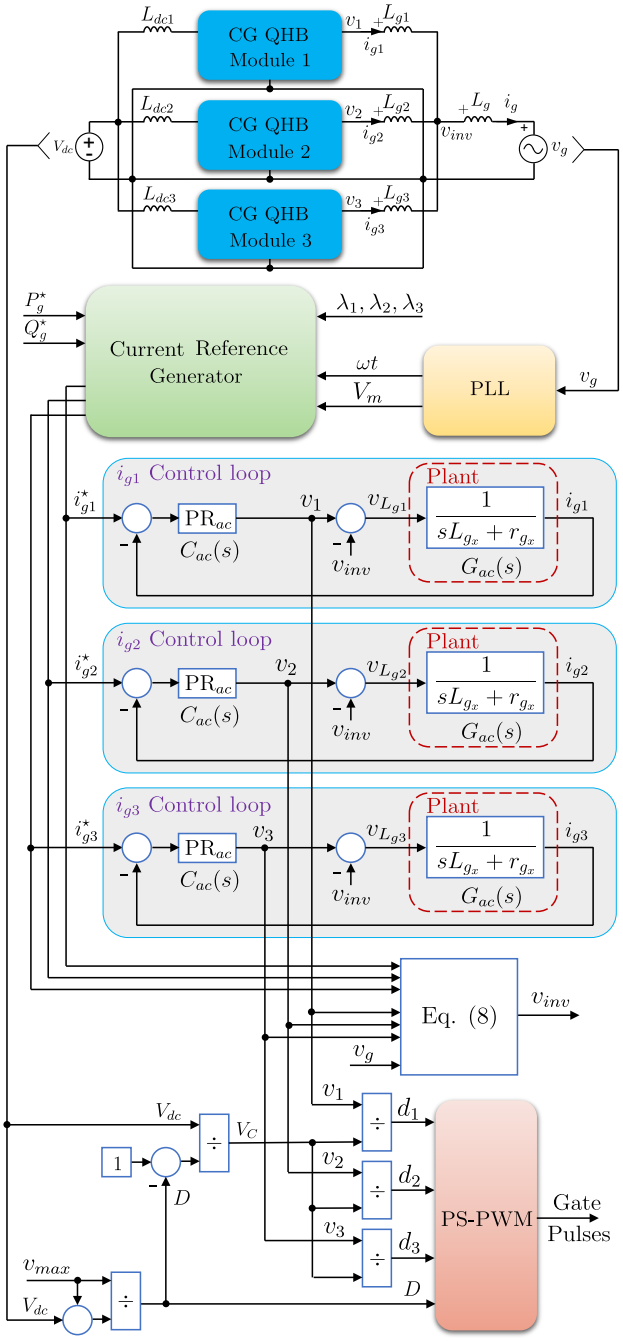


Fig. 6.3. Controller block diagram.

6.3 Passive Elements Design Guidance

This section presents a straightforward method for determining the passive component values of the proposed interleaved CGSB-based MLI. To simplify the analysis, the following assumptions are made:

- All the components are ideal (e.g., no parasitic resistance, inductance, or capacitance in the circuit).
- The inverter is operating at unity power factor.
- Only the second harmonic (2ω) has been considered for the low-frequency ripple estimations.
- All the CG-QHB modules are identical.

6.3.1 Design of L_{dc_x} and C_x

Due to the high-frequency SB-based action and single-phase operation of the proposed structure, both low- and high-frequency ripples are expected for the current passing through each of the input boost inductors, i_{in_x}, and the instantaneous voltage across each of CG-QHB module capacitor, v_{C_x}. To estimate the low-frequency ripples of these variables, an AC equivalent circuit of the proposed converter using its averaged model is extracted [160]. Hence, the following low-frequency ripples of i_{in_x} and v_{C_x} are taken as:

$$\Delta v_{LF,C_x} = \frac{2V_m I_{m_x} \omega L_{dc_x}(1-D_x)}{|4\omega^2 L_{dc_x} C_x - (1-D_x)^2| V_{dc}} \tag{6.15}$$

$$\Delta i_{LF,dc_x} = \frac{V_m I_{m_x}(1-D_x)^2}{|4\omega^2 L_{dc_x} C_x - (1-D_x)^2| V_{dc}} \tag{6.16}$$

where $\Delta v_{LF,C_x}$ and $\Delta i_{LF,in_x}$ are the low-frequency peak-to-peak ripples of v_{C_x} and i_{in_x}, respectively, and I_{m_x} is the peak module AC current, i_{g_x}.

Next, the high-frequency ripples of v_{C_x} and i_{in_x} can also be derived as follows [67]:

$$\Delta v_{HF,C_x} = \frac{D_x(1-D_x) i_{dc,\max_x}}{C_x f_{sw}} \tag{6.17}$$

$$\Delta i_{HF,dc_x} = \frac{D_x V_{dc}}{L_{dc_x} f_{sw}} \tag{6.18}$$

where $\Delta v_{HF,C_x}$ and $\Delta i_{HF,dc_x}$ are the high-frequency peak-to-peak ripples of v_{C_x} and i_{dc_x}, respectively. Additionally, $i_{dc,\max_x}$ is the maximum value of the

low-frequency component of the input current per module, estimated as:

$$i_{dc,\max_x} = \frac{P_{g_x}}{V_{dc}} + \frac{\Delta i_{LF,dc_x}}{2} \tag{6.19}$$

where P_{g_x} is the power injected from each CG-QHB module.

It is worth noting that there is a coupling between $\Delta v_{LF,C_x}$ and $\Delta i_{LF,in_x}$, as both expressions include L_{dc_x} and C_x. Assuming 10% ripple on the voltage across capacitors, the required value of the boost duty cycle is obtained from (6.3). Then, considering a sinusoidal 50 Hz grid voltage with $V_m = 340$ V as the peak amplitude, and maximum injected power to the grid as $P_g = 5.1$ kW, the values of the passive components are calculated and shown in Fig. 6.4 for a wide range of DC input voltages. It should be noted that the points above the boundary surface in Fig. 6.4 result in a smaller low-frequency ripple and stable operation of the proposed converter. As can be seen, smaller values of L_{dc_x} allow for a wider range of DC input voltages. Therefore, a smaller value of L_{dc_x} is desirable when a wide operating DC voltage range is required. Having said that, an intuitive procedure for passive component values determination is suggested as follows:

1. L_{dc_x} is obtained using (6.18) for any given desired high-frequency inductor current ripple and operating condition.

2. Given L_{dc_x}, and the desired low-frequency capacitor voltage ripple, the required value of C_x can be estimated using (6.15).

3. Substitute the selected L_{dc_x} and C_x values into (6.16) and (6.17) and check if the estimated ripples are acceptable.

4. Fine-tune the values if needed and verify the results using (6.15)-(6.18).

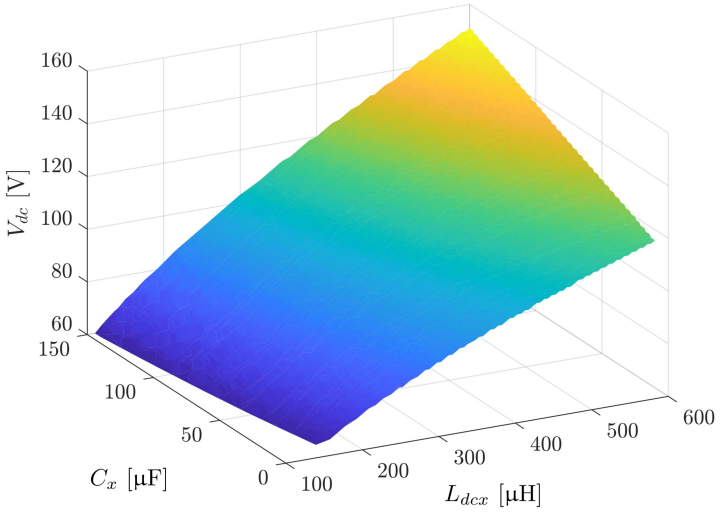


Fig. 6.4. Boundary values for passive circuit components using three CG-QHB modules assuming 10% ripple on capacitor voltages at different DC input voltages, $V_m = 340$ V, and $P_g = 5.1$ kW.

Considering Fig. 6.4 and the above-mentioned procedure, for a given value of $V_{dc} = 120$ V, a value of 340 µH and 75 µF can be taken for the L_{dc_x} and C_x, respectively.

On the other hand, getting to know the nature of the input current drawn from the DC source in terms of high-frequency ripple is helpful to better monitor the performance of the input DC power supply, i.e., battery, PV strings, fuel cells, etc. It is also particularly important for the DC and/or EMI filter design. As mentioned earlier, due to the interleaved configuration of the proposed CGSB-based MLI, the high-frequency ripple contents of the input current drawn from the DC source is always lower than the ripple current passing through each of the boost inductors L_{dc_x}. To derive the high-frequency ripple values for the proposed converter, first, the switched voltages are expressed in terms of high-frequency harmonics using the Fourier series. Then, the resultant waveforms are superimposed to obtain the maximum ripple amplitudes. Hence, the high-frequency peak-to-peak ripple value for the input current is taken as:

$$\Delta i_{HF,dc} = \frac{V_{dc}}{4N(1-D_x)f_{sw}L_{dc_x}} \sum_{k=1}^{+\infty} \frac{\sin(kN\pi(1-D_x))}{k^2}. \tag{6.20}$$

The resultant normalized high-frequency ripple drawn from the DC input source is shown in Fig. 6.5 for different number of interleaved CG-QHB

modules. As can be seen, for any given N, the high-frequency input current ripple is zero at $D_x = A/N$, where $A \in \{0, 1, ..., N-1\}$.

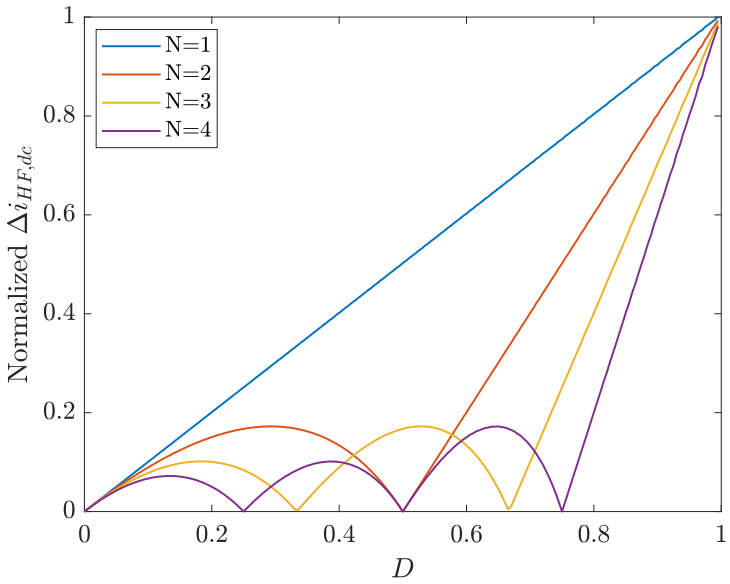


Fig. 6.5. Normalized high-frequency input current ripple for different number of interleaved CG-QHB modules.

6.3.2 Design of L_{g_x} and L_g

Following the same procedure, the maximum high-frequency peak-to-peak ripple current of the interleaved AC inductors, L_{g_x}, is approximated as:

$$\Delta i_{HF,gx} \approx \frac{V_{dc}}{4(1-D_x) f_{sw} L_{g_x}} \sum_{h=1}^{+\infty} \frac{\sin(h\pi/2)}{h^2}. \tag{6.21}$$

Herein, the normalized curves showing the actual high-frequency peak-to-peak ripple amplitude of current passing through L_{g_x} for different values of N over a positive half-cycle of the grid voltage are shown in Fig. 6.6. Here, the approximated value obtained by (6.21) is depicted with a dashed line, indicating the maximum limit of the normalized $\Delta i_{HF,g_x}$ for any given N, which is useful for determining the minimum required value of L_{g_x}. Herein, a case study of $V_{dc} = 120$ V, $V_m = 340$ V, unity power factor, and $D_x = 0.76$ has been considered. It should be noted that in the case of $N = 1$, L_{g_1} and L_g are connected in series, and therefore the total inductance between the CG-QHB module and the grid becomes $L_{g_1} + L_g$. Hence, the ripple is significantly lower.

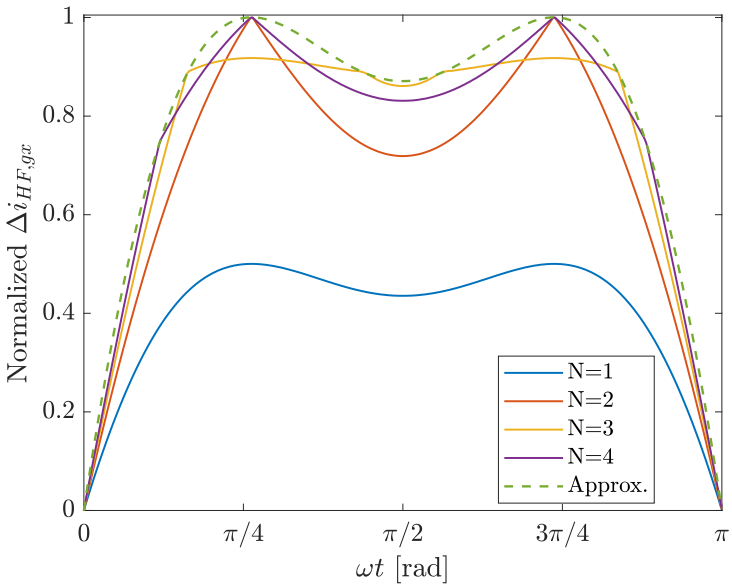


Fig. 6.6. Normalized high-frequency AC inductors current ripple for different number of interleaved CG-QHB modules at $V_{dc} = 120$ V, $V_m = 340$ V, unity power factor, and D_x= 0.76.

Similarly, an expression for the high-frequency peak-to-peak ripple amplitude of the resultant grid current passing through L_g can be derived as follows:

$$\Delta i_{HF,g} = \frac{V_{dc}}{4N^2(1-D_x)f_{sw}(L_g + L_{g_x}/N)} \sum_{k=1}^{+\infty} \frac{\sin(k\pi/2)}{k^2}. \tag{6.22}$$

Regarding this, Fig. 6.7 shows the normalized value of $\Delta i_{HF,g}$ for different values of N over a positive half-cycle of the grid voltage.

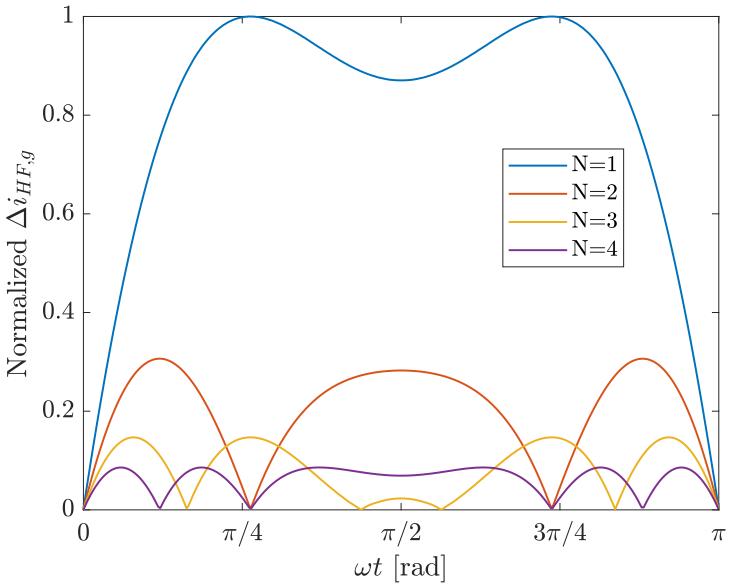


Fig. 6.7. Normalized high-frequency grid current ripple for different number of interleaved CG-QHB modules at $V_{dc} = 120$ V, $V_m = 340$ V, unity power factor, and $D_x = 0.76$.

Based on the above-mentioned relations, the procedure for determining L_{g_x} and L_g is suggested as follows:

1. L_{g_x} is obtained using (6.21), for any given desired high-frequency inductor current ripple and operating condition.

2. Given the value of L_{g_x}, and the desired high-frequency grid current ripple, the required value of L_g can be calculated using (6.22).

6.4 Sensitivity Analysis

In this section, the impact of mismatched component values in CG-QHB modules has been investigated. The ripple analysis under an ideal condition and identical modules has been performed in Section 6.3. However, in practice, achieving such perfect matching among the module components, especially for the inductors might be challenging due to manufacturing tolerances and uncertainties. Therefore, following a similar approach used in Section 6.3 and assuming a mismatched value for L_{g1}, the high-frequency ripples of the AC inductors, L_{gx}, and grid current are calculated over a fundamental half-cycle for three CG-QHB interleaved modules are shown in Fig. 6.8 and Fig. 6.9, respectively. As can be seen in Fig. 6.8, a higher L_{g1} value results

in a smaller high-frequency ripple. In addition, Fig. 6.9 depicts the grid current high-frequency ripple over a wide range of mismatched L_{g1} values. In this case, the ripple cancellation effect of the PS-PWM has degraded as L_{g1} deviates from its nominal value. It also can be observed that lower values of L_{g1} have a more destructive effect on the grid-side ripple cancellation.

Furthermore, a similar sensitivity analysis has been conducted for the DC-side under mismatched L_{dc1} values. The results of this analysis are shown in Fig. 6.10. As can be realized from Fig. 6.10, a mismatched L_{dc1} leads to an increased ripple on the total DC current. As indicated by the sensitivity analysis, the mismatched inductor values among the modules decreases the effective ripple cancellation at both DC and AC sides. More specifically, incomplete cancellation of switching frequency harmonics results in non-zero harmonic clusters below Nf_{sw} frequency. Such emerging harmonics can increase THD and larger filters might be required at both DC and AC ports.

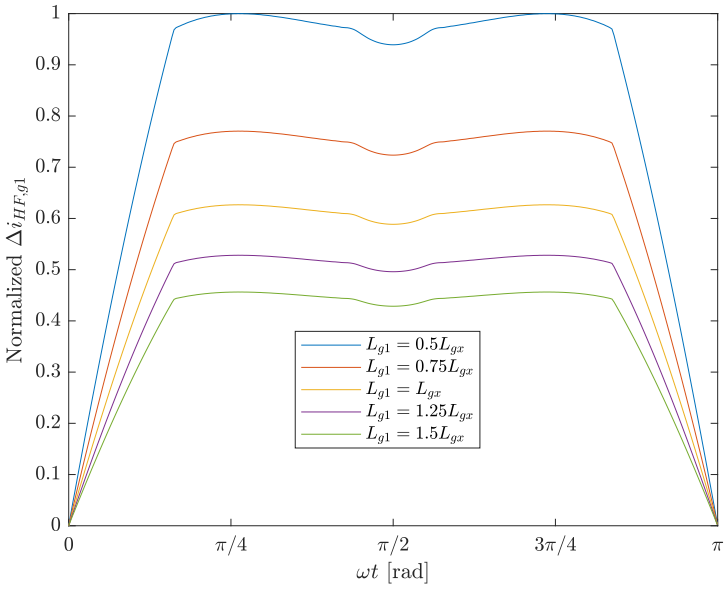


Fig. 6.8. Normalized high-frequency AC inductors current ripple under mismatched L_{g1} at $V_{dc} = 120$ V, $V_m = 340$ V, unity power factor, and $D_x = 0.76$.

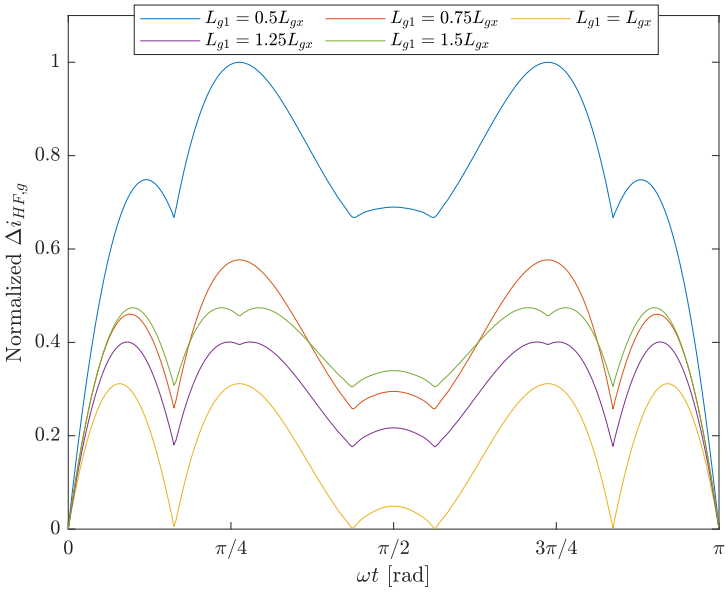


Fig. 6.9. Normalized high-frequency grid current ripple under mismatched L_{g1} at $V_{dc} = 120$ V, $V_m = 340$ V, unity power factor, and $D_x = 0.76$.

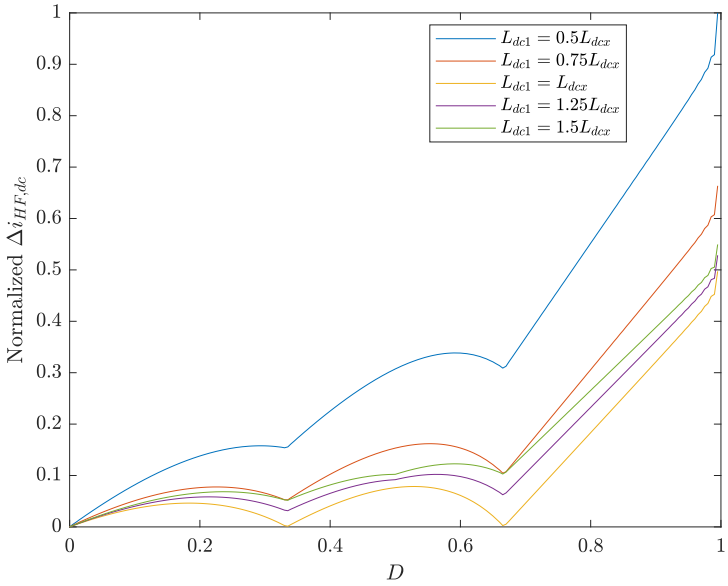


Fig. 6.10. Normalized high-frequency input current ripple under mismatched L_{dc1}.

6.5 Comparative Study

The interleaved circuit configuration of the proposed CGSB-based MLI is compared with some well-known 3L-inverter structures connected through an interleaved configuration in this section. The compared topologies are illustrated in Fig. 6.11(a)-(f) that are based on an interleaved connection of either a single-stage or two-stage circuit design to achieve a dynamic voltage conversion gain. As can be seen, due to the unity voltage gain of the conventional H-bridge inverter, the *Siwakoti*-H CGSC-based inverter [52], and the T-type inverter, a front-end DC-DC boost converter is needed to achieve a dynamic voltage conversion gain at their AC output. Additionally, the 3L-quasi Z-source topology [16], the split-source inverter [39], and the dual-boost H-bridge topology [175] are all based on an integrated voltage boosting feature with a dynamic gain. Hence, such topologies are known as single-stage DC-AC converters in which they do not need an additional front-end boost circuit. It should be noted that only modules with a 3L output voltage waveform have been considered in this section for a fair comparison, since the required filter inductor for a 2L module (such as a half-bridge) must be much larger for the same ripple and switching frequency.

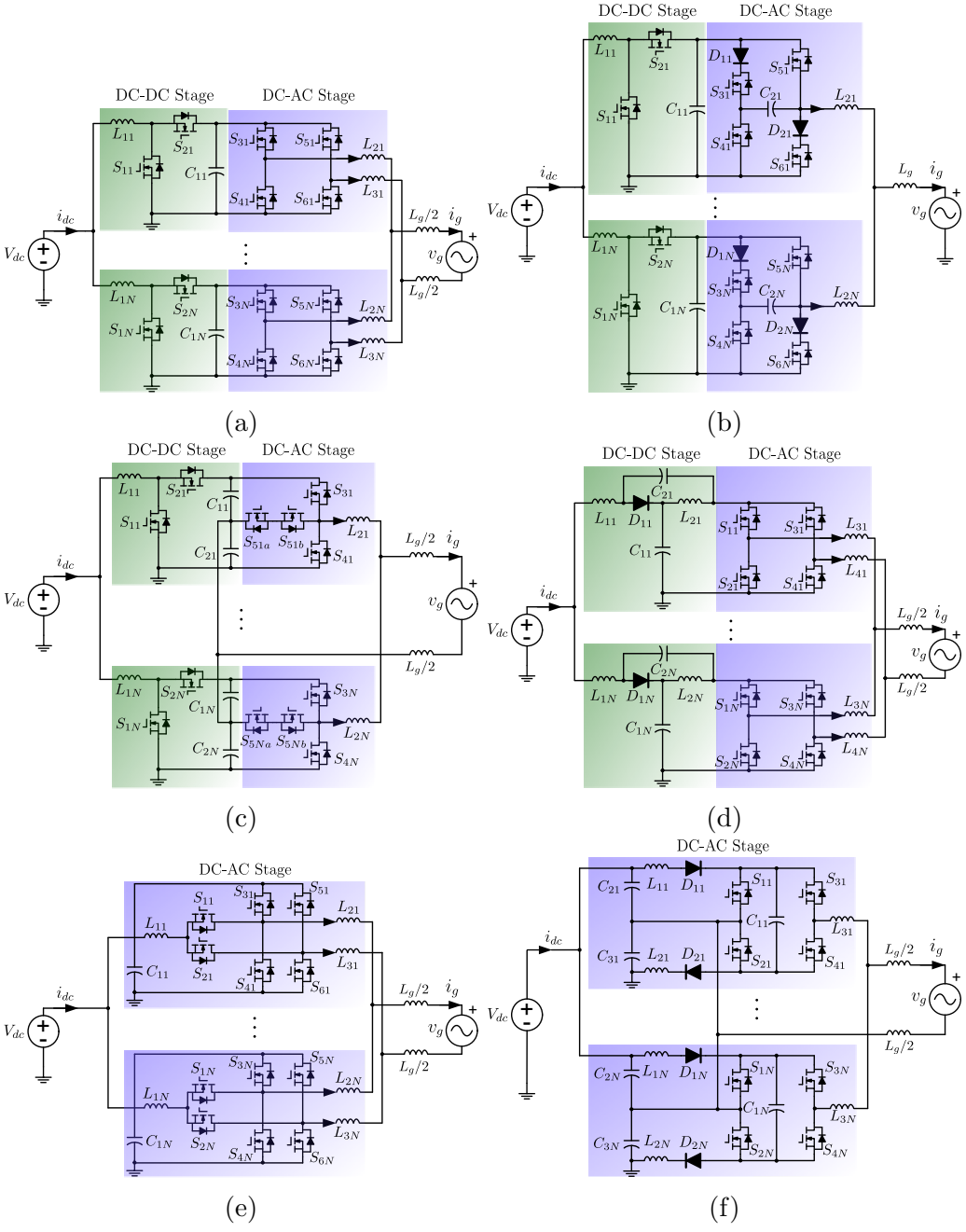


Fig. 6.11. Two-stage and single-stage single-phase interleaved DC-AC converters based on 3L modules: (a) conventional H-bridge topology; (b) Siwakoti-H topology [52]; (c) T-type topology; (d) quasi Z-source topology [16]; (e) split-source inverter topology [39]; (f) dual-boost H-bridge topology [175].

Table 6.2
A comparison of the proposed interleaved CGSB-MLI and other interleaved topologies with 3L modules

Topology	Number of Components				No. of stages	MVS (p.u.) / Uniform MVS	Bidirectional / CG feature	Continuous i_{dc} / Inrush spikes	Maximum voltage gain
	S(G)	D	C	L					
Boost + H-bridge	6N (6N)	0	N	3N	2	1 / YES	YES / NO	YES / NO	$1/(1-D)$
Boost + Siwakoti-H [52]	6N (6N)	0	2N	2N	2	1 / YES	NO / YES	YES / YES	$1/(1-D)$
Boost + T-type	6N (5N)	0	2N	3N	2	2 / NO	YES / NO	YES / NO	$0.5/(1-D)$
qZ-source + H-bridge [16]	4N (4N)	N	2N	3N	2	1 / YES	NO / NO	YES / NO	$1/(1-2D_{st}^{\star})$
Split-source [39]	6N (6N)	0	N	3N	1	1 / YES	YES / NO	YES / NO	$1/(1-D)$
Dual-boost H-bridge [175]	4N (4N)	2N	N	3N	1	1 / YES	NO / YES	NO / NO	$(1-D)/D$
Proposed CGSB-MLI	5N (5N)	0	N	2N	1	1 / YES	YES / YES	YES / NO	$D/(1-D)$

$\star$ D_{st} is the shoot-through duty cycle of the qZ-source converter.

The comparison is summarized in Table 6.2, where the comparative items are the number of required circuit components, i.e., switches (S), gate drivers (G), diodes (D), capacitors (C), and inductors (L), the number of power processing stages, the MVS and its uniformness across devices, bidirectional power flow capability and CG-based feature, continuous input current and spike-free current stress performance of the circuit, and the maximum voltage conversion gain.

As can be seen among all the above-mentioned converters with an interleaved design, which leads to the same number of output voltage levels, the proposed interleaved CGSB-based MLI needs the least number of circuit components. Continuous input current profile, spike-free current stress over the devices, uniform MVS across the switches, and the CG-based feature are other notable advantages of the proposed CGSB-based MLI. Herein, although the interleaved configuration of the quasi z-source inverter [see Fig. 6.11(d)] needs less number of power switches compared to the proposed one with larger voltage conversion gain, its leakage current propagation is prone to be high due to the lack of CG-feature. For the same reason, its interleaved design needs more number of split inductors as the grid-interface filter. Moreover, the design requirements of the coupled inductor in its two-stage-based configuration can effectively limit its power density. Regarding the dual-boost H-bridge cell with a CG-based configuration illustrated in Fig. 6.11(f), although it needs less number of active power switches compared to the proposed one, its power diode utilization can restrict the bidirectional power flow performance. The smaller size of the passive elements required for the proposed topology, as explained earlier, is also a crucial advantage for designing the whole proposed interleaved system more compact with acceptable overall efficiency.

As an analytical comparative study in terms of stresses on devices and overall efficiency, a standard PLECS simulation over all the illustrated topologies is performed, and the results are compiled in Fig. 6.12 and Fig. 6.13. The simulations are based on the same condition of the dc input voltage, $V_{dc} = 120$ V, the same switching frequency, $f_{sw} = 50$ kHz, the same devices with part number of UJ4C075018K4S, and the same peak voltage of the grid, $V_m = 340$ V for three interleaved modules to realize a 7L interleaved output voltage at 5.1 kW injected power, i.e., 1.7 kW per each module. As the *Siwakoti*-H CGSC-based inverter [52], and the T-type inverter shown in Fig. 6.11(b) and (c), respectively, require some devices with an MVS larger than 700 V, a series connection of two same SiC FETs has been considered for them to realize the large MVS required. Moreover, the diodes used in *Siwakoti*-H CGSC-based inverter [52], quasi Z-source topology [16] and dual-boost H-bridge [175] are selected from the same manufacturer with the part

number of UJ3D0650KSD as it induces a very low reverse recovery charge and forward voltage drop. Concerning the voltage conversion gain of different converters highlighted in Table 6.2, the boost duty cycle of each topology, which is either in the front-end dc-dc boost stage or in the integrated dc-ac module, is adjusted to meet the grid peak amplitude requirement and thus to inject the power to the grid. The value of passive elements, i.e., the input boost/filter inductors and capacitors, for all the compared topologies, is chosen based on the same guideline principles introduced earlier, while their ESR used in PLECS has also been highlighted in Fig. 6.12 and Fig. 6.13. Here, the same percentage of the input/injected grid currents for their low- and high-frequency ripples contents is considered for all topologies to have a fair comparison.

As can be seen from Fig. 6.12 and Fig. 6.13, the MVS across all the devices and their current stresses for the proposed topology is comparable with the two-stage boost+H-bridge converter and are always less than the most other counterparts. The same observation can be stated for the overall efficiency as the proposed interleaved CGSB-based MLI outperforms almost all its counterparts from this perspective. Even though the two-stage boost+H-bridge interleaved converter has such a comparable MVS/current stress and overall efficiency, it lacks a CG feature causing leakage current propagation issues. This can be more prominent as the proposed topology requires at least one switch less than their two-stage-based counterparts per module, as highlighted in Table 6.2, while introducing a CG feature within a single dc-to-ac conversion process. One can also notice that to achieve the same low- and high-frequency ripple contents for both the input and the injected grid currents, the capacitor required per each module of the proposed topology is smaller than all the other cases.

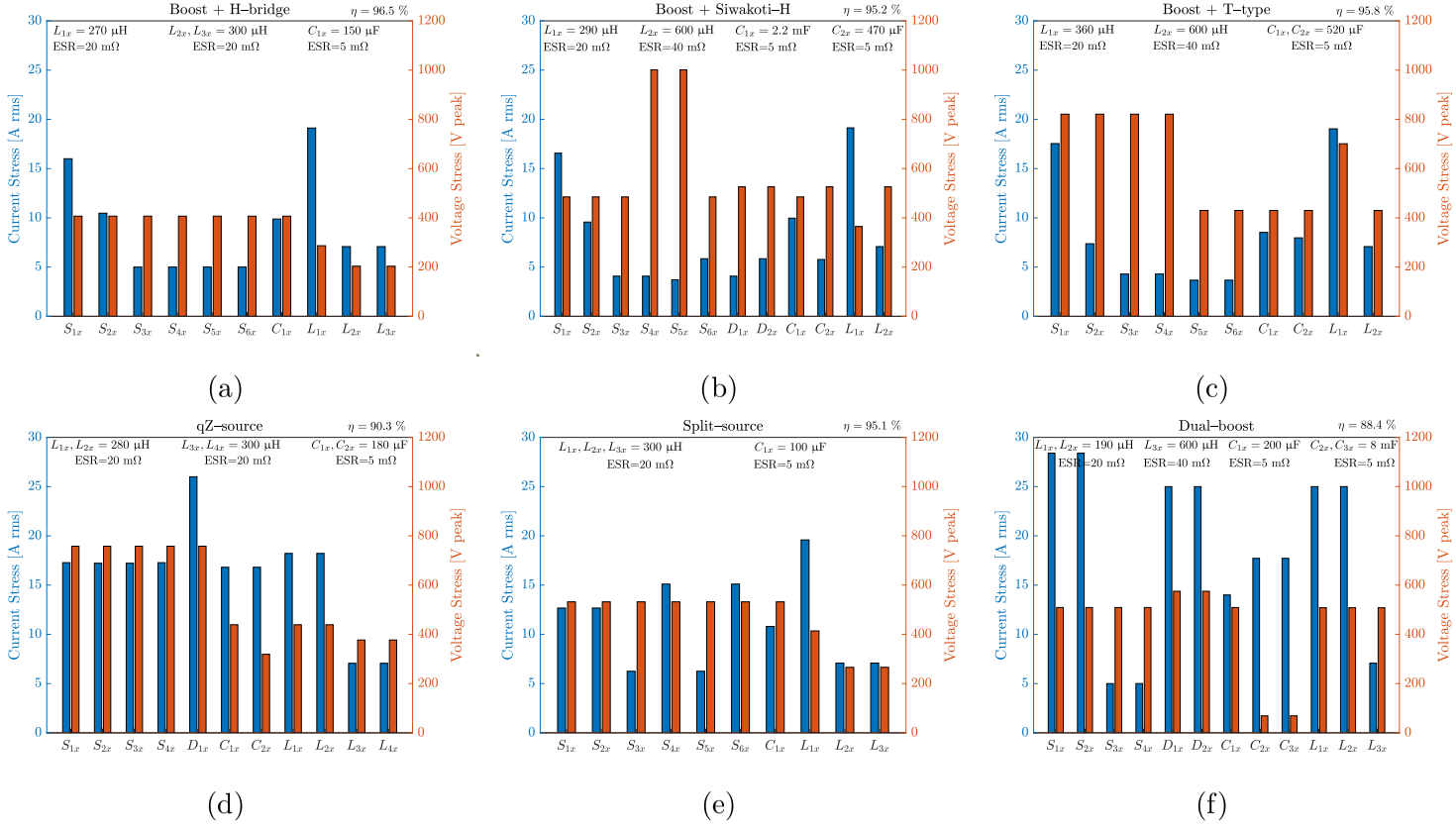


Fig. 6.12. Voltage and current stress analysis of components at 1.7kW injected power per module for the two-stage and single-stage single-phase interleaved dc-ac converters, when V_{dc}=120 V based on: (a) conventional H-bridge topology; (b) Siwakoti-H topology [52]; (c) T-type topology; (d) quasi Z-source topology [16]; (e) split-source inverter topology [39]; (f) dual-boost H-bridge topology [175].

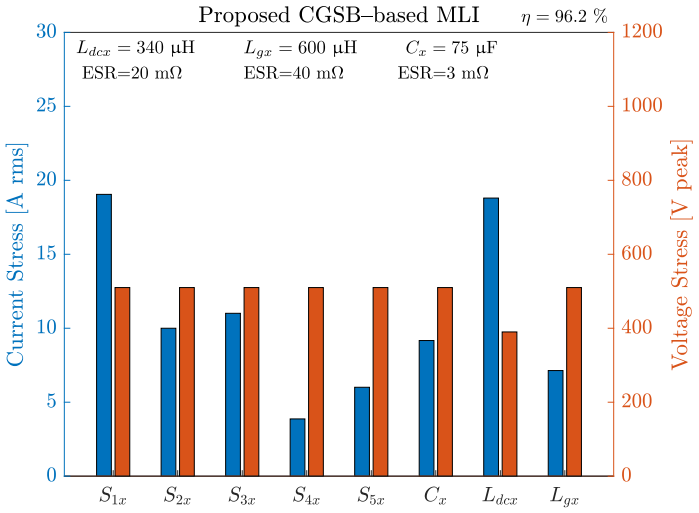


Fig. 6.13. Voltage and current stress analysis of components at 1.7kW injected power per module, when V_{dc}=120 V for the proposed CGSB-based MLI.

6.6 Experimental Results

To verify the performance of the proposed interleaved CGSB-based MLI, a 7L variant of the converter is considered and several experimental results under the grid-connected condition are presented in this section. To do this, a 5.1 kW laboratory-built prototype has been designed and implemented based on three CG-QHB modules. The closed-loop control and modulation strategy are based on the described PR controller per each module with the PS-PWM technique at 50 kHz switching frequency. All the CG-QHB modules are controlled by a custom-made controller board for rapid prototyping using a TI C2000 series DSP. Regarding the lab equipment, a four-quadrant AC grid simulator (REGATRON TC30.528.43-AC) has been used to emulate the required grid voltage and sink/source power from/to the converter. As for the DC source, four programmable DC power supplies (EA-PSI 9360-15) have been connected in parallel to provide the required DC power. Table 6.3 summarizes the system parameters, and Table 6.4 lists the key elements of the experimental prototype, while the size of chosen passive elements is based on design consideration presented in Section 6.3. In addition, an annotated view of the experimental setup is shown in Fig. 6.14. The performance of the built prototype is verified under various grid-connected steady-state and dynamic test scenarios. As for the nominal AC grid parameters, a sinusoidal

Table 6.3
System parameters used in simulation and experimental setup

Parameter	Value
f_{sw}	50 kHz
C_x, r_{C_x}	75 µF, 3 mΩ
L_{dc_x}, r_{dc_x}	340 µH, 20 mΩ
L_{g_x}, r_{g_x}	600 µH, 40 mΩ
L_g	600 µH, 10 mΩ
V_{dc}	120 V
v_g	240 V RMS, 50 Hz

Table 6.4
Components used for the experimental prototype

Element	Type and Description
Power Switches	UJ4C075018K4S
Controller	DSP-TMS320F28379D
Gate Drivers	UCC21710
Isolated DC-DC Converters	MGJ2D121505SC
Grid Simulator	TC30.528.43-AC
DC Source	EA-PSI 9360-15 (×4)

240 V RMS and 50 Hz have been considered as the grid voltage and its fundamental frequency, respectively.

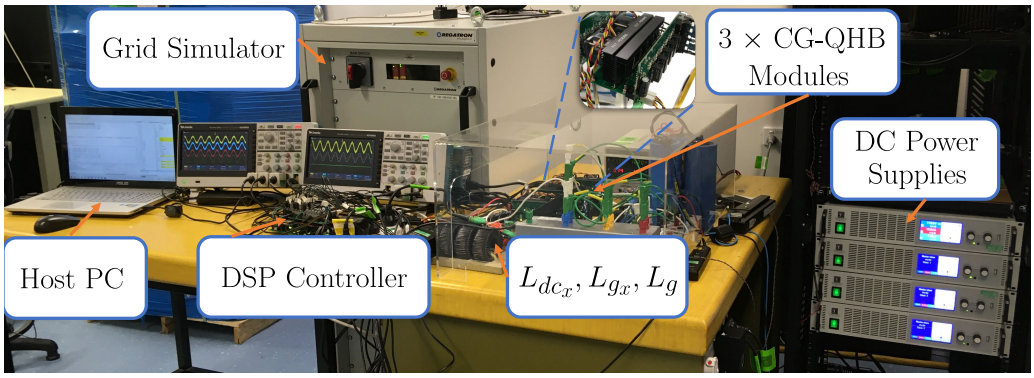


Fig. 6.14. A view of the experimental setup.

To show the single-stage operation of the proposed converter, the DC

input voltage is set at 120 V. Hence, to meet the grid peak voltage, the boost duty cycle D_x for all three integrated CG-QHB modules is set at 0.76. The steady-state experimental result of the proposed converter showing the DC input voltage V_{dc}, the 7L resultant inverter output voltage v_{inv}, the grid voltage v_g, and the injected grid current i_g at the rated 5.1 kW injected power is shown in Fig. 6.15(a). The boosted voltage across the capacitor of each module is shown in Fig. 6.15(b) at $P_g = 4.6$ kW. Furthermore, the bidirectional power flow operation of the proposed converter has been shown in Fig. 6.15(c) at $P_g = -1.3$ kW (transferring the power from the grid to the DC source). As it can be confirmed, all the 7L output voltage through the interleaved connection of the CG-QHB modules with a quality injected current are generated, while the input current profile of the converter possesses a double-line frequency, and the boosted voltage across the capacitor per module is around 500 V.

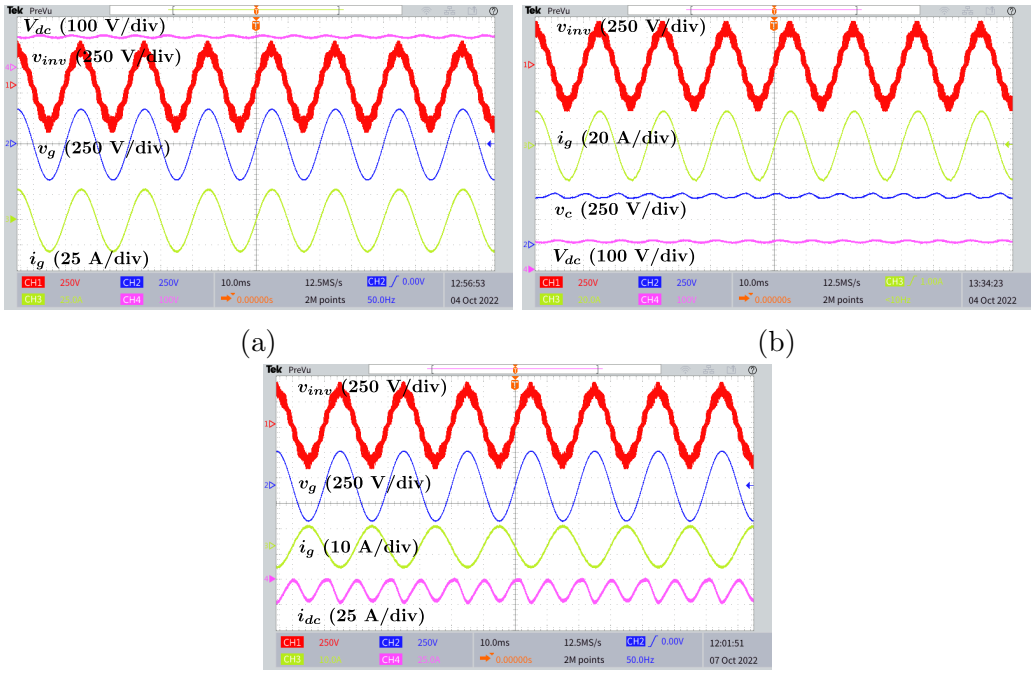


Fig. 6.15. Experimental results at $V_{dc} = 120$ V (a) steady-state at $P_g = 5.1$ kW and $D_x = 0.76$; (b) steady-state DC input voltage and capacitor voltages at $P_g = 4.6$ kW and $D_x = 0.76$; (c) steady-state input currents at $P_g = -1.3$ kW and $D_x = 0.75$.

The 3L output voltage of each of CG-QHB modules and the resultant 7L output voltage of the inverter at the rated power of 5.1 kW; the injected

AC output current of each module and the total injected grid current at the same rated power; and the input current of each module with the resultant input current of the converter at the rated power of 4.6 kW are also provided in Fig. 6.16(a)-(c), respectively. Here, in order to share an equal injected current per each CG-QHB module, the value of λ_x in the control system is set at 1/3. The zoomed-in views of the same set of the results shown in Fig. 6.16(d)-(f) can further emphasize the applied PS-PWM technique, where the module output voltage and currents are shifted by 120° at the switching frequency.

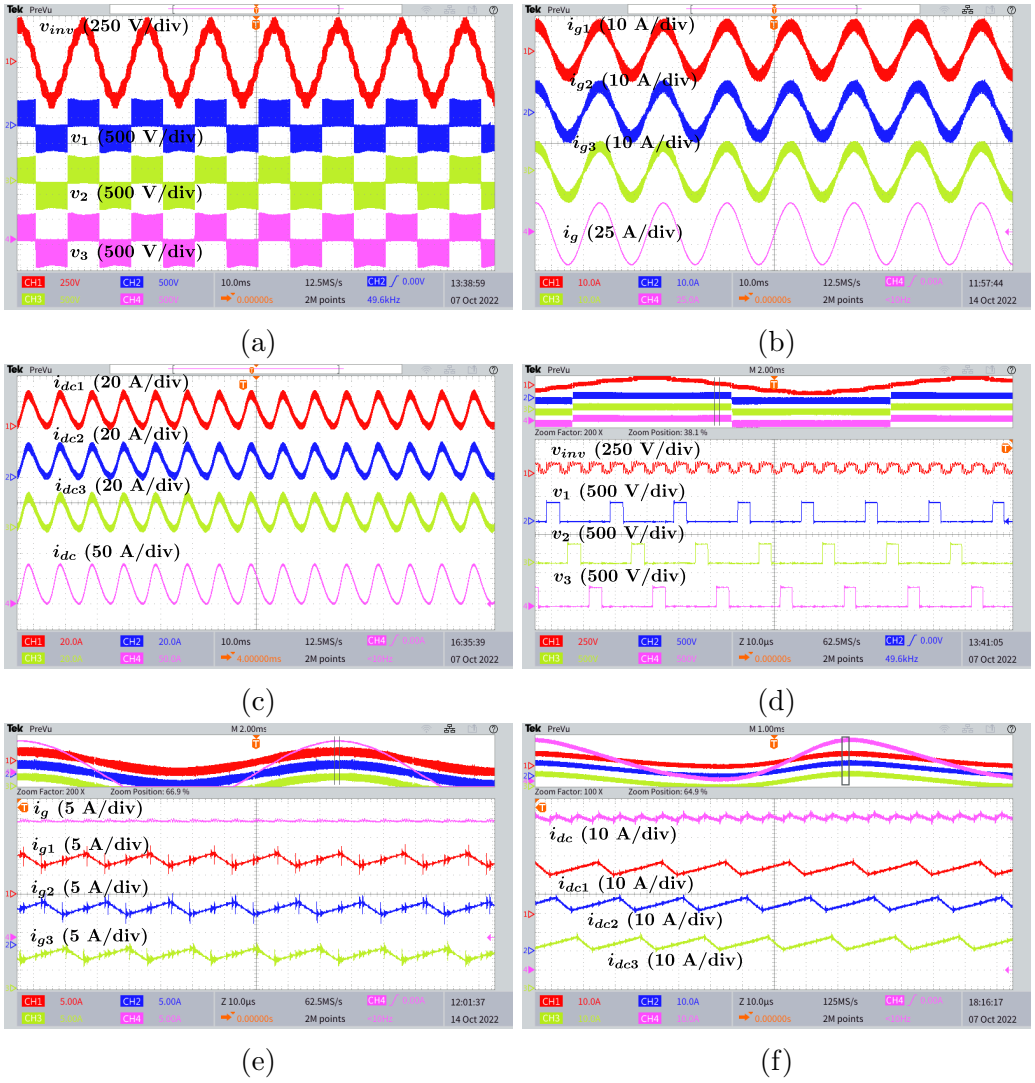


Fig. 6.16. Experimental steady-state results at $V_{dc} = 120$ V and $D_x = 0.76$ (a) inverter and individual modules' output voltages at $P_g = 5.1$ kW; (b) module AC currents at $P_g = 5.1$ kW; (c) module DC input currents at $P_g = 4.6$ kW; (d) zoomed-in view of inverter and modules' output voltages at $P_g = 5.1$ kW; (e) zoomed-in view of module AC currents at $P_g = 5.1$ kW; (f) zoomed-in view of module DC input currents at $P_g = 4.6$ kW.

Considering the same value of the DC input voltage and the same boost duty cycle per each CG-QHB module, the reactive power support results of the proposed converter, i.e., lagging and leading power factors, have been shown in Fig. 6.17(a)-(b). Additionally, the measured leakage current of the resultant system, the 7L output voltage of the proposed converter, the

grid voltage, and the resultant injected current at 4.6 kW are presented in Fig. 6.17(c). As can be seen, due to the CG-based configuration of the proposed system, the reported value of the leakage current is less than 20 mA, which meets the requirements of the available standards for transformerless grid-connected converters.

In the following, the experimental result shown in Fig. 6.17(d) confirms the dynamic response of the proposed interleaved configuration in injecting 20 A peak overall current to the grid, while the current reference of each CG-QHB module is suddenly changed as per (6.13)-(6.14). Here, 3.4 kW is constantly injected into the grid, while one of the modules is injecting zero current, i.e., $i^{\star}_{g_1} = 0$. Hence, the other two modules must support the grid with a larger injected current as per (6.13)-(6.14). The associated dynamic results of the proposed converter from zero to 3.4 kW injected power have also been taken by the experiment and shown in Fig. 6.17(e). The set of waveforms in this result is the 7L inverter output voltage, the grid voltage, the injected grid current and the input current drawn from the DC source. To further emphasize on single-stage dynamic voltage conversion gain of the proposed interleaved CGSB-based MLI, the DC input voltage is changed within a ramp trend in the next dynamic test, i.e., from 60 V to 120 V. Here, to inject a constant power of 1.2 kW to the grid, the fundamental component of the converter output voltage is kept fixed at 400 V. As per (6.3), the boost duty cycle D_x per each module is dynamically changed to meet the peak amplitude of the grid voltage by the output voltage of the proposed converter. The experimental results of this dynamic test showing the 7L output voltage of the proposed converter without having any distortion, the grid voltage, and the injected current are illustrated in Fig. 6.17(f).

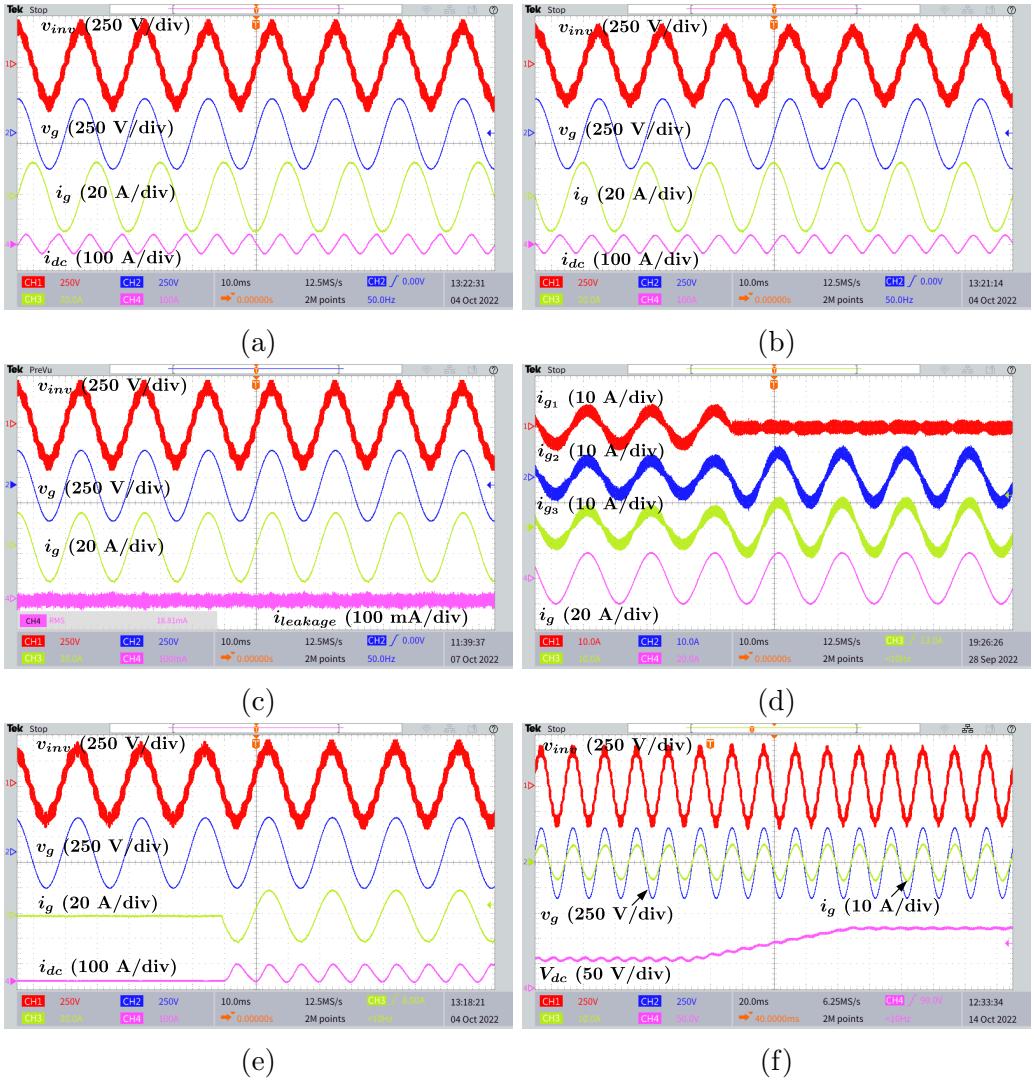


Fig. 6.17. Experimental results at (a) $V_{dc} = 120$ V, D_x= 0.76, $P_g = 0$ kW, and $Q_g = -4.1$ kVAr; (b) $V_{dc} = 120$ V, D_x= 0.76, $P_g = 0$ kW, and $Q_g = +4.1$ kVAr; (c) $V_{dc} = 120$ V, D_x= 0.76, $P_g = 4.6$ kW, showing leakage current; (d) $V_{dc} = 120$ V, D_x= 0.76, $P_g = 3.4$ kW, showing dynamic unequal current sharing for active thermal control; (e) $V_{dc} = 120$ V, D_x= 0.76, showing a step change transition from $P_g = 0$ kW to $P_g = 3.4$ kW; (f) $P_g = 1.2$ kW, showing dynamic voltage boosting capability of the proposed CGSB-7L converter under a ramp transition of $V_{dc} = 60$ V to $V_{dc} = 120$ V.

Furthermore, the start-up operation of the proposed 7L-CGSB-based interleaved converter before and after the connection to the grid at the zero injected power is verified through the experiment as shown in Fig. 6.18(a).

Similar to the previous case studies, the DC input voltage and the boost duty cycle of all three involved CG-QHB modules are set at 120 V and 0.76, respectively. To further attest the unequal power handling capability of each CG-QHB module in the proposed interleaved system and to evaluate the bidirectional power flow capability of CG-QHB modules while injecting a 15 A peak grid current, i.e., $i_g^\star = 15A$, the experimental results shown in Fig. 6.18(b)-(c) can be considered. Here, the peak current reference of two out of three CG-QHB modules is set at 10 A, while for the third one, it is set at -5 A. Hence, considering (6.13) and (6.14), the power for the first two modules is flowing from the DC source to the grid, while for the third module, a reverse power flow can be observed. As can be seen from Fig. 6.18(b), due to the 50 kHz frequency of each module, their output current possesses a high-frequency ripple while tracking their current references. However, because of the interleaved configuration and the described PS-PWM strategy, the total injected grid current maintains a clean sinusoidal waveform with a peak of 15 A and a 150 kHz apparent switching frequency. The same observation can also be realized from the input current of each CG-QHB module and the resultant input current of the DC source shown in Fig. 6.18(c), while a double-line frequency of the grid is dominant. These results confirm that the proposed CGSB-based converter does not induce any large pulsating inrush spikes even though offering an integrated voltage-boosting feature.

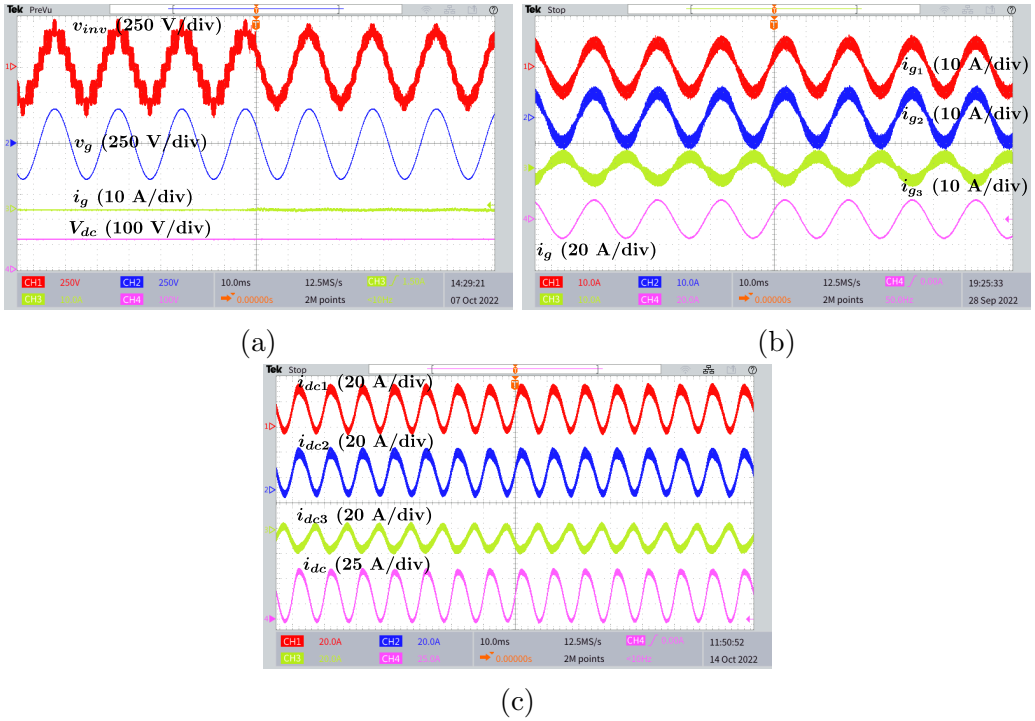


Fig. 6.18. Experimental results at V_{dc} = 120 V, D_x= 0.76 (a) before and after the grid connection; (b) AC output currents at unequal power references and power flow directions; (c) DC input currents at unequal power references and power flow directions.

Additionally, to show the impact of the PS-PWM strategy on the proposed inverter output voltage harmonics, the FFT results shown in Fig. 6.19 can be considered. As can be realized, the first high-frequency harmonic cluster of the proposed 7L-CGSB-based interleaved converter output voltage is located at around 150 kHz (three times the switching frequency of each CG-QHB module), leading to around 0.1% THD for the first 50 low-frequency harmonics.

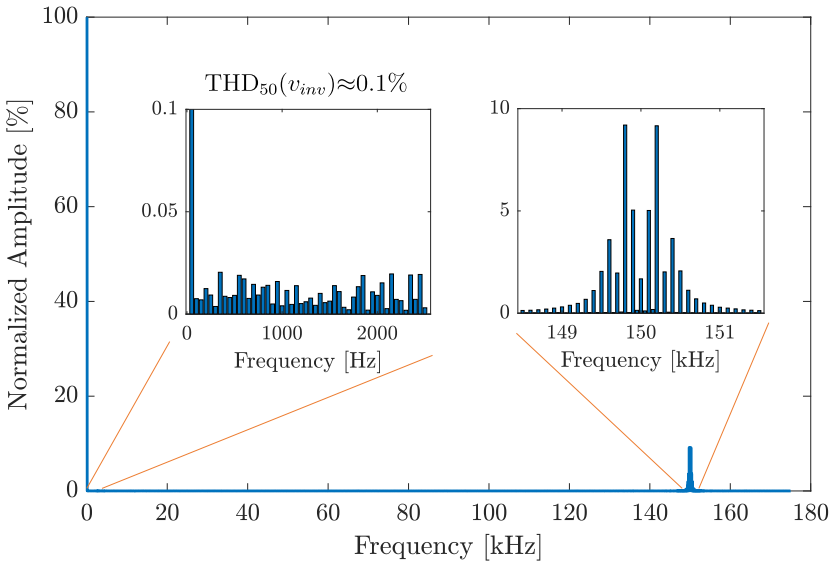


Fig. 6.19. Inverter output voltage harmonics of the proposed interleaved CGSB-based MLI with three CG-QHB modules at $V_{dc} = 120$ V, $D_x = 0.76$, and $P_g = 5.1$ kW.

Finally, a loss breakdown analysis has been developed and shown in Fig. 6.20 using PLECS and the provided thermal model of the semiconductor devices. The used parameters for this analysis are indicated in Table 6.4. The results are taken at 50 kHz switching frequency and under the same condition of the grid voltage at the rated power of 5.1 kW, while the DC input voltage and the boost duty cycle of the proposed 7L-CGSB-based interleaved converter are set at 120 V and 0.76, respectively. Regarding the obtained results, the overall efficiency of the entire system, including the effects of the grid-interface filters through both PLECS and measurement results, are shown in Fig. 6.21. As can be seen, the efficiency of the proposed grid-connected CG-based converter over a wide range of the injected grid power is more than 95%, which is an acceptable range for a boost-based MLI feeding through a low magnitude of the available DC input voltage.

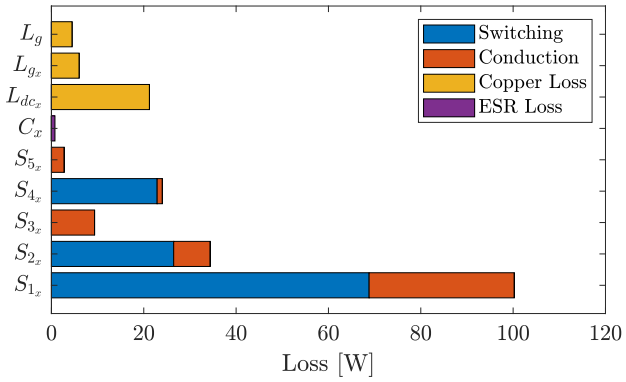


Fig. 6.20. Loss breakdown of the proposed interleaved CGSB-based MLI using PLECS with three CG-QHB modules at $V_{dc} = 120$ V, $P_g = 5.1$ kW, and $D_x = 0.76$.

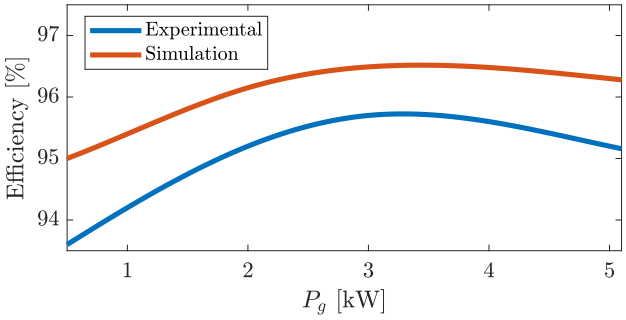


Fig. 6.21. Simulated and experimental efficiency curves of the proposed interleaved CGSB-based MLI with three CG-QHB modules at $V_{dc} = 120$ V and $D_x = 0.76$.

6.7 Conclusion

The interleaved configuration of a new CGSB-based MLI featuring a single-source single-stage SB-based concept has been developed in this work. Details of the working principles, modulation strategy and closed-loop control under the grid-connected condition have been presented. The proposed topology has a high power handling capability compared to the existing CGSB-based MLIs due to its interleaved-based modular design, as it is comprised of several identical CG-QHB modules. All the switches have equal MVS, while the converter can be modulated using a PS-PWM technique leading to further reducing the size of the grid-interface filter. The input current of the proposed converter is continuous with a dominant double-line frequency

component in a single-phase grid-connected application, while it has a generalization capability to realize any number of output voltage levels. Design guidelines for the passive elements and extensive experimental results over a 7L variant of the proposed topology have also been presented. The results show around 96% efficiency over a wide range of the injected grid power even when a low magnitude of the DC input voltage for a 240 V RMS grid voltage is available.

Chapter 7

Conclusions and Future Work

In this thesis, the available solutions for power conversion systems in smart grids and microgrids have been reviewed. In terms of converter topologies, various DC-AC converters have been considered, categorized, and compared based on their overall configuration and working principles. Then, numerous conventional linear and more advanced non-linear control methods and controller types have been studied. Moreover, the common modulation techniques used in switching power converters have been included and briefly explained.

Furthermore, some of the identified design and control challenges in power converters, and more specifically grid-connected inverters, are provided. The summary of these challenges are as follows:

- Output filter size, leakage current, and power quality: The filtering requirements and THD of the injected current of grid-connected inverters can be reduced by reducing the volt-second applied to the filter inductors. This can be achieved by increasing the apparent output frequency and/or by using multilevel inverters (e.g., 5L or higher). Moreover, using inverter structures with constant or zero CMV (e.g., NPC-based or CG-based inverters) allows for employing smaller common-mode filters or even eliminating it. These steps are aligned with the available grid codes and power quality standards (e.g., IEEE 519-2014 [113]).

- Non-ideal grids and voltage harmonics: The grid voltage in real-life conditions might be distorted with low-frequency harmonics due to high-impedance power transmission lines, unbalanced loads, unbalanced faults, and non-linear loads such as diode-bridge rectifiers with capacitive DC filters. A grid-connected inverter should be able to still inject a sinusoidal current into the distorted grid to comply with the grid codes and help the grid stability. Hence, some challenges in grid synchronization

and current reference generation can be observed. The non-ideal grid conditions such as high grid impedance (weak grid), voltage harmonics, and unbalanced voltages in three-phase systems can negatively impact the performance of synchronization methods and power quality of the system.

- Scalability: A modular structure helps to reach the required power levels without redesigning the whole system, while respecting the voltage/current limitations of the power components. It also allows for an optimized and economic solution to be used in a wide range of systems. Cascading and paralleling techniques can be used at different scales (i.e., device-level, module-level, or converter-level) to scale the power levels. Interleaving and active current/voltage sharing techniques should be utilized to achieve advanced features, such as ATC, reliability and lifetime improvements, etc.

- Power decoupling: Reducing the low-frequency ripples on the DC-side of the single-phase converters is essential for PV, battery, and fuel-cell applications. Passive (PPD) and active (APD) methods can be used to achieve a flat DC input current in a single-phase inverter, while injecting the power to an AC grid and meeting power quality constraints. Most of the APD implementations need additional circuit components to be added to the inverter. However, some single-stage single-phase inverters have a potential to integral APD into their structure without any additional components. However, most of them are only 2L or 3L inverters. Moreover, achieving a high-quality APD under non-ideal grid conditions (e.g., distorted grid voltage with low-frequency harmonics) makes APD implementation more challenging in practice.

- Single-stage dynamic voltage boosting and bidirectional power flow: Conventional two-stage DC-AC architecture can be found in many residential and industrial applications. Nonetheless, the efficiency and power density of the whole system might be limited due to the associated losses with each power processing stage. Therefore, single-stage inverters with built-in dynamic voltage-boosting capability can be potential solutions to overcome the mentioned limitations. In addition, bidirectional power flow is essential in battery and EV applications as two of the most impactful technologies in smart grids.

Considering the above-mentioned literature review and the identified opportunities and challenges in control, modulation, and topologies of grid-connected multilevel converters, the following motivations have been pursued in the proposed ideas in this thesis:

- To develop topologies, modulation methods, and control strategies for single-stage grid-connected inverters with the dynamic voltage-boosting capability
- To improve the overall efficiency and power density of single-stage boost inverters fed by low-voltage and wide-varying DC sources such as PV panels or batteries
- To propose and control modular DC-AC converters with bidirectional power flow handling capability
- To meet power quality requirements even under non-ideal grid conditions
- To propose APD control strategies for single-stage multilevel inverters

Considering the above-mentioned motivations, several topology and control ideas have been proposed in this work: In Chapter 3, a novel single-stage 5L boost inverter with a large dynamic voltage gain is proposed for PV and battery applications. The other notable features of this inverter are the reduced number of active and passive components, continuous input current profile, uniform MVS across all circuit components, reduced CMV, and bidirectional power flow capability. In Chapter 4, an APD control strategy for the proposed single-phase 5L boost inverter is introduced. The major contributions of the proposed controller are achieving a flat and ripple-free DC input current even under a distorted grid voltage condition, using a single PR controller as the grid current controller, and robust and stable operation under a wide range of uncertainties and disturbances in the system parameters and measurements. Next, in Chapter 5, a flexible APD control strategy has been proposed based on the CCS-MPC method. The main benefit of the proposed controller is obtaining an adjustable tradeoff between the capacitor voltage ripple and DC input current ripple. Furthermore, in Chapter 6, a modular interleaved single-stage boost inverter is proposed. The major features of this inverter are uniform voltage stress across all circuit components, bidirectional power flow and full reactive power support, and increased apparent output frequency by using a hybrid PS-PWM technique.

7.1 Recommendations & Future Works

Based on the contributions of this work, the following directions for the future works are recommended:

- Exploring the possibility of soft-switching transitions through different modulation techniques (e.g., triangular) to improve the overall efficiency and power density of the system
- Applying high-frequency isolation techniques to broaden the applications of the proposed converters
- Including higher-order filters (e.g., LCL) with active damping strategies for improving power quality and power density
- Investigating the fault-tolerance capabilities of the proposed converters with custom modulation and control methods, designed for smooth transition to the faulty mode
- Evaluating the proposed solutions from the reliability viewpoint and comparative assessment based on expected lifetime under different mission profiles
- Implementing the proposed APD methods to other modular inverter systems
- Considering the DC source limitations and characteristics (e.g., maximum current, degradation, etc.) in the proposed flexible APD method to improve the transient power handling capability of grid-connected boost inverters and extending the system's lifetime and operating range.
- Exploring APD methods in unbalanced three-phase systems

Bibliography

[1] "Australia's energy strategies and frameworks." [Online]. Available: https://www.energy.gov.au/government-priorities/australias-energy-strategies-and-frameworks

[2] "National energy performance strategy." [Online]. Available: https://www.energy.gov.au/government-priorities/australias-energy-strategies-and-frameworks/national-energy-performance-strategy

[3] "Australian energy statistics." [Online]. Available: https://www.energy.gov.au/publications/australian-energy-.statistics-table-o-electricity-generation-fuel-type-2021-22-and-2022

[4] "Net zero." [Online]. Available: https://www.dcceew.gov.au/climate-change/emissions-reduction/net-zero

[5] J. Kim, J. Lee, and B. H. Cho, "Equivalent circuit modeling of pem fuel cell degradation combined with a lfrc," *IEEE Transactions on Industrial Electronics*, vol. 60, DOI 10.1109/TIE.2012.2226414, no. 11, pp. 5086–5094, 2013.

[6] V. Monteiro, J. G. Pinto, and J. L. Afonso, "Operation modes for the electric vehicle in smart grids and smart homes: Present and proposed modes," *IEEE Transactions on Vehicular Technology*, vol. 65, DOI 10.1109/TVT.2015.2481005, no. 3, pp. 1007–1020, 2016.

[7] Z. Liu, D. Wang, H. Jia, N. Djilali, and W. Zhang, "Aggregation and bidirectional charging power control of plug-in hybrid electric vehicles: Generation system adequacy analysis," *IEEE Transactions on Sustainable Energy*, vol. 6, DOI 10.1109/TSTE.2014.2372044, no. 2, pp. 325–335, 2015.

[8] B. Chauhan and S. K. Jain, "Scheduling of electric vehicle's power in v2g and g2v modes using an improved charge-discharge opportunity-

based approach," *IEEE Transactions on Transportation Electrification*, DOI 10.1109/TTE.2023.3265681, pp. 1–1, 2023.

[9] M. G. Varzaneh, A. Rajaei, M. Forouzesh, Y. P. Siwakoti, and F. Blaabjerg, "A single-stage multi-port buck-boost inverter," *IEEE Transactions on Power Electronics*, vol. 36, no. 7, pp. 7769–7782, 2021.

[10] A. Abramovitz, B. Zhao, and K. M. Smedley, "High-gain single-stage boosting inverter for photovoltaic applications," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3550–3558, 2016.

[11] H. K. Jahan, R. Pourebrahim, S. Tohidi, S. Peyghami, A. M. Shotorbani, and F. Blaabjerg, "Two-stage single-source full-bridge based three- phase inverter for medium voltage applications," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1–6, 2020.

[12] B. Wei, A. Marzàbal, J. Perez, R. Pinyol, J. M. Guerrero, and J. C. Vásquez, "Overload and short-circuit protection strategy for voltage source inverter-based ups," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2019.2898165, no. 11, pp. 11 371–11 382, 2019.

[13] M. Guacci, D. Zhang, M. Tatic, D. Bortis, J. W. Kolar, Y. Kinoshita, and H. Ishida, "Three-phase two-third-pwm buck-boost current source inverter system employing dual-gate monolithic bidirectional gan e-fets," *CPSS Transactions on Power Electronics and Applications*, vol. 4, DOI 10.24295/CPSSTPEA.2019.00032, no. 4, pp. 339–354, 2019.

[14] P. P. Dash and M. Kazerani, "Dynamic modeling and performance analysis of a grid-connected current-source inverter-based photovoltaic system," *IEEE Transactions on Sustainable Energy*, vol. 2, DOI 10.1109/TSTE.2011.2149551, no. 4, pp. 443–450, 2011.

[15] L. Ding, Y. Lian, and Y. W. Li, "Multilevel current source converters for high power medium voltage applications," *CES Transactions on Electrical Machines and Systems*, vol. 1, DOI 10.23919/TEMS.2017.8086110, no. 3, pp. 306–314, 2017.

[16] J. Anderson and F. Peng, "Four quasi-z-source inverters," in *2008 IEEE Power Electronics Specialists Conference*, DOI 10.1109/PESC.2008.4592360, pp. 2743–2749, 2008.

[17] P. C. Loh and F. Blaabjerg, "Magnetically coupled impedance-source inverters," *IEEE Transactions on Industry Applications*, vol. 49, DOI 10.1109/TIA.2013.2262032, no. 5, pp. 2177–2187, 2013.

[18] F. Z. Peng, "Z-source inverter," *IEEE Transactions on Industry Applications*, vol. 39, DOI 10.1109/TIA.2003.808920, no. 2, pp. 504–510, 2003.

[19] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, "Impedance-source networks for electric power conversion part i: A topological review," *IEEE Transactions on Power Electronics*, vol. 30, DOI 10.1109/TPEL.2014.2313746, no. 2, pp. 699–716, 2015.

[20] L. Zhou, F. Gao, and T. Xu, "Implementation of active npc circuits in transformer-less single-phase inverter with low leakage current," *IEEE Transactions on Industry Applications*, vol. 53, DOI 10.1109/TIA.2017.2736965, no. 6, pp. 5658–5667, 2017.

[21] W. Chen, X. Yang, W. Zhang, and X. Song, "Leakage current calculation for pv inverter system based on a parasitic capacitor model," *IEEE Transactions on Power Electronics*, vol. 31, DOI 10.1109/TPEL.2016.2517740, no. 12, pp. 8205–8217, 2016.

[22] H. Xiao, "Overview of transformerless photovoltaic grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 36, DOI 10.1109/TPEL.2020.3003721, no. 1, pp. 533–548, 2021.

[23] S. S. Lee, Y. P. Siwakoti, R. Barzegarkhoo, and F. Blaabjerg, "A novel common-ground-type nine-level dynamic boost inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, DOI 10.1109/JESTPE.2021.3104939, no. 4, pp. 4435–4442, 2022.

[24] R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, S. S. Lee, F. Blaabjerg, and Y. P. Siwakoti, "Common-ground grid-connected five-level transformerless inverter with integrated dynamic voltage boosting feature," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, DOI 10.1109/JESTPE.2022.3159706, no. 6, pp. 6661–6672, 2022.

[25] F. B. Grigoletto, "Five-level transformerless inverter for single-phase solar photovoltaic applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, DOI 10.1109/JESTPE.2019.2891937, no. 4, pp. 3411–3422, 2020.

[26] S. S. Lee and K.-B. Lee, "Switched-capacitor-based modular t-type inverter," *IEEE Transactions on Industrial Electronics*, vol. 68, DOI 10.1109/TIE.2020.2992963, no. 7, pp. 5725–5732, 2021.

[27] R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, F. Blaabjerg, and Y. P. Siwakoti, "A novel active neutral point-clamped five-level inverter with single-stage-integrated dynamic voltage boosting feature," *IEEE Transactions on Power Electronics*, vol. 38, DOI 10.1109/TPEL.2023.3257959, no. 6, pp. 7796–7809, 2023.

[28] Q.-C. Zhong, W.-L. Ming, W. Sheng, and Y. Zhao, "Beijing converters: Bridge converters with a capacitor added to reduce leakage currents, dc-bus voltage ripples, and total capacitance required," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 325–335, 2017.

[29] P. Poblete, S. Neira, R. P. Aguilera, J. Pereda, and J. Pou, "Sequential phase-shifted model predictive control for modular multilevel converters," *IEEE Transactions on Energy Conversion*, vol. 36, DOI 10.1109/TEC.2021.3074863, no. 4, pp. 2691–2702, 2021.

[30] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on Industry Applications*, vol. IA-17, DOI 10.1109/TIA.1981.4503992, no. 5, pp. 518–523, 1981.

[31] D. Floricau, E. Floricau, and M. Dumitrescu, "Natural doubling of the apparent switching frequency using three-level anpc converter," in *2008 International School on Nonsinusoidal Currents and Compensation*, DOI 10.1109/ISNCC.2008.4627496, pp. 1–6, 2008.

[32] Z. Wang, Y. Wu, M. H. Mahmud, Z. Zhao, Y. Zhao, and H. A. Mantooth, "Design and validation of a 250-kw all-silicon carbide high-density three-level t-type inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, DOI 10.1109/JESTPE.2019.2951625, no. 1, pp. 578–588, 2020.

[33] J. Huber and J. W. Kolar, "Monolithic bidirectional power transistors," *IEEE Power Electronics Magazine*, vol. 10, DOI 10.1109/MPEL.2023.3234747, no. 1, pp. 28–38, 2023.

[34] P. Wheeler, J. Rodriguez, J. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *IEEE Transactions on Industrial Electronics*, vol. 49, DOI 10.1109/41.993260, no. 2, pp. 276–288, 2002.

[35] S. Bhattacharya, R. Narwal, S. S. Shah, B. J. Baliga, A. Agarwal, A. Kanale, K. Han, D. C. Hopkins, and T.-H. Cheng, "Power conversion systems enabled by sic bidfet device," *IEEE Power Electronics Magazine*, vol. 10, DOI 10.1109/MPEL.2023.3237060, no. 1, pp. 39–43, 2023.

[36] H. Schmidt, C. Siedle, and K. Ketterer, "DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current," *U.S. Patent*, vol. US20050174817A1, 2006.

[37] M. Victor, G. F., S. Bremicker, and U. Hubler, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into an alternating current voltage," *U.S. Patent*, vol. US7411802B2, 2008.

[38] L. Zhang, K. Sun, L. Feng, H. Wu, and Y. Xing, "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," *IEEE Transactions on Power Electronics*, vol. 28, DOI 10.1109/TPEL.2012.2205406, no. 2, pp. 730–739, 2013.

[39] S. S. Lee and Y. E. Heng, "Improved single-phase split-source inverter with hybrid quasi-sinusoidal and constant pwm," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2016.2624724, no. 3, pp. 2024–2031, 2017.

[40] J. Azurza Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, DOI 10.1109/OJPEL.2020.3018220, pp. 322–338, 2020.

[41] Y. Y. Syasegov, M. Farhangi, R. Barzegarkhoo, L. Li, D. D.-C. Lu, R. P. Aguilera, and Y. P. Siwakoti, "Heric-clamped and pn-npc inverters with five-level output voltage and reduced grid-interfaced filter size," *IEEE Open Journal of Power Electronics*, vol. 4, DOI 10.1109/OJPEL.2023.3265062, pp. 306–318, 2023.

[42] J. Chivite-Zabalza, D. R. Trainer, J. C. Nicholls, and C. C. Davidson, "Balancing algorithm for a self-powered high-voltage switch using series-connected igbts for hvdc applications," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2018.2889375, no. 9, pp. 8481–8490, 2019.

[43] Z. Gao, S. Shao, W. Cui, J. Zhang, X. Chen, and K. Sheng, "A voltage balancing method for series-connected power devices based on active clamping in voltage source converters," *IEEE Transactions on Power Electronics*, vol. 37, DOI 10.1109/TPEL.2022.3163586, no. 9, pp. 10 620–10 632, 2022.

[44] Z. Lu, C. Li, A. Zhu, H. Luo, C. Li, W. Li, and X. He, "Medium voltage soft-switching dc/dc converter with series-connected sic mosfets," *IEEE Transactions on Power Electronics*, vol. 36, DOI 10.1109/TPEL.2020.3007225, no. 2, pp. 1451–1462, 2021.

[45] Q. Wu, M. Wang, W. Zhou, and X. Wang, "Current balancing of paralleled sic mosfets for a resonant pulsed power converter," *IEEE Transactions on Power Electronics*, vol. 35, DOI 10.1109/TPEL.2019.2952326, no. 6, pp. 5557–5561, 2020.

[46] R. H. Cuzmar, J. Pereda, and R. P. Aguilera, "Phase-shifted model predictive control to achieve power balance of chb converters for large-scale photovoltaic integration," *IEEE Transactions on Industrial Electronics*, vol. 68, DOI 10.1109/TIE.2020.3026299, no. 10, pp. 9619–9629, 2021.

[47] D. Karwatzki and A. Mertens, "Generalized control approach for a class of modular multilevel converter topologies," *IEEE Transactions on Power Electronics*, vol. 33, DOI 10.1109/TPEL.2017.2703917, no. 4, pp. 2888–2900, 2018.

[48] L. Ren, L. Zhang, L. Wang, and S. Dai, "Capacitor voltage regulation strategy for 7-level single dc source hybrid cascaded inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, DOI 10.1109/JESTPE.2022.3172146, no. 5, pp. 5773–5784, 2022.

[49] T. Debnath, K. Gopakumar, L. Umanand, D. Zielinski, and K. Rajashekara, "A nine-level inverter with single dc-link and low-voltage capacitors as stacked voltage sources with capacitor voltage control irrespective of load power factor," *IEEE Open Journal of the Industrial Electronics Society*, vol. 3, DOI 10.1109/OJIES.2022.3209333, pp. 522–536, 2022.

[50] C. D. Fuentes, C. A. Rojas, H. Renaudineau, S. Kouro, M. A. Perez, and T. Meynard, "Experimental validation of a single dc bus cascaded h-bridge multilevel inverter for multistring photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2016.2619661, no. 2, pp. 930–934, 2017.

[51] R. Caceres and I. Barbi, "A boost dc-ac converter: analysis, design, and experimentation," *IEEE Transactions on Power Electronics*, vol. 14, DOI 10.1109/63.737601, no. 1, pp. 134–141, 1999.

[52] Y. P. Siwakoti and F. Blaabjerg, "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems," *IEEE Transactions on Industrial Electronics*, vol. 65, DOI 10.1109/TIE.2017.2740821, no. 3, pp. 2100–2111, 2018.

[53] R. Barzegarkhoo, M. Forouzesh, S. S. Lee, F. Blaabjerg, and Y. P. Siwakoti, "Switched-capacitor multilevel inverters: A comprehensive review," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 11 209–11 243, 2022.

[54] Z. Ye, Y. Lei, Z. Liao, and R. C. N. Pilawa-Podgurski, "Investigation of capacitor voltage balancing in practical implementations of flying capacitor multilevel converters," *IEEE Transactions on Power Electronics*, vol. 37, DOI 10.1109/TPEL.2021.3119409, no. 3, pp. 2921–2935, 2022.

[55] A. Shukla, A. Ghosh, and A. Joshi, "Natural balancing of flying capacitor voltages in multicell inverter under pd carrier-based pwm," *IEEE Transactions on Power Electronics*, vol. 26, DOI 10.1109/TPEL.2010.2089807, no. 6, pp. 1682–1693, 2011.

[56] R. Barzegarkhoo, Y. P. Siwakoti, R. P. Aguilera, M. N. H. Khan, S. S. Lee, and F. Blaabjerg, "A novel dual-mode switched-capacitor five-level inverter with common-ground transformerless concept," *IEEE Transactions on Power Electronics*, vol. 36, DOI 10.1109/TPEL.2021.3074517, no. 12, pp. 13 740–13 753, 2021.

[57] R. Barzegarkhoo, M. Farhangi, S. S. Lee, R. P. Aguilera, M. Liserre, and Y. P. Siwakoti, "New family of dual-mode active neutral point-clamped five-level converters," *IEEE Transactions on Power Electronics*, DOI 10.1109/TPEL.2023.3283694, pp. 1–18, 2023.

[58] K. Wang, L. Xu, Z. Zheng, and Y. Li, "Capacitor voltage balancing of a five-level anpc converter using phase-shifted pwm," *IEEE Transactions on Power Electronics*, vol. 30, DOI 10.1109/TPEL.2014.2320985, no. 3, pp. 1147–1156, 2015.

[59] G. Gateau, T. Meynard, and H. Foch, "Stacked multicell converter (smc): properties and design," in *2001 IEEE 32nd Annual Power*

Electronics Specialists Conference (IEEE Cat. No.01CH37230), vol. 3, DOI 10.1109/PESC.2001.954345, pp. 1583–1588 vol. 3, 2001.

[60] A. Kadam and A. Shukla, "A multilevel transformerless inverter employing ground connection between pv negative terminal and grid neutral point," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2017.2696460, no. 11, pp. 8897–8907, 2017.

[61] F. B. Grigoletto, "Multilevel common-ground transformerless inverter for photovoltaic applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, DOI 10.1109/JESTPE.2020.2979158, no. 1, pp. 831–842, 2021.

[62] Y. P. Siwakoti, A. Palanisamy, A. Mahajan, S. Liese, T. Long, and F. Blaabjerg, "Analysis and design of a novel six-switch five-level active boost neutral point clamped inverter," *IEEE Transactions on Industrial Electronics*, vol. 67, DOI 10.1109/TIE.2019.2957712, no. 12, pp. 10 485–10 496, 2020.

[63] W. Zhang, H. Wang, X. Zhu, H. Wang, X. Deng, and X. Yue, "A three-phase five-level inverter with high dc voltage utilization and self-balancing capacity of floating capacitor," *IEEE Transactions on Power Electronics*, vol. 37, DOI 10.1109/TPEL.2022.3163158, no. 9, pp. 10 609–10 619, 2022.

[64] X. Zhu, H. Wang, W. Zhang, H. Wang, X. Deng, and X. Yue, "A single-phase five-level transformer-less pv inverter for leakage current reduction," *IEEE Transactions on Industrial Electronics*, vol. 69, DOI 10.1109/TIE.2021.3075874, no. 4, pp. 3546–3555, 2022.

[65] H. Vahedi, P.-A. Labbé, and K. Al-Haddad, "Sensor-less five-level packed u-cell (puc5) inverter operating in stand-alone and grid-connected modes," *IEEE Transactions on Industrial Informatics*, vol. 12, DOI 10.1109/TII.2015.2491260, no. 1, pp. 361–370, 2016.

[66] S. S. Lee, C. S. Lim, and K.-B. Lee, "Novel active-neutral-point-clamped inverters with improved voltage-boosting capability," *IEEE Transactions on Power Electronics*, vol. 35, DOI 10.1109/TPEL.2019.2951382, no. 6, pp. 5978–5986, 2020.

[67] S. S. Lee, Y. Yang, Y. P. Siwakoti, and K.-B. Lee, "A novel boost cascaded multilevel inverter," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 9, pp. 8072–8080, 2021.

[68] S. S. Lee, R. J. S. Lim, R. Barzegarkhoo, C. S. Lim, F. B. Grigoletto, and Y. P. Siwakoti, "A family of single-phase single-stage boost inverters," *IEEE Transactions on Industrial Electronics*, vol. 70, DOI 10.1109/TIE.2022.3215827, no. 8, pp. 7955–7964, 2023.

[69] Y. Ye, Y. Zhang, X. Wang, and K.-W. E. Cheng, "Quasi-z-source-fed switched-capacitor multilevel inverters without inrush charging current," *IEEE Transactions on Industrial Electronics*, vol. 70, DOI 10.1109/TIE.2022.3163461, no. 2, pp. 1115–1125, 2023.

[70] C. Silva, J. Rodriguez, and P. Lezana, "Zero steady-state error input current controller for regenerative multilevel converters based on single-phase cells," in *31st Annual Conference of IEEE Industrial Electronics Society, 2005. IECON 2005.*, DOI 10.1109/IECON.2005.1568990, pp. 6 pp.–, 2005.

[71] R. Shi, X. Zhang, D. Kong, N. Deng, and P. Wang, "Dynamic impacts of fast-charging stations for electric vehicles on active distribution networks," in *IEEE PES Innovative Smart Grid Technologies*, DOI 10.1109/ISGT-Asia.2012.6303270, pp. 1–6, 2012.

[72] M. M. Mahfouz and M. R. Iravani, "Grid-integration of battery-enabled dc fast charging station for electric vehicles," *IEEE Transactions on Energy Conversion*, vol. 35, DOI 10.1109/TEC.2019.2945293, no. 1, pp. 375–385, 2020.

[73] T.-W. Huang, H.-J. Chiu, G.-C. Wang, and Y.-C. Chang, "Current-fed phase-shifted full-bridge converter with secondary harmonic current reduction for two-stage inverter in energy storage system," *IEEE Transactions on Power Electronics*, DOI 10.1109/TPEL.2023.3282911, pp. 1–12, 2023.

[74] Y. Bi, C. Wu, J. Xu, H. Li, Y. Wang, G. Shu, and T. B. Soeiro, "An integrated power decoupling method for single-phase ev onboard charger in v2g application," *IEEE Transactions on Power Electronics*, DOI 10.1109/TPEL.2023.3281085, pp. 1–11, 2023.

[75] S. Peyghami, P. Palensky, and F. Blaabjerg, "An overview on the reliability of modern power electronic based power systems," *IEEE Open Journal of Power Electronics*, vol. 1, DOI 10.1109/OJPEL.2020.2973926, pp. 34–50, 2020.

[76] D. Zhou, Y. Wu, F. Gao, E. Breaz, A. Ravey, and A. Miraoui, "Degradation prediction of pem fuel cell stack based on multiphysical aging

model with particle filter approach," *IEEE Transactions on Industry Applications*, vol. 53, DOI 10.1109/TIA.2017.2680406, no. 4, pp. 4041–4052, 2017.

[77] K. Yamazaki and Y. Seto, "Iron loss analysis of interior permanent-magnet synchronous motors-variation of main loss factors due to driving condition," *IEEE Transactions on Industry Applications*, vol. 42, DOI 10.1109/TIA.2006.876080, no. 4, pp. 1045–1052, 2006.

[78] D. Hadiouche, H. Razik, and A. Rezzoug, "On the modeling and design of dual-stator windings to minimize circulating harmonic currents for vsi fed ac machines," *IEEE Transactions on Industry Applications*, vol. 40, DOI 10.1109/TIA.2004.824511, no. 2, pp. 506–515, 2004.

[79] J. Chen, D. Jiang, and X. Zhao, "A comprehensive investigation on conducted emi reduction for variable switching frequency pwm," in *2018 IEEE International Symposium on Electromagnetic Compatibility and 2018 IEEE Asia-Pacific Symposium on Electromagnetic Compatibility (EMC/APEMC)*, DOI 10.1109/ISEMC.2018.8393751, pp. 121–126, 2018.

[80] R. P. Aguilera, P. Acuna, G. Konstantinou, S. Vazquez, and J. I. Leon, "Chapter 2 - basic control principles in power electronics: Analog and digital control design," in *Control of Power Electronic Converters and Systems*, pp. 31–68. Academic Press, 2018.

[81] A. Bahrami and M. Narimani, "A sinusoidal pulsewidth modulation (spwm) technique for capacitor voltage balancing of a nested t-type four-level inverter," *IEEE Transactions on Power Electronics*, vol. 34, DOI 10.1109/TPEL.2018.2846618, no. 2, pp. 1008–1012, 2019.

[82] K. Taniguchi and H. Irie, "Trapezoidal modulating signal for three-phase pwm inverter," *IEEE Transactions on Industrial Electronics*, vol. IE-33, DOI 10.1109/TIE.1986.350216, no. 2, pp. 193–200, 1986.

[83] J. Zhou, S.-c. Shie, and P.-t. Cheng, "A loss redistribution technique for the power devices in the npc converter by pwm zero-sequence injection," *IEEE Transactions on Power Electronics*, vol. 36, DOI 10.1109/TPEL.2020.3035189, no. 6, pp. 7049–7059, 2021.

[84] H. Wang, J. Xu, J. Ye, B. Li, S. Huang, Y. Huang, D. Liu, and A. Shen, "Harmonic spectra analysis of digital spwm in vsi with dc bus ripple and dead-time effects," *IEEE Transactions on Power Electronics*, DOI 10.1109/TPEL.2023.3272381, pp. 1–20, 2023.

[85] P. Sochor and H. Akagi, "Theoretical and experimental comparison between phase-shifted pwm and level-shifted pwm in a modular multilevel sdbc inverter for utility-scale photovoltaic applications," *IEEE Transactions on Industry Applications*, vol. 53, DOI 10.1109/TIA.2017.2704539, no. 5, pp. 4695–4707, 2017.

[86] P. Lezana, R. Aceiton, and C. Silva, "Phase-disposition pwm implementation for a hybrid multicell converter," *IEEE Transactions on Industrial Electronics*, vol. 60, DOI 10.1109/TIE.2012.2228139, no. 5, pp. 1936–1942, 2013.

[87] Y. Li, H. Tian, and Y. W. Li, "Generalized phase-shift pwm for active-neutral-point-clamped multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 67, DOI 10.1109/TIE.2019.2956372, no. 11, pp. 9048–9058, 2020.

[88] S. Rahman, M. Meraj, A. Iqbal, B. P. Reddy, and I. Khan, "A combinational level-shifted and phase-shifted pwm technique for symmetrical power distribution in chb inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, DOI 10.1109/JESTPE.2021.3103610, no. 1, pp. 932–941, 2023.

[89] I. Barbi and F. A. B. Batista, "Space vector modulation for two-level unidirectional pwm rectifiers," *IEEE Transactions on Power Electronics*, vol. 25, DOI 10.1109/TPEL.2009.2025861, no. 1, pp. 178–187, 2010.

[90] A. Gupta and A. Khambadkone, "A space vector pwm scheme for multilevel inverters based on two-level space vector pwm," *IEEE Transactions on Industrial Electronics*, vol. 53, DOI 10.1109/TIE.2006.881989, no. 5, pp. 1631–1639, 2006.

[91] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Transactions on Industrial Electronics*, vol. 63, DOI 10.1109/TIE.2016.2519321, no. 5, pp. 2688–2701, 2016.

[92] O. Lopez, J. Alvarez, A. G. Yepes, F. Baneira, D. Perez-Estevez, F. D. Freijedo, and J. Doval-Gandoy, "Carrier-based pwm equivalent to multilevel multiphase space vector pwm techniques," *IEEE Transactions on Industrial Electronics*, vol. 67, DOI 10.1109/TIE.2019.2934029, no. 7, pp. 5220–5231, 2020.

[93] O. Dordevic, M. Jones, and E. Levi, "A comparison of carrier-based and space vector pwm techniques for three-level five-phase voltage source inverters," *IEEE Transactions on Industrial Informatics*, vol. 9, DOI 10.1109/TII.2012.2220553, no. 2, pp. 609–619, 2013.

[94] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE Transactions on Power Electronics*, vol. 23, DOI 10.1109/TPEL.2007.911865, no. 1, pp. 45–51, 2008.

[95] N. Oikonomou, C. Gutscher, P. Karamanakos, F. D. Kieferndorf, and T. Geyer, "Model predictive pulse pattern control for the five-level active neutral-point-clamped inverter," *IEEE Transactions on Industry Applications*, vol. 49, DOI 10.1109/TIA.2013.2263273, no. 6, pp. 2583–2592, 2013.

[96] A. Birth, T. Geyer, H. d. T. Mouton, and M. Dorfling, "Generalized three-level optimal pulse patterns with lower harmonic distortion," *IEEE Transactions on Power Electronics*, vol. 35, DOI 10.1109/TPEL.2019.2953819, no. 6, pp. 5741–5752, 2020.

[97] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A review of multilevel selective harmonic elimination pwm: Formulations, solving algorithms, implementation and applications," *IEEE Transactions on Power Electronics*, vol. 30, DOI 10.1109/TPEL.2014.2355226, no. 8, pp. 4091–4106, 2015.

[98] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel selective harmonic elimination pwm technique in series-connected voltage inverters," *IEEE Transactions on Industry Applications*, vol. 36, DOI 10.1109/28.821811, no. 1, pp. 160–170, 2000.

[99] J. Napoles, J. I. Leon, R. Portillo, L. G. Franquelo, and M. A. Aguirre, "Selective harmonic mitigation technique for high-power converters," *IEEE Transactions on Industrial Electronics*, vol. 57, DOI 10.1109/TIE.2009.2026759, no. 7, pp. 2315–2323, 2010.

[100] L. G. Franquelo, J. Napoles, R. C. P. Guisado, J. I. Leon, and M. A. Aguirre, "A flexible selective harmonic mitigation technique to meet grid codes in three-level pwm converters," *IEEE Transactions on Industrial Electronics*, vol. 54, DOI 10.1109/TIE.2007.907045, no. 6, pp. 3022–3029, 2007.

[101] G. Goodwin, S. Graebe, and M. Salgado, *Control System Design*. Prentice Hall, 2001.

[102] D. Zmood and D. Holmes, "Stationary frame current regulation of pwm inverters with zero steady-state error," *IEEE Transactions on Power Electronics*, vol. 18, DOI 10.1109/TPEL.2003.810852, no. 3, pp. 814–822, 2003.

[103] Z. Yao, L. Xiao, and Y. Yan, "Dual-buck full-bridge inverter with hysteresis current control," *IEEE Transactions on Industrial Electronics*, vol. 56, DOI 10.1109/TIE.2009.2022072, no. 8, pp. 3153–3160, 2009.

[104] L. Malesani, P. Mattavelli, and P. Tomasin, "Improved constant-frequency hysteresis current control of vsi inverters with simple feedforward bandwidth prediction," *IEEE Transactions on Industry Applications*, vol. 33, DOI 10.1109/28.633796, no. 5, pp. 1194–1202, 1997.

[105] M. Xue, Y. Zhang, Y. Kang, Y. Yi, S. Li, and F. Liu, "Full feedforward of grid voltage for discrete state feedback controlled grid-connected inverter with lcl filter," *IEEE Transactions on Power Electronics*, vol. 27, DOI 10.1109/TPEL.2012.2190524, no. 10, pp. 4234–4247, 2012.

[106] A. Sharma, P. D. Achlerkar, and B. K. Panigrahi, "Assessment of linear quadratic regulator based optimal stabilization of weak-grid-following inverter interface," *IEEE Transactions on Power Delivery*, DOI 10.1109/TPWRD.2023.3283280, pp. 1–13, 2023.

[107] J. Samanes, L. Rosado, E. Gubia, J. Lopez, and M. A. Perez, "Deadbeat voltage control for a grid-forming power converter with lcl filter," *IEEE Transactions on Industry Applications*, vol. 59, DOI 10.1109/TIA.2022.3219040, no. 2, pp. 2473–2482, 2023.

[108] R. P. Aguilera, P. Acuna, Y. Yu, G. Konstantinou, C. D. Townsend, B. Wu, and V. G. Agelidis, "Predictive control of cascaded h-bridge converters under unbalanced power generation," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2016.2605618, no. 1, pp. 4–13, 2017.

[109] R. P. Aguilera, P. Lezana, and D. E. Quevedo, "Finite-control-set model predictive control with improved steady-state performance," *IEEE Transactions on Industrial Informatics*, vol. 9, DOI 10.1109/TII.2012.2211027, no. 2, pp. 658–667, 2013.

[110] M. P. Kazmierkowski, "Advanced and intelligent control in power electronics and drives [book news]," *IEEE Industrial Electronics Magazine*, vol. 8, DOI 10.1109/MIE.2014.2335411, no. 3, pp. 72–72, 2014.

[111] X. Liu, L. Qiu, J. Rodríguez, W. Wu, J. Ma, Z. Peng, D. Wang, and Y. Fang, "Data-driven neural predictors-based robust mpc for power converters," *IEEE Transactions on Power Electronics*, vol. 37, DOI 10.1109/TPEL.2022.3171100, no. 10, pp. 11 650–11 661, 2022.

[112] Y. Chen, D. Xu, and J. Xi, "Common-mode filter design for a transformerless zvs full-bridge inverter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, DOI 10.1109/JESTPE.2015.2503428, no. 2, pp. 405–413, 2016.

[113] "Ieee recommended practice and requirements for harmonic control in electric power systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, DOI 10.1109/IEEESTD.2014.6826459, pp. 1–29, 2014.

[114] H. Xiao, S. Xie, Y. Chen, and R. Huang, "An optimized transformerless photovoltaic grid-connected inverter," *IEEE Transactions on Industrial Electronics*, vol. 58, DOI 10.1109/TIE.2010.2054056, no. 5, pp. 1887–1895, 2011.

[115] G. Lou, Q. Yang, W. Gu, X. Quan, J. M. Guerrero, and S. Li, "Analysis and design of hybrid harmonic suppression scheme for vsg considering nonlinear loads and distorted grid," *IEEE Transactions on Energy Conversion*, vol. 36, DOI 10.1109/TEC.2021.3063607, no. 4, pp. 3096–3107, 2021.

[116] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on Industrial Electronics*, vol. 53, DOI 10.1109/TIE.2006.881997, no. 5, pp. 1398–1409, 2006.

[117] M. K. Mishra and V. N. Lal, "An enhanced control strategy to mitigate grid current harmonics and power ripples of grid-tied pv system without pll under distorted grid voltages," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, DOI 10.1109/JESTPE.2021.3107869, no. 4, pp. 4587–4602, 2022.

[118] S. Silwal, S. Taghizadeh, M. Karimi-Ghartemani, M. J. Hossain, and M. Davari, "An enhanced control system for single-phase inverters interfaced with weak and distorted grids," *IEEE Transactions on Power*

Electronics, vol. 34, DOI 10.1109/TPEL.2019.2909532, no. 12, pp. 12 538–12 551, 2019.

[119] S. K. and B. C. Babu, "A novel adaptive bandpass filter based pll for grid synchronization under distorted grid conditions," *IEEE Transactions on Instrumentation and Measurement*, vol. 71, DOI 10.1109/TIM.2022.3165829, pp. 1–11, 2022.

[120] B. Liu, F. Zhuo, Y. Zhu, H. Yi, and F. Wang, "A three-phase pll algorithm based on signal reforming under distorted grid conditions," *IEEE Transactions on Power Electronics*, vol. 30, DOI 10.1109/TPEL.2014.2366104, no. 9, pp. 5272–5283, 2015.

[121] A. Marquez, J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, E. Freire, and S. Kouro, "Variable-angle phase-shifted pwm for multilevel three-cell cascaded h-bridge converters," *IEEE Transactions on Industrial Electronics*, vol. 64, DOI 10.1109/TIE.2017.2652406, no. 5, pp. 3619–3628, 2017.

[122] A. Marquez, J. I. Leon, V. G. Monopoli, S. Vazquez, M. Liserre, and L. G. Franquelo, "Generalized harmonic control for chb converters with unbalanced cells operation," *IEEE Transactions on Industrial Electronics*, vol. 67, DOI 10.1109/TIE.2019.2956383, no. 11, pp. 9039–9047, 2020.

[123] G. J. Capella, J. Pou, S. Ceballos, G. Konstantinou, J. Zaragoza, and V. G. Agelidis, "Enhanced phase-shifted pwm carrier disposition for interleaved voltage-source inverters," *IEEE Transactions on Power Electronics*, vol. 30, DOI 10.1109/TPEL.2014.2338357, no. 3, pp. 1121–1125, 2015.

[124] V. G. Monopoli, A. Marquez, J. I. Leon, Y. Ko, G. Buticchi, and M. Liserre, "Improved harmonic performance of cascaded h-bridge converters with thermal control," *IEEE Transactions on Industrial Electronics*, vol. 66, DOI 10.1109/TIE.2018.2868304, no. 7, pp. 4982–4991, 2019.

[125] V. G. Monopoli, A. Marquez, J. I. Leon, M. Liserre, G. Buticchi, L. G. Franquelo, and S. Vazquez, "Applications and modulation methods for modular converters enabling unequal cell power sharing: Carrier variable-angle phase-displacement modulation methods," *IEEE Industrial Electronics Magazine*, vol. 16, DOI 10.1109/MIE.2021.3080232, no. 1, pp. 19–30, 2022.

[126] C.-H. Chang and K.-H. Ho, "A transformer-less high-gain inverter with step-up/down and single energy-processing features," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4726–4738, 2021.

[127] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum energy and capacitance requirements for single-phase inverters and rectifiers using a ripple port," *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4690–4698, 2012.

[128] I. Serban, "Power decoupling method for single-phase h-bridge inverters with no additional power electronics," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4805–4813, 2015.

[129] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of active power decoupling topologies in single-phase systems," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4778–4794, 2016.

[130] Z. Qin, Y. Tang, P. C. Loh, and F. Blaabjerg, "Benchmark of ac and dc active power decoupling circuits for second-order harmonic mitigation in kilowatt-scale single-phase inverters," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 15–25, 2016.

[131] Z. Liao and R. C. Pilawa-Podgurski, "A high power density multilevel bipolar active single-phase buffer with full capacitor energy utilization and controlled power harmonics," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 13 067–13 079, 2021.

[132] Z. Liao, N. C. Brooks, and R. C. Pilawa-Podgurski, "Design constraints for series-stacked energy decoupling buffers in single-phase converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7305–7308, 2018.

[133] S. G. Jorge, J. A. Solsona, and C. A. Busada, "Nonlinear control of a two-stage single-phase dc–ac converter," *IEEE Trans. Emerg. Sel. Topics Ind. Electron.*, vol. 3, no. 4, pp. 1038–1045, 2022.

[134] Y. Shen, M. D Antonio, S. Chakraborty, A. Hasnain, and A. Khaligh, "Comparison of ccm- and crm-based boost parallel active power decoupler for pv microinverter," *IEEE Transactions on Power Electronics*, vol. 37, no. 8, pp. 9889–9906, 2022.

[135] J. Jiang, S. Pan, J. Gong, F. Liu, X. Zha, and Y. Zhuang, "A leakage current eliminated and power oscillation suppressed single-phase single-stage nonisolated photovoltaic grid-tied inverter and its improved con-

trol strategy," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6738–6749, 2021.

[136] Y. Xia, J. Roy, and R. Ayyanar, "A capacitance-minimized, doubly grounded transformer less photovoltaic inverter with inherent active-power decoupling," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5188–5201, 2017.

[137] H. F. Ahmed, M. S. El Moursi, B. Zahawi, and K. Al Hosani, "Single-phase photovoltaic inverters with common-ground and wide buck–boost voltage operation," *IEEE Trans. Ind. Informat.*, vol. 17, no. 12, pp. 8275–8287, 2021.

[138] P. Nandi and R. Adda, "An active power decoupling-integrated reduced-switch current-fed switched inverter," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, DOI 10.1109/JESTPE.2022.3214734, pp. 1–1, 2022.

[139] X. Xu, M. Su, Y. Sun, B. Guo, H. Wang, and G. Xu, "Four-switch single-phase common-ground pv inverter with active power decoupling," *IEEE Transactions on Industrial Electronics*, vol. 69, no. 3, pp. 3223–3228, 2022.

[140] H. Tian, M. Chen, G. Liang, and X. Xiao, "A single-phase transformerless common-ground type pv inverter with active power decoupling," *IEEE Transactions on Industrial Electronics*, DOI 10.1109/TIE.2022.3181361, pp. 1–10, 2022.

[141] O. Ellabban and H. Abu-Rub, "Z-source inverter: Topology improvements review," *IEEE Ind. Electron. Mag.*, vol. 10, no. 1, pp. 6–24, 2016.

[142] P. Thounthong, B. Davat, S. Rael, and P. Sethakul, "Fuel cell high-power applications," *IEEE Ind. Electron. Mag.*, vol. 3, no. 1, pp. 32–46, 2009.

[143] D. Meneses, F. Blaabjerg, O. Garcia, and J. A. Cobos, "Review and comparison of step-up transformerless topologies for photovoltaic ac-module application," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2649–2663, 2013.

[144] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, G. E. Town, and S. Yang, "Impedance-source networks for electric power conversion part

ii: Review of control and modulation techniques," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1887–1906, 2015.

[145] A. Abdelhakim, P. Mattavelli, and G. Spiazzi, "Three-phase split-source inverter (ssi): Analysis and modulation," *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7451–7461, 2016.

[146] A. Abdelhakim, P. Mattavelli, P. Davari, and F. Blaabjerg, "Performance evaluation of the single-phase split-source inverter using an alternative dc–ac configuration," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 363–373, 2018.

[147] C. Yin, W. Ding, L. Ming, and P. C. Loh, "Single-stage active split-source inverter with high dc-link voltage utilization," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6699–6711, 2021.

[148] N. Guler and H. Komurcugil, "Energy function based finite control set predictive control strategy for single-phase split source inverters," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2021.

[149] S. S. Lee, A. S. T. Tan, D. Ishak, and R. Mohd-Mokhtar, "Single-phase simplified split-source inverter (s3i) for boost dc–ac power conversion," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 10, pp. 7643–7652, 2019.

[150] M. Chen, Y. Yang, P. C. Loh, and F. Blaabjerg, "A cascaded half-bridge three-level inverter with an inductive dc-link for flexible voltage boosting," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2021.

[151] P. Nandi and R. Adda, "Integration of boost-type active power decoupling topology with single-phase switched boost inverter," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11 965–11 975, 2020.

[152] Y. Tang, W. Yao, P. C. Loh, and F. Blaabjerg, "Highly reliable transformerless photovoltaic inverters with leakage current and pulsating power elimination," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 1016–1026, 2016.

[153] S. S. Lee, C. Shen Lim, Y. P. Siwakoti, and K.-B. Lee, "Single-stage common-ground boost inverter (s2cgbi) for solar photovoltaic systems," in *2019 IEEE Energy Conv. Congr. and Expo. (ECCE)*, pp. 4229–4233, 2019.

[154] X. Hu, P. Ma, B. Gao, and M. Zhang, "An integrated step-up inverter without transformer and leakage current for grid-connected photovoltaic system," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9814–9827, 2019.

[155] R. Barzegarkhoo, S. S. Lee, Y. P. Siwakoti, S. A. Khan, and F. Blaabjerg, "Design, control, and analysis of a novel grid-interfaced switched-boost dual t-type five-level inverter with common-ground concept," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 9, pp. 8193–8206, 2021.

[156] S. S. Lee, Y. Yang, and K.-B. Lee, "A five-level common-ground-t-type inverter for solar photovoltaic applications," in *IECON 2020 46th Annu. Conf. IEEE Ind. Electron. Soc.*, pp. 1160–1164, 2020.

[157] A. Pourfaraj, M. Monfared, and H. Heydari-doostabad, "Single-phase dual-mode interleaved multilevel inverter for pv applications," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 4, pp. 2905–2915, 2020.

[158] S. S. Lee, Y. Yang, and Y. P. Siwakoti, "A novel single-stage five-level common-ground-boost-type active neutral-point-clamped (5l-cgbt-anpc) inverter," *IEEE Transactions on Power Electronics*, vol. 36, no. 6, pp. 6192–6196, 2021.

[159] L. Zhang, X. Ruan, and X. Ren, "Second-harmonic current reduction and dynamic performance improvement in the two-stage inverters: An output impedance perspective," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 394–404, 2015.

[160] R. D. Middlebrook and S. Cuk, "A general unified approach to modelling switching-converter power stages," in *1976 IEEE Power Electronics Specialists Conference*, DOI 10.1109/PESC.1976.7072895, pp. 18–34, 1976.

[161] Y. Xia, J. Roy, and R. Ayyanar, "Optimal variable switching frequency scheme to reduce loss of single-phase grid-connected inverter with unipolar and bipolar pwm," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 1013–1026, 2021.

[162] X. Ding, Y. Hao, K. Li, H. Li, Z. Wei, and W. Wu, "Extensible z-source inverter architecture: Modular construction and analysis," *IEEE Transactions on Power Electronics*, vol. 36, no. 2, pp. 1742–1763, 2021.

[163] V. P. N. Galigekere, "Stead-state and small-signal modeling of power-stage of pwm z-source converter," Ph.D. dissertation, Wright State Univ., 2012.

[164] G. V. Bharath, A. Hota, and V. Agarwal, "A novel 1-ϕ, 5-level transformerless inverter with voltage boosting capability," in *2017 Nat. Power Electronics Conf. (NPEC)*, pp. 370–373, 2017.

[165] A. Hota, V. Sonti, S. Jain, and V. Agarwal, "A novel single-phase switched-capacitor transformer-less 5-level inverter topology with voltage boosting," in *2021 Int. Conf. on Sustainable Energy and Future Electric Transportation (SEFET)*, pp. 1–5, 2021.

[166] C. Rech and W. A. P. Castiblanco, "Five-level switched-capacitor anpc inverter with output voltage boosting capability," *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2022.

[167] S. S. Lee, Y. P. Siwakoti, R. Barzegarkhoo, and K.-B. Lee, "Switched-capacitor-based five-level t-type inverter (sc-5ti) with soft-charging and enhanced dc-link voltage utilization," *IEEE Transactions on Power Electronics*, vol. 36, no. 12, pp. 13 958–13 967, 2021.

[168] R. Barzegarkhoo, M. Farhangi, R. P. Aguilera, Y. P. Siwakoti, and S. S. Lee, "Switched-boost common-ground five-level (sbcg5l) grid-connected inverter with single-stage dynamic voltage boosting concept," in *2021 IEEE Energy Conv. Congr. and Expo. (ECCE)*, pp. 1014–1019, 2021.

[169] P. Lezana, C. A. Silva, J. Rodriguez, and M. A. Perez, "Zero-steady-state-error input-current controller for regenerative multilevel converters based on single-phase cells," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 2, pp. 733–740, 2007.

[170] M. Liserre, R. Teodorescu, and F. Blaabjerg, "Multiple harmonics control for three-phase grid converter systems with the use of pi-res current controller in a rotating frame," *IEEE Transactions on Power Electronics*, vol. 21, DOI 10.1109/TPEL.2006.875566, no. 3, pp. 836–841, 2006.

[171] M. Castilla, J. Miret, J. Matas, L. Garcia de Vicuna, and J. M. Guerrero, "Control design guidelines for single-phase grid-connected photovoltaic inverters with damped resonant harmonic compensators," *IEEE Transactions on Industrial Electronics*, vol. 56, DOI 10.1109/TIE.2009.2017820, no. 11, pp. 4492–4501, 2009.

[172] S. Vazquez, E. Zafra, R. P. Aguilera, T. Geyer, J. I. Leon, and L. G. Franquelo, "Prediction model with harmonic load current components for fcs-mpc of an uninterruptible power supply," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 322–331, 2022.

[173] M. Farhangi, R. Barzegarkhoo, R. P. Aguilera, S. S. Lee, D. D.-C. Lu, and Y. P. Siwakoti, "A single-source single-stage switched-boost multilevel inverter: Operation, topological extensions, and experimental validation," *IEEE Transactions on Power Electronics*, vol. 37, no. 9, pp. 11 258–11 271, 2022.

[174] M. Farhangi, R. Brazegarkhoo, S. S. Lee, D. Lu, and Y. Siwakoti, "An interleaved switched-boost common-ground five-level inverter," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, DOI 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807154, pp. 867–872, 2022.

[175] M. Chen and P. C. Loh, "A dual-boost h-bridge inverter with common ground for photovoltaic interfacing," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 10, pp. 9515–9526, 2021.