A Three-Channel Package-Scale Galvanic Isolation Interface for Wide Bandgap Gate Drivers

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***Abstract*— This article presents the design of a three-channel package-scale galvanic isolation interface for SiC and GaN power switching converters. The isolation interface consists of two side-by-side co-packaged chips fabricated in a low-cost 0.32-μm bipolar CMOS–DMOS (BCD) technology and includes three isolation data channels based on RF-coupled integrated microantennas. The isolation interface provides a channel for the gate driver control, a bidirectional channel for diagnostic, and a channel for the isolated power supply control. They use on–off keying (OOK)-modulated RF carriers of 1.5, 0.5, and 1.5 GHz, respectively. The galvanic isolation interface provides a maximum signal rate of 2 and 1.9 MHz for the driver and the power control channels, respectively, whereas the diagnostic channel guarantees half-duplex bidirectional communication up to 15 MHz. Thanks to the package-scale isolation approach, both reinforced galvanic isolation and first-rate common-mode transient immunity (CMTI) are achieved. High immunity to adjacent channel crosstalk is guaranteed by using channel frequency/physical separation. To best of the authors' knowledge, this is the first implementation of a package-scale galvanic isolation interface with three independent communication channels, including a bidirectional channel, in silicon technology.**

***Index Terms*— Bipolar CMOS–DMOS (BCD), common-mode transient immunity (CMTI), crosstalk, electromagnetic coupling, galvanic isolation rating, on-chip antennas, package, radio frequency.**

I. Introduction

WIDEBAND power devices, such as gallium nitride high-electron mobility transistors (GaN HEMTs) and silicon carbide (SiC) MOSFETs have increased the switching frequency of gate driver applications [1], [2], while the galvanic isolation rating required by both industrial and automotive applications has progressively moved from basic-to-reinforced levels [3]. Higher switching frequencies have produced more stringent specifications in terms of common-mode transient immunity (CMTI), which measures the capability of the isolation device to withstand rapid shifts of grounds. Therefore, standard CMTI values of traditional isolators (i.e., around 100 kV/μs) are not sufficient, and CMTI higher than 200 kV/μs are now required. On the other hand, the reinforced galvanic isolation standard introduced a more demanding performance in terms of maximum surge isolation voltage, V_{SURGE}. This parameter quantifies the capability of the isolator to withstand very high voltage impulses, which can arise from direct or indirect lightning strikes, faults, and short-circuit events or from operative conditions. The reinforced isolation is certified if a single isolation barrier passes the 10-kV surge test [4]. The combination of CMTI higher than 200 kV/μs and V_{SURGE} better 10 kV reveals the severe limitations of traditional chip-scale isolators based on capacitors [5], [6], [7], transformers [8], [9], [10], [11], [12], [13], [14], [15], and *LC* hybrid networks [16]. Indeed, chip-scale galvanic isolators exploit either thick silicon dioxide or polyimide layers as isolation barrier. They present inherent limitations in terms of both isolation rating and CMTI due to the maximum manufacturable dielectric thickness and related parasitic capacitances, respectively. Moreover, special isolation components must be developed to comply with the increasing application needs, thus raising the overall cost of products.

Two series-connected on-chip thick dioxide capacitors are used in [7] to achieve a 12.8-kV surge voltage and a CMTI of 100 kV/μs at a data rate of 100 Mb/s. A double-isolation channel consisting of two series-connected integrated transformers demonstrated an 11-kV_{pk} isolation in [17], but no CMTI performance was reported. A 20-kV_{PK} surge voltage and a CMTI of 200 kV/μs are claimed in [18] along with a current consumption of 2.8 mA at a data rate of 1 Mb/s. However, such performance was achieved by means of a stand-alone isolation transformer exploiting 30-μm-thick polyimide layer in a three-chip package. A record of 650-kV/μs CMTI is claimed in [19] by using on-chip lateral coupling at the cost of an isolation rating as low as 5 kV_{PK}. A back-to-back split-ring resonators coupler built on a 100-μm laminate film was exploited as on-board isolation component in [20], obtaining an isolation rating of 24 kV with a CMTI of 100 kV/μs and a 10-Gb/s data rate. Despite the excellent result, this solution has a very low level of integration, which limits a widespread adoption, especially in those applications in which a small form factor is mandatory. The turning point to maximize both isolation rating and CMTI with a very compact two-chip SiP is the package-scale isolation approach. It uses standard packaging/assembling techniques and RF coupling

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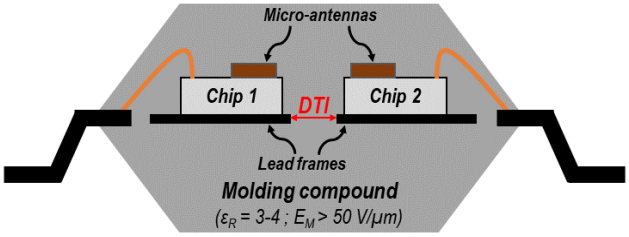


Fig. 1. Package-scale galvanic isolation based on co-planar RF coupling [25].

between microantennas to implement a data communication interface with high isolation rating [21]. The package-scale isolation based on a stacked chip configuration with dielectric isolator film leads to high manufacturing complexity and costs [22], [23], [24]. On the other hand, the side-by-side chip configuration with coplanar antennas shown in Fig. 1 is cost-effective and simple [24], [25]. The communication channel exploits the weak near-field coupling between two microantennas placed on two side-by-side co-packaged dice (i.e., chip TX and chip RX). The distance through insulation (DTI) can be properly set to guarantee the required V_{SURGE}. Since standard molding compounds have a dielectric strength of at least 50 V/μm [26], [27], a DTI of about 300 μm is widely sufficient to guarantee reinforced isolation. Moreover, the parasitic capacitances between dice are very low, thus enabling CMTI to be higher than 200 kV/μs.

Although significant works have demonstrated the feasibility of package-scale isolation based on RF planar coupling, only CMOS implementations on standard low-conductivity substrate (about 10 S/m) have been reported with at most two isolation channels [25], [28]. Recently, a two-channel package-scale isolated interface has been proposed in a 0.5-μm GaN technology on high-resistivity silicon substrate [29]. However, there are further aspects that can contribute to effectively use this approach with silicon technologies in actual applications, such as isolated gate drivers. Indeed, silicon implementations are usually characterized by higher complexity than the GaN ones, since they require multichannel interface with independent communication channels. They are typically developed in standard bipolar-CMOS–DMOS (BCD) technologies on high-conductivity substrate (about 10^3 S/m) [30], [31], [32].

This article presents the very first galvanic isolation interface integrated in a standard BCD technology providing three independent communication channels (i.e., the gate-driver control channel, the diagnostic bidirectional channel, and the gate-driver power supply control channel). Moreover, for the first time, isolated channels based on RF-coupled integrated microantennas are demonstrated on the highly conductive substrate of BCD technology. The proposed galvanic interface, which was developed for wideband gate-driver applications, includes all the features to drive an advanced power converter up to 2-MHz switching frequency. Finally, a novel technique is adopted in the RX front end to implement offset cancellation.

This article is organized as follows. Section II describes the galvanic isolator architecture detailing the implementation of the three isolation channels, while providing the main information on the adopted fabrication technology. Section III is focused on the design of microantennas for the isolation channels. The main circuit blocks are described in Section IV. Experimental results and comparison with the state of the art are discussed in Section V. Finally, the conclusion is drawn in Section VI.

II. Galvanic Isolator Description

An advanced power converter based on high-speed switching devices requires a galvanically isolated interface with independent multiple communication channels to manage different control signals.

1) A pulsewidth modulation (PWM) signal for the gate driver/power switch control (from the low-voltage to the high-voltage domain.
2) Digital signals with bidirectional communication for the power stage diagnostic, which is used in critical environments to prevent failure.
3) A PWM signal for the isolated power supply control (from the high-voltage to the low-voltage domain).

The proposed isolator implements all these functionalities by using only two BCD dice, namely, the controller and driver chip, which can be assembled in a standard plastic package on two properly spaced metal frames. Specifically, to guarantee reinforced isolation (i.e., higher than 10 kV), the DTI was set to 300 μm, assuming a typical molding compound for the package assembly with a dielectric strength of around 50 V/μm. Unfortunately, the implementation of multiple channels using the package-scale isolation approach is hindered by TX-to-RX crosstalk problems. Typically, crosstalk mitigation strategies are frequency separation and/or physical spacing between channels [25], [28].

In this work, a simple but effective layout/frequency arrangement was exploited to allow the integration of three independent channels, as depicted in the simplified photograph shown in Fig. 2. The PWM driver and power supply control channels are placed on the top and bottom, respectively, and both are operated at 1.5 GHz. The bidirectional channel for the self-test diagnostic is instead inserted in the middle and operates at 500 MHz. This allows exploiting a 1-GHz frequency separation between the carriers of adjacent channels that are the main contribution for the crosstalk. The adopted floor plan guarantees sufficiently low crosstalk between isolation channels while saving silicon area, as demonstrated in Section V.

A. Fabrication Technology

The two chips of the galvanic isolator were designed and fabricated in a low-cost 0.32-μm BCD technology by STMicroelectronics [33]. It provides a standard back-end-of-line (BEOL) with three thin Al layers along with a top thick Cu metal. This technology is widely adopted in a large variety of switching power converters for both industrial and automotive applications. Besides CMOS and bipolar transistors, the BCD technology offers double-diffused MOS (DMOS) transistors well suited for the generation of high-voltage RF carriers by means of a class-D oscillator [10], [38]. On the other hand, the highly conductive silicon substrate of the BCD technology

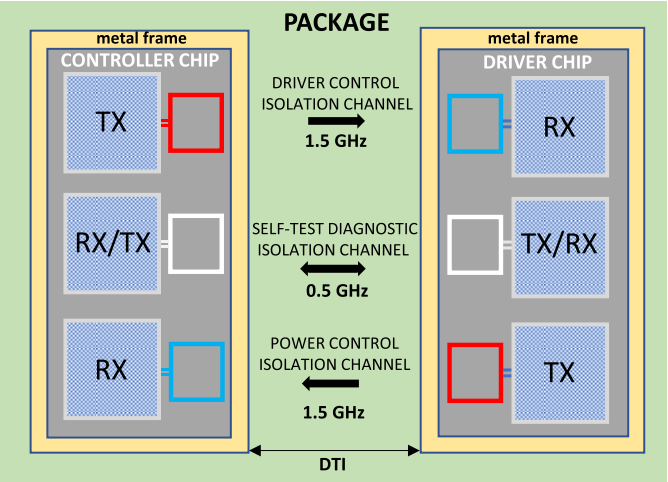


Fig. 2. Simplified photograph of three-channel package-scale galvanic isolator.

is very critical for the electromagnetic (EM) coupling between microantennas, as well as for the microantenna quality factor, due to strong magnetically induced substrate currents [32]. Moreover, due to stringent planarization requirements, metal dummies must be inserted nearby the microantennas, thus further degrading the quality factor.

B. System Architecture

The system architecture of the galvanic isolator is represented in Fig. 3. An on–off keying (OOK)-modulated RF carrier is used to perform a narrowband communication between coplanar microantennas of each isolation channel. Since the channel loss is extremely high due to both large DTI and the conductive substrate of the adopted BCD process, the system is operated in narrowband mode with microantennas resonating at the RF carrier frequency, $f_{RF.}$ The three isolation channels adopt a similar basic architecture. The RF carrier in each channel is provided by a class-D oscillator with a microantenna as tank inductance (i.e., L_{TX} or L_{TRX} shown in Fig. 3), which is properly turned on and off by a digital signal to produce an OOK-modulated RF carrier. On the RX side, a rectifier with a second microantenna (L_{RX} or L_{TRX} shown in Fig. 3) is used for envelope detection of the weak RF signal, which is magnetically induced into the resonant source impedance at the rectifier input. After rectification and filtering, the envelope voltage at the rectifier output is further amplified by the amplifier, G. At this level, an offset compensator is mandatory to compensate for the bias variations due to process tolerances, which can lead to amplifier saturation. Finally, the amplified envelope signal drives a hysteresis comparator to reconstruct the transmitted digital signal. This basic architecture is properly modified to comply with the specifications of each isolation channel, as detailed in Fig. 3. Specifically, the driver and the power control channels are both operated at 1.5 GHz and share the same layout for the transmitter (L_{TX}) and receiver (L_{RX}) microantennas, which exploit a proper turn ratio to stepup the received signal. The driver control channel must comply with very demanding specifications in terms of transmission delay, pulsewidth distortion (PWD), and CMTI, and therefore, no signal coding was adopted. On the other hand, the power control link that has less stringent requirements allows a PWM edge coding to be profitably exploited to reduce power consumption. Specifically, short (i.e., about 60 ns) and long (about 130 ns) pulses are used to code the PWM signal rising and falling edges, respectively, thus reducing the overall time in which the oscillator is on. Therefore, PWM edge coding and decoding blocks are added in the transmitter and receiver chains, respectively, of the power control channel. The adopted edge coding reduces power consumption at the cost of a higher transmission delay.

The proposed isolation interface also integrates a bidirectional channel operated at 0.5 GHz for half-duplex communication. It is implemented by using two equal microantennas (i.e., L_{TRX}), which are switched between the TX and RX front end, both integrated in each of the two chips. In our implementation, a digital signal with a 50% duty cycle (DC) is used for the demonstration of bidirectional communication.

III. Microantenna Design

Main performance parameters of silicon-integrated microantennas are the quality factors, Q_{TX} and Q_{RX}, the magnetic coupling coefficient, k, and especially the TX-to-RX coupling loss, TRX_L, as defined as follows:

$$TRX_L = -20\log_{10}\left|V_{RX}/V_{TX}\right| \quad (1)$$

where V_{TX} and V_{RX} are the voltage at the TX and RX antennas, respectively. Indeed, the design of microantennas for package-scale galvanic isolators is mainly aimed at reducing the isolation channel coupling loss, TRX_L. In a first approximation, the TRX_L minimization is achieved with the maximization of k, Q_{TX}, and the antenna turn ratio, N (i.e., $N = (L_{RX}/L_{TX})^{1/2}$). Unfortunately, an effective antenna design is very challenging due to the high substrate conductivity of the adopted BCD technology and the consequent loss phenomena within the substrate, which degrade both the magnetic coupling and Q-factors, while reducing the antenna self-resonance frequency (SRF). In this work, a rectangular U-shaped differential configuration was adopted for the microantennas, as shown in Fig. 4(a). The differential configuration with the central tap is required by both the TX oscillator and the RX front end for the supply voltage and ground connection, respectively. The U-shaped configuration is a simple but effective solution to increase the EM coupling between antennas since the current flowing in the antenna has a clockwise direction in both single windings. Finally, the rectangular shape allows exploiting longer laterally facing sides of the antennas to improve the magnetic coupling. However, the aspect ratio (AR) (i.e., the ratio of its longer facing side to its shorter side), of a rectangular antenna must be properly set to account for contrasting performance. Indeed, if the AR increases, and hence the EM coupling between antennas thanks to longer facing sides, the coil Q-factor reduces due the higher current crowding into the inner windings [34]. The adopted geometrical parameters are summarized in Fig. 4(b) for each microantenna. A turn ratio,

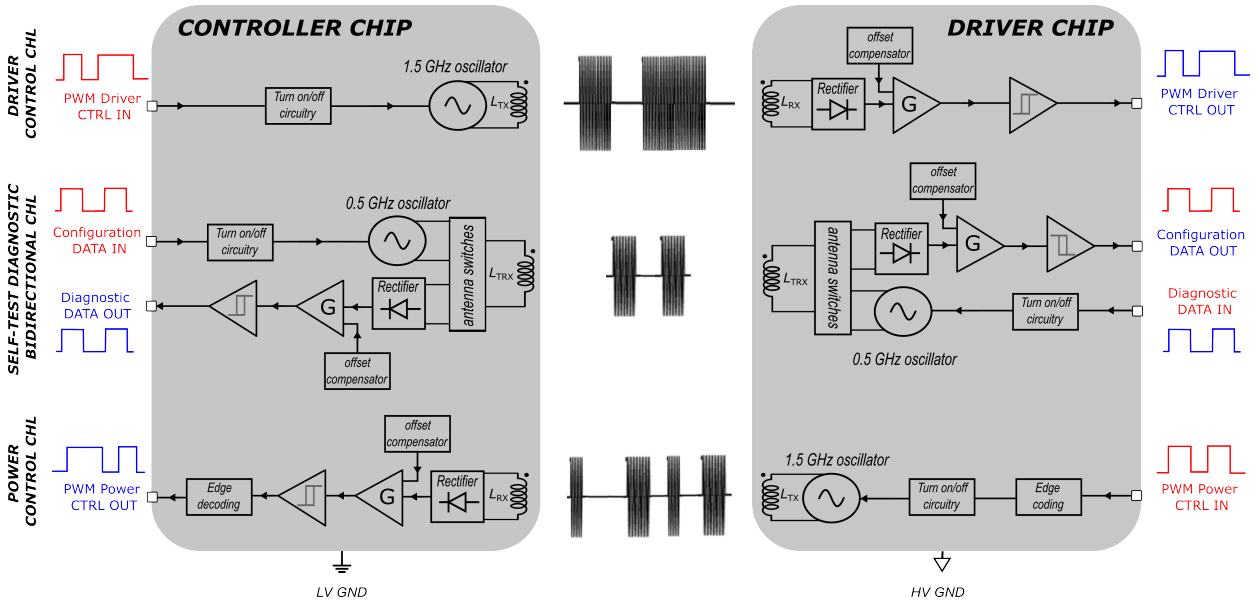
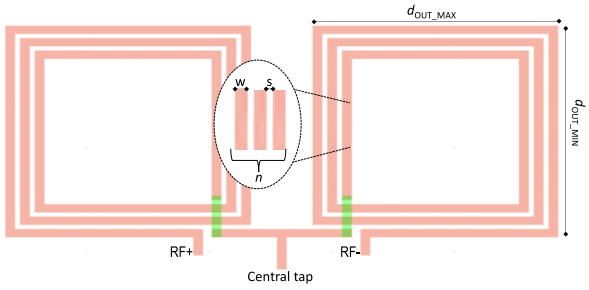


Fig. 3. System architecture of the proposed galvanic isolator.

N, of about 2 was exploited to stepup the RX-induced voltage for both the unidirectional isolation channels (i.e., the driver control channel and the power control). This was accomplished by means of a turn ratio of about 1.75 along with a smaller metal width, w, for the L_{RX} antenna, while maintaining the same overall outer size for both L_{TX} and L_{RX} antennas to preserve the magnetic coupling between them. Indeed, using a small metal width along with a high number of turns for the L_{RX} antenna allows achieving a high value of inductance-to-area ratio and hence a high value of SRF. On the other hand, the degradation of the Q_{RX}, and hence of the equivalent parallel loss resistance, due to a small w does not appreciably affect the induced voltage at the RX antenna, thanks to the high input impedance of the RX (i.e., the rectifier input impedance in Fig. 3). An AR of about 1.3 was adopted for both L_{TX} and L_{RX}, as a trade-off between the RF coupling and the Q-factors. As far as the bidirectional channel is concerned, the same antenna layout must be used in both chips and thus no step-up ratio can be exploited. The value of inductance L_{TRX} was selected as the best trade-off between the oscillator and the rectifier requirements, and it was obtained by properly setting main geometrical parameters (i.e., n, w, and s), while external sizes and AR are kept almost the same of L_{TX}/L_{RX} microantennas.

A key fabrication issue is the placing of fill dummy cells to comply with metal density rules and guarantee physical IC integrity and reliability. Although a predictive model for CMOS inductors with dummy metal filling was presented in [35], no analytical study is available in the BCD technology. Therefore, EM simulations were carried out to set the distance of dummies from the antennas for the best trade-off between loss effects and density rules. The photograph of the fabricated antennas is shown in Fig. 5. Metal dummies were placed both inside and outside the coils at 60 μm. Table I reports the main performance parameters for the three microantennas, L_{TX}, L_{RX}, and L_{TRX} drawn from on-wafer



(a)

Channel	Antenna	*n*	*w* [µm]	*s* [µm]	d_{OUT_MAX} [µm]	d_{OUT_MIN} [µm]	*AR*
Driver / power control	L_{TX}	4	10	2	317	244	1.3
	L_{RX}	7	2.5	2.5	317	244	1.3
Bidirectional data	L_{TRX}	8	7	1.8	324	257	1.3

(b)

Fig. 4. Differential U-shaped rectangular microantenna. (a) Layout. (b) Geometrical parameters for the three antennas, L_{TX}, L_{RX}, and L_{TRX}.

TABLE I
MEASURED PERFORMANCE PARAMETERS OF THE MICROANTENNAS

Parameters	L_{TX}	L_{RX}	L_{TRX}	Units
Operative frequency, f_{RF}	1.5	1.5	0.5	GHz
Low-frequency inductance	12	44	40	nH
Inductance @ f_{RF}	12	62	43	nH
Q-factor @ f_{RF}	7	4	6	-
Self-resonance frequency, *SRF*	4.3	2.6	1.9	GHz

S-parameter measurements by using a five-step de-embedding procedure [36]. Additional details about microantenna design for a package-scale galvanic isolation interface can be found in [37].

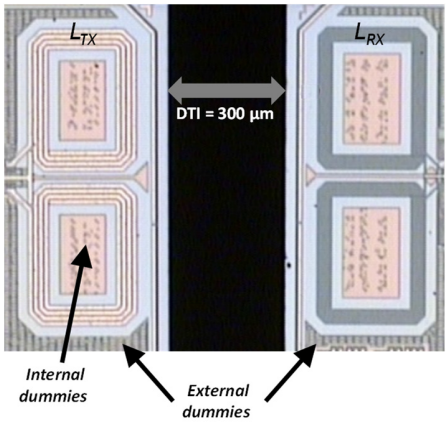


Fig. 5. Photograph of microantennas L_{TX} and L_{RX} with metal dummies.

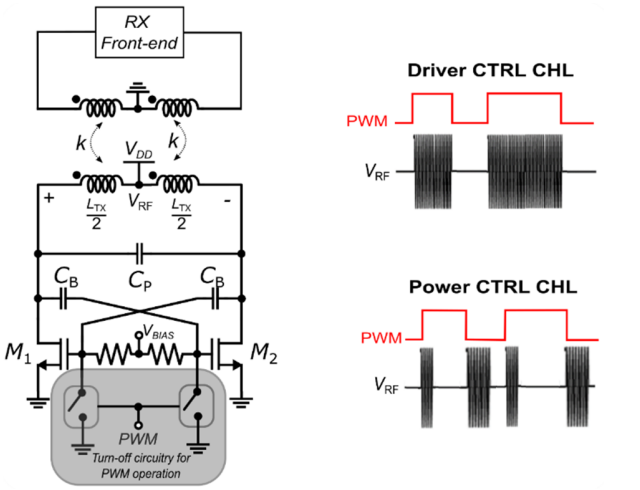


Fig. 6. Class-D oscillator for unidirectional isolation channels and OOK modulation w/o edge coding.

IV. Circuit Block Design

In this Section, the most important circuit topologies of the proposed galvanic isolation interface are discussed along with the main design issues. According to the system architecture shown in Fig. 3, they are the main building blocks of the 1.5-GHz unidirectional isolation channels and the 0.5-GHz half-duplex bidirectional isolation channel for self-test and diagnostic.

A. RF Oscillator for Unidirectional Isolation Channels

The design of an RF oscillator for a package-scale isolator is very challenging due to stringent specifications in terms of turn on/off delay (T_{on}, T_{off}), PWD, and current consumption. Thanks to the availability of DMOS transistors with a breakdown voltage higher than 7 V in the adopted BCD technology, the class-D oscillator in Fig. 6 was adopted, which guarantees a high oscillation amplitude. Indeed, considering a supply voltage, V_{DD}, of 3 V, the class-D topology boosts the oscillation voltage above two times V_{DD}, [10] and [38] provided that the technology maximum safe drain-gate voltage, $V_{DG-MAX,}$ is high enough. Since the maximum allowable gate–source voltage, V_{GS_MAX}, is smaller than V_{DG_MAX}, the coupling capacitors, C_B, are also exploited to perform a voltage partition with the gate–source capacitances of $M_{1,2}$, thus properly limiting the gate peak voltage of the transistor pair and preventing gate oxide breakdown. The oscillator core parasitic capacitances are highly nonlinear and hence very difficult to be accurately modeled [39], due to a signal variation of several volts. Therefore, the oscillation frequency was set to 1.5 GHz, since this value allows a resonator capacitator, C_P, that is much higher than the parasitic capacitances, thus guaranteeing a better accuracy between expected and simulated oscillation frequencies. Moreover, the impact of process–voltage–temperature (PVT) variations was evaluated with Monte Carlo simulations. The oscillation frequency of 1.5 GHz is also a good trade-off between the contrasting performance of the oscillator active core and the *LC* tank. A final consideration is about the layout of the TX antenna, L_{TX}, which must be symmetric to guarantee a central tap connection for the supply voltage, V_{DD}, as provided by the configuration in Fig. 4(a). On/off circuitry was also included, which is driven by the control terminal PWM and allows the cross-coupled pair to be on/off switched. This terminal is used to feed the PWM signal. According to Fig. 3, the driver control channel uses the PWM signal to directly drive the oscillator, whereas a PWM edge coding circuit is adopted to drive the oscillator in the power control channel (see modulation schemes in Fig. 6).

B. RX Front End for Unidirectional Isolation Channels

A simplified schematic of the RX front end is shown in Fig. 7. It adopts a common-source (CS) topology as the rectifier stage, which inherently provides high input impedance along with good voltage gain, and low current consumption [40], [41]. The CS rectifier is ac coupled to the RX microantenna, L_{RX}, to allow central tap grounding to be achieved, which is essential to provide a low-impedance path for the common-mode transient currents and thus improving CMTI [11], [12]. By setting the transistor aspect ratio of the bias branch, M_3, equal to the ones of $M_{1,2}$, and using the same resistances, R_L, the input bias voltages of the amplifier, G, have equal nominal values. Therefore, the envelope signal of the PWM-modulated RF carrier at the output of the rectifier can be amplified and provided to the hysteresis comparator to recover the PWM signal. The amplifier gain was set to 10.

The correct operation of the RX front end depends on the accurate setting of the quiescent voltage at the input of the comparator, which is highly sensitive to the offset voltage at the amplifier input. Unfortunately, typical mismatches between transistors $M_{1,2}$ and M_3 and resistances R_L, even with an accurate layout, give rise to an offset voltage at the amplifier input, which cannot be accepted. Therefore, to guarantee robustness to process tolerances without postfabrication trimming (e.g., efuse), a novel digital self-calibration technique for automatic offset cancellation [42] is here adopted, as shown in Fig. 8. Resistance R_L is split into two resistor strings, R_A and R_B, with $N + 1$ elements and a dominant resistance, R_L^*. The compensation strings, R_A and R_B, and R_L^* are replicated in the rectifier load to reduce the systematic offset.

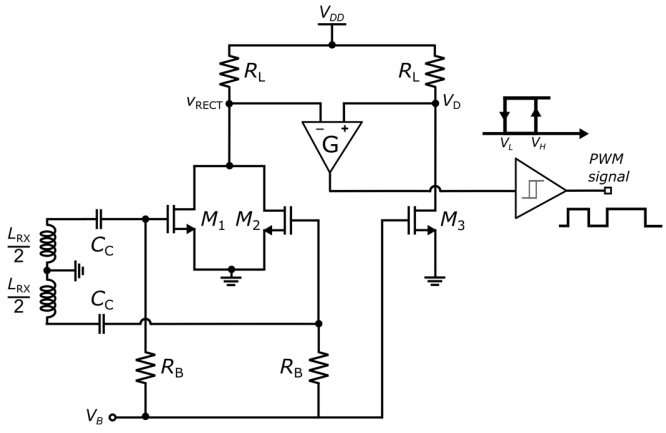


Fig. 7. Simplified schematic of the RX front end for the 1.5-GHz unidirectional isolation channels.

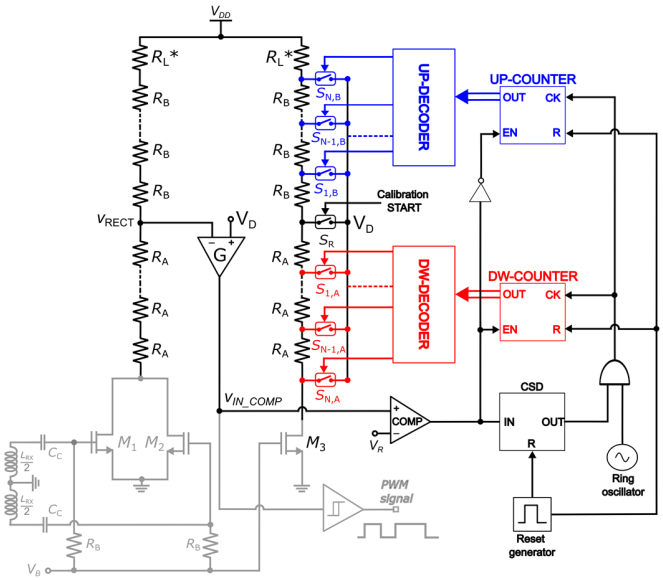


Fig. 8. Simplified schematic of the RX front end with offset cancellation.

The offset maximum variation at the amplifier input was estimated by means of statistical simulations to be about ±300 mV. Therefore, a residual input offset of about ±20 mV at the amplifier input is achieved by setting N equal to 16 (i.e., 4 bits of resolution), which means an offset of around 200 mV at the amplifier output (i.e., the comparator input). This residual offset can well be tolerated provided that proper threshold voltages are used in the hysteresis comparator. The calibration procedure starts at the end of a short reset pulse. At the beginning, switch S_R is closed, and the other switches, S_A and S_B, are open. The comparator detects the offset sign and enables the down counter or up counter depending on whether its value is positive or negative, respectively. The status of the comparator output is stored in the comparator switching detector (CSD) that stops calibration when a sign change is detected. A ring oscillator provides the clock. Assuming a positive offset voltage at the noninverting input of the amplifier, the down counter drives the 4-bit down decoder, which progressively closes switches S_A, starting from $S_{1,A}$, thus reducing V_D. Conversely, if the offset is negative the up counter increases V_D by acting on the 4-bit up decoder, which progressively closes switches S_B, starting from $S_{1,B}$. When the comparator output changes status, the CSD stops calibration by disabling the counter clock. This happens when V_{IN_COMP} is about 200 mV, that is, the nominal value is defined by V_R. Since both counters are driven by a 2-MHz clock signal provided by the ring oscillator, the maximum calibration time is about 8 μs.

C. Bidirectional Half-Duplex Channel Circuits

The proposed galvanic isolation interface provides a bidirectional isolation channel for driver configuration/diagnostic purposes. As already discussed, the channel is operated with a 500-MHz RF carrier and adopts the same antenna, L_{TRX}, in both controller and driver chips. The antenna is shared between the RX and TX front end by means of antenna switches, thus allowing bidirectional half-duplex communication between low-voltage (controller chip) and high-voltage (driver chip) domains, as shown in Fig. 3. This solution was adopted to reduce the overall area of the galvanic isolator and is well suited to the application requirements.

The simplified schematic of the bidirectional half-duplex channel circuitry (included in each chip of the galvanic isolator) is depicted in Fig. 9. The L_{TRX} antenna is switched between the class-D oscillator and the RX input by means of the switches $M_{TX1,2}$ and $M_{RX1,2}$. Offset cancellation was also implemented in the bidirectional channel according to the scheme previously discussed, but it is not reported here for simplicity.

In stand-by conditions, the TX (RX) of the controller chip and the RX (TX) of the driver chip are on (off). Therefore, the enabling signal, EN_{TRX}, in the controller is set high, thus connecting the antenna to the TX oscillator that is turned on/off by the signal, $DATA_{IN}$. The coupling capacitors, C_C, are shorted to ground, and the antenna is being resonated with an equivalent parallel capacitor equal to $C_P + 0.5C_C$. At the same time, EN_{TRX} in the driver chip is set low, and the antenna is ac-coupled to the RX input by means of coupling capacitors C_C, while the TX oscillator is turned off by $\overline{EN_{TRX}}$ that is high. In this condition, the equalization capacitors, C_{C_EQ}, in the driver chip are shorted to ground by transistors $M_{TX1,2}$ to tune the resonant frequency of the LC network at the RX input to the same value of the TX. When a query is sent by the controller to the driver to acquire diagnostic data, a time window is generated in the driver and controller sides during which data communication in the opposite direction (i.e., from the driver to the controller chip) is enabled. This is achieved by setting EN_{TRX} low and high in the controller and driver chips, respectively. After this time window, the diagnostic channel switches in its stand-by condition, i.e., with the controller chip configured as TX and the driver chip as configured RX, ready for another query.

V. Experimental Results

The micrographs of the galvanic isolator chips (i.e., the controller and driver chips) are shown in Fig. 10. The three isolation channels are highlighted along with corresponding

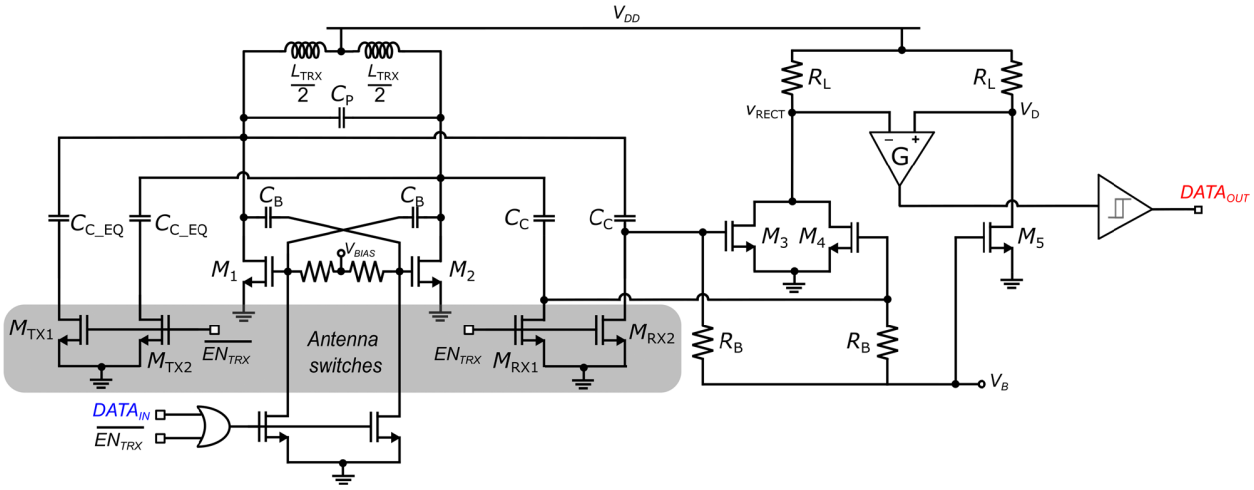


Fig. 9. Simplified schematic of the bidirectional half-duplex channel circuitry.

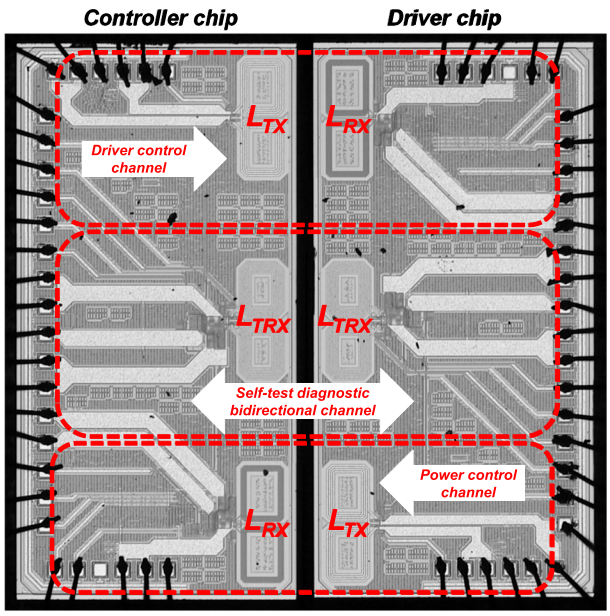


Fig. 10. Micrograph of the galvanic isolation interface chips.

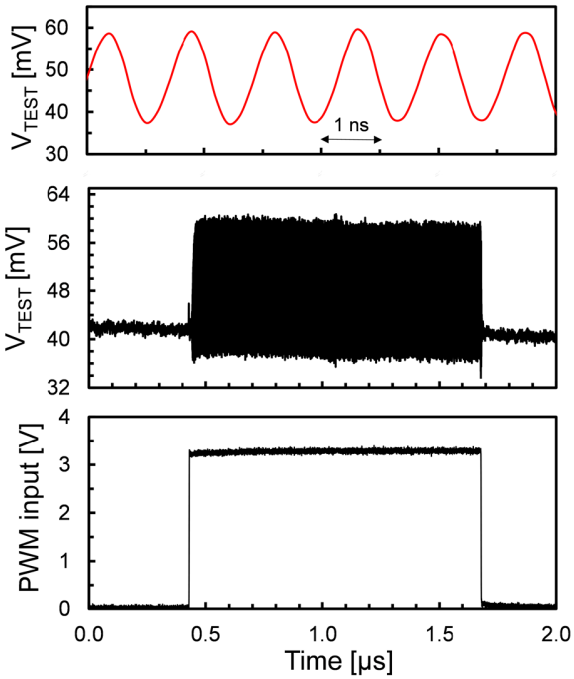


Fig. 11. Single-ended drain voltage of the class-D oscillator used in the driver and power control channels (PWM at 400 kHz and DC = 50%).

microantennas. Each chip has a size of 3.4 × 1.7 mm. Both dice were assembled chip-on-board side-by-side at a 300-μm DTI, with the aim of exhaustively characterizing the three channels. All measurements were performed at the nominal supply voltage of 3 V.

Fig. 11 shows the single-ended drain voltage of the class-D oscillator used in the unidirectional isolation channels (i.e., the driver and power control channels) with a PWM frequency and DC of 400 kHz and 50%, respectively. The drain voltage, V_{TEST}, is attenuated by the integrated circuitry used for the measurement. The oscillation frequency is about 1.4 GHz. The slight deviation from the nominal f_{RF} (i.e., 1.5 GHz) does not significantly affect the functionality of the isolation link. The error can be ascribed to the highly nonlinear parasitic capacitance of the oscillator that is difficult to model accurately. The turn on/off delays, $T_{\text{on}}/T_{\text{off}}$, are about 19 and 5 ns, respectively, and hence, the TX pulsewidth distortion, PWD_{TX}, is 14 ns.

At the nominal supply voltage, the differential oscillation amplitude, V_{RF}, is as high as 7 V, and the oscillator average current consumption is about 7.8 mA with a 50% DC.

Similar measurements were carried out for the class-D oscillator used in the bidirectional half-duplex isolation link (i.e., the self-test diagnostic bidirectional channel). The measured oscillation frequency is about 0.5 GHz and closely agrees with the nominal one. T_{on} and T_{off} are about 22 and 6 ns, respectively. At the nominal supply voltage, the differential oscillation amplitude is as high as 7 V, while the average current consumption is about 7 mA with a 50% DC.

The RX exhibits a gain of about 36 dB, thus providing the hysteresis comparator with a rectified voltage as high as 2.3 V. The overall current consumption of the RX is as low as 0.9 mA.

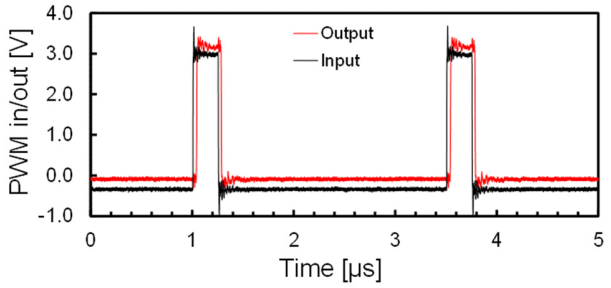


Fig. 12. 400-kHz PWM signals of the driver control channel (DC = 10%).

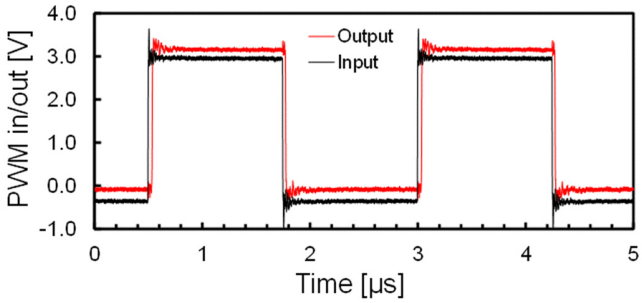


Fig. 13. 400-kHz PWM signals of the driver control channel (DC = 50%).

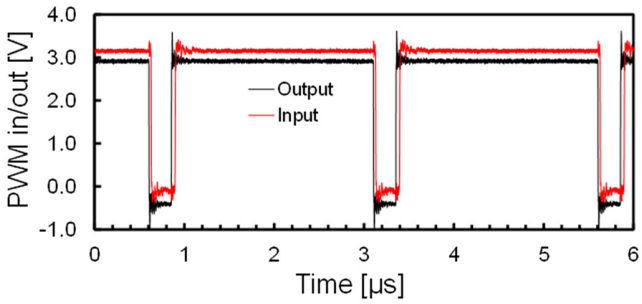


Fig. 14. 400-kHz PWM signals of the driver control channel (DC = 90%).

Figs. 12–14 show the 400-kHz PWM input/output signals of the driver control channel for three DCs (i.e., 10%, 50%, and 90%). The propagation delay is 34 ns and the PWD around 10 ns. Therefore, the PWD of the oscillator (i.e., about 14 ns) is partially compensated by the PWD due to the RX. It is worth mentioning that the overall PWD will be nominally compensated in a second design step by simply delaying the falling edge of the PWM signal of about 10 ns to meet a typical PWD requirement that is around 5 ns.

The overall current consumption of the driver control channel is 15.4, 8.6, and 1.7 mA for DC of 90%, 50%, and 10%, respectively. The channel was also tested at higher PWM frequencies and demonstrated full functionality up to 2 MHz.

Fig. 15 shows the PWM input/output signals along with the edge-coded TX oscillator signal of the power control channel with a PWM signal frequency and DC of 200 kHz and 50%, respectively. The channel was also tested at higher PWM frequencies and demonstrated full functionality up to 1.8 MHz. Thanks to the adopted edge coding, the overall current consumption of the power control channel for a 400-kHz PWM signal is as low as 2.8 mA and is almost constant with the DC value. The edge coding introduces a delay of about

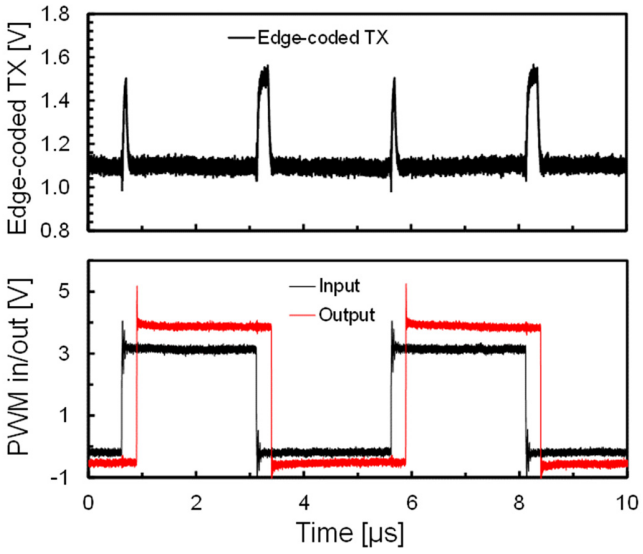


Fig. 15. 200-kHz PWM signals of the power control channel (DC = 50%).

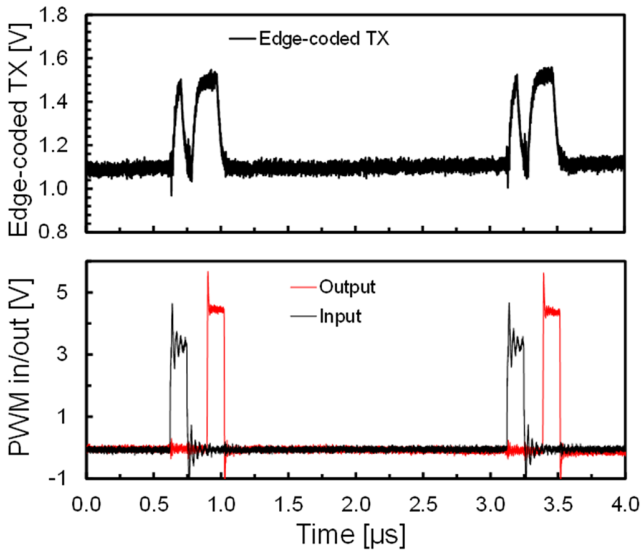


Fig. 16. 400-kHz PWM signals of the power control channel (DC = 5%).

250 ns in the PWM signal transmission that does not impact the power control channel frequency stability since the power control loop is characterized by a low bandwidth. The link demonstrated functionality in a wide DC range from 5% to 90%, as shown in Figs. 16 and 17.

Fig. 18 depicts the input/output data signals of the bidirectional half-duplex isolation link (i.e., the self-test diagnostic bidirectional channel) with a 15-MHz digital signal. The average current consumption is about 14 mA. It is worth noting that the diagnostic link provides a full symmetric performance in the two directions.

Achieved performance of all isolation channels was measured after starting the digital self-calibration described in Section IV. Fig. 19 shows the differential input of the hysteresis comparator ($V_{IN\_COMP} - V_R$) during the calibration operation. In this integrated sample, the starting value of $V_{IN\_COMP} - V_R$ is about 2 V, whereas the maximum allowable

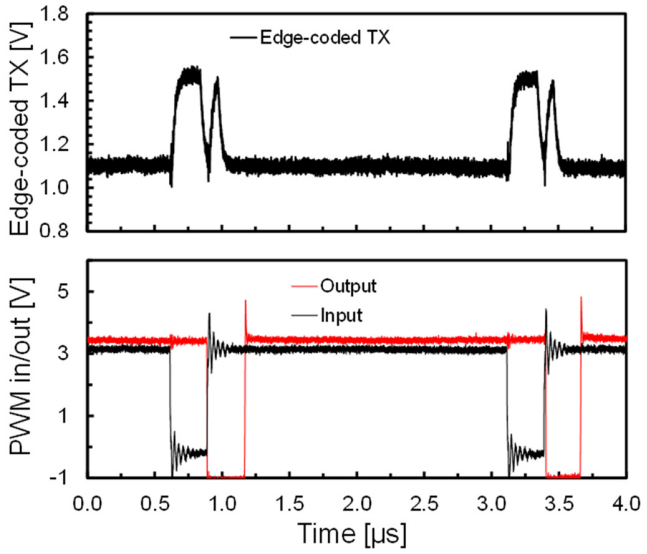


Fig. 17. 400-kHz PWM signals of the power control channel (DC = 90%).

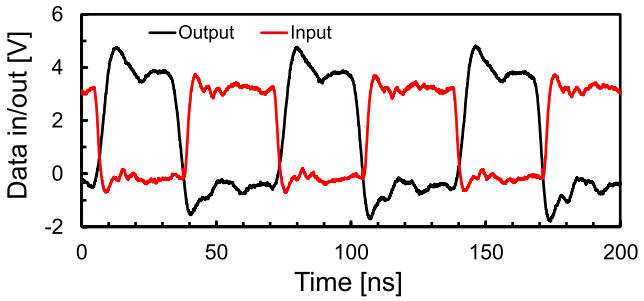


Fig. 18. Data input/output signals of the bidirectional half-duplex link at 15 MHz.

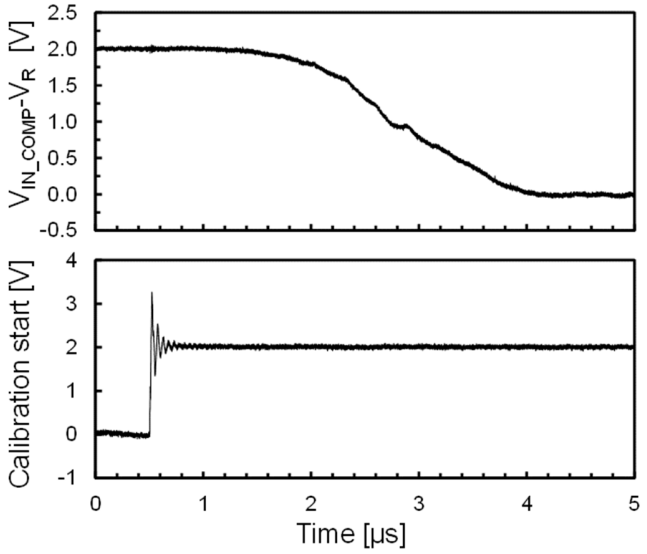


Fig. 19. Offset self-calibration measurements.

offset voltage at the amplifier output is around 200 mV as mentioned before. However, thanks to the self-calibration the offset is almost canceled after about 3.5 μs from the calibration startup.

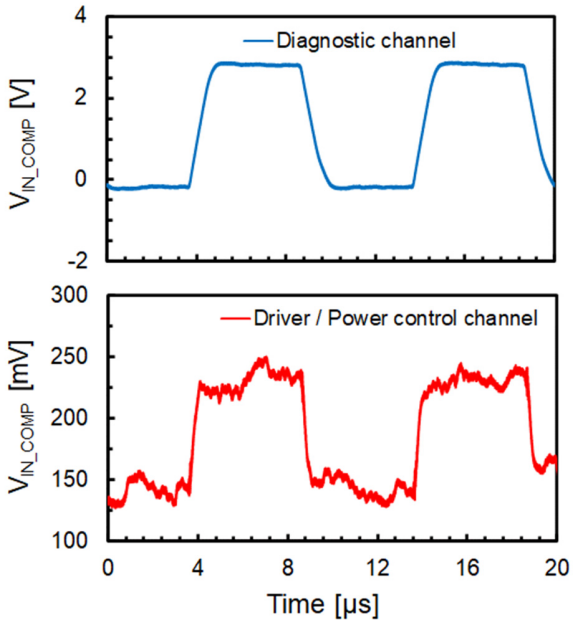


Fig. 20. Immunity to the adjacent channel crosstalk.

Thanks to the adopted layout/frequency configuration of the galvanic isolation interface, excellent immunity to the adjacent channel crosstalk is achieved. This is demonstrated by the measurements in Fig. 20, which shows the input voltage of the hysteresis comparator of the driver/power control channel during the operation of the diagnostic channel (i.e., the disturbing channel). Data transmission in the diagnostic bidirectional channel produces a peak-to-peak crosstalk signal of about 130 mV in the driver/power control channel, which is sufficiently low with respect to the adopted comparator threshold voltages.

The performance of the proposed galvanic isolation interface is summarized and compared with the state-of-the-art in Table II. Both driver and power control channels provide higher PWM rates with respect to the data links in [43] and [44], which are based on traditional inductive and capacitive devices, respectively. Moreover, only [44] guarantees reinforced isolation at the cost of a lower level of integration (i.e., it consists of three dices). The general-purpose isolator in [45] exploits a 3-kV$_{\text{rms}}$ polyimide transformer as an isolation device, which allows a 150-Mbit/s data rate to be achieved, but the CMTI performance is as low as 100 kV/μm. Only package-scale solutions achieve isolation ratings higher than 10 kV/μs thanks to the small capacitive parasitics between the two chips [28], [29]. The work in [28] addressed high-data-rate applications at very poor CMTI, no propagation delay is given, and the silicon area consumption is very high for two isolated links. The isolation interface recently published in [29] was addressed to gate-driver applications and has comparable performance with this work. However, the proposed solution is more complex since it has three isolation links with a bidirectional diagnostic channel, thus including all the features to drive an advanced high-switching frequency power converter. Moreover, the work in [29] benefits from high-voltage GaN transistors and is operated at a higher

TABLE II
SUMMARIZED PERFORMANCE AND COMPARISON WITH THE STATE OF THE ART

Parameters	[42]	[44]	[45]	[28]	[29]	This work
Application	Gate drivers	Gate drivers	General-purpose	n.a.	Gate drivers	Gate drivers
No of isolation channels	2	2	2	2	2	3
Max data/PWM rate	1 MHz	1 MHz	150 Mbit/s	500 Mbit/s	4 / 0.5 MHz[(1)]	2 /1.9 MHz[(1)] 15 MHz[(2)]
Propagation delay [ns]	44	28	13	n.a.	30	34[(3)]
Isolation technology	Polyimide transformers	On-chip SiO_2 capacitors	Polyimide transformers	Package-scale planar	Package-scale planar	Package-scale planar
Isolation level	Basic (5.7 V_{RMS})	Reinforced (8 kV_{PK})	Basic (3 kV_{RMS})	Reinforced (> 10 kV_{PK})	Reinforced (> 10 kV_{PK})[(4)]	Reinforced (> 10 kV_{PK})[(4)]
CMTI [kV/µs]	150	100	100	50	>250[(4)]	>300[(5)]
Supply voltage [V]	5	3 / 5.5	5 V	1.8 V	6	3 V
Technology	n.a.	n.a.	CMOS	0.18-µm CMOS	0.5-µm GaN on Si	0.32-µm BCD
No. of dice	2	3	3	2	2	2
Silicon area [mm^2]	n.a.	n.a.	n.a.	12.8[(6)]	5.8	11.6

[(1)] Driver/power control channels. [(2)] Diagnostic channel. [(3)] Driver control channel.
[(4)] Estimated with package assembly (50-V/µm dielectric strength molding compound and 250-µm DTI).
[(5)] Estimated with package assembly (50-V/µm dielectric strength molding compound and 300-µm DTI). [(6)] From micrographs in [19], [46].

supply voltage. In addition, the high resistivity substrate of the GaN technology in [29] guarantees lower losses for the microantennas and higher EM coupling at the same DTI. The higher silicon area consumption of the proposed interface is due to the presence of three isolation channels, as well as the adoption of higher physical separation to minimize the TX-to-RX crosstalk.

VI. CONCLUSION

A highly integrated galvanic isolation interface based on the package-scale planar isolation approach has been demonstrated. For the first time, a package-scale isolated interface in a BCD technology with a high conductivity substrate has been implemented. It provided three independent channels to comply with the control signals of an advanced power converter. The package-scale isolation approach with microantennas enables both reinforced isolation and high CMTI, thus addressing the stringent requirements of wide bandgap gate drivers. Channel immunity to crosstalk has been guaranteed by using layout/frequency separation.

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