A Lossless Passive Snubber for Soft-Switching of Flyback Converters

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***Abstract*—To improve power density, flyback converters are required to operate at high switching frequencies, resulting in higher power dissipation and lower efficiency. This study aims to reduce the switching power losses of semiconductor switches and voltage spikes at the switch turn-off. A lossless passive snubber consisting of two diodes and an LC circuit is designed to achieve zero-voltage and zero-current switching during the turn-on/turn-off and suppresses the voltage spikes caused by the magnetic energy stored in the transformer leakage inductance. For this, the passive snubber utilizes the discontinuous conduction mode in a single-switch flyback converter. The effectiveness of the proposed design is demonstrated in a designed example of a 15W (15V/1A) step-up DC-DC converter, operating at a switching frequency of 300 kHz.**

***Index Terms*—flyback converter, discontinuous conduction mode, passive snubber, soft switching, zero-current switching, zero-voltage switching.**

I. Introduction

The conversion of DC voltage from one level to another level is obtained by using electronics devices called DC-DC converters. Many applications of DC-DC converters include DC micro grid, hybrid electric vehicles, Uninterruptible Power Supply (UPS), and regenerative braking of DC motors. A flyback converter is one of the most widely accepted isolated DC-DC converters because of its design simplicity, cost-effectiveness, small parts count, and affordability in low-power applications. In practice, the flyback transformer is used as an energy storage device.

The main drawbacks of a traditional flyback converter are high power dissipation and reduced power efficiency due to high switching frequency. Conduction losses increase due to high voltage stress on a switch at the turn-off. When a transistor turns off, a large voltage spike arises due to resonance between the transformer leakage inductance and the transistor's output capacitance. Voltage spikes can be controlled by using the dissipative RCD or non-dissipative LCD clamp circuits [1].

To achieve high performance of flyback converters, some soft switching techniques, such as zero-voltage switching (ZVS) and/or zero-current switching (ZCS), can be applied to the main switch. Both active and passive snubbers are employed for soft switching. The advantage of ZVS/ZCS includes reduced switching and dissipation losses, as well as increased efficiency and life cycle of converter. In general, the control-loop structures of the active snubbers are more complicated due to the number of parts, thereby, making them less cost-effective [2] [3]. The passive snubbers use passive components, i.e., diodes, resistors, inductors, and capacitors. Passive snubbers are less efficient than active ones; they are however more reliable [4]. They offer a simple, robust, and economical way to optimize the switching performance in power devices.

Efficiency can be improved by using zero voltage transition and zero current transition of DC-DC boost converter with PWM [5]. There are two conduction modes for flyback converter, namely the continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The modelling of CCM and DCM in boost converters is presented in [6], while performance of flyback converter with CCM and DCM is described in [7]. The primary-side regulation is commonly used for flyback converters thanks to its lower costs and simple structures.

Primary-side regulation (PSR) active-clamp flyback converter was implemented in [8] using the continuous conduction mode (CCM) with digital control of the constant current output. The influence of parasitic elements in a flyback transformer was considered along with its impact on the input current for DC-DC converters [9]. A comparative study was conducted between bidirectional flyback and split-inductor boost converter topologies in photovoltaic differential power processing systems [10].

Quality characteristics of different passive snubbers, such as RC snubber, RCD snubber, and clamped RCD snubber are compared in [11] for Silicon-Carbide power MOSFET applications. A double-section passive snubber presented in [12] restricts the voltage spikes throughout the main semiconductor switch; however, the interleaved structure suffers from high voltage stresses and spikes. A primary dual pulse-pulse with modulation (PWM) control technique was proposed for CCM flyback with synchronous rectification [13] to bypass the output diode in those carriers to achieve high performance. A soft-switching bidirectional DC-DC converter using a lossless active snubber [14] was proposed to enhance efficiency with ZVS of the main switch. The power loss reduction may however depend on the ratio of energy storing time with respect to the switching period in the case of variations in loading conditions. A digital constant voltage sampling algorithm with adaptive modes switching strategy for both DCM and CCM was introduced in [15] to achieve high accuracy of the constant output voltage of a PSR flyback converter.

Since energy dissipates by the resistor may reduce the output, lossless snubbers are attractive with their design simplicity, and low cost [16]. The Taguchi method was applied in [17] for an optimal design of lossless passive snubber for DC-DC converters, focusing on improved the S/N ratio. Taking this advantage, a lossless passive snubber (LPS) consisting of a capacitor, inductor, and two diodes for an operating in the DCM mode is proposed in this paper to overcome the issues of power losses and voltage spikes in flyback converters.

In this paper, by considering the parasitic capacitance present at the transistor output and transformer leakage inductance, we highlight the performance of the proposed design in achieving soft-switching operations such as ZVS at turn-on and ZCS at turn-off of the switch. Here, the transistor switching losses are reduced with the soft switching technique developed to increase the power conversion efficiency. For a testbed, a single PWM, 15W, 15V/1A, DCM step-up flyback converter is used. The fundamental and design concepts with systematic steps are presented, featuring (i) a detailed design methodology and optimal values of the passive snubber elements, (ii) discussion of switching transients of the transistor, and (iii) analysis of the power loss in the transistor. Significant contributions of this study include:

- ZCS/ZVS operation for the transistor soft switching,
- Effective suppression of voltage surges, and
- Reduction of switching losses.

The remaining of this paper is structured as follows: Section II describes the circuitry of the flyback converter. Section III includes the design of the converter and the LPS in DCM. Simulation results and discussion are included in Section IV. Finally, a conclusion is drawn in Section V.

II. CIRCUITRY AND OPERATION

In this section, we configure the circuitry and analyses the operational principle of the flyback converter.

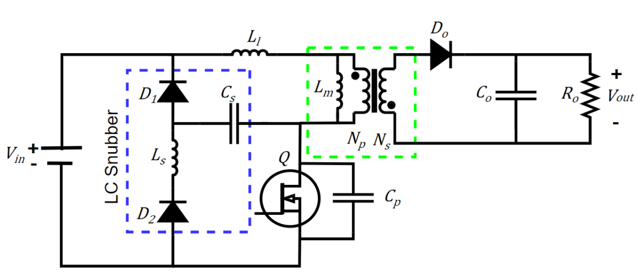

Fig. 1. Lossless passive snubber and flyback converter

Figure 1 shows the flyback converter with the lossless passive snubber, where D_1, D_2, L_s, C_s are respectively the diodes, inductance, and capacitance of the snubber; D_o is the output rectifier diode, C_o is the filter capacitance, R_o is the load resistance, and C_p is the parasitic capacitance. There are two phases of a flyback converter: storage and transfer of energy. During the energy storage phase, while the power diode is reversely biased, the transistor can be treated as a switch connected to a series inductor. The current in the magnetizing inductor of the transformer rises and the energy is stored in it. The current decreases to zero in the energy transfer phase and the accumulated energy is passed to the secondary side. On the other side, the output diode begins to conduct and the current flows.

A. Discontinuous Conduction Mode

In DCM operation of a flyback converter, the current through inductor current (I_{Lm}) falls to zero. There are two stages in a DCM switching period T_{sw}, namely Q_{ON} for switch turn-on and Q_{OFF} for switch turn-off, as described in Fig. 2, where D_{1t}, D_{2t} and D_{3t} are the respective duty cycles for charging, discharging and zero inductor current with respect to the switching period.

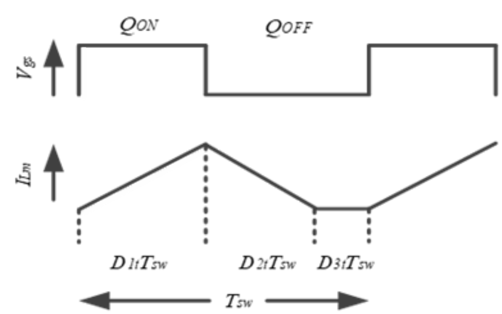

Fig. 2. Basic switching operation in DCM

B. Switch Closed

The closed switch applies a constant input voltage on the transformer magnetizing inductor. The current in the inductor rises linearly, following the equation:

$$V = L_m \frac{dI_{Lm}}{dt}, \quad (1)$$

where L_m is the magnetizing inductance. The power diode D_o blocks the current on the secondary side of the transformer due to polarity. The energy is then stored in the magnetizing inductor.

C. Switch Open

The current on the primary side is interrupted when the switch is opened. The transformer inductance attempts to sustain energy flow by adjusting the polarity on the secondary side. When the diode D_o is conducting, a decreasing linear current is flowing in the secondary side. For every switching cycle, with a peak current $I_{p,pk}$ flowing in the primary side the associated energy transferred to the output through L_m is:

$$E_t = \frac{1}{2} L_m I_{p,pk}^2. \quad (2)$$

The primary peak current is the maximum current flowing through the primary winding of the transformer during each switching cycle. It is determined by the input power, magnetizing inductance, and switching frequency. In a flyback converter, the power transferred via the transformer is equal to the power output plus losses:

$$P_{in} = P_{out} + P_{loss}. \tag{3}$$

The losses mainly consist of switching losses and conduction losses, which are often lumped together as a single term P_{loss}. The energy stored in the inductor per the switching cycle is then:

$$E = P_{in}T_{sw} = \frac{1}{2}L_m I_{p,pk}^2, \tag{4}$$

where $I_{\mathrm{p,pk}}$ is the primary peak current.

D. DCM condition

In a flyback converter, to maintain the DCM operation, the inductor current I_{Lm} must be discharged completely before the next switching cycle starts, as shown in Fig. 2. During the charging phase, energy is stored in the inductor with a charging current given by:

$$I_{charge} = \frac{V_{in}D_{1t}T_{sw}}{L_m}. \tag{5}$$

The inductor then discharges with a current given by:

$$I_{discharge} = \frac{V_{out}(1-D_{1t})T_{sw}}{L_m}. \tag{6}$$

The DCM of the converter requires a certain duration of the zero current period, i.e., $D_{3t} = 1 - D_{1t} - D_{2t} > 0$. So, a good design of a DCM flyback converter should keep D_{1t} as large as possible while satisfying the following condition:

$$D_{1t} + D_{2t} < 1. \tag{7}$$

III. DESIGN METHODOOGY

A brief design process for the flyback converter is described in this section. Table I shows the system design specifications, where f_{sw}=$1/T_{sw}$, V_{in}, and V_{out} are the input and output voltages, P_{in} and P_{out} are input and output powers, respectively.

TABLE I
DESIGN SPECIFICATIONS

Parameter	*Symbol*	Value
Supply voltage	V_{in}	5V
Output voltage	V_{out}	15V
Output current	I_{out}	1A
Output power	P_{out}	15W
Switching frequency	f_{sw}	300kHZ

A. Design of flyback converter

According to the volt-second balance equation, the average voltage across the primary winding over a switching cycle is equal to the average voltage across the secondary winding, referred to the primary side:

$$V_{in}D_{max} = (V_{out} + V_f)'(1 - D_{max}), \tag{8a}$$

where the maximum duty cycle D_{max}=T_{on}/T_{sw} and V_f is the flyback voltage. This expression also provides the relationship between the maximum duty cycle D_{max} and the turns ratio of the flyback converter transformer. When operating in DCM, the transformer turns ratio is:

$$n_{ps} = \frac{N_p}{N_s} = \frac{V_{in}D_{max}}{(V_{out}+V_f)(1-D_{max})}, \tag{8b}$$

where N_p and N_s are respectively the number of primary and secondary turns. This is to ensure the balance between the stored and transferred energy in the transformer during each switching cycle, an essential requirement for the proper operation of the flyback converter in DCM.

At the primary side, the average input power, P_{in}, can be calculated as:

$$P_{in} = V_{in}I_{in,avg}, \tag{9}$$

where, by considering Fig. 2, the average input current $I_{in,avg}$ can be expressed in terms of the peak current I_{pk} and D_{max} as:

$$I_{in,avg} = \frac{1}{T_{sw}}\int_0^{T_{\mathrm{sw}}} I_{\mathrm{lm}}dt = \frac{I_{pk}T_{on}}{2T_{sw}} = \frac{I_{pk}D_{max}}{2}. \tag{10}$$

Therefore, from (9) and (10), the peak current is:

$$I_{pk} = \frac{2P_{in}}{V_{in}D_{max}}, \tag{11}$$

and from the expression (4) for the energy stored in the inductor, we obtain:

$$L_m = \frac{V_{in}^2 D_{max}^2}{2P_{in}f_{sw}}. \tag{12}$$

The magnetizing inductance should ensure the full delivery of the stored energy during each switching cycle. Given the coupling coefficient k, the transformer's leakage inductance, L_l, can be obtained as L_l=$(1-k)L_m$.

At the secondary side, the peak current $I_{s,pk}$ can be calculated from the turn ratio as:

$$I_{s,pk} = I_{p,pk}n_{ps}. \tag{13}$$

The output filter capacitance should be selected such that the time constant R_oC_o with respect to the turn-on time $T_{on} = D_{max}T_{sw}$ is sufficiently large in comparison with the ratio $V_{out}/\Delta V_{out}$, where ΔV_{out} is the output voltage ripple. In other words, the capacitance C_o is chosen therefore:

$$C_o \geq \frac{D_{max}V_{out}}{f_{sw}R_o\Delta V_{out}}. \tag{14}$$

B. Design of Passive Snubber

The snubber capacitor C_s should ensure that the peak voltage of the drain-to-source V_{ds} does not exceed to the limit of the MOSFET transistor breakdown voltage, $V_{ds,\,max}$. From the circuit of the flyback primary side (see Fig. 1) with current I_p, the peak voltage drop across the drain and source can be obtained as

$$V_{in} = n_{ps}(V_{out} + V_f) + I_p\sqrt{\frac{L_l}{C_s}}. \tag{15a}$$

Therefore, given the breakdown voltage across the drain and source $V_{ds,max}$, the snubber capacitor C_s should be chosen to satisfy the following condition:

$$C_s \geq \frac{I_p^2 L_l}{[V_{ds,max} - V_{in} - n_{ps}(V_{out} + V_f)]^2}. \tag{15b}$$

To minimize the influence of resonance, the half cycle of the resonant swinging of the LC circuit should be well completed during T_{on}. By choosing that limit to be $T_{on}/2$, we have

$$T_{on} \geq \pi\sqrt{L_s C_s}. \tag{16a}$$

Therefore, the value of the snubber inductance should be selected subject to the following conditions:

$$L_s \leq \frac{(T_{on}/2)^2}{\pi^2 C_s}. \tag{16b}$$

The maximum reverse voltage across the output diode D_0 can be taken as the maximum voltage at the secondary side:

$$V_{D_0,off} = (V_{out} + V_f) + \frac{V_{in}}{n_{ps}}. \tag{17}$$

At the primary side, the maximum reverse voltage across the snubber diode D_1 and D_2 can be taken in the worst case as equally:

$$V_{D_1,off} = V_{D_2,off} = V_{in} + n_{ps}(V_{out} + V_f). \tag{18}$$

When the MOSFET transistor is off, a leakage current will flow through the total inductor (L_l+L_m) and the lumped capacitor C_p while diode D_1 starts to conduct. At a full reverse voltage of the primary side, the diode D_2 conducts such that the leakage current decays and the lumped capacitor discharges according to the condition that the energy stored in the leakage inductance L_l should be equal or exceed the energy stored in the lumped capacitor C_p [18]. Similarly to (15a), the maximum value $V_{ds,off}$ across the transistor in OFF state, $V_{ds,off}$, can be obtained therefore:

$$V_{ds,off} = V_{in} + n_{ps}(V_{out} + V_f) + I_p\sqrt{\frac{L_l}{C_p}}. \tag{19}$$

C. PWM control

In the proposed design, the PWM pulse is regulated by an ideal controlled voltage source, which controls the pulse of the switch gate. The average output voltage is compared to the corresponding reference value, and the error signal is provided to a PI compensator. The output of the compensator is fed to the voltage source control (VSC). The PI controller allows for maintaining the same voltage at its output irrespective of the loading conditions.

IV. SIMULATION AND DISCUSSION

This section presents simulation results followed by a discussion to show the merits of the proposed LPS and flyback converter, in terms of soft switching and power loss reduction. Table II lists the design parameters of the designed circuit.

A. Transistor ZVS/ZCS

Hard switching occurs due to the overlapping of voltage and current waveforms in a power electronic switch at the instant of turning ON/OFF. The power loss sustains during each switching cycle associated with the overlapped area between voltage and current wave forms. This effect is more prominent at higher switching frequencies. The passive snubber is utilized to achieve soft switching to facilitate zero-crossing of the voltage and current waveforms of the semiconductors.

TABLE II
DESIGN PARAMETERS

Parameter	*Symbol*	Value
Turns ratio	n_{ps}	1/3.795
Magnetizing inductance	L_m	506.2 nH
Leakage inductance	L_l	5.06 nH
Snubber capacitance	C_s	1.38 nF
Snubber inductance	L_s	37.06 µH
Output capacitance	C_o	10 µF

Figure 3 shows the simulated voltage and current waveforms obtained with Matlab Simscape. As can be seen, the DCM-based lossless passive snubber can achieve ZVS operation at turn-on and ZCS at the turn-off the switch. With the benefits of soft switching, the proposed LPS is expected to be useful for applications requiring reduced switching losses, low electromagnetic interference, reduced voltage stress, and better thermal management.

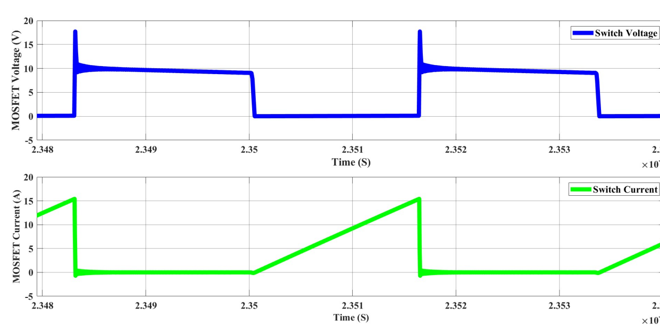

Fig. 3. Transistor ZVS and ZCS

B. Transistor Switching and Power Loss

Figure 4 shows the drain-source voltage during the MOSFET transistor switching. It can be expected that presence of the parasitic components induces unavoidable switching transient. The voltage $V_{ds,off}$ rises from 0 V to about 18 V during the transistor switching off due to a resonance between the leakage inductance L_l and the parasitic capacitance C_p of the transistor. However, this takes a short time of a little fraction of a millisecond owing to a small value of C_p.

It is interesting to note that the proposed design can significantly reduce the transistor power loss. Due to a high input current, there are high power losses, close to 23.56W at the starting point. However, there is almost instantaneously an obvious decrease after that, as shown in Fig. 5.

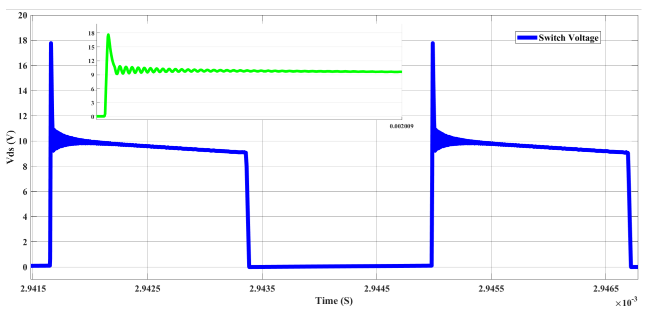

Fig. 4. Transistor switching

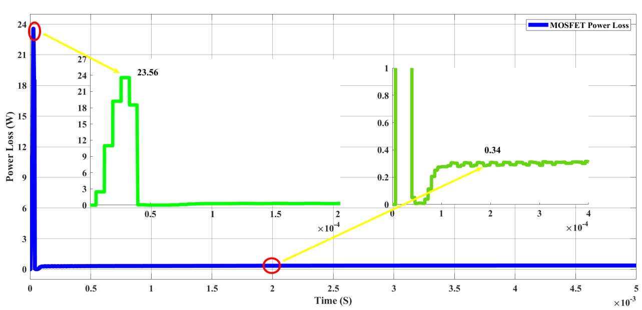

Fig. 5. Power loss of transistor

The steady-state loss is 0.34 W or less (about 2.2% of the power specification) after 0.2 ms, as depicted in the inset therein, when the output voltage and current reach their ultimate final values, which are shown in Figs. 6 and 7, respectively. The simulation results indicate that the output voltage is quickly approaching to 15 V, its target value, after a small time about 0.6 s. So is the output current at the steady state of 1 A. It is quite often that the power supply uses soft-start circuits to lower the inrush currents, but the cost involved may increase and additional time to achieve the required voltage. As such, our design proposed here offers a useful solution to DC-DC conversion as it does not require a start-up circuit and exhibits a short transient period with low power losses.

To compare with another snubber for flyback converters, we consider an RDC snubber employed with a 680-pF snubber capacitor to enhance efficiency recently reported in [19]. To ensure a fair comparison, we adopted identical system specifications therein with the RDC snubber circuitry for the simulation. The switching voltage and switching current are shown in Fig. 8 and power loss across MOSFET in Fig. 9.

The results obtained indicate that the DC-Dc converter with RDC snubber draws larger peaks of the transistor's ZVS current and ZVC voltage at the switching points than with our proposed LPS to supply a steady-state output voltage of 15 V. Moreover, the peak power loss in the transistor is almost 25.76 W and steady-state loss is 0.77W, which are higher than with our proposed snubber. The merits of our proposed snubber can be explained by effectively mitigating transients of the drain-to-source voltage $V_{\rm ds}$, thereby also reducing power losses across the switch. Our future work will be to verify them in experiments with the snubber implementation.

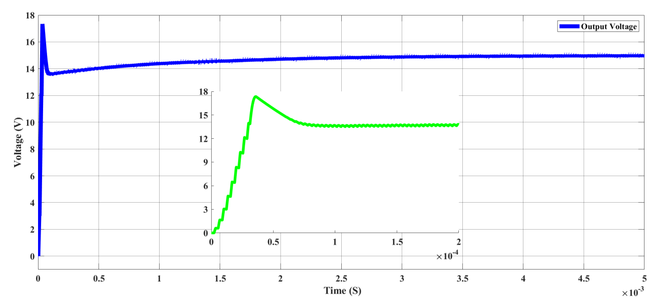

Fig. 6. Output voltage of flyback converter

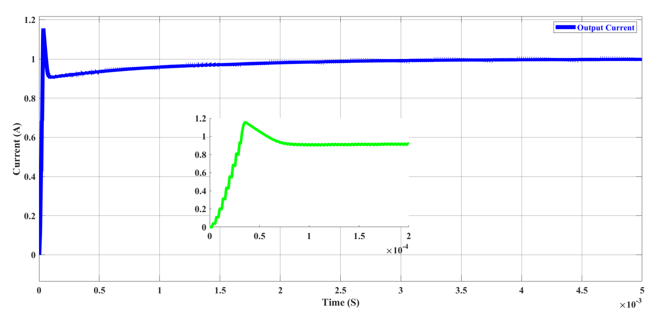

Fig. 7. Output current of flyback converter

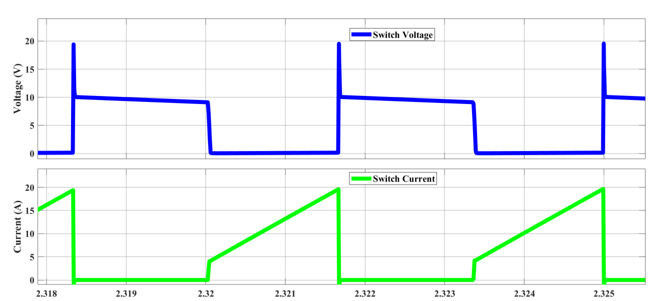

Fig. 8. Transistor ZVS and ZCS for RCD snubber

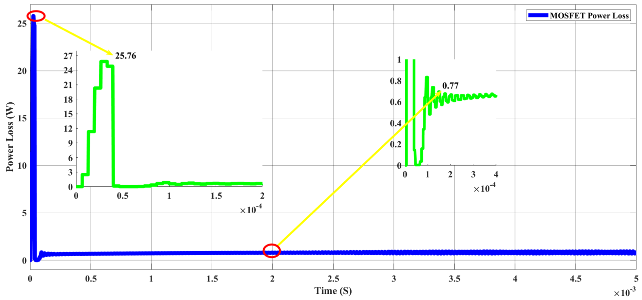

Fig. 9. Power loss of transistor for RCD snubber

V. Conclusions

In this paper, we have presented the design of a lossless passive snubber (LPS) for a single PWM flyback converter operating in the discontinuous conduction mode (DCM) with the aim to minimize the power losses and the voltage spikes during transistor switching. The ZVS/ZCS operation of the transistor has been made possible by using the LPS for the flyback DC/DC converter. The transient merits process, operational principles, and comprehensive analyses of the design have been described in detail. A 15W, 15V/1A, step-up DCM flyback converter including the passive snubber was modelled and simulated to demonstrate the snubber performance and its effectiveness in suppressing the voltage spikes and reducing power losses. A comparison with a recent RCD snubber was also included to show advantages of the proposed approach.

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