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Two-Switch Ultrahigh Step-Up DC–DC Converterer With Low Input Current Ripple and Low Switch Voltage Stress

VAHID ABBASI [1], MOHAMMAD MEHDI KASHANI [1], MILAD REZAIE [1], AND DYLAN DAH-CHUAN LU [2] (Senior Member, IEEE)

[1]Department of Electrical Engineering, Kermanshah University of Technology, Kermanshah 6715685420, Iran
[2]School of Electrical and Data Engineering, Faculty of Engineering and IT, University of Technology Sydney, Sydney, NSW 2007, Australia

CORRESPONDING AUTHOR: VAHID ABBASI (e-mail: V_abbasi@kut.ac.ir).

ABSTRACT Existing high step-up DC-DC converters suffer from various issues, including limited voltage gain, high voltage stress on semiconductors, and high current ripple. To solve these issues, a step-up converter with ultrahigh gain (40x at 50% duty cycle for a turn ratio of 2) composed of two boosting stages, a three-winding coupled inductor, a charge pump and a switched capacitor is presented. The other positive structural properties of the proposed converter are the low current ripple of its input source, the low voltage stress on its switches and most of the diodes, and the existence of a common ground between the input and output sides. The circuit configuration of the proposed converter requires a smaller series inductor due to its ability to achieve the same voltage gain as similar converters with a smaller duty cycle. Additionally, the proposed converter exhibits a low input current ripple, further distinguishing it from similar converters. The coupled inductor is placed in a way to effectively decreases voltage stress on the switches. The converter is compared with the other high step-up converters from different viewpoints demonstrating its superiorities including power density and cost-effectiveness. An experimental prototype, rated at 240 W with 20 V input voltage and 400 V output voltage, is reported to validate the theoretical analysis, performance quality, and dynamic response of the converter.

INDEX TERMS Three windings coupled inductor, two boosting stages, ultrahigh step-up converter, and low input current ripple.

I. INTRODUCTION

Renewable sources such as solar PV and fuel cells generate power with low DC voltages typically and require high voltage conversion for practical applications. Thus, many high-gain step-up DC-DC converters have been reported [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. DC-DC converters can be categorized as isolated or non-isolated. Isolated converters employ high-frequency transformers that can achieve high voltage gain through large turn ratios. However, this approach can introduce specific challenges, such as significant leakage inductance, which can decrease efficiency and increase switch voltage stress. As a result, non-isolated voltage boosting topologies based on the conventional boost converter are commonly utilized to increase the voltage level of renewable energy sources (RES). These topologies offer advantages such as simple design, cost-effectiveness, and absence of isolation. However, they are not suitable for high-power applications due to inherent limitations such as low voltage gains and reverse recovery issues [2], [5], [11]. Certain boosting techniques have been proposed in to address this challenge such as cascading [3], [11], interleaving [12], coupled inductor, switched capacitors and multiplier cells [8], [13], [14]. The cascading method, although well-known and widely used, limits power density and reduces efficiency due to an increase in the number of semiconductors [11]. The interleaving method needs to be combined with other boosting methods to achieve ultrahigh voltage gain [13]. Two other usually used techniques are switched capacitors and multiplier cells [14], [15], [16]. When combined with other techniques, these methods contribute to ultrahigh step-up converters and are typically

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placed close to the output side. They double or triple the voltage gain with minimal additional components, and this is the reason for their acceptance. Coupled inductors (CI) can be integrated with other methods such as switched inductors (SI) to increase voltage gain [2], [8], [13], and [17]. CIs have the advantage of isolating certain parts of the configurations and reducing the number of magnetic cores by twisting multiple coils on a single core [15], [16]. Based on the coupled inductor (CI), these converters can be classified into two categories: two-winding (2WCI) and three-winding (3WCI) configurations. In the proposed converter, three-coil coupled inductors (3WCIs) have increased voltage gain and offered a promising solution. However, using high turn ratios in some converters can increase leakage inductance and conduction loss [18]. Therefore, the correct use of CIs requires appropriate placement in a way to take part in boosting voltage effectively, as is obvious in [9] and the proposed converter. Moreover, the location of CIs affects the voltage stress on semiconductors, which must be considered during converter design. While some converters have shown negative impacts of turns ratios on maximum voltage stress in their diodes [1], [2], [4], [8], [9], and [19], other converters, including the proposed one and those in [1], [8], [9], and [19], demonstrate that increasing the turns ratio of the CI reduces the stress on the switches. The quadratic boost converter (QBC) and the cascaded two boosting stages converters (CBC) can be used due to their high voltage gain, which has a relation with a quadratic function of the duty cycle [12], [19], and [20]. However, the voltage stress on the power switch of the conventional QBC is equal to the output voltage. Recently developed CBCs offer improved features compared to the conventional QBC, including lower voltage stress on the switches. This is achieved by utilizing two switches with distributed voltage stress and appropriate location of them [14]. Due to the other advantages of CBCs and modified QBCs such as continuity of input current and their common grounded structure, they have been used in various studies [21], [22].

This paper presents an ultrahigh voltage gain converter composed of two boosting stages, along with a switched capacitor unified with a three-winding coupled inductor. In addition to the positive structural points of CBCs, the voltage stress on their switches is low, which is the reason of being selected as the base of the proposed converter. The proposed converter has achieved the following outcomes by employing an appropriate number of components while existing converters do not possess all of these advantages simultaneously: 1 high voltage gain 2 Having a continuous input current with low input current ripple 3 Low voltage stress on switches 4 Common ground structure 5 Enhanced power density and reduced cost. A section is provided to validate these achievements through various comparisons with similar high-step-up converters. The paper provides a comprehensive description of the presented structure, operation states of the converter, and its main equations analysis in Sections II, III, and IV, respectively. Moreover, Sections V and VI present a comparison with other high step-up converters and experimental results,

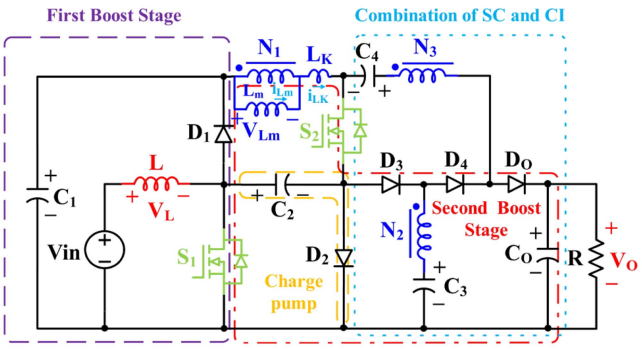

FIGURE 1. Structure of the proposed converter.

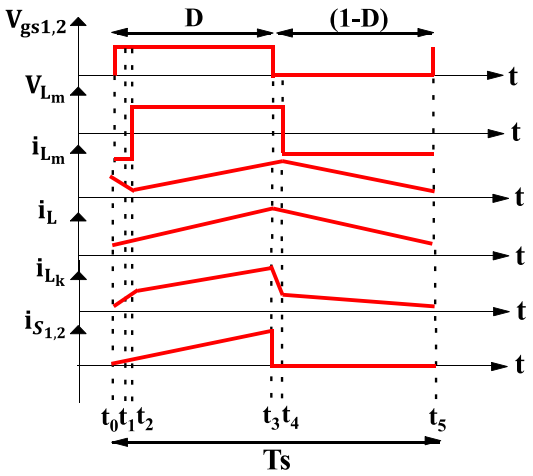

FIGURE 2. Key waveforms of the proposed converter.

highlighting the converter's advantages and its high-quality performance in practical applications.

II. STRUCTURE OF THE PROPOSED CONVERTER

Fig. 1 illustrates different sections of the proposed configuration. The CI's windings are utilized instead of the second boosting stage's inductors and incorporated into the SC unit (Fig. 1). This arrangement enables the achievement of higher voltage gain and reduction of used components. Additionally, the voltage gain of the converter can be regulated at higher levels by the turns ratio of the coupled inductor, providing an additional degree of freedom.

The first boosting stage is composed of L, D_1, S_1 and C_1. The primary coil of the inductor, along with C_1, C_2, S_2, S_1, and D_2, forms the second boosting stage, where C_1 plus C_2 acts as a source during its discharge. The charge pump consists of D_2 and C_2 as shown in Fig. 1. A switched capacitor, consisting of C_3, C_4, D_3, and D_4, is combined with the second and third windings of the CI. Figs. 2 and 3 illustrate the key waveforms and equivalent circuits of the converter for its operation states.

The proposed converter performs power transferring with five operation states during a switching cycle. The two

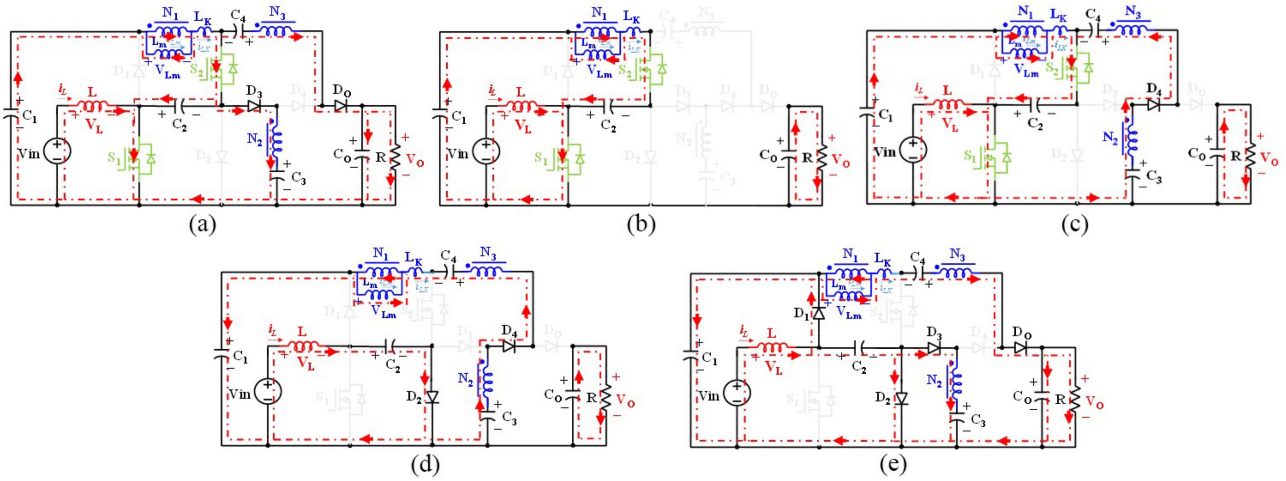

FIGURE 3. Switching states of the proposed converter. (a) First switching state [t_0-t_1]. (b) Second switching state [t_1-t_2]. (c) Third switching state [t_2-t_3]. (d) Fourth switching state[t_3-t_4]. (e) Fifth switching state [t_4-t_5] in CCM.

switches (S_1 and S_2) are used in a way to operate synchronously that needs easy control and distributes voltage stress on them. To analyze the converter, it is assumed that all components except CI are ideal, the capacitances of the capacitors are high and the converter performance occurs in continuous conduction mode (CCM). The magnetic inductance (L_m) and leakage inductance (L_K) of the CI are shown with L_m and L_K in Fig. 1.

III. OPERATION STATES

According to the time divisions of a cycle in Fig. 3, this section provides an explanation of the five states.

State 1 (t_0-t_1): In this state, the switches (S_1 and S_2) are turned on by similar PWM pulses (as shown in Fig. 2). In addition, D_3 and D_O are the only forward-biased diodes. The input source energizes the inductor L through S_1, resulting in a linear increase of the inductor current. As illustrated by the current loops in (Fig. 3(a)), the coupled inductor is charging during this state via C_1 and C_2. Additionally, C_3 is energized through the loop that includes C_1, S_2, D_3, the primary and secondary windings of CI. Moreover, a portion of the discharged power from C_1 and C_4 supplies the load and energizes C_O in the other loop, which consists of D_O, C_1, C_4, and the windings of CI.

State 2 (t_1-t_2): Continuing from the previous state, the switches (S_1 and S_2) remain turned on. In this configuration, there is no conducting diode, and all the diodes are reverse-biased. The inductor L and the primary winding of CI continue to charge similarly to the first state, as shown in (Fig. 3(b)). Additionally, the output capacitor (C_O) supplies the load with its stored energy.

State 3 (t_2-t_3): In this state (Fig. 3(c)), the two power switches (S_1 and S_2) and D_4 are the conducting semiconductors. The status of L and the primary winding of CI remains the same as the previous states, as they continue to receive energy from the input source and C_1. However, in contrast to the first state, C_4 is charged by C_2, C_3, and the windings of CI through the loop that includes D_4, S_1, and S_2. The output capacitor (C_O) supports the load like the second state.

State 4 (t_3-t_4): At the beginning of this state ($t = t_3$), the switches' status is varied from on to off. The conducting diodes are D_2 and D_4, which result in the formation of two current loops (Fig. 3(d)). Unlike the previous states, L discharges its stored energy and charges C_2 in the loop that includes D_2 and the input source. Additionally, C_1 and C_4 are energized by the first winding of CI. Furthermore, C_3 releases its energy in the loop comprising D_4, C_4, C_1, and the windings of CI. Similar to the previous state, C_O continues to supply the output.

State 5 (t_4-t_5): The diodes D_1, D_2, D_3, and D_O are the forward-biased semiconductors in state 5. The inductor L discharges its stored energy into the three current loops including C_1-D_1, C_2-D_2, and C_3-D_3, which causes the charging of the capacitors by L along with the input source. the conduction of D_O establishes a current pathway to supply the load and charge C_O using the input source, C_4, and the two windings of CI.

IV. ANALYSIS OF THE PROPOSED CONVERTER

The third and the fifth states have the most influence on the converter performance due to their higher time intervals during a switching cycle. By considering the assumptions mentioned in the previous section and the equivalent circuits of these two states, the following equations can be derived.

A. VOLTAGE GAIN

Equations (1) to (3) result from the third state (Fig. 3(c)), which can be referred to as the "switch-on" state due to its longer duration compared to the other states, where the switches are turned on.

$$V_{in} = V_L \tag{1}$$

$$V_{Lm} = V_{C1} + V_{C2} \tag{2}$$

$$(n_3 + n_2)\, V_{Lm} = V_{C4} - V_{C2} - V_{C3} \tag{3}$$

Similarly, the fifth state (Fig. 3(e)) can be considered as the "switch-off" state to write (4) to (8).

$$V_L = V_{in} - V_{C1} \tag{4}$$

$$V_{C1} = V_{C2} \tag{5}$$

$$V_L = V_{in} - V_{C2} \tag{6}$$

$$n_2 V_{Lm} = -V_{C3} \;\rightarrow V_{Lm} = \frac{-V_{C3}}{n_2} \tag{7}$$

$$(1 + n_3)\, V_{Lm} = V_{C1} + V_{C4} - V_O \tag{8}$$

By utilizing (1) to (8) and applying the volt-second balance theory of the inductors, the following equations can be formulated:

$$D(V_{in}) + (1 - D)\,(V_{in} - V_{C2}) = 0 \tag{9}$$

$$D(V_{C1} + V_{C2}) + (1 - D)\left(\frac{-V_{C3}}{n_2}\right) = 0 \tag{10}$$

Simplifying (9) gives the voltages of C_1 and C_2 as:

$$V_{C1} = V_{C2} = \frac{V_{in}}{1 - D} \tag{11}$$

From (10) and (11), it can be concluded:

$$V_{C3} = \frac{n_2 2 D V_{in}}{(1 - D)^2} \tag{12}$$

Replacing (11) and (12) into (3), voltage of C_4 is extracted:

$$V_{C4} = \frac{V_{in}\,(1 - D)\,(2n_3 + 1) + 2n_2 V_{in}}{(1 - D)^2} \tag{13}$$

Substituting (13), (11), and (8) into (7), the output voltage and the voltage gain are obtained such as written in (14) and (15).

$$V_O = V_{CO} = \frac{(2 + 2n_2 + 2n_3) V_{in}}{(1 - D)^2} \tag{14}$$

$$M = \frac{V_O}{V_{in}} = \frac{2 + 2n_2 + 2n_3}{(1 - D)^2} \tag{15}$$

According to (15), a quadratic function of the duty cycle $\left(\frac{1}{(1-D)^2}\right)$ appears in the voltage gain equation due to the use of the two boosting stages. Additionally, the combination of the coupled inductor and SC unit has significantly increased the voltage gain by adding incremental coefficients to the numerator of the equation. Assuming that the turns ratio of the CI's windings is equal to one ($n_2 = n_3 = 1$), the numerator of (15) becomes 6, which is a noteworthy coefficient for the gain of a step-up converter. Based on the results, the converter achieves a voltage boost with a gain of 20 when $n = 1$ and $D = 0.458$, or when $n = 2$ and $D = 0.3$. This voltage gain analysis confirms the converter's ability to achieve extremely high gains at low-duty cycles.

B. VOLTAGE STRESS OF THE COMPONENTS

The selection of appropriate components is dependent on the evaluation of voltage stress. One advantageous aspect is the inverse relationship between the stress on switches and the turns ratio of the coupled inductor (CI). The voltage stress on capacitors can be determined by substituting (15) into (11), (12), (13), and (14). This makes the possibility of the voltage stress calculation for all capacitors. Furthermore, the voltage stress of the semiconductors is determined by their turn-off state. Using Fig. 3 and equations of Section IV, the voltage stress of the components related to V_O can be extracted as (16) to (22).

$$V_{S1} = V_{C2} = \frac{(1 - D)\, V_O}{2 + 2n_2 + 2n_3} \tag{16}$$

$$V_{S2} = \frac{(2D\,(n_3 - n_2) + (1 + D))V_O}{2 + 2n_2 + 2n_3} \tag{17}$$

$$V_{D1} = V_{C1} = \frac{V_{in}}{1 - D} = \frac{(1 - D)\, V_O}{2 + 2n_2 + 2n_3} \tag{18}$$

$$V_{D2} = V_{C2} = \frac{V_{in}}{1 - D} = \frac{(1 - D)\, V_O}{2 + 2n_2 + 2n_3} \tag{19}$$

$$V_{D3} = V_{C4} - 2V_{C2} = \frac{((2n_3 - 1)\,(1 - D) + 2n_2)V_O}{2 + 2n_2 + 2n_3} \tag{20}$$

$$V_{D4} = V_O = \frac{(2n_3 + 2n_2 + 1)V_{in}}{(1 - D)^2} \tag{21}$$

$$V_{DO} = V_O - V_{C3} - V_{Lm2} = V_O - V_{C3} - 2V_{C1} = \frac{((2n_2)\,(1 - D)) + 2n_3 + 2D)V_O}{2 + 2n_2 + 2n_3} \tag{22}$$

C. DESIGN CONSIDERATION OF COMPONENTS

There are two main approaches for designing inductors in DC-DC converters. The first approach is regulating the inductance to limit the current ripples on specific values to achieve higher quality, and the second one is to ensure minimum inductance to enable CCM operation. The suggested converter is compared to other converters using the minimum inductance approach, and the first method is chosen for designing and constructing the converter in the experimental setting. The following formula demonstrates the minimum inductance of the inductors in the worst condition guarantees operation in CCM. Hence, equations of L_{min} for the inductors are extracted in from the converter analysis as (23) to (24).

$$L_{\min} \geq \frac{d(1 - d)^4}{72f} R \tag{23}$$

$$L_{N-\min} \geq \frac{d^2(1 - d)^2}{6f\,(1 + d)} R \tag{24}$$

The components are designed for the nominal operation point with properties as: $V_{in} = 20$ V, $I_{in} = 12.5$ A, $P_O = 240$ W, $V_O = 400$ V, $n = 1$, $R_O = 670\ \Omega$, $d_1 = d_2 = d = 0.458$, and $f = 50$ kHz. As described, the minimum inductance can be checked for the worst condition and CCM in different

modes. The L_{min} of the inductors for the nominal point and desired output power range as 50 W$\leq P_O \leq$ 200 W should be $L_{min} \geq 20\,\mu H$ and $L_{m-min} \geq 140\,\mu H$ (the curves of L_{min}s using (23) and (24) are checked to find the required largest inductances for CCM). A 188 μH coupled inductor (L_m) is prepared for the experiments that granites operation in CCM and low current ripple in the nominal condition. The size of the inductor series with the input source (L) has been selected for the prototype in a way to limit the input current ripple at nominal power and output voltage. Using the (25), the results will show that the size of the inductor must be larger than 39 μH to keep current ripple lower or equal to 30% at the nominal power (a 100 μH inductor was chosen during the experiments).

$$L_{Ripple-30\%} \geq \frac{d(1-d)^4}{0.3 \times f \times 36} R \quad \rightarrow \quad L_{Ripple-30\%} \geq 39\,\mu H \tag{25}$$

The capacitors should be designed with considering maximum voltage drop and voltage stress. The following equations are extracted to calculate capacity of C_1, C_2, C_3 , C_4 and C_O.

$$C_1 \geq \frac{(2+d)\,V_O}{(1-\mathrm{d})\,\Delta V_{C1} f_s R} \tag{26}$$

$$C_2 \geq \frac{3V_O}{(1-\mathrm{d})\,\Delta V_{C2} f_s R} \tag{27}$$

$$C_3 \geq \frac{V_O}{\Delta V_{C3} f_s R} \tag{28}$$

$$C_4 \geq \frac{V_O}{\Delta V_{C4} f_s R} \tag{29}$$

$$C_O \geq \frac{dV_O}{\Delta V_{CO} f_s R} \tag{30}$$

Utilizing (26) to (30), the size of the capacitors are calculated for nominal output power, $\frac{\Delta v_C}{v_C} = 0.01$, and V_o = 400 V. Thus, C_1, C_2, C_3, C_4, and C_O must be larger than 35 μF,37 μF, 13 μF, 13 μF and 6 μF. respectively. Due to component limitations, capacitors with higher capacitances respecting lower ESRs (equivalent series resistance) were used in the prototype. Furthermore, the selected capacitors must withstand maximum voltage stress calculable by (11) to (14), which was considered in the design procedure.

Selection of the semiconductors has relations with voltage stress and current stress. Using (16) to (22) for the nominal condition, Maximum voltage stress on S_1, S_2 are 36.9 and 99.2 and for the diodes D_1, D_2, D_3, D_4 and D_O is 36.9, 36.9, 173.06, 408.49, and 272.32 V, respectively. The calculations and datasheets of the selected MOSFET and diodes in Table III can demonstrate the suitability of the used semiconductors in the prototype (Although the selected MOSFET can carry higher currents, the other properties like the lower drain-source resistance, nominal voltage, and quality of the available MOSFET were preferred in the selections). Similar to the procedure used for the switch, the other quality factors like the forward voltage of the diodes and their internal resistance were considered during choosing them.

D. POWER LOSS ANALYSIS

The power loss analysis is performed in this section. The calculations are done for V_{in} = 20 V, I_{in} = 12.5, P_o = 240 W, V_o = 400 V, R_o = 670 Ω, $d_1 = d_2 = d = 0.458$ and f = 50 kHz. The other information like t_{rr}, V_{FD}, Tr, T_f, R_D, R_{DS} are extracted from datasheets of the components. Diodes losses include forward voltage loss (P_{VFD}), reverse recovery loss (P_{rrD}), and conduction loss (P_{rD}). The following equations can be used to calculate these losses.

$$P_{VFD} = \sum_{i=1}^{5} V_{FDi} I_{Di-ave} \tag{31}$$

$$P_{rD} = \sum_{i=1}^{5} r_{Di} I_{Di-RMS}^2 \tag{32}$$

where V_{FD} and r_D are the forward voltage and resistance of the diode, respectively. The diodes' average current, I_{RMS}, and voltage can be extracted from the circuit analysis. Reverse recovery loss (P_{rrD}) is the last part of the diodes losses that can be calculated by (33).

$$P_{rrD} = \sum_{i=1}^{5} V_{Di} \times I_{Diave} \times t_{rr} \times \frac{F_{sw}}{2} \tag{33}$$

F_{SW} and t_{rr} are the switching frequency, and the diodes reverse recovery time. The total loss of the diodes can be calculated by:

$$P_D = P_{VFD} + P_{rD} + P_{rrD} \tag{34}$$

According to the data from the datasheets and the results extracted from the converter analysis, the diodes losses are calculated, and the total loss of the diodes is 5.42W.

The inductor losses include core loss (P_{core}), DC conduction loss (P_{dcL}) and AC conduction loss (P_{acL}) that can be calculated by the equations given in (35) to (38) and the current analysis results.

$$P_L = P_{core} + P_{dcL} + P_{acL} \tag{35}$$

$$P_{core} = \sum_{i=1}^{2} K f^x B^y V_{ei} \tag{36}$$

$$P_{dcL} = \sum_{i=1}^{4} {I_{RMSi}}^2 R_{dci} \tag{37}$$

$$P_{acL} = \sum_{i=1}^{4} {I_{RMSi}}^2 R_{aci} \tag{38}$$

where R_{dci} and R_{aci} are the dc and ac resistances of the inductors, respectively. K, x, y are constant values that depend on the material properties of the core and its type. Using the equations, data of the cores, and current analysis, the total loss of the inductors can be calculated as equal to 4.457 W.

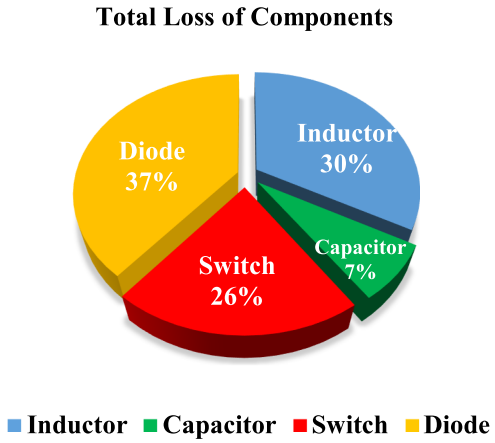

FIGURE 4. Power loss distribution on the components per V_{in} = 20 V, V_o = 400 V, and P_o = 240 W.

The resistance of the capacitors (R_c) causes conduction loss (P_{cap}) and can be calculated by (39).

$$P_{cap} = \sum_{i=1}^{4} R_{Ci} {I_{CiRMS}}^2 \tag{39}$$

Using the data and current analysis, the total loss of the capacitors for the converter is obtained as 0.99W.

The switch imposes conduction loss (P_{con}) and switching loss to the converter. The switching loss is divided into turn on loss (P_{on}) and turn off loss(P_{off}) which can be calculated by (40).

$$P_{on,off-S} = V_{S1} I_{S1} \frac{t_{r1} + t_{f1}}{2} f_{sw} \tag{40}$$

In addition, the conduction loss of the switch can be obtained using (41):

$$P_{con} = (I_{RMS1})^2 R_{DS1} \tag{41}$$

where P_{con}, $P_{on,\,off}$, R_{DS}, f_{sw}, t_r and t_f are conduction loss, switching loss, resistance of MOSFET, switching frequency, rise time, and fall time, respectively. Using datasheets of the switch and the analysis of the converter, the total loss of the switch is 4.14 W.

Based on the above calculations, the component's power loss distribution is shown in Fig. 4. According to the results, the diodes impose the highest percentage of power loss into the converter, especially D_1 and D_2. The power loss of forward voltage in the diodes has impressive values, which can be reduced by replacing the diodes with the more qualified ones. According to the loss distribution percentages, the conduction loss in the switches and the inductors imposes the highest losses and the maximum loss percentage in the diodes belongs to the forward voltage loss. Therefore, utilizing components with higher quality can be more effective than the soft-switching methods.

E. SMALL SIGNAL ANALYSIS

The proposed converter has five capacitors, one inductors, and one coupled inductor (CI). Therefore, the total number of state variables is eight, as shown in below. In addition, the introduced input and output matrixes are visible in (42).

$$X = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \\ x_8 \\ x_9 \end{bmatrix} \Rightarrow \begin{bmatrix} I_L \\ I_{LN1} \\ I_{LN2} \\ I_{LN3} \\ V_{C1} \\ V_{C2} \\ V_{C3} \\ V_{C4} \\ V_{Co} \end{bmatrix}, \quad U = \begin{bmatrix} V_{in} \end{bmatrix}, \; Y = [V_o] \tag{42}$$

According to the perturbation theory, the small signal model of the converter can be obtained. Generally, this model consists of two transfer functions (TFs), namely, G_{vg} (output voltage to input voltage TF), and G_{vd} (output voltage to duty cycle TF). From the perturbation theory and small signal model, state space models of the converter are:

$$\begin{aligned} \frac{d}{dt}\hat{x} &= A\hat{x} + B\hat{u} + ((A_1 - A_2)X + (B_1 - B_2)V_{in})\hat{d} \\ y &= C\hat{x} + D\hat{u} \end{aligned} \tag{43}$$

In which: A = dA$_1$ + (1-d)A$_2$, B = dB$_1$ + (1-d) B$_2$, C = dC$_1$ + (1-d)C$_2$ and D = dD$_1$ + (1-d)D$_2$. where A$_1$, B$_1$, C$_1$ and D$_1$ are the state equation matrices when the converter switches are on for 0<t<DT and, A$_2$, B$_2$, C$_2$ and D$_2$ are those when the converter switches are off for the time period of DT<t<T. In order to find G_{vd}, the perturbation on the input (V_{in}) has to be zero, i.e., $\hat{v}in = 0$ or $G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}\,(s)}\big|_{\hat{v}_{in}=\hat{i}_{load}=0}$ (the input voltage is kept constant), therefore:

$$\begin{aligned} \frac{d}{dt}\hat{x} &= A\hat{x} + ((A_1 - A_2)X + (B_1 - B_2)V_{in})\hat{d} \\ y &= C\hat{X} + \{(C_1 - C_2)X + (D_1 - D_2)U\}\hat{d} \end{aligned} \tag{44}$$

where X and V_{in} are the DC values of the states and the input voltage, respectively. Furthermore, the matrixes $(A_1 - A_2)X + (B_1 - B_2)V_{in}$ and $(C_1 - C_2)X + (D_1 - D_2)U$ can be defined as $B'$and D', respectively. Similarly, in order to find G_{vg}, the perturbation on the duty cycle (d) has to be zero, i.e., $\hat{d} = 0$ or $G_{vg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{in}\,(s)}\big|_{\hat{d}=\hat{i}_{load}=0}$ (the duty is constant), so:

$$\frac{d}{dt}\hat{x} = A\hat{x} + B\hat{u}, \text{ and } y = C\hat{x} + D\hat{u} \tag{45}$$

The final step is to obtain the corresponding TFs from the state equations which is straightforward. A$_1$, B$_1$, C$_1$, A$_2$, B$_2$,

and C_2 can be calculated as:

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_{N1}} & \frac{1}{L_{N1}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_{N2}} & \frac{1}{L_{N2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{L_{N3}} & \frac{1}{L_{N3}} & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_2} & 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_4} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \quad (46)$$

$$B_1 = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C_1 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \text{ and } D_1 = 0 \quad (47)$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & -\frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{N1}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{N2}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{L_{N3}} & 0 & 0 \\ \frac{1}{C_1+C_2} & -\frac{1}{C_1+C_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C_1+C_2} & -\frac{1}{C_1+C_2} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_4} & 0 & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{C_O} & 0 & 0 & 0 & 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix} \quad (48)$$

$$B_2 = \begin{bmatrix} \frac{1}{L} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad C2 = C1 \text{ and } D2 = 0 \quad (49)$$

In the next step the control-to-output ($G_{vd}(s)$) and the line-to-output ($G_{vg}(s)$) transfer functions can be obtained (using $G_{vg} = C(SI - A)^{-1}B + D$, $G_{vd} = C(SI - A)^{-1}B' + D'$ and properties of the converter) (50) and (51) shown at the bottom of this page:

Utilizing bode plots of the calculated TFs, the compensator is designed to regulate phase margin (Pm) in the range of 40 ° to 80 °. The obtained compensator considering the properties is given here:

$$G_c = \frac{50}{s} \times \frac{\left(1 + \frac{s}{550}\right)\left(1 + \frac{s}{400}\right)}{\left(1 + \frac{s}{60000}\right)\left(1 + \frac{s}{75000}\right)} \quad (52)$$

Fig. 5(a) and (b) illustrate bode diagrams of the open loop functions (G_{vg} and G_{vd}) and the closed loop TFs ($T = G_cG_{vd}$ and $G_{vg}/1 + T$). The results indicate suitable effects on T and $G_{vg}/1 + T$ functions based on the Pm values of the closed loop functions set at 65 and 60. Also, the magnitudes of the controlled variables in Fig. 5(a) and (b) depict their appropriate gain margins (Gm). The magnitudes in switching frequency of 50 kHz show suitable values to reduce variations and noises for the case with the controller (they have negative values <-70dB, which decreases the effect of changing parameters). Bode diagrams confirm the stability of the converter, which is verified by the experiments.

V. COMPARISON WITH OTHER CONVERTERS

In this section, quantitative and qualitative comparisons related to the converters' configurations and their performances are provided to verify the merits and drawbacks of the proposed converter. Table I provides detailed information on the factors considered for the compared converters. It should be noted that increasing the voltage conversion ratio generally requires a greater number of components, as seen in high step-up converters. Despite achieving a higher voltage gain, the proposed converter utilizes the same number of components as the converters mentioned in [7], [8], [9], [23], [25]. On the other hand, the converters discussed in [1], [2], [3], [4], [5], [6], [24] have fewer components (along with lower voltage gain), while the converter in [10] has a higher number of components. It is noteworthy that all the compared converters include a coupled inductor (CI), and they can boost voltage with higher gain by either increasing the turns ratio (n) of the coupling inductors or by raising the duty cycle.

To evaluate the voltage-gain of the converters, it is preferable to compare them at an equal turns ratio. Thus, voltage

$$G_{vd} = \frac{\left(1.627e04s^8\right) - \left(1.499e09s^7\right) + \left(1.151e12s^6\right) - \left(9.537e15s^5\right) + \left(2.375e18s^4\right) + \left(1.576e06s^3\right) - \left(6.169e10s^2\right) - (0.02727\ s) + (9.805e-13)}{\left(s^9\right) + \left(3.259e-07s^8\right) + \left(5.263e07s^7\right) + \left(17.15s^6\right) + \left(1.459e14s^5\right) + \left(4.756e07s^4\right) - \left(4.168e04s^3\right) - \left(0.01359s^2\right) + (2.396e-15\ s)} \quad (50)$$

$$G_{vg} = \frac{(-1.277e14s^5) - (8.406e-13s^4) + (7.694e-12s^3) + (6.277e-36s^2) + (1.051e-53\ s) + (3.793e-77)}{(s^9) + (3.259e-07s^8) + (5.263e07s^7) + (17.15s^6) + (1.459e14s^5) + (4.756e07s^4) - (4.168e04s^3) - (0.01359s^2) + (2.396e-15s)} \quad (51)$$

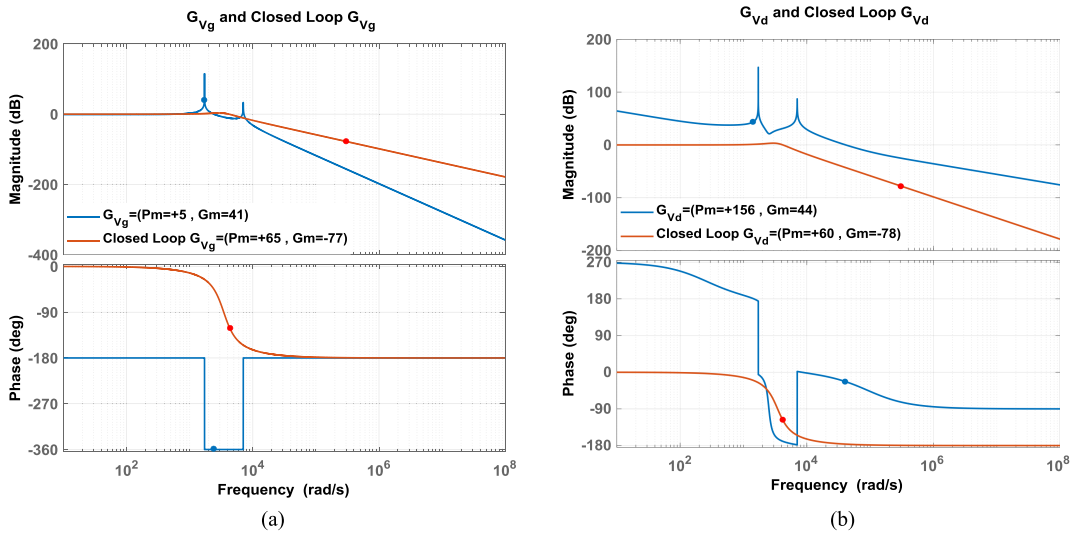

FIGURE 5. Bode digrams of (a) G_{vg} without control and with control ($\frac{G_{vg}}{1+T}$ which is named closed loop G_{vg} on the figure) (b) open loop function G_{vd} and closed loop function ($T = G_c G_{vd}$ which is named closed loop G_{vd} on the figure).

TABLE 1. Comparison of the Proposed Converter With the Presented Ones in the References. S (Switch), D (Diode), C (Capacitor), CI (Coupled Inductor), L (Inductor), T = Total Device Count, 3w (3-Windings CI), 2w (2-Windings CI), T-R = Turns Ratio, I.I.S.P.C.R.W = Input Inductor Size With 30 Percent Current Ripple in the Worst Condition, Eff = Efficiency

Ref	Number of the used components (S/D/C/CL/L/T)	Voltage Gain(M)	voltage stress of Switch(s) ($\sum V_s$)	voltage stress of the main Switch (v_{SMAX})	voltage stress of Diodes ($\sum V_D$)	(I.I.S.P.C.R.W) (μH)	Eff (At nominal power-) %
[1]	1/5/4/1^{2W}/1/12	$\frac{2+n}{(1-D)^2}$	$\frac{V_o}{(2+n)}$	$\frac{V_o}{(2+n)}$	$2V_o$	136.5(Medium)	92.5(80W)
[2]	1/5/5/2^{2W}/0/13	$\frac{1+n}{(1-D)^2}$	$\frac{V_o}{(1+n)}$	$\frac{V_o}{(1+n)}$	$2V_o$	242.7(High)	93(100W)
[3]	1/6/5/1^{2W}/1/12	$\frac{2+n+Dn}{(1-D)^2}$	$\frac{V_o}{(2+n+Dn)}$	$\frac{V_o}{(2+n+Dn)}$	$\frac{(4n+4)V_o}{(2+n+Dn)}$	114.3(Medium)	94.6(150w)
[4]	2/4/4/1^{2W}/1/12	$\frac{1+D+2n(1-D)}{(1-D)^2}$	$\frac{2V_o}{(1+D+2n(1-D))}$	$\frac{(1+D)V_o}{(1+D+2n(1-D))}$	$\frac{(4+2n)V_o}{(1+D+2n(1-D))}$	116.8(Medium)	94(200w)
[5]	2/4/3/1^{3W}/2/12	$\frac{2+n}{(1-D)}$	$\frac{2V_o}{(2+n)}$	$\frac{V_o}{(2+n)}$	$\frac{(8+2n)V_o}{(2+n)}$	246.9(High)	94.7(3000w)
[6]	2/4/4/2^{2W}/0/12	$\frac{1+n+D}{(1-D)^2}$	$\frac{(2-D)V_o}{(1+n+D)}$	$\frac{V_o}{(1+n+D)}$	$\frac{(4+2n-D)V_o}{(1+n+D)}$	214.6(High)	94.4(400w)
[7]	1/6/5/1^{3W}/1/14	$\frac{1+n_2+n_3}{(1-D)^2}$	$\frac{V_o}{(1+n_2+n_3)}$	$\frac{V_o}{(1+n_2+n_3)}$	$\frac{(3+2n_2+2n_3)V_o}{(1+n_2+n_3)}$	87.4(Medium)	95.94(1014w)
[8]	2/5/5/1^{2W}/1/14	$\frac{2n+1+D}{(1-D)^2}$	$\frac{2V_o}{2n+1+D}$	$\frac{(1+D)V_o}{2n+1+D}$	$\frac{(4-2D+4n)V_o}{2n+1+D}$	81(Medium)	94.3(280w)
[9]	2/5/5/1^{2W} /1/14	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{(2-D)V_o}{3+2n-D(3+n-D)}$	$\frac{V_o}{3+2n-D(3+n-D)}$	$\frac{(2n(2-D)+(5-3D))V_o}{3+2n-D(3+n-D)}$	62.5(Low)	93.3(150W)
[10]	2/6/5/3^{2W}/0/16	$\frac{2(N+1)+n}{(1-D)}$	$\frac{2V_o}{2(N+1)+n}$	$\frac{V_o}{2(N+1)+n}$	$\frac{(8N+4n+6)V_o}{2(N+1)+n}$	61.7(Low)	96.9
[23]	2/5/5/1^{3W} /1/14	$\frac{2+3n-2D}{(1-D)^2}$	$\frac{2V_o}{2+3n-2D}$	$\frac{V_o}{2+3n-2D}$	$\frac{(4+5n)V_o}{2+3n-2D}$	90(Medium)	95.2(250W)
[24]	2/4/4/1^{3W} /1/12	$\frac{3+2n-D(1+n)}{(1-D)^2}$	$\frac{(2-D)V_o}{3+2n-D(1+n)}$	$\frac{V_o}{3+2n-D(1+n)}$	$\frac{(7+2(2n-nD-2D))V_o}{3+2n-D(1+n)}$	150(Medium)	96.1(200W)
[25]	2/5/4/1^{3W} /2/14	$\frac{(1+2nD-nD^2+D-D^2)}{(1-D)^3}$	$\frac{(2-D+nD-nD^2)V_o}{1+2nD-nD^2+D-D^2}$	$\frac{(1+nD)V_o}{1+2nD-nD^2+D-D^2}$	$\frac{(4+2n-3d-nD^2)V_o}{1+2nD-nD^2+D-D^2}$	267(High)	94.8(263W)
Proposed	2/5/5/1^{3W}/1/14	$\frac{2+2n_2+2n_3}{(1-D)^2}$	$\frac{(2D(n_3-n_2)+2)V_o}{(2+2n_2+2n_3)}$	$\frac{(2D(n_3-n_2)+(1+D))V_o}{(2+2n_2+2n_3)}$	$\frac{((n_3+n_2)(6-2D)+3+D)V_o}{(2+2n_2+2n_3)}$	21.8(Low)	94.4(240W)

gain curves for n = 2, based on the equations provided in Table I, are plotted in Fig. 6(a).

Since the converters feature either one or two switches, a fair comparison requires considering the sum of the normalized voltage stress and the normalized maximum voltage stress on the switches (Fig. 6(b) and (c)). Fig. 6(b) indicates that the normalized values of ΣV_S in the proposed converter are lower than that of the converters in [1], [2], [4], [5], [6], [8], [9], [10], [23], [24], [25], while it is equal to that of the converter in [7]. Additionally, the converters in [3], [7], and the proposed converter demonstrate similar values for the sum of normalized voltage stress approximately.

Furthermore, Fig. 6(c) specifies that the voltage stress of the main switch in the proposed converter is lower than all converters presented in Table I except the converter in [10], [23]. It should be noted that the superiority of the converter

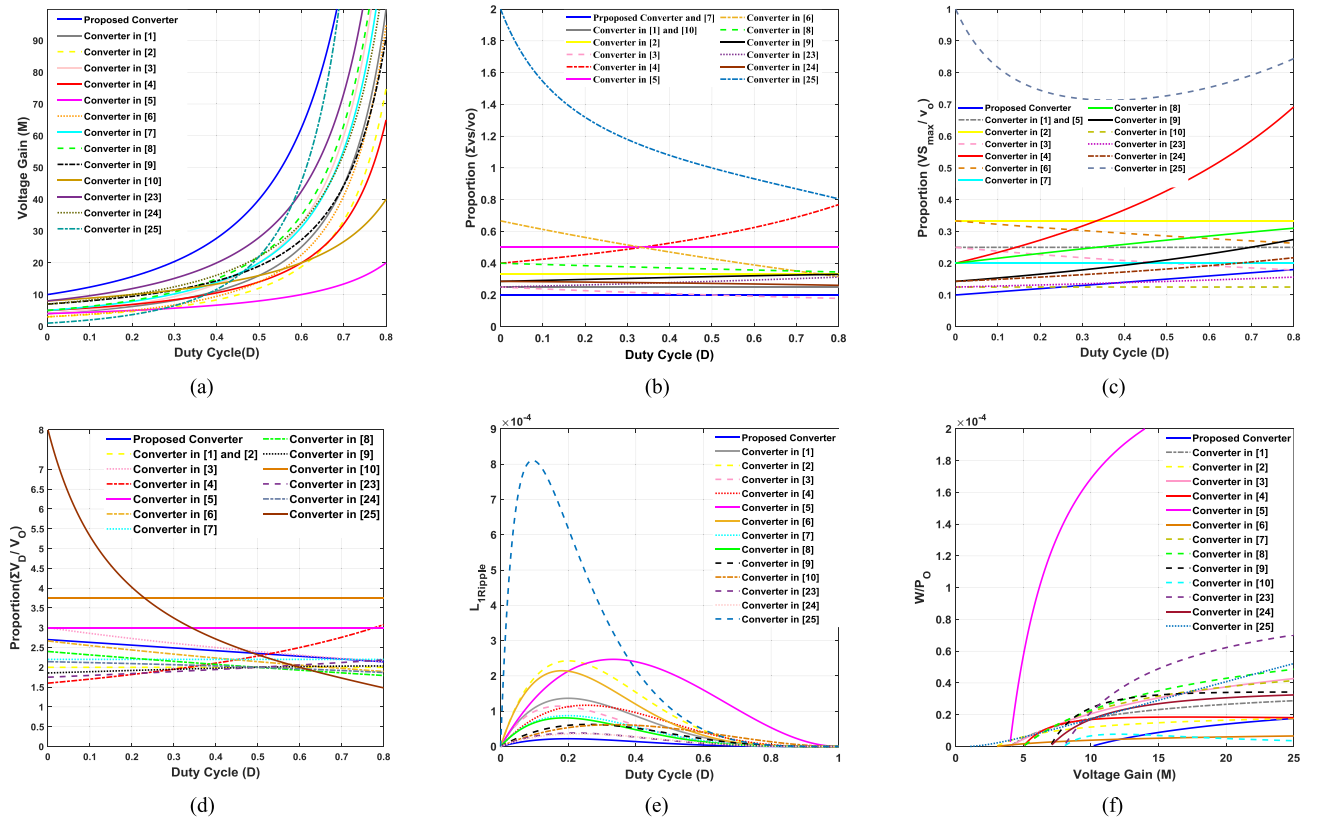

FIGURE 6. Comparison curves of the converters– turn ratio of the CIs is equal to 2 (n = 2). (a) Voltage gain versus duty cycles. (b) Sum of the normalized voltage stress on the power switches. (c) Voltage stress on the main power switch. (d) Sum of the normalized voltage stress on the diodes. (e) Inductance of the main inductor per 30 percent current ripple– R = 400 Ω, f = 50 kHz. (f) Normalized energy of the main inductor versus voltage gain.

in [10], [23] is not significant when compared to the proposed converter. Moreover, the converter in [10] has a low voltage gain and experiences high voltage stress on its diodes. Also the converter in [23] has lower voltage gain, higher input current ripple, and higher normalized energy of the main inductor compared to the proposed converter.

As shown in Fig. 6(d), the sum of the normalized voltage stress of the diodes in the proposed converter is lower than the converters in [3], [4], [5], [10]. Although the proposed converter experiences higher voltage stress on its diodes compared to the converters in [1], [2], [6], [7], [8], [9], [24], [25], it exhibits lower voltage stress on its switches. Additionally, the proposed converter requires a smaller inductor in series with the input source and achieves a higher voltage gain. The main reason of the requiring smaller inductor is higher gain of the proposed converter. In the same voltage gain, the converter operates with lower duty cycle that causes obtaining lower inductance values for the converter. It has to be noticed, the calculations can be validated for the conditions close to the renewable sources features and properties, where the output voltage is regulated and the input voltage may vary during power production by the sources. The size of inductors significantly influences the volume and efficiency of DC-DC converters, particularly the inductor that is in series with the input source due to the high magnitude current involved in the input side of high step-up converters. Consequently, the inductance of the input inductor for 30 percent current ripple is compared with other converters in Fig. 6(e). The inductances are calculated under specific condition with equal frequency (50 kHz), load resistance (400 Ω), and turns ratio (2). The results indicate that even under the worst condition where the inductor requires the largest inductance, the proposed converter necessitates the smallest L. Furthermore, the energy stored of L in the proposed converter exhibits low values across various gains, indicating that the inductor requires a small-sized core or a small area product (A_P) for the core. The parameter A_P and energy are directly related in the design equations, and they have been compared for the main inductors of the converters in Fig. 6(f). The plotted curves depict the inductor's energy (per unit) versus different gains under the worst operating conditions. Although the proposed converter has higher inductor energy compared to the converters in [6], [10], it features a smaller inductor size for a 30 percent current ripple. In comparison to the other converters, the proposed converter holds an advantage from this perspective.

Finally, the proposed converter has been compared with the converters in [7], [8], [9], [23] and [25] from the points of view of volume, cost, and power density, which all contain 14 elements in their structures. For a fair comparison, the components of the converters are redesigned for the same

TABLE 2. Comparison of Cost, Volume and Power Density of the References With 14 Components

	Volume	Power Density	Cost
proposed converter	$139.9cm^3$	$1.78\ \frac{w}{cm^3}$	**$16.538**
converter [7]	$150.05cm^3$	$1.66\frac{w}{cm^3}$	**$22.474**
converter [8]	$144.95cm^3$	$1.72\ \frac{w}{cm^3}$	**$18.91**
converter [9]	$141.63cm^3$	$1.76\ \frac{w}{cm^3}$	**$18.975**
converter [23]	$145.14cm^3$	$1.72\ \frac{w}{cm^3}$	**$18.44**
converter [25]	$143.17cm^3$	$1.74\ \frac{w}{cm^3}$	**$27.88**

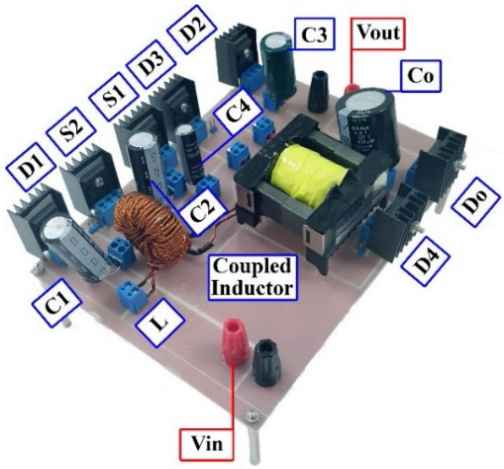

FIGURE 7. Prototype of the proposed converter.

conditions, including the following values: V_{in} = 20 V, V_{out} = 400 V, switching frequency = 50 kHz, n = 1, and 100 W ≤ P_O ≤ 300 W. According to the results listed in Table II, the superiority of the proposed converter can be seen due to its lower volume, lower price, and higher power density compared to the other three converters. It has to be noticed, that the proposed converter presents more improved properties in comparison to the converters in [7], [8], [9], [23], [25] as discussed above.

VI. EXPERIMENTAL RESULTS

To validate the performance and theoretical analysis of the proposed converter, a 240 W prototype has been constructed, as illustrated in Fig. 7. Table III provides the properties and details of the components used in the prototype. The voltage stress on the power switches and diodes is calculated using (16) to (22). The calculation results with consideration of the semiconductors' current in nominal power are utilized to choose them. Fig. 8 illustrates the experimental results per D = 0.458 and input voltage equals 20 V. The output voltage, output power, and turns ratio (n) are 400 V, 240 W, and 1, respectively. The waveforms in Fig. 8 depict the voltages and

TABLE 3. Used Components in the Prototype

PARAMETERS	Value
Input and Output Voltage	20V-400V
Output power	240W
inductor (L)	100μH
turn ratio of the coupled inductor ($n_3 = N_3/N_1$ $n_2=N_2/N_1$)	1
magnetic inductance of the coupled inductor (L_m)	188μH
leakage inductance of the coupled inductor (L_K)	0.9 μH
C_1, C_2, C_3, C_4 and C_O	100μF, 100μF, 120μF, 150μF and 220μF
Switching Frequency	50kHz
MOSFETs S_1 and S_2	IRF064N and IXTK90N15
D_1, D_2, D_3, D_4 and D_O	FEP30BP, FEP30BP, F30UP20DN, MM60F060PC, SBR10U300CT
Resistive load	670Ω

currents of the components and the dynamic responses of the converter during changes. By utilizing the analysis (16), (17), (22), and (14), the calculated voltage stress on S_1 and S_2, the output diode, and the output capacitor should be 36.9, 99.26, 272.32, and 408.49V, respectively. Fig. 8(a) shows that the voltage stress on S_1, S_2, D_O, and C_O is equal to 39.5, 102, 269, and 400V, respectively. Therefore, the experimental results demonstrate low voltage stress on the switches, where their values are 1/8 and 1/4 of V_O. According to the calculations, the voltage stress values corresponding to C_1, C_2, C_3, C_4, D_1, D_2, D_3, and D_4 should be 36.90, 36.90, 62.36, 246.89, 36.90, 36.90, 173.06 and 408.49V. The experimental results confirm that the voltages in Fig. 8(b) and (c) closely match those calculated, i.e., 38, 38, 62, 243, 36, 38, 174 and 399V. These results cooperated in selecting suitable diodes and MOSFETs, as detailed in Table III. Based on the analysis, the output voltage should be 408.49 for D = 0.458 and n = 1 which is in good accordance with the result in Fig. 8(d). As can be seen, the current ripple of the input inductor is a little higher than 30% which proves possibility of achieving low current ripple with a small inductor. To investigate the quality performance of the converter, dynamic and transient responses were examined during sudden changes in input voltage and output power. Fig. 8(e) illustrates the variation of input voltage from 20 V to 32 V and reverse, validating the dynamic response of the converter. Additionally, Fig. 8(f) shows the variation of output power from 120 W to 200 W and then back to 120 W. Based on the results, it is evident that the controller effectively regulates the output voltage during these significant changes. The observed results confirm the stability and good dynamic performance of the converter, indicating its capability to handle variable conditions.

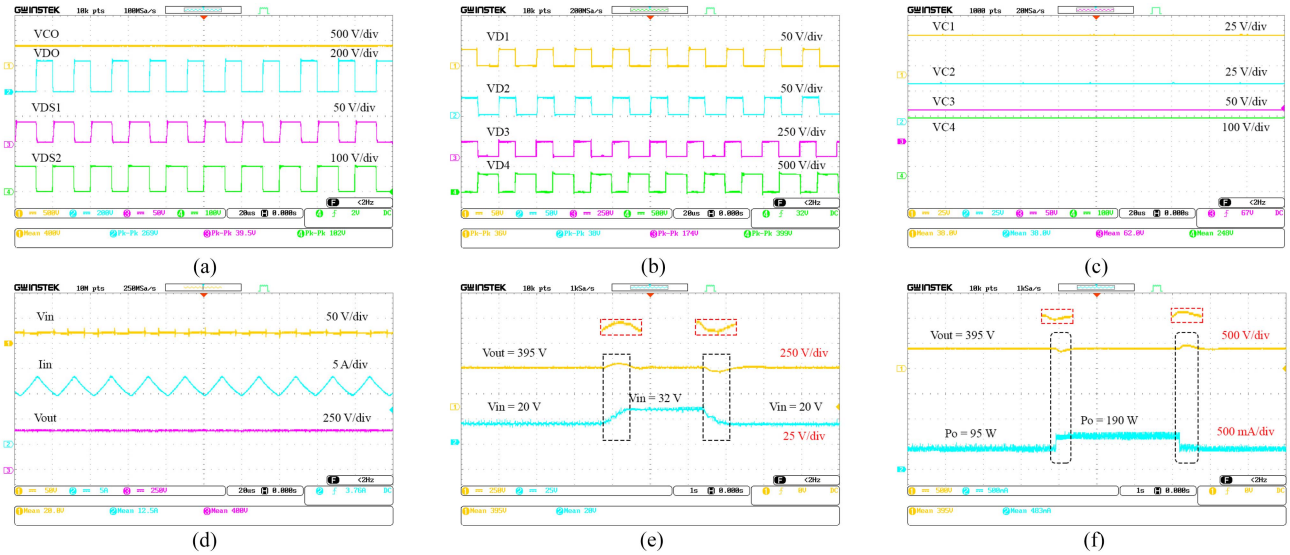

FIGURE 8. Experimental results. (a) Voltage of the switches, C_O, and D_O. (b) Voltage of D_1, D_2, D_3, and D_4. (c) Voltage of C_1, C_2, C_3, and C_4. (d) Input voltage, output voltage, and input current. (e) Dynamic response of the converter per changes of the input voltage from 20 to 32 V. (f) Transient response of the proposed converter during sudden variations of the load.

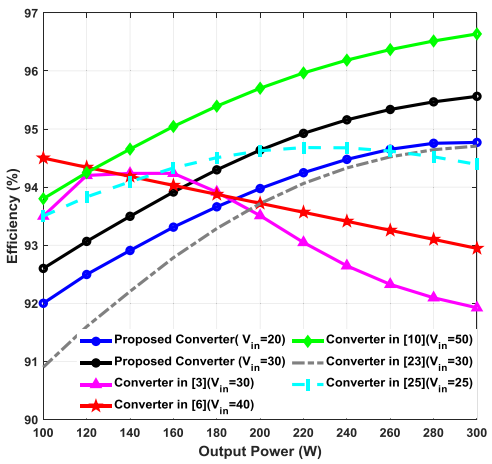

FIGURE 9. Comparison of experimental efficiency between the proposed converter and the others per different output power.

The converter efficiency per the different output power ($100W \leq P_o \leq 300$ W) is compared with the references in Fig. 9. To ensure a fair comparison, the efficiency of the proposed converter was plotted for input voltages of both 20 and 30 volts. As it can be seen, the proposed converter operates with high efficiency like the converters in [10] and [25], especially in output power higher than 200 W and $V_{in} = 30$ for the proposed converter. It has to be noticed, the input voltage of [10] is higher than the proposed converter, which causes higher efficiency. Also, the voltage gain of the proposed converter has the highest values in the compared plots and its efficiency would be higher than most of them at the voltage gains like the compared references or lower than 20. The efficiency of the proposed converter ranges from 92% to 95.7% for power levels between 100 W and 300 W for different input voltages (20 V and 30 V), which is 94.4% at the nominal power of 240 W and rated input voltage of 20 V, confirming the high-efficiency performance of the proposed converter.

VII. CONCLUSION

This paper presents a step-up converter with ultrahigh voltage gain. As compared with existing converter topologies, the proposed converter has across the board low input current ripple and low voltage stress. It also uses a smaller input inductor and achieves a higher power density than the relevant topologies compared. To validate of the analysis of the proposed converter, experiments were conducted at a voltage gain of 20, while maintaining an efficiency of 94.4% at the nominal output power. The analysis and experimental results prove that the voltage stress on the switches is $0.125V_O$ and $0.25V_O$, confirming the appropriate design of the converter in this aspect. The dynamic responses of the converter during the sudden changes ensure its high-quality performance under unpredictable conditions.

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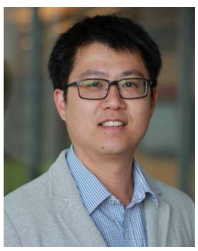
VAHID ABBASI received the B.S. degree in electrical engineering from Shahid Chamran University, Ahvaz, Iran, in 2002, and the M.S. and PhD. degrees in electrical engineering from the Iran University of Science and Technology, Tehran, Iran, in 2004 and 2012, respectively. He is currently an Associate Professor with the Department of Electrical Engineering, Kermanshah University of Technology, Kermanshah, Iran. His research interests include the design and implementation of power electronic converters.

MOHAMMAD MEHDI KASHANI was born in Kermanshah, Iran, in 1996. He received the B.S. degree in electrical engineering from the Razi University of Kermanshah, Kermanshah, Iran, in 2019, and the M.S. degree in electrical engineering from Kermanshah University of Technology, Kermanshah, Iran, in 2024. His research interests include design and implementation of power electronic converters, especially high step-up and multi-port DC–DC converters.

MILAD REZAIE was born in Kermanshah, Iran. He received the B.S. degree in electrical engineering from the Technical University of Imam Mohammad Bagher, Sari, Iran, in 2016, and the M.S. degree in electrical engineering from Kermanshah University of Technology, Kermanshah, Iran, in 2019. His research interests include design and implementation of power electronic converters, especially high step-up DC-DC converters.



DYLAN DAH-CHUAN LU (Senior Member, IEEE) received the Ph.D. degree in electronic and information engineering from Hong Kong Polytechnic University, Hong Kong, in 2004. In 2003, he began his professional career with PowerELab Ltd., as a Senior Design Engineer, focusing on industrial switching power supply projects. From 2006 to 2016, he was a full-time Faculty Member with The University of Sydney, Australia. In 2016, he joined the University of Technology Sydney, where he currently a Professor and the Head of Discipline of Electrical Power and Energy Systems with the School of Electrical and Data Engineering. His research interests include developing efficient, cost-effective, and reliable power conversion solutions for renewable energy sources, energy storage systems, and microgrids. From 2020 to 2023, he was the Chair of the Joint Chapter IAS/IES/PELS (IEEE New South Wales Section) and continues to support the Joint Chapter through his Past Chair role in 2024. He is also an Associate Editor for IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS.