UTS UNIVERSITY OF TECHNOLOGY SYDNEY

RF MEMS-Based True Time Delay Units for Wideband Phased Arrays: Theoretical Advancements, Design Innovations and Beamforming Optimisation

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Thesis submitted in fulfilment of the requirements for the degree of

Doctor of Philosophy

under the supervision of
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CERTIFICATE OF ORIGINAL AUTHORSHIP

I, David W. K. Thomas, declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the School of Electrical and Data Engineering in the Faculty of Engineering and Information Technology at the University of Technology Sydney.

This thesis is wholly my own work unless otherwise referenced or acknowledged. In addition, I certify that all information sources and literature used are indicated in the thesis.

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ABSTRACT

The increasing demand for high-speed, wideband and adaptive communication systems has necessitated advancements in phased array antenna technology, particularly in achieving electronic beam scanning, adaptive nulling and multi-beam capabilities. Large aperture phased arrays have been widely adopted in radar, satellite communications and 5G networks, where the ability to maintain beam stability across broad frequency bands is critical. However, traditional phased arrays relying on phase shifters are susceptible to beam squint and signal dispersion when operating over wide bandwidths. This challenge has led to the emergence of timed arrays, which incorporate time delay units (TDUs) instead of phase shifters to achieve true-time delay compensation, ensuring consistent beam pointing over a wide frequency range.

This thesis systematically investigates the theoretical foundations and practical implementation of true time delay (TTD) phase shifters in timed arrays, presenting novel contributions in several key areas. A switched-line TDU architecture is proposed, leveraging microelectromechanical system (MEMS) switches to achieve an enhanced performance in delay-to-loss ratio. A prototype printed circuit board (PCB) covering a broad frequency band of 0.4 GHz to 6 GHz has been designed and fabricated, with experimental validation demonstrating a Figure of Merit (delay in ps per dB loss) superior to existing TDU designs reported in the literature. Beyond TDU design, this thesis explores the beamforming network (BFN) for large timed arrays, presenting an innovative methodology to optimise space efficiency while mitigating grating lobes, thereby enhancing beamforming accuracy and overall array performance. Additionally, a detailed analysis of TDU truncation and quantisation errors is conducted, revealing their critical impact on array performance. Unlike conventional studies that often overlook these factors, an analytical framework is developed to precisely quantify and mitigate these errors, providing a more accurate basis for TDU delay value selection. This research also introduces a probabilistic approach to TDU design, addressing the challenge of determining optimal TDU sizing for metaheuristic and stochastic beamforming optimisations across various scan angles. This approach improves the adaptability of timed arrays in dynamic environments, facilitating more efficient and robust wideband beam-steering solutions.

In summary, this thesis delivers fundamental advancements in TDU technology, beamforming networks and array performance optimisation, providing a pathway for next-generation phased arrays capable of supporting 6G communications, advanced radar systems and next-generation satellite networks.

PEER-REVIEWED JOURNAL ARTICLES

1. D. W. K. Thomas, K. Wu and Y. J. Guo, "Tradeoffs in Avoiding Truncation in Hierarchical Time Delay Beamforming Networks," in *IEEE Antennas and Wireless Propagation Letters*, vol. 24, no. 10, pp. 3809-3813, Oct. 2025, doi: 10.1109/LAWP.2025.3605713
2. D. W. K. Thomas, K. Wu and Y. J. Guo, "A New TDU-Based Hierarchical Beamforming Framework to Suppress Grating Lobes and Save Space," in *IEEE Open Journal of Antennas and Propagation*, doi: 10.1109/OJAP.2025.3575424
3. D. W. K. Thomas, K. Wu, and Y. J. Guo, "A switched-line true time delay unit for wideband phased arrays using packaged RF MEMS switches," *Sensors*, vol. 25, no. 21, doi: 10.3390/s25216806.

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1. INTRODUCTION

Next generation satellite, radar, and broadband wireless systems require agile, wideband beamforming solutions capable of supporting high-data-rate, low-latency communication links [1]. Electronically scanned arrays (ESAs) enable rapid, programmable beam steering and spatial multiplexing, forming the foundation of modern communication and sensing networks. Conventional ESAs rely on phase shifters to steer beams electronically, but this approach introduces frequency-dependent distortion: beam squint and signal dispersion degrade spatial accuracy and time-domain fidelity, particularly over wide instantaneous bandwidths [2].

Replacing the phase shifters of a phased array with true-time-delay units (TDUs), forming a timed array, overcomes these limitations by introducing frequency-independent delays that preserve waveform integrity across the band [3], [4]. Despite these advantages, TDUs have seen limited adoption due to practical constraints of physical size, fabrication cost, reliability and manufacturability [5]. These trade-offs have shaped decades of research into photonic, MMIC (Monolithic Microwave Integrated Circuit) and distributed MEMS transmission-line (DMTL) TDUs, each offering unique benefits but none providing an ideal balance between bandwidth, loss and integration complexity.

The emergence of reliable, commercially packaged RF MEMS switches now offers a practical pathway to realising compact, low-loss TDUs on standard PCB platforms [6], [7], [8]. RF MEMS devices combine low insertion loss, high linearity, and negligible static power consumption, making them well suited for integration into broadband beamforming modules. The availability of such components transforms timed-array architectures from theoretical constructs into manufacturable subsystems, motivating the investigation undertaken in this work.

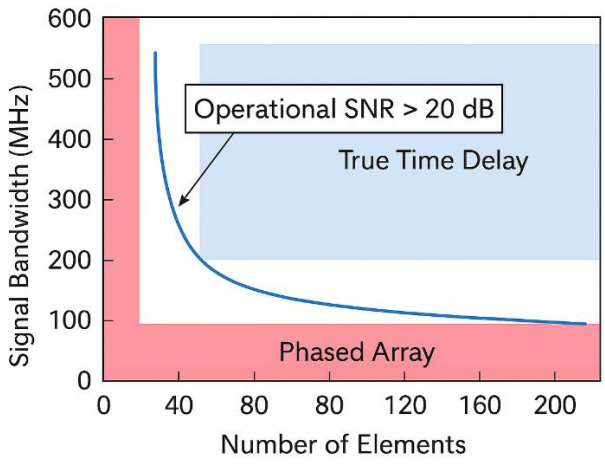


Figure 1. Maximum signal bandwidth vs number of antenna elements in a uniform linear array.

To illustrate this important concept, consider Figure 1. The blue curve indicates the boundary for a signal SNR of better than 20 dB with a phased array at an arbitrary scan angle off boresight. To the left of the curve is the indicative signal bandwidth capability of a phased array and to the right is the potential signal bandwidth capability of a true timed array [9]. (For a full explanation, see Appendix 1.)

The important realisation is the inherent narrow bandwidth nature of phased arrays, especially with large arrays. The bandwidth limitation is primarily a function of signal dispersion. As the number of elements in an array increases, the required phase shift across the face of an array that is necessary to add all the received signals coherently exceeds 360°, the limit for phase shifters and the signals start to disperse as they are no longer added together precisely in time.

Phased arrays also suffer from beam squint as the phase shift required for a precise beam scan angle changes with frequency and phase shifters can only provide a fixed phase shift at all frequencies. These issues severely limit the effective operational bandwidth of large arrays, presenting a significant bottleneck for emerging wideband applications. The solution lies in replacing conventional phase shifters with true time delay units (TDUs) [3], ensuring that all frequency components of a signal experience the same propagation delay. Timed arrays, which employ TDUs instead of phase shifters, eliminate the signal dispersion problem and enable truly wideband operation.

While phased arrays incorporating active electronically scanned arrays (AESAs) are already a cornerstone of radar and communications technology, their effectiveness in wideband scenarios depends on the availability of high-performance TDUs. Until recently, the lack of suitable switching technology limited the feasibility of practical, cost-effective TDUs. The advent of reliable, packaged RF MEMS switches has fundamentally changed this landscape, bringing the possibility of commercially viable RF MEMS-based TDUs closer to reality. RF MEMS switches offer several advantages over traditional semiconductor-based solutions, particularly silicon CMOS switches, which suffer from higher insertion loss and limited power handling. In contrast, MEMS devices exhibit exceptionally low loss, high linearity and negligible power consumption when static, making them ideal for high-frequency and high-power applications.

Historically, RF MEMS-based solutions faced two major barriers to commercialisation: the availability of packaged, standardised components and concerns over long-term reliability. For many years RF MEMS switches were available only as custom-built, hermetically sealed dies, limiting their scalability and making mass production challenging. Additionally, early MEMS

devices suffered from issues such as stiction and charge accumulation, leading to degraded performance over time. These reliability concerns, combined with limited commercial availability, hindered the adoption of MEMS technology in large-scale phased array systems.

However, recent advancements in MEMS packaging and reliability have addressed these concerns, opening the door to the large-scale deployment of RF MEMS-based TDUs. With the emergence of commercially available packaged RF MEMS switches, it is now possible to design TDUs that leverage the inherent benefits of MEMS technology while meeting the practical requirements of manufacturability and integration. The ability to implement true time delay networks on standard PCB platforms using RF MEMS switches represents a significant step forward, making high-performance, low-cost TDUs feasible for both military and commercial applications.

For clarity, this thesis uses the term phase shifter to include both true phase delay, i.e., a constant phase shift regardless of frequency, limited to a range of 0° to 360°, and true time delay, i.e., a varying phase shift linearly related to frequency. The term time delay unit, TDU or time delay phase shifter is used to be clear when referring only to a true time delay phase shifter.

1.1. Motivation for Investigating Timed Arrays

The motivation for this research stems from the increasing demand for advanced beamforming and phased array technologies driven by the rapid expansion of 5G and emerging 6G networks, the growing LEO satellite market (Starlink, OneWeb, Project Kuiper (Amazon) and China's GW constellations) and military radar and communication systems. These sectors require ultra-wideband (UWB), high-performance antenna systems, making TDUs a crucial enabling technology.

The global 5G infrastructure market is projected to reach USD 590 billion by 2032, driven by the deployment of massive MIMO antennas and advanced beamforming to support high-capacity, low-latency networks. The 6G market, though in early development, is expected to grow exponentially, reaching USD 68.7 billion by 2035. In parallel, the LEO satellite market is expanding rapidly, with forecasts predicting growth from USD 13.5 billion in 2025 to USD 66.5 billion by 2035, as providers race to offer global broadband coverage [10-12].

Crucially, these multi-billion-dollar markets rely on high-performance components, including antennas and beamforming networks. Specifically, the smart antenna market, which includes adaptive and beam-steering technologies, is set to double in size to USD 14.5 billion by 2032 [13-15].

Beyond commercial applications, military radar and advanced communication systems are adopting phased array technologies to enhance target tracking, situational awareness and secure communications. These applications require precise, frequency-independent beamforming, making TDUs a critical component for next-generation defence systems.

This thesis examines the potential role of RF MEMS switches for inclusion in the next generation of TDUs. By analysing the limitations of and demonstrating the advantages of RF MEMS-based TDUs, this work aims to establish their technical viability and practical significance in next-generation communication systems. Through a combination of theoretical modelling, circuit design and experimental validation, the research presented here demonstrates the potential of RF MEMS-based TDUs to transform the field of electronically steered arrays, bridging the gap between academic research and real-world deployment. While time delay beamforming is widely recognised as the optimal solution for wideband arrays, its practical feasibility has been limited by technology constraints. The recent advancements in MEMS-based RF switching provide an opportunity to bridge this gap, offering a pathway to efficient and manufacturable TDUs with minimal insertion loss.

This research also aims to explore strategies to optimise beamforming network architectures, particularly those optimised for TDU-based arrays. The optimisation of beamforming networks, in conjunction with TDUs, presents an opportunity to achieve more efficient space utilisation, reduced sidelobe levels and improved beamforming accuracy. By addressing these challenges, this work seeks to contribute to the next generation of electronically scanned arrays.

1.2. Research Challenges

The transition from phase-based to time-based beamforming presents several technical challenges. These include:

- **Size, cost, weight and complexity.** These are the perennial research areas to make phased arrays more compact and cost-effective for large-scale integration in phased arrays. It is generally accepted that the high cost of phased arrays has limited their applications [16]. Research is active in such areas as transmit/receive modules, hybrid arrays, tile vs slat designs, modularisation, subarrays, thinned arrays, sparse arrays and time-modulated arrays.
- **Maximum delay time:** Seeking ever increasing time delays sufficient to support wideband beamforming and to be practical for large array sizes.

- **Quantisation errors:** Research continues into methods to reduce the detrimental effects of discrete phase/time states with such methods as randomising errors, mixed-resolution phase shifters and array element rotation.
- **Improving performance parameters:** Any improvements in insertion loss, isolation, power handing, power consumption all add to the objective of achieving compact and cost-effective time delay solutions.
- **Wide-angle scanning arrays**. Research continues to improve the performance in such areas as grating lobe suppression, gain variation with scanning, mutual coupling and poor impedance matching.

1.3. Contribution

This thesis advances the field of electronically steered arrays by demonstrating the feasibility of MEMS-based TDUs and optimising their integration into phased arrays. Key contributions include:

- An essential step forward in the development of RF MEMS TDUs, addressing key historical challenges and demonstrating a practical and commercially viable solution for a wide range of phased array beamforming networks. The work conducted here represents novel contributions to the field.
- A novel approach to optimising beamforming networks by varying TDU delay values within a single layer is proposed. This method reduces required PCB space by up to 30% and improves sidelobe suppression, demonstrating a 18 dB reduction in grating lobes. No prior work has reported this approach, making it a significant contribution to phased array design.
- A rigorous analysis of quantisation induced truncation errors in hierarchical beamforming networks overcoming the conventional design assumptions that fail to account for cumulative quantisation effects. This study introduces a correction framework to mitigate truncation-induced performance degradation, a topic often overlooked in the literature.
- A probabilistic analysis of phase-only synthesis for wide-angle beam scanning, leading to new insights into the required TDU delay range. This study provides practical design rules that help balance sidelobe control with physical constraints, ensuring that TDUs are neither excessively over-dimensioned nor inadequately provisioned.

1.4. Structure of Thesis

The remainder of this thesis is structured as follows.

- Chapter 2 – Introduces the fundamentals of timed arrays and details of the current state-of-the-art for TDUs and RF MEMS switches along with recent development with beamforming networks.
- Chapter 3 – Reviews the published literature on TDUs and analyses the challenges of RF MEMS-based TDUs.
- Chapter 4 - Introduces a novel RF MEMS switched-line TDU for UWB phased arrays, detailing the design methodology, simulation-driven optimisation, electromagnetic simulation validation and experimental characterisation of the developed TDU.
- Chapter 5 - Explores the beamforming network for large timed arrays, introducing an innovative methodology to optimise space efficiency while mitigating grating lobes.
- Chapter 6 - A detailed analysis of TDU truncation and quantisation errors is conducted, revealing their critical impact on array performance. Unlike conventional studies that often overlook these factors, an analytical framework is developed to precisely quantify and mitigate these errors, providing a more accurate basis for TDU delay value selection. A further contribution of this research is the introduction of a probabilistic approach to TDU design, addressing the challenge of determining optimal TDU sizing for metaheuristic and stochastic beamforming optimisations across various scan angles.
- Chapter 7 – Concluding remarks.

2. Fundamentals for Timed Arrays

The purpose of this chapter is to establish the theoretical and technological foundations required to understand timed arrays and their implementation in wideband beamforming networks. It introduces the underlying concepts of phased and timed arrays, TDUs, feeder architectures, and enabling device technologies such as RF MEMS. Together, these elements form the basis for the practical designs and optimisation methods developed in subsequent chapters.

The demand for agile, wideband beamforming has highlighted the limitations of conventional phase-based beamformers, whose frequency-dependent phase shifts cause beam squint and pulse dispersion. Timed arrays address these limitations by providing frequency-independent delays that preserve waveform integrity across bandwidth. The implementation of such true-time-delay architectures, however, introduces new challenges in physical realisation, size and manufacturability, which are the focus of this chapter.

This chapter is structured as follows. Section 2.1 reviews phased-array operation and identifies the sources of beam squint. Section 2.2 introduces the concept and implementation of TDUs, followed by Sections 2.3 – 2.5, which examine feeder networks, constrained feeds, and multibeam architectures. Sections 2.6 – 2.9 describe enabling technologies and performance metrics, including MEMS and monolithic solutions. Finally, Section 2.10 provides a practical review of recent developments in TDU and beamforming architectures, summarising emerging directions that guide the research presented in the following chapters.

2.1. Phased Arrays

Figure 2 depicts the simplest form of a phased array with four evenly spaced elements, each with a series phase shifter. By controlling the individual phase shifter values, the array beam can be scanned.

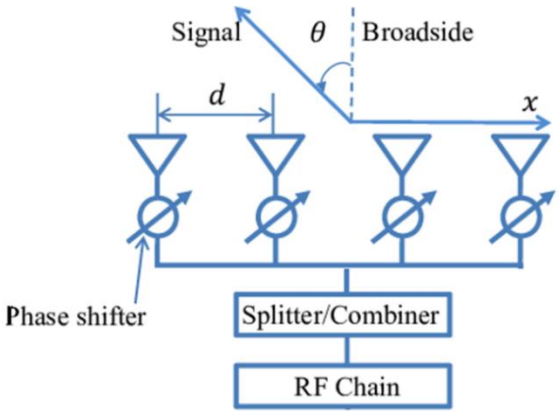


Figure 2. A linear phased array.

The Introduction stated that a phased array is an inherently narrowband antenna. This chapter explores why this is so and discusses its narrowband characteristics, specifically beam squint and quantisation sidelobes.

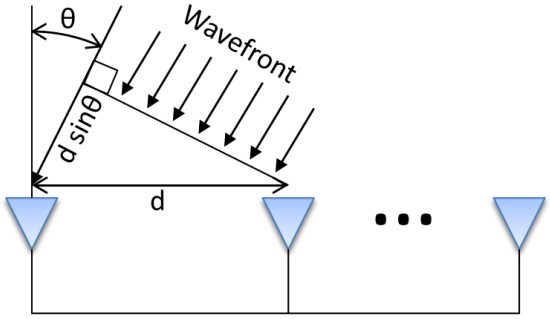


Figure 3. Geometry of phase shift or time delay.

Consider the geometry in Figure 3. A uniform wavefront is arriving from a distant source (i.e. the wavefront is planar) from a direction of θ off boresight. The extra distance that the wavefront must travel to an adjacent element is $d\sin(\theta)$. Assuming free space, the time delay between adjacent elements is

$$\Delta t = \frac{d\sin\theta}{c}. \tag{2.1}$$

Here, d is the inter-element spacing, θ is the scan angle and c is the speed of light.

The corresponding progressive phase $\Delta\phi$ required by a phase-steered array, for a given frequency f with a wavelength of λ, is

$$\Delta\phi = 2\pi f\Delta t = \frac{2\pi d\sin\theta}{\lambda}. \tag{2.2}$$

This formula can be rearranged to give the scan angle θ as a function of the phase shift $\Delta\phi$,

$$\theta(f) = \sin^{-1}\left(\frac{c}{2\pi fd}\Delta\phi\right). \tag{2.3}$$

This formula is insightful as it helps explain the reason a constant phase shift between adjacent elements gives rise to the narrowband nature of a phased array. When the phase shift $\Delta\phi$ is fixed across frequency, the scan angle becomes frequency-dependent, leading to a phenomenon known as beam squint or a pointing error. This effect arises because the phase shift introduced by each element is fixed and as the frequency varies, the scan angle θ varies.

Figure 4 illustrates this effect, showing how the pointing error increases as frequency deviates from the design frequency. This behaviour is particularly problematic for wideband arrays, where beam squint limits the usable bandwidth [17].

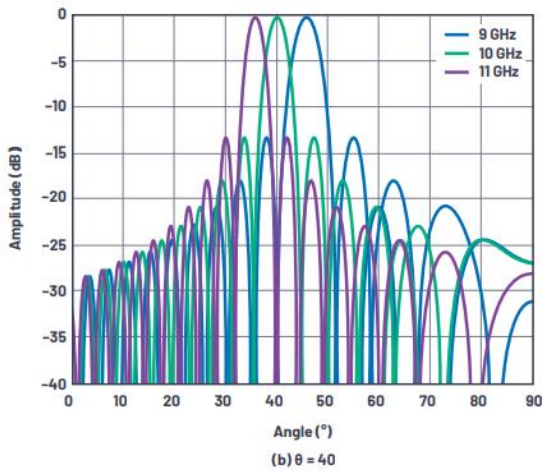


Figure 4. Beam squint with frequency [17].

As the scan angle increases, beam squint becomes more pronounced due to the nonlinear relationship between θ and frequency**,** as illustrated in Figure 5 [17].

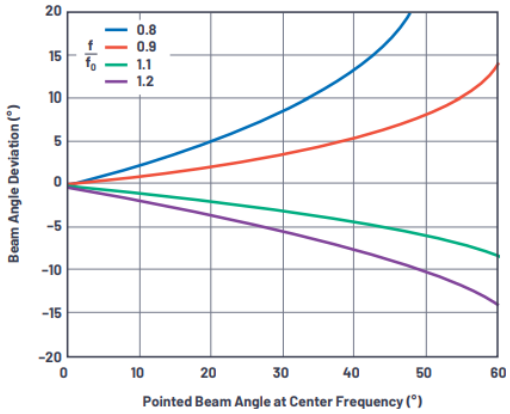


Figure 5. Beam squint vs beam angle for several frequencies [17].

A direct consequence of beam squint is the reduced beamforming efficiency at off-axis angles, resulting in degraded gain and increased sidelobe levels. The severity of this effect depends on the array size, element spacing and fractional bandwidth. Conventional phased arrays mitigate this issue by using narrowband beamforming, but for ultra-wideband applications, a different approach is required.

As already mentioned, the most effective solution to eliminate beam squint is the use of true time delay units instead of phase shifters. Unlike phase shifting, which applies a frequency-dependent phase offset, time delay units introduce a frequency-independent time

delay, preserving scan angle consistency across a wide bandwidth. This allows for wideband beamforming without squint-induced degradation.

Another characteristic alluded to in Figure 1 is that the signal bandwidth decreases as the number of array elements increases in a phased array. To help understand this, consider a pulse of RF representing a data symbol, arriving off boresight across the face of a linear array. To maintain the integrity of the symbol, it is necessary that the combination of all the array elements truly add up to the original symbol. If the symbol has already passed over any element, then the output of that element will not contain the symbol and will corrupt the combined output of the array. Hence the duration of the symbol needs to be approximately long enough to cover the full array at once, less a delay of 360° as the maximum delay of any element. So as an array becomes physically bigger, the symbol period must increase to still fully illuminate the array all at once and so the signal bandwidth decreases. It is the same logic as the scan angle increases, the time delay of arrival of the symbol between elements increases and hence the symbol period needs to increase to compensate. Figure 6 shows the changes in signal bandwidth versus the scan angle and the number of elements in a linear array [3].

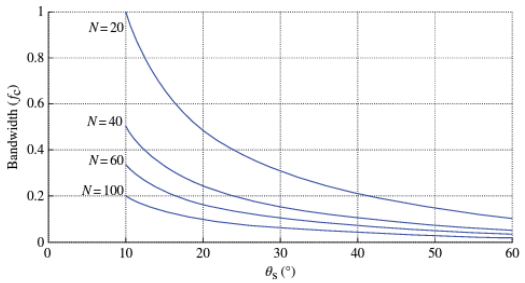


Figure 6. Signal bandwidth vs scan angle and number of elements [3].

2.1.1. Non-Ideal Effects and Practical Limitations

The preceding discussion has assumed ideal conditions: identical antenna elements, perfectly matched feed networks and frequency-independent components. In practice, such assumptions are never fully realised. Real arrays operate under a combination of component and electromagnetic level non-idealities that introduce both static and frequency-dependent amplitude and phase deviations. Even when these deviations are constant with frequency, such as from fixed impedance mismatch or manufacturing tolerances, they can still distort the beam and reduce efficiency. Any phase or amplitude deviation from ideal can cause beam squint, elevated sidelobes and signal dispersion, degrading spatial accuracy and time-domain fidelity and limiting the usable scan range. The following paragraphs summarise the main contributors.

a) **Component-level non-idealities.**

Power dividers, hybrid couplers, TDUs and other feed components exhibit frequency-dependent behaviour. Small variations in insertion loss, phase shift and impedance with frequency lead to unequal array element excitations across the band. Imperfect impedance matching produces standing-wave ratios above unity, generating reflections that interact with adjacent devices and create frequency-dependent ripple in amplitude and group delay. Comprehensive analyses of the impact of component imperfections on wideband beamforming architectures have been reported [18].

Dispersion within each component, particularly within long delay lines, causes frequency-dependent phase velocity that accumulates along the feed path, introducing residual delay error. Quantised control states in digitally controlled TDUs further perturb the ideal delay profile, a topic addressed in more detail in later chapters.

b) **Array-level effects.**

At the array level, electromagnetic coupling and geometric factors dominate. Mutual coupling alters the active impedance of each element, producing scan-angle-dependent impedances changes that lead to amplitude and phase errors varying across the aperture. Even in well-matched designs, the input VSWR of individual elements changes with scan angle and with their position in the array; elements at the edge or corner experience different coupling environments from those at the centre. These variations distort the intended array excitation and contribute to elevated sidelobe and grating-lobe levels, particularly for wide-angle scanning arrays. Comprehensive discussions of wide-angle scanning challenges are given in [19].

Another important array-level limitation is dispersion in the time domain, as described by Haupt [3]. When a wideband signal pulse impinges on a large array at an oblique angle, the waveform no longer illuminates all elements simultaneously. Portions of the array receive different parts of the symbol sequence and multiple symbols may coexist across the aperture simultaneously. The result is pulse spreading and intersymbol interference, which intensify with increasing scan angle and physical aperture size. This time-domain dispersion complements the frequency-domain beam squint discussed earlier and represents a fundamental limit on the wideband performance of phase-based arrays. Timed arrays employing true-time-delay compensation are specifically intended to suppress these effects by aligning the temporal response of all elements.

c) **System-level consequences.**

The combined influence of component and array non-idealities manifests as increased sidelobe levels, main-beam distortion, including beam pointing error, broadening, asymmetry and temporal pulse spreading, reduced aperture efficiency and in extreme cases, instability in beam pointing. These degradations become particularly severe in ultra-wideband and wide-angle scanning applications where small amplitude or phase deviations vary rapidly with frequency.

In summary, the practical limitations of wideband arrays arise from a complex interaction between frequency-dependent component behaviour and array-level electromagnetic coupling. Recognising these effects is essential when evaluating new time-delay and beamforming architectures, as subsequent chapters will demonstrate.

2.2. True Time Delay Units

TDUs can be implemented using various technologies, CMOS, electromechanical switches (relays), MEMS and GaAs-based designs. Each approach offers different trade-offs in terms of insertion loss, size and complexity. This section focuses on the MEMS options and covers the TDU design options available. As TDUs are typically digitally controlled with a set of defined delays, this section also covers the effects of quantisation errors.

2.2.1. Time Delay Unit Design Options

As the name suggests, a time delay unit controls the amount of time that a signal takes to pass through the unit by either forcing the signal to take a shorter or longer path or by increasing or decreasing the phase velocity over a fixed distance.

Time delay units have been implemented using varying technologies such as ferroelectric materials, photonics and liquid crystals. However the emerging technology of microelectromechanical systems (MEMS) has opened up the option of low-loss and low-cost phase shifters, including TDUs [20]. This represents both the opportunity and the challenge to bring electronic array scanning to a mass market. Broadly, TDUs fall into 2 categories: switched line and distributed MEMS transmission line (DMTL), with RF MEMS switched line phase shifters demonstrating solid performance up to 40 GHz and DMTL variants reported up to 110 GHz.[20]

Among available implementations, switched-line TDUs are the most promising for low-cost designs because they (i) deliver true time delay over wide bandwidths, (ii) scale to long delays with straightforward layout, and (iii) avoid the high switch counts and dispersion typical of DMTLs. Detailed comparisons follow in the next subsection.

2.2.1.1. DMTL, also called Loaded line

Distributed phase shifters work on the principle of dispersion. Consider a simple model for a transmission line.

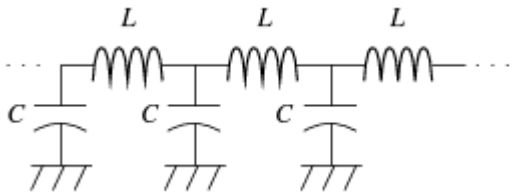


Figure 7. Lumped circuit model for transmission line.

The delay offered by such a circuit is

$$\tau = N\sqrt{LC}\,, \tag{2.4}$$

where N is the number of LC Pi network elements. Obviously by controlling C the time delay can be controlled. In this design, RF MEMS switches are used to switch shunt capacitance in and out of circuit. See Barker and Rebeiz [21]. Nagra and York [22] used varactor diodes to load a line.

In reality, a circuit looks like this:

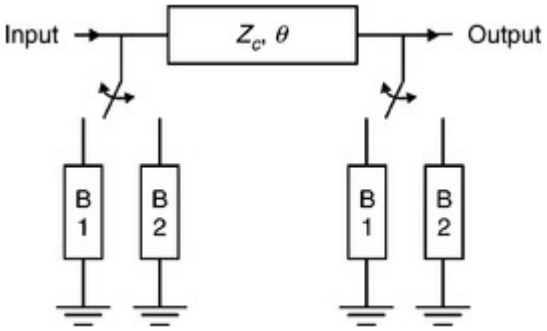


Figure 8. Loaded-line phase shifter section.

The theory of loaded lines can be found in Atwater [23].

From published reports [24], it seems that typically 8 RF MEMS switches are required to provide for a 90° phase shift. This can be an impediment if a significant delay is required. DMTL designs tend to occupy less space than switched line designs however the number of switches required to meet the design specifications tends to make the DMTL option unattractive for large time delays.

2.2.1.2. Reflection-type

Beyond canonical loaded-line DMTLs, reflection-type time-delay units, implemented with a 90° hybrid and tunable reactive loads, offer an alternative approach (Figure 9). A reflection-

type phase shifter uses a 90° hybrid coupler and varying reactive loads on ports 2 and 3 to produce a time delay / phase change on port 4.

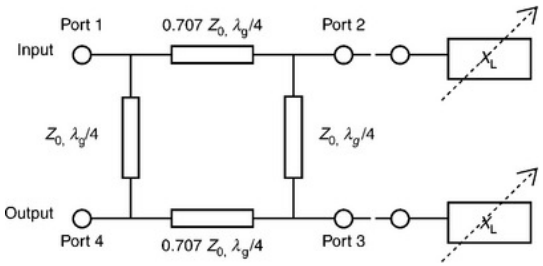


Figure 9. Reflection-type phase shifter section.

There are a number of methods to vary the loads and Wu et al. [25] give a good overview of the options. One example of an implementation is shown in Figure 10 [26]. Here RF MEMS switches are used to switch in and out capacitive loads for the 22° and 45° bits and RF MEMS switches are also used to short out the transmission line behind the coupler on ports 2 and 3. The shorting causes the signal to be reflected back through the coupler. This design has the advantage that the transmission lines can be shorter as the signal travels up and back however the design is somewhat bandwidth constrained by the passband of the coupler. To meet the specifications of this research work, there would need to be 3 of these units in series in order to achieve the required delay.

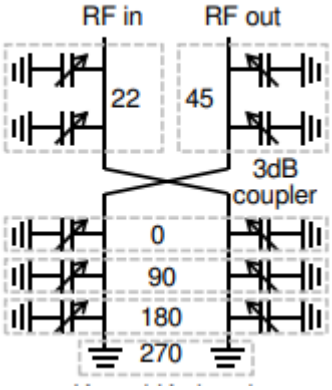


Figure 10. Hybrid reflection time delay unit.

This technique also has the disadvantage of requiring space for a hybrid coupler but this can be reduced as shown in the paper by Karmaker [27] and reproduced here.

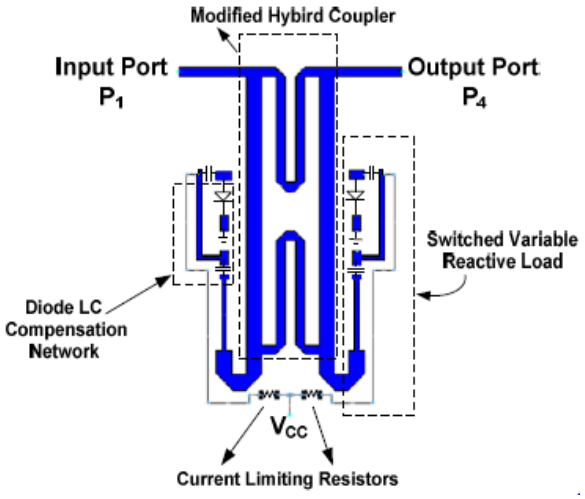


Figure 11. Reduced size hybrid coupler.

There is not much to recommend a reflection-type phase shifter for this application over and above the switched-line option.

2.2.1.3. Switched-line Time Delay

Conceptually this is a very simple design, simply switching lines of different lengths in and out of the transmission path in order to achieve the desired time delay.

For example, speaking in terms of phase, although this is a true time delay unit, a 3-bit switched-line phase shifter will have one 180° path, a 90° path and a 45° path. These 3 options can be combined in 8 different ways to achieve 0° to 315° of phase shift in 45° increments.

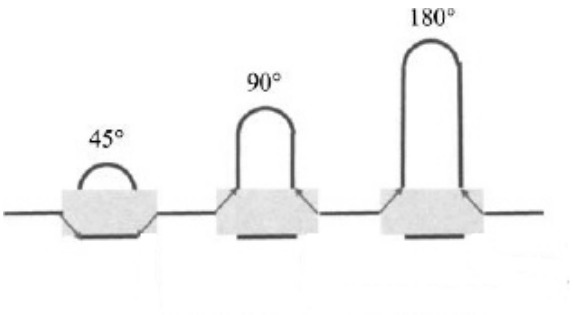


Figure 12. Switched line phase shifter.

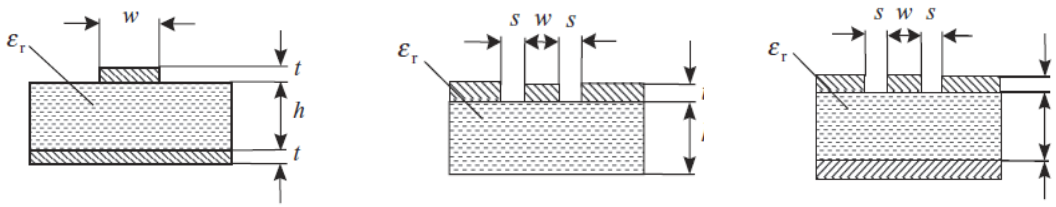
Note that 6 switches are required to achieve all the 8 combinations. A 4-bit switched line phase shifter will require 8 switches. These switches can be as simple as PIN diodes, RF MEMS switches or MMICs (monolithic microwave integrated circuit).

The switched-line delay unit is an attractive design for a TDU as it is easy to design, is a true time delay option, can deliver long delay values, has relatively favourable insertion loss and is stable over temperature. The major downside is the size. Assuming a microwave Rogers

Duroid substrate with a relative dielectric constant of 2.2, a delay of 400 ps requires a total line length of 80 mm.

An important consideration in the design of a switched line TDU is signal loss in the transmission line. It is important that the signal level is relatively constant across the band of operation such that switching between different delays doesn't incur any significant loss differential between delay lines and also that the circuit is stable as different line lengths are switched in and out. Any signal level changes could impact the array pattern.

The transmission line can be any transmission line, including co-axial cable. Common transmission lines for PCB and integrated TDUs are microstrip as the simplest to build however the losses may be too much necessitating a coplanar waveguide (CPW) structure with or without a bottom ground plane. Below in Figure 13 is the cross section of these 3 common transmission lines [28].



(a) (b) (c)

Figure 13. Cross section of three transmission structures (a) microstrip (b) coplanar waveguide (c) Conductor backed coplanar waveguide.

A switched-line phase shifter requires a number of RF switches and these typically set the limitations of the phase shifter parameters such as maximum power, insertion loss and switching time.

For example, a general-purpose RF MOS switch from Infineon (BGS12S3N6) has an operating range from 50MHz to 6 GHz, maximum input power level of 30 dBm, insertion loss of 0.7 dB at 6 GHz, return loss of 16 dB and a switching time of 0.5 µs.

For a 3-bit shifter, this would require 6 switches in series so a typical insertion loss of about 4.2 dB plus some transmission losses for a total loss of around 5 dB.

2.2.2. Control Bits and Quantisation Errors

Digitally controlled TDUs are constrained to a finite number of discrete delay states, $(2^b - 1)$, where b is the number of control bits. This limitation introduces quantisation errors when the desired continuous delay cannot be exactly realised, forcing the system to approximate it with the nearest available setting. These errors lead to deviations in the intended phase progression across the array, which in turn cause distortions in the radiation

pattern. Specifically, quantisation errors result in increased sidelobe levels, reducing beamforming efficiency and introduce pointing errors, i.e., shifting the main beam away from its intended direction.

Miller [29] in 1964 was the first to publish a detailed analysis of the adverse effects of using phase shifters with discrete phase states, all assuming a maximum phase shift of 360°.

He derived an expression for the pointing error, normalised to the array beamwidth, given by

$$\delta = \frac{\pi}{4.2^N}. \tag{2.5}$$

Other authors have also derived approximations for the pointing error [30]. Taking equation (2.3), multiplying both the top and bottom of the division inside the brackets by N, being the number of elements in the linear array and set d to be half a wavelength, plus set the full phase shift across the full linear array to be the phase equal to LSB, then the resolution bandwidth θ_{Res} becomes

$$\theta_{\mathrm{Res}} \propto \sin^{-1}\left(\frac{\phi_{LSB}}{N\pi}\right). \tag{2.6}$$

Plotting this equation gives Figure 14. Comparing the results of equations (2.5) and (2.6), the approximation in equation (2.6) gives results that are about 5% larger than Miller's equation except when the array is only 2 antenna elements, then the approximation is 13% smaller than Miller.

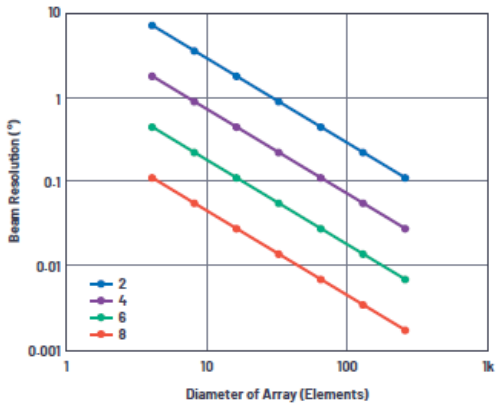


Figure 14. Beam angle resolution vs array size N for phase shifter resolution of 2 to 8 bits [30].

The reader might wonder why for equation (2.6) the phase shift across the array is set to be the phase shift of the LSB. A plot best explains the reason. With reference to Figure 15, assuming a 2-bit phase shifter, then the LSB is equal to a phase shift of 90° and this becomes the maximum phase shift across the array for the purposes of calculating the greatest beam

pointing error. The ideal phase shift for each element in a 30-element array is shown in purple as a gradually increasing value for each antenna element. As shown, the phase shifters will be set to zero for the first 15 elements and then be set to 90° for the last 15 elements. This gives rise to the sawtooth error waveform shown as blue and represents the greatest errors. Hence, the phase equal to the LSB is used as the phase change across the array.

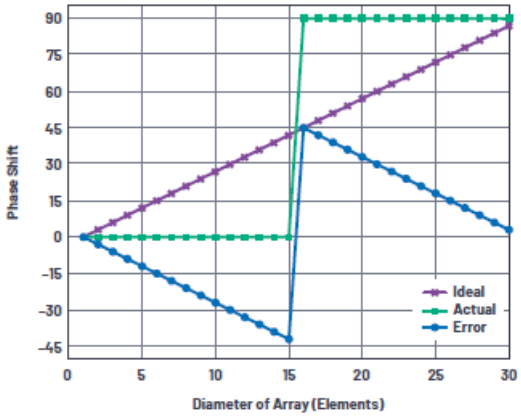


Figure 15. Element phase shift and error across array [30].

Note, this formula does assume a 2π full range phase shift and a ϕ_{LSB} equal to $\frac{2\pi}{2^b}$.

This formula can be made more general to accommodate designs with different maximum phase shifts, as in the case of this research work with a TDU maximum delay of 413 ps, equivalent to 892° of phase shift at 6 GHz. Considering the top line of equation (2.6) the maximum phase error that exist along the length of the array is from a phase equivalent to - LSB/2 at one end and LSB/2 at the other end. However, as these phase errors cause the beam to swing left and right about the centre, as such, the maximum beam pointing error is with a phase equal to LSB/2. This gives a generic beam pointing error formula

$$\theta_{error} = \sin^{-1}\left(\frac{\phi_{LSB}}{2\pi N}\right). \tag{2.7}$$

Given that a 2-bit phase shifter can achieve a pointing error of only 3.5° (using equation(2.6)) for an 8-element array, with the main lobe having a beamwidth of 12.8°, why use any more than 2-bits? The answer is sidelobes. The discrete phase values have a major impact on sidelobes.

The quantised phase values on each array element results in discrete phase shifts between elements rather than an ideal continuous phase shift and this gives rise to amplitude errors in the far-field pattern.

Figure 16 shows the increase in sidelobe levels with 2-bit phase shifters for the 30-element antenna array on boresight (green plot) and then scanned slightly off boresight (blue plot) by the resolution beamwidth, θ_{Res} (i.e., 0.95°). The sidelobes have degraded by at least 20 dB.

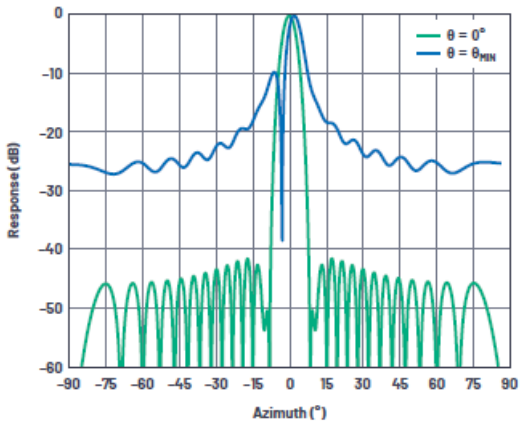


Figure 16. Antenna pattern with quantisation sidelobes [30].

The maximum quantisation sidelobe level (QSLL) is proportional to the maximum quantisation error and this occurs at certain scan angles when individual elements in the array have phase errors nearly equal to the phase equal to LSB/2. Consider the case in Figure 15, the maximum error is nearly 45°, being equal to the phase equal to LSB/2. However, if the number of bits was increased to 3, the phase equivalent to LSB/2 would be 22.5°, improving the QSLL.

Figure 17 shows the worst case QSSL for a 100-element array, using a Hamming weighting profile to keep the classic windowing sidelobes from covering the quantisation sidelobes.

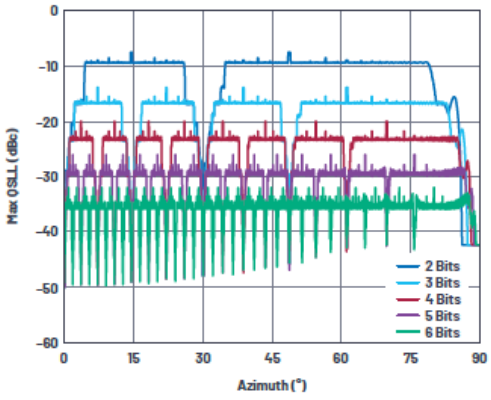


Figure 17. Worst case quantisation sidelobes vs scan angle for phase shifter resolutions of 2 to 6 bits [30].

A pattern is clearly discernible. The worst case QSLL is evident for each quantisation choice along with a “shelf” of typical QSLL and times of minimum QSLL at -50 dB. A 6 dB improvement is evident for each increase in the number of control bits for the phase shifters. The worst case QSLL with 2-bits is -7.5 dB.

The scan angle for the worst QSLL is given by the equation

$$\theta_{MaxQSLL} = \sin^{-1}\left(\frac{\pm m}{2^b}\right)$$
$$m = 1,3,5,....,2^n - 1 \quad , \tag{2.8}$$

where b is the number of control bits. In summary, the QSLL is as per Figure 18 which depicts the worst case QSLL for different numbers of phase shifter control bits. Consequently, the required number of TDU control bits is set by the maximum acceptable QSLL rather than pointing accuracy, since QSLL is the more sensitive design metric.

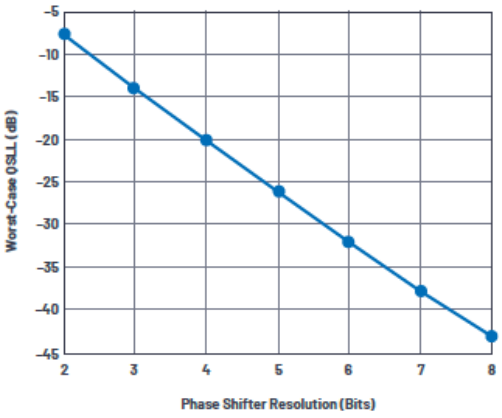


Figure 18. Worst case quantisation sidelobe levels vs phase shifter resolution [30].

Miller also considered the problem of quantisation sidelobes and was the first to determine the 6 dB improvement in QSLL with each additional phase shifter control bit. However, Miller only considered an infinite array. He proposed the formula for the maximum QSLL to be

$$P(dB) = -6N \, , \tag{2.9}$$

where N is the number of bits for a N-bit phase shifter.

Subsequent researchers such as Mailloux [31] refined Miller's work to account for finite arrays, however much of the research talks in terms of average sidelobe levels rather than peak sidelobe levels which isn't really helpful when considering a system design that should work under all scenarios of QSLL. Hence, the preceding calculation of the maximum QSLL was considered in this design specification.

2.3. Array Feeder Network

This section summarises the state-of-the-art for beamforming networks (BFN), also called feed architectures and feeder networks. The BFN provides the necessary amplitudes and phases to each of the radiating elements to produce the desired beam or beams [32]. Note that a BFN can be used for either a single beam or with multiple beams with multiple transceivers.

Mailloux [33] describes two feeds: a) constrained feeds as a combination of power splitters and phase shifters and b) multibeam feeds such the Butler matrix, Blass matrix and Rotman Lens. The term constrained feeds denotes that the feeds are constrained in some way and only offer a limited scan. DuFort [34] used the term in an early paper in 1978 where he proposed fewer active elements in order to reduce cost and complexity of phased arrays. (Just proves how the quest to simplify and reduce cost is perennial.)

2.4. Constrained Feeds

Considering the constrained feeds, Mailloux describes a parallel and series topologies (Figure 19); the parallel feed is also known as a corporate feed.

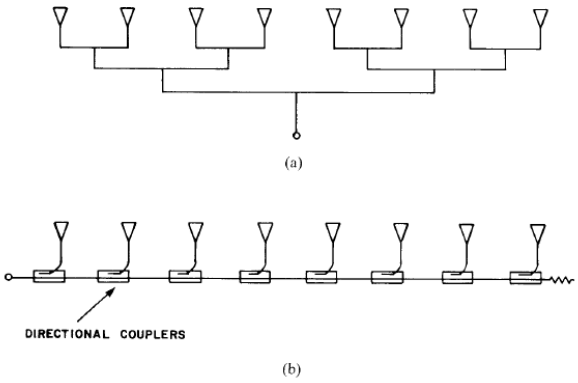


Figure 19. (a) parallel (equal line length) corporate feed and (b) series fed array.

Despite sustained interest in phased and timed arrays, recent innovation in constrained feeds appears limited. For example, Obukhovets' 2019 review [16] only flags one new feeder concept for feeders, a technique called CORPS - coherently radiating periodic structures. Betancourt and del Rio Bocio introduced the concept in their 2007 paper [35]. They called their new feeder methodology C-BFN, short for CORPS Beamforming network.

Figure 20 shows the general structure for a planar C-BFN of two layers. The design includes the alternative iteration of split (S) and recombination (R) nodes. The S-nodes are equal power splitters with equal phase change on both outputs and the R-nodes combine the 2 input signals, taking into account any phase difference between the 2 inputs.

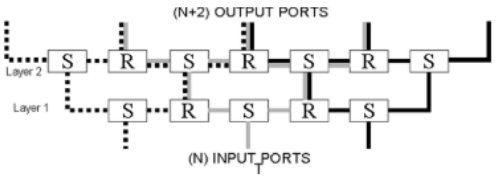


Figure 20. C-BFN of two layers.

The structure can be expanded to any number of layers and in 3 dimensions for operation with a planar array. The design has the attraction that a single phase shifter on one input can control the phase slope across a linear array aperture and only 4 phase shifters are required to steer a beam with any N x N antenna array.

In their paper, the authors construct a C-BFN feeding a 3x3 array at 2.9 GHz fed by 4 inputs and a single phase shifter. They selected a Gysel cell as the S and R nodes, shown in Figure 21. The Gysel cell is a 3λ/2 ring impedance transformer such that a signal entering port 1 is divided equally between ports 2 and 3 leaving ports 4 and 5 isolated. Ports 4 and 5 are terminated. As a R-node, signals entering ports 2 and 3 are combined on port 1. However, depending on the relative amplitudes and phases of the 2 input signals, losses will appear as the loads on ports 4 and 5 required for matching will be different from the resistive loads.

Obviously, the bandwidth is set by the performance of the Gysel cell, in this case the authors achieved a bandwidth from 2.8 to 3 GHz. They achieved scan angles of up to 10° and conclude that "in general terms, behaviour of C-BFN Systems agrees with proposed theory concepts."

However, there are obvious compromises with the design. Considering this research work with an eight-element linear array, a C-BFN design requires 6 layers and a quick calculation of the amplitude and phase distribution across the array shows a deviation from ideal. (The amplitude distribution closely resembles a Gaussian function after taking into account losses in the R-nodes.) This is evident in the published results of the performance of the array with raised sidelobes and a distorted beam. Further, the feeder is not efficient as power is lost in the resistive terminations on ports 4 and 5 of the Gysel cell as the frequency deviates from centre.

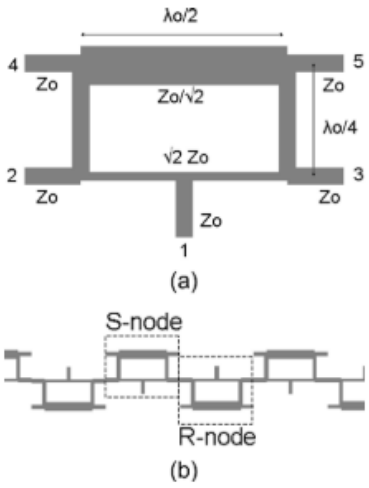


Figure 21. Gysel cell.

A formal study of the performance of the C-BFN was undertaken by Ferrando and Fonseca in 2011 [36]. They noted:

- The feeder losses with 6 layers is 1.5 dB rising to 2dB for 20 layers, plus insertion losses, for a single beam on boresight.
- Because of the Gaussian amplitude distribution, the sidelobe levels are better than those with a uniform amplitude distribution at -20 dB for 6 layers. There is a corresponding broadening of the beamwidth. (single beam on boresight)
- With a single phase shifter, the losses increase with the phase shift, rising to 2.5 dB with 6 layers and a 90° shift. (4.7 dB loss with 20 layers)
- The phase distribution across the antenna arrays quickly goes nonlinear with an increasing phase shift on a single phase shifter design. The authors note that it is the array elements at the edge that experience the greatest deviation from a linear value but that the impact is lessened because of the amplitude distribution. However, they conclude that the maximum phase shift is only 90°, after which "beam steering capability is lost". For the research work the subject of this thesis, a single phase shifter value of 90° would equate to a maximum scan angle of 4.3°, not very practical.
- The scan angle can be improved by increasing the number of phase shifters; however, their recommendation is for 11 phase shifters for a 6-element array. This seems excessive given only 6 phase shifters would be required for a traditional corporate feed.
- The authors conclude that the "C-BFN will most likely be used in association with reflectors to compensate for the naturally low gain of this structure in association with a linear array."

Several alternative constrained feeder arrangements have been proposed in recent years, including a MEMS differential delay shifter and a compact tree-based true-time-delay BFN; representative designs are summarised below.

2.4.1. MEMS Differential Delay Shifter

The manufacturer of RF MEMS switches, Menlo Micro, in Nov 2020 proposed a differential delay shifter design utilising their RF MEMS switches, shown below in Figure 22. This is a true time delay design and is an efficient use of space as a single switched delay line is used for 2 array elements [37].

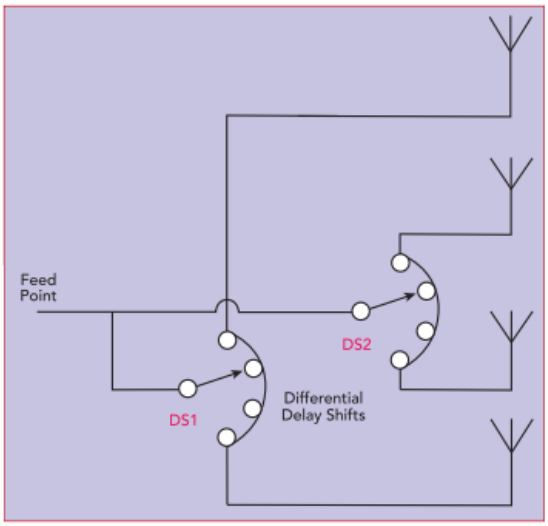


Figure 22. Two differential delay shifters.

2.4.2. Novel Tree-Based BFN

In their 2020 paper, Lialios et al [38] proposed a simple tree topology based on microwave photonics.

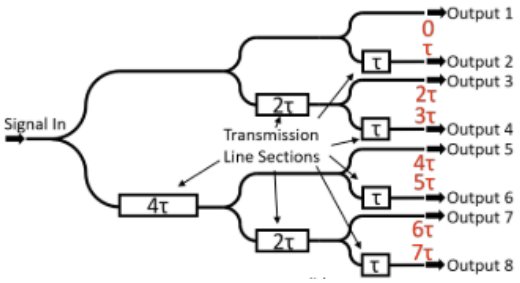


Figure 23. Hierarchical true time delay tree beamformer.

The concept is simple enough. The novelty is the minimal use of delay units, arranged in a hierarchical structure in the common branches instead of in each small branch as with a corporate feed. This makes the design significantly more compact than a corporate feed. In this paper the delay units are fixed but there is no reason they couldn't be variable.

The paper reports a prototype with unequal power dividers using a Chebyshev power distribution achieving a sidelobe level down 21 dB. (The unequal power dividers use a technique proposed by Qi et al in 2016 [39].)

The authors achieve an operational bandwidth of 15 GHz to 45 GHz.

2.4.3. PhD Dissertations

In his 2011 PhD dissertation, Ehyaie proposed an interesting alternative design for a phased array feeder [40].

The design is shown here in Figure 24

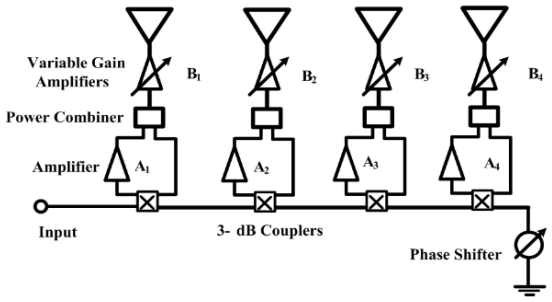


Figure 24. Single phase shifter and series fed array.

The design is for a series fed array with a single phase shifter at the end of the transmission line. Energy passes along the line from the input, through the phase shifter and is reflected back along the line such that the input to each antenna element is the vector sum of the forward and reflected signals.

While this may be novel, it does require active components to get levels correct and is not a strong candidate for this research work. DuFort proposed a very similar design in 1978 with a variable phase shifter at the end of the transmission line so the basic design has been around for 47 years at least [34].

Ehyaie also proposed a variation on a bidirectional feed arrangement. See Figure 25. This is attractive as it significantly reduces the range required for each of the series phase shifters, however it is lossy as some energy is lost in the termination required at the end of the transmission line and is not a strong candidate for this research work.

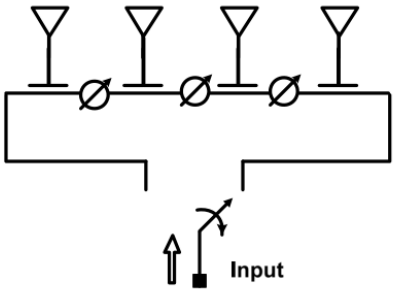


Figure 25. Bi-directional series-fed phased array.

2.4.4. Patents

There are a couple of patents that propose designs for remote beam tilts on cellular antennas that are relevant to this research work. A representative patent is US 10,211,529 B2, (Feb 2019) Phased Array Antenna System with Electrical Tilt Control [41].

It is arguable whether it includes any novel design features as it appears to be a slight variation on a corporate feed, however it is reproduced here as indicative of the state-of-the-art.

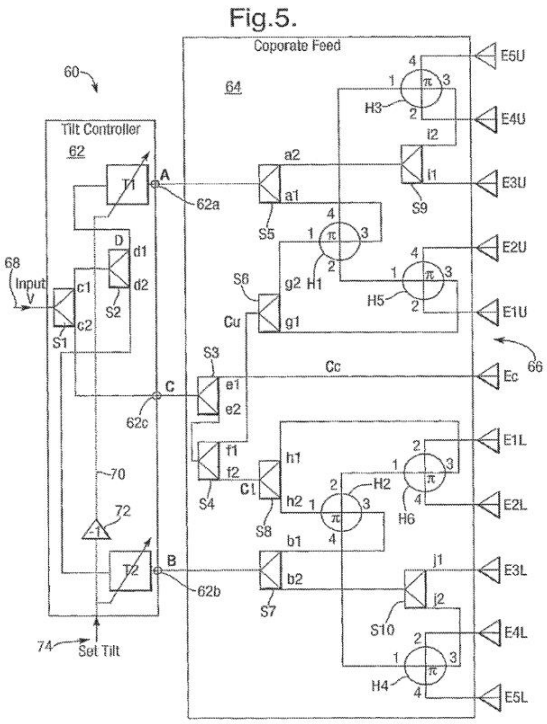


Figure 26. Beam tilt control patent.

This design is composed of a tilt controller and a corporate feed. Items denoted as “S” are splitters, i.e., power dividers and items denoted as “H” are 90° hybrids. Note that only two time delay units are required however a large number of splitters and hybrids are required and as such these would require considerable space and would be bandwidth limited for this research work’s application.

2.5. Multibeam Feeds Review

Multi-beam feeds for phased arrays enable simultaneous beamforming in multiple directions, enhancing spatial coverage and system efficiency in radar, satellite communications and advanced wireless networks. These feed networks distribute signals to phased array elements in a controlled manner, generating independent beams without requiring multiple active beamforming channels.

2.5.1. Butler Matrix

The Butler matrix was invented in 1961 by J. Butler and R. Lowe and is in effect a hardware version of the FFT (Fast Fourier Transform) in that it resolves received signals into angular space.

Butler matrices consist of a number of 90° hybrid couplers and fixed phase delays and have N input ports and N output ports such that $N = 2^m$ with $m = 1,2,3.....$

For an N x N Butler matrix, a total of $\log_2 N$ phase shifters are required.

Butler matrices are reciprocal in that they can operate in either direction, i.e., from the transmitter(s) to the antenna array or from the antenna array to the receiver(s).

In transmit mode the output ports are connected to a linear antenna array and the combination of Butler matrix and the antenna array generates a fixed radiation pattern with N beams all within a defined arc, set by the antenna spacing. The maximum defined arc is 180^0. Each individual beam can be accessed by feeding into the corresponding input port. So, by switching the output of a transmitter between the input ports of a Butler matrix, the output signal from the array will appear on one of the fixed beams and so appear to be moving.

In reverse, when the array is receiving signals, energy arriving on a beam will appear on the corresponding output port (which is an input port for transmit). Hence the FFT functionality, arriving signals are resolved automatically into an angle of arrival. Therefore, a full scan of an arc can happen near instantaneously with receivers listening on each receive port.

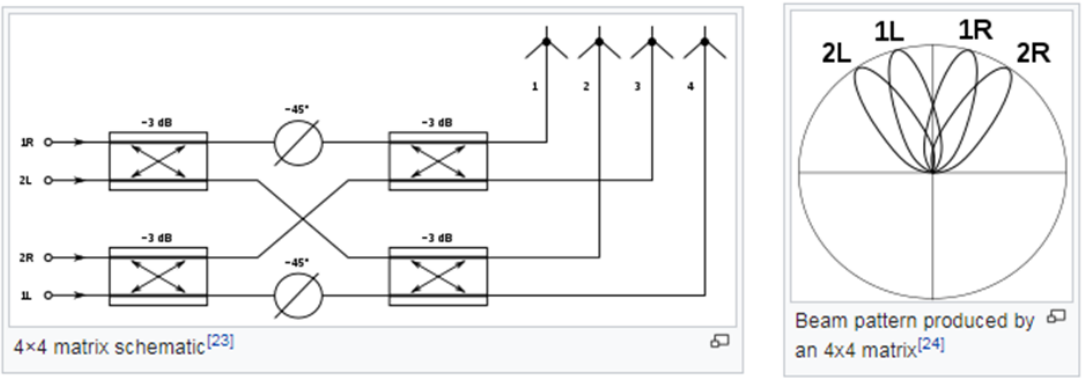


Figure 27. 4x4 Butler Matrix – Wikipedia.

This functionality of keeping a fixed radiation pattern and switching the feed to different beams is an area of current research and is often called beamspace MIMO using switching or lens antennas.

The Butler matrix is a popular feed arrangement for a phased array and there are many examples in the literature. For example, Zhang et al [42] report a 4 beam antenna array of 16 elements with fixed beams at ±7° and ±21°, covering the band 2.4 to 2.8 GHz.

However, there are limitations with the standard Butler matrix that make it unsuitable for some applications. The standard design produces beams that are symmetrical with respect to

the broadside axis leading to a shadowed area [43]. This means there is a beam in the wanted direction and another shadow lobe in an unwanted direction meaning that as a receiver, controlling the beams to avoid interfering signals is impossible to guarantee. Further, a full 360^{o} scanning arc is not possible with a standard Butler matrix.

The Butler matrix also produces a uniform amplitude distribution across the antenna array leading to high sidelobe levels and the high number of crossovers (where signals must crossover each other) leads to increased insertion loss [44].

For application requiring ultra-wideband operation, the Butler matrix is bandwidth limited and is not true time delay. A recent design achieved a bandwidth of 3:1 (based on a 10 dB return loss) with 1 dB insertion loss variation and 7° phase deviation. See Chen et al [45].

This is not to say that an alternative design variation couldn't be developed to overcome these limitations, more investigation needs to be done in this area. However, it should be recognised that a Butler matrix takes up a lot of space in comparison with individual phase shifters and as such there would need to be a compelling reason to use Butler matrices as the feed arrangement, such as near instantaneous scanning for example.

The instantaneous scanning is an interesting feature of a Butler matrix. When acting as a receiver, the Butler matrix gives a designer the option to use monopulse radar techniques to get instantaneous readings of a target or the bearing of a remote transmitter.

Early radar involved moving an antenna array beam to locate a target and this was called scanning and required a number of readings to determine the location of the target. This all took time. The solution was to have a number of fixed beams and to note the position of a target on all beams at the same time. If both elevation and azimuth locations are required, then at least 4 beams are required, left, right, up and down. If only azimuth location is required, then only 2 beams are required. By adding and subtracting the signal level from all 4 beams, the location of the target in relation to the antenna beams can be ascertained with one measurement, one pulse, hence the name monopulse.

2.5.2. Blass Matrix

The Blass matrix was invented in 1960 and is shown here in Figure 28 [46]. It consists of a matrix of transmission line sections and multiple directional couplers. The phase shift is realised through the line length. The figure shows 3 beams with 4 antenna elements. The transmission line sections have equal lengths and radiate out from a centre point. The circumferential lines leading to the antenna have different lengths with the same circle centre as the radial transmission lines. All lines are terminated with their characteristic impedance at

the end. Looking at each beam transmission line, it is evident that there is a phase shift across the face of the antenna array that gives rise to the beam forming properties of the Blass matrix. The coupling factor of each coupler can be varied to provide a non-uniform amplitude distribution across the array face [32].

The Blass matrix has the advantage that it can be designed as a true time delay network and can provide non-uniform amplitudes, leading to lower sidelobes, thus overcoming some of the short comings of the Butler matrix.

However, Blass matrices tend to be large and inefficient as energy is lost in the matched terminations. Their bandwidth can be limited as well.

A true time delay active Blass matrix with an instantaneous bandwidth of 5:1 has been reported [47].

Alternative designs have been developed including a space saving circular design built with transmission lines on two levels where the authors claim a 60% reduction in size [38].

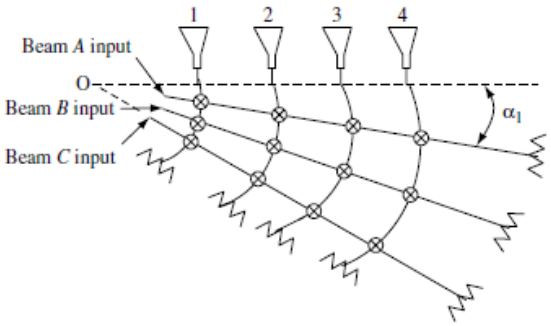


Figure 28. Blass Matrix.

2.5.3. Rotman Lens

The Rotman lens was invented in 1963 [48]. It is called a lens as it functions on the principles of geometrical optics, much like an optical lens. In this case, a microwave lens. The schematic of a 2D Rotman lens is shown in Figure 29. The figure shows a cavity with a number of beam ports on one side and a number of array ports on the other side. To understand the operation, consider a single signal source into a single beam port in transmit mode. Each array port will receive a portion of the signal from the single beam port with a phase proportional to the length of the path from the beam port to each array port. If the array port surface is designed such that the distance from a beam port to each array port is a linear, then a beam is formed and using the individual beam ports means a scanning beam can be formed [32].

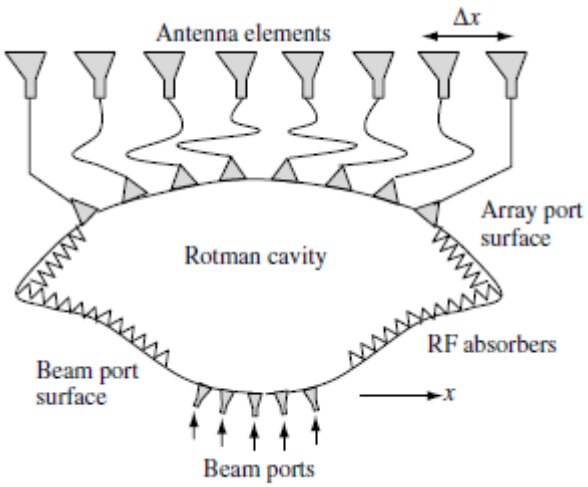


Figure 29. Rotman Lens.

Rotman lenses have the advantage of being a true time delay network with a low number of switching elements and they can achieve relatively wide bandwidths, up to 10:1 [49]. They are also low cost, reliable and relatively easy to design with wide scanning angles, up to 360° has been reported [50]. However, they are large in size and relatively inefficient as significant power is lost in the RF absorber, or dummy ports, away from the array surface. Efficiency of just 20-50% [49].

The reason for the large size is that the Rotman lens is a travelling wave structure and it needs to be several wavelengths in size to perform properly.

Vashist et al provide a recent review of the development of the Rotman lens [50].

2.5.4. GJC Matrix

The Generalised Joined Coupler (GJC) matrix was first proposed in 2022 [51] as an advanced beamforming network architecture that unifies and extends traditional designs like the Blass and Nolen matrices. It offers enhanced flexibility and performance in multibeam antenna systems.

As has been discussed, the Butler matrix is based on the hybrid coupler and is best suited to giving fixed coverage with fixed beams such as for cellular base stations. On the other hand, Blass matrices and Nolen matrices employ directional couplers and phase shifters without crossovers and produce flexible multibeams. The design for a Blass or Nolen matrix requires determining the parameters of the joined couplers. The GJC matrix introduces a universal optimisation algorithm and the mathematical tools for synthesising such matrices as the Blass matrix, the Nolen matrix and other variants.

One variant of the GJC matrix has the phase shifter associated with each matrix node placed to the right of the directional coupler instead of above it as is the case in conventional Nolen and Blass matrices. This makes it possible to realise independent individual beam scanning.

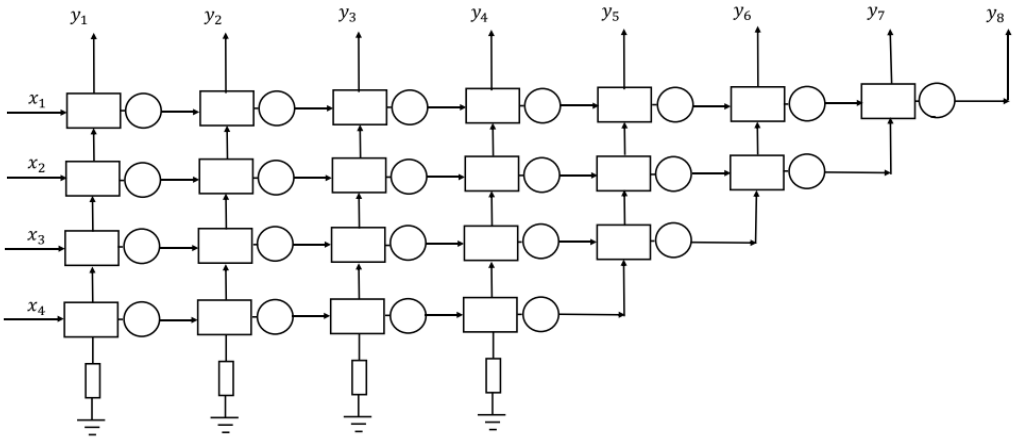


Figure 30. Illustration of a 4 x 8 Nolen-like GJC matrix.

Key Features:

- Unified framework: The GJC matrix encapsulates both Blass and Nolen matrices, providing a comprehensive approach to multibeam synthesis.
- Independent beam control**:** Each row of the GJC matrix is associated with a set of phase shifters, allowing for independent adjustment of beam directions. This facilitates simultaneous and independent beam steering for multiple beams.
- Design flexibility: The GJC matrix can be implemented using planar circuits, enabling compact and efficient designs suitable for various applications.

Advantages:

- Customizable beam directions: The GJC matrix allows for the generation of multiple beams with customizable directions, which is crucial for applications requiring precise beam steering.
- Low sidelobe levels**:** By adjusting the phase shifters, the GJC matrix can achieve low sidelobe levels, enhancing signal quality and reducing interference.
- Compact design: The planar implementation of the GJC matrix results in a compact design, making it suitable for applications with space constraints.

Subsequent publications have provided experimental validation of the GJC matrix using both microstrip and stripline technologies, demonstrating its suitability for next-generation communication systems, particularly in beyond 5G, 6G and satellite-terrestrial networks [52]. In summary, the GJC matrix claims a significant advancement in beamforming network design, offering enhanced flexibility, performance and compactness for multibeam antenna applications.

2.6. Subarrays and Hybrid Antenna Arrays

Along with increasing signal bandwidths, there is also demand for increasing the number of signal streams feeding one antenna array, thus forming multiple beams and spatial streams.

In the field of massive MIMO (multiple-input and multiple-output), or large-scale antenna systems (LSAS), researchers often speak in terms of hundreds of antennas, up to 400 in the simulations although operational arrays have fewer antennas for practical reasons. Sprint USA has reported using antenna arrays with 128 antennas in their mobile phone networks. There are research reports of experimental arrays of up to 256 antennas at 3.5 GHz and 6 GHz, [53] and 32 antennas at 28GHz, [54] and published plans to build an array of 256 antennas at millimetre wave [55].

These reports all highlight the practical considerations of massive arrays, namely physical space requirements, power consumption, cost and data sampling rates.

In the simplest case, for an array with N elements, the number of required phase shifters is also N. This is the baseline analogue beamforming architecture, where each antenna element receives an individually adjusted phase shift, providing maximum beamforming flexibility but also requiring the largest number of phase shifters.

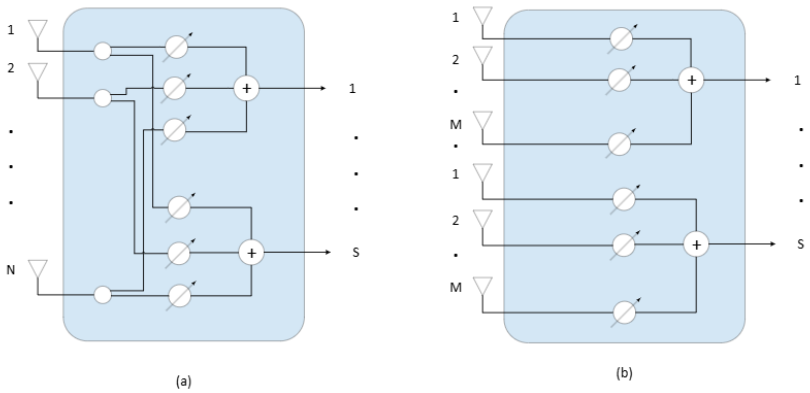


Figure 31. Analogue processing for hybrid beamforming based on phase shifters. (a) each RF chain is connected to all antennas, (b) each RF chain is connected to a subarray.

When a system must accommodate multiple simultaneous data streams, such as in multi-user MIMO or multi-beam satellite communications, the number of phase shifters expands significantly. In a fully connected beamforming architecture, where each data stream has independent phase control over every antenna element, the total number of required phase shifters N_{ps} grows to

$$N_{ps} = SN, \tag{2.10}$$

where S is the number of independent data streams. This approach provides the highest flexibility for per-user beamforming and beam tracking, but it also results in high hardware complexity, cost and power consumption.

A solution suggested by researchers is to introduce analogue subarrays, where one transceiver is connected to each subarray and the phase of each antenna in each subarray is controlled by an analogue phase shifter [56], [57], [58]. In practice, one transceiver generates one beam towards one user with the analogue phased array. Thus, the subarray acts as an analogue phased array. This arrangement reduces the total number of phase shifters required to

$$N_{ps} = SM = N, \tag{2.11}$$

where M is the number of antenna elements per subarray and $M < N$. This is a hybrid array as it is a combination of both analogue and digital beamforming. The digital beamforming is enabled in the digital domain in a traditional manner, i.e., weighting (phase and amplitude) each digital signal to form an antenna beam.

While this method significantly lowers hardware complexity, it reduces beamforming resolution, since all elements within a subarray receive the same phase shift and cannot be controlled independently.

The question of optimal joint digital and analogue beamforming is an active area of research.

A more sophisticated alternative is multilevel phase distribution, or hierarchical beamforming, where multiple layers of phase shifters distribute phase shifts progressively across the array. Instead of a single phase shift controlling each subarray, lower-level phase shifters apply coarse phase adjustments, which are then refined at higher hierarchical levels. This allows for precise beamforming while still reducing the number of phase shifters. The number of phase shifters in a multilevel architecture is given by

$$N_{PS} = S\left(\frac{N}{M_1} + \frac{N}{M_2} + ... + \frac{N}{M_L} \right), \quad (2.12)$$

where L is the number of hierarchical levels and each layer progressively refines the phase shift and M_L is the size of the subarray on layer L.

Note for the most part, true digital beamforming does not require any phase shifters as all the beam steering is done in the digital domain. In hybrid designs, beamforming is a combination of digital and analogue techniques.

2.6.1. RF Chain

The design of the RF chain involves a few options:

- Whether to apply the phase shift at RF or IF and
- Whether or not to include active components with each antenna. That is, whether to combine signals before or after amplification.

Figure 32 shows the broad alternatives.

(a) In this option, there is just a phase shifter per antenna and then all antennas in a subarray are combined before the LNA, or PA in the case of the transmitter. This arrangement is often called corporate power combining / splitting and the array can be called a passive array.

This option has the advantage of minimising the active components, hence a cost and power saving, however the phase shifter adds to the loss at the front end and will degrade the link budget. Similarly with the transmitter, the phase shifter has loss and will degrade the transmit power.

Phase shifters may also introduce non-linearities and errors due to a finite number of phase shift values.

(b) To overcome the short comings of option (a), this option includes an LNA per antenna to overcome the loss of the phase shifter. Both these options perform the phase shift at RF. This per-element amplification constitutes an ‘active array’.

(c) This option introduces the phase shift at IF. This may be more practical as phase shifters are more readily available and easier to design at lower frequencies compared with higher RF frequencies.

However, there are many more mixers that can introduce additional I/Q mismatches and there is a requirement to route numerous LO feeds around the array which can be a routing problem.

(d) This option is much the same as (c) except the phase of the LO is adjusted rather than directly shifting the phase of the IF. Of course, shifting the LO phase causes a phase shift in the IF. This has the advantage of taking the phase shifter out of the signal path and minimising its impact on the system SNR, however it has the same issue of routing numerous LO feeds around the array and maintaining a constant phase throughout.

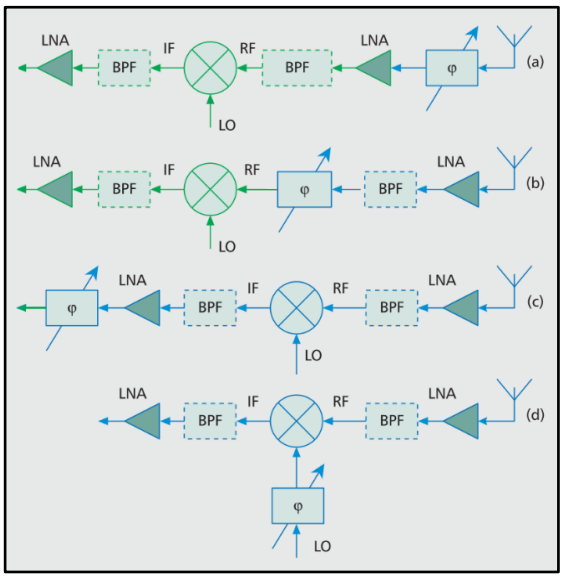


Figure 32. Block diagrams of RF chain alternative designs for a receive hybrid array. The phase shifter is denoted by the block φ. The band pass filters (BPF) may be required for band limiting and image rejection. Blocks in blue are connected to a single antenna and blocks in green are per subarray.

To help gauge the cost and component count of the numerous design options, Table 1 below details the component count for each option of the hybrid array listed above in Figure 32, plus the component count for a fully connected array of a similar RF chain design. There is also an indicative cost per array based on the costings for an experimental hybrid array with N = 4 and M = 8 at 28GHz [54]. It is interesting to note how much cheaper it is to do the phase shifting at IF in the millimetre wave band.

	Subarray Design			Fully connected Design	
RF Chain option	**(a) RF Phase Shift**	**(b) RF Phase Shift**	**(c) and (d) IF Phase Shift**	**(b) RF Phase Shift**	**(c) IF Phase Shift**
RF front end	N	NM	NM	NM	NM
Phase shifter	NM	NM	NM	N^2M	N^2M
Mixer	N	N	NM	N	N^2M
ADC/DAC	N	N	N	N	N
Total cost ($)	6,368	10,876	6,684	27,196	10,620

Table 1. Component count and indicative cost for N=4 and M=8 hybrid array at 28GHz. Digital and analogue beamforming.

Beamforming refers to the generation of a narrow beam of radio energy directed in a particular direction, typically towards another receiver. It is important to note that beamforming and space diversity are two different functions.

Beamforming is all about maximising the signal power at the receiver to increase the SNR. Diversity is all about overcoming fading in the channel through space diversity (separation of antennas in space, also called antenna diversity) along with time diversity and frequency diversity to combine all multipath signals into a robust signal.

Diversity relies on the channels between the TX and RX being uncorrelated while beamforming benefits from correlation.

Beams are formed in the analogue domain by adjusting the value of all the phase shifters connected to each of the antennas and thereby altering the direction of the wavefront leaving or arriving at the array. These phase shifter values constitute an analogue beamforming vector, $\mathbf{A}$.

In the digital domain, beams are produced by weighting (amplitude and phase) each of the digital streams before they are applied to the RF chains such that they constructively and destructively add to shift the wavefront leaving or arriving at the array. The weighting values form a digital beamforming vector, $\mathbf{D}$.

The joint optimal design of $\mathbf{D}$ and $\mathbf{A}$ is an open area of research. In practice, systems often combine an analogue beamforming vector and a digital beamforming vector; the joint optimal design of the analogue and digital weights remains an open problem, particularly under constraints on RF chains, quantisation and wideband performance [59].

2.7. MEMS

Microelectromechanical systems (MEMS) is a class of device integrating electronics and mechanical elements. Some literally having moving parts. MEMS is a wide category and includes many devices such as sensors, transducers, actuators and accelerometers. However, this section is purely focused on MEMS that operate in the microwave and millimetre frequency ranges, explicitly designated as RF MEMS. RF MEMS switches promise low cost, low loss, high linearity and low power consumption.

RF MEMS technology has been in development for decades. For example, reference [60] in 1995, reported:

> "A surface micromachined miniature switch has been made on a semi-insulating GaAs substrate using a suspended silicon dioxide micro-beam as the cantilevered arm,

a platinum-to-gold electrical contact and electrostatic actuation as the switching mechanism."

However, the ready adoption of MEMS technology in RF applications has been relatively slow due to a combination of reliability concerns, packaging challenges and manufacturing limitations. In the early years, RF MEMS switches were particularly susceptible to failure mechanisms such as:

1. Contact degradation (Wear and Stiction)

   The switch contacts were prone to surface wear, oxidation and stiction (adhesion between contact surfaces) that could lead to increased contact resistance or inconsistent switching behaviour.

2. Mechanical fatigue of the cantilever beam

   The cantilever-based design experiences repeated mechanical stress as it actuates over millions of cycles, leading to buckling, fracture or becomes stiff and doesn't move.

3. Dielectric charging

   Electrostatic actuation often leads to charge accumulation in insulating layers which can cause a shift in actuation voltage, leading to a higher pull-in voltage or even actuation failure.

4. Particle contamination or surface roughness changes

   The switch contacts can suffer from particle contamination, which prevents proper contact closure. Over time, surface roughness can change, leading to higher insertion loss.

These reliability concerns were exacerbated in high-frequency applications where consistent, long-term performance was crucial [8].

Another major barrier to widespread RF MEMS adoption was packaging. Unlike conventional semiconductor devices, RF MEMS switches require hermetic packaging to protect their moving parts from environmental contaminants, such as moisture and airborne particles, which could degrade their performance over time. While early RF MEMS devices relied on complex and costly custom packaging solutions, advances in wafer-level packaging (WLP) and thin-film packaging (TFP) have significantly improved manufacturability, reducing both size and

cost while enhancing environmental resilience. These improvements have played a key role in making RF MEMS switches more commercially viable.

Beyond reliability and packaging, the cost and scalability of MEMS manufacturing also presented challenges. Unlike MMIC and CMOS switches, which benefit from well-established semiconductor fabrication infrastructure, MEMS production initially suffered from lower yields and higher costs due to the complexity of microfabrication techniques. The industry lacked standardised processes for large-scale MEMS production, further restricting their availability to niche applications, particularly in research and military settings. Over time, however, process standardisation and advancements in RF MEMS-compatible semiconductor manufacturing have significantly improved production efficiency, leading to reduced costs and increased accessibility.

Despite these early setbacks, MEMS technology has reached a stage where it is now commercially viable for specific applications. One of the key drivers behind this shift has been the growing demand for low-power, high-frequency RF switching solutions in phased arrays, 5G/6G networks and satellite communications. In these domains, RF MEMS-based RF switches provide compelling advantages over traditional semiconductor alternatives, advantages including lower insertion loss, higher isolation and superior linearity. Unlike MMIC and CMOS-based RF switches, MEMS devices also offer the ability to operate with near-zero power consumption in their static state, making them attractive for energy-efficient and high-frequency applications.

Recent breakthroughs in contact materials, structural design and fabrication techniques have further improved the long-term reliability of RF MEMS switches. Modern devices are now capable of operating for billions of switching cycles, a significant leap from their earlier limitations. Companies such as Analog Devices and Menlo Micro have capitalised on these advancements, bringing packaged RF MEMS switches to the market, thereby shifting the perception of MEMS from a laboratory-based technology to a commercially deployable solution.

While RF MEMS switches will not fully replace MMIC-based solutions, they now present an alternative for applications where low loss, high isolation, high power capability and power efficiency are critical factors. The choice between MEMS and MMIC technologies should be guided by application-specific requirements, as each offers distinct advantages depending on the use case. The advancements in MEMS over the past three decades have thus transformed

them from an experimental concept into a practical solution for wideband TDUs and other RF switching applications.

2.7.1. RF MEMS Reliability

Dey et al have published a couple of papers on MEMS reliability. They comment in 2015 [61] that all the published papers to that date that they had reviewed on the subject of RF MEMS based phase shifters with more than 4 bits did not report on reliability performance over large cycles. They sought to address this issue with an analysis of a 5-bit switched line phase shifter using four SP4T and two SPDT (single pole double throw) switches at 17 GHz.

As the authors are actually building RF MEMS switches, a lot of detail is to do with switch design and performance which is not really part of this research work, however the principles and progress are applicable to this research work.

The authors measured the performance of individual switches and then measured the complete phase shifter as a unit.

The researchers built their RF MEMS switches with short cantilever beams, DC contact (as distinct from capacitive MEMS) using electroplated gold contacts on an alumina substrate (Al_2O_3), 635 µm thick, using a surface micromachining process.

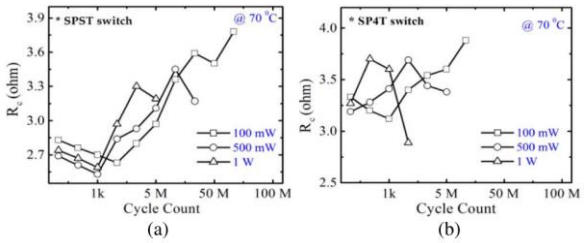


Figure 33. Reliability of (a) SPST and (b) SP4T switches for 0.1 to 1 W of RF power at 70° C and 70V activation.

Figure 33 shows the contact resistance of each switch (SP4T and SPST) vs the number of switch cycles for differing amounts of RF power at 70°C. As is evident, lower RF power increases the longevity of the switch however both switches fail after 50 million and 5 million switch cycles, respectively.

Dropping the temperature to 25° C improves reliability to greater than 10 million cycles for both switches. Thus, RF power and temperature are determinants of reliability. The researchers explain the high RF power and elevated temperature cause degradation at the contact points, leading to increased contact resistance and eventual failure. The study discusses electromigration leading to localised heating and contributing to failures. (Electromigration is the gradual movement of metal atoms in a conductor due to the momentum transfer from high-density electrical current.)

While more commonly associated with capacitive MEMS, the paper mentions dielectric charging as a failure mode in DC-contact MEMS, especially under high incident power and elevated temperature.

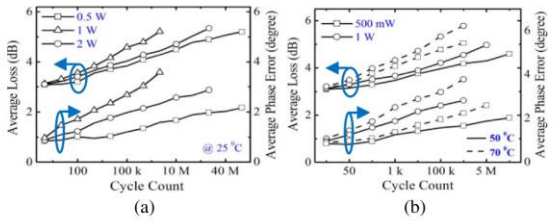


Figure 34. Reliability of phase shifter for 0.5 - 2 W of RF power and (b) at elevated temperature and 0.5 - 1 W.

When the switches are combined into the complete phase shifter, the reliability is shown in Figure 34. At 70° C and 0.5 W of RF power, the phase shifter fails after 1 million cycles. Note here that a cycle is a full cycle through all delay values so individual switches are switching many times per test cycle. In this case, the course bits switch activates 8 times and the higher bit section activates 16 times. This nonuniform switch activation is a function of the 5 control bits and will not be the case with an even number of control bits.

Figure 35 and Figure 36 show a schematic diagram and image of the 5-bit phase shifter.

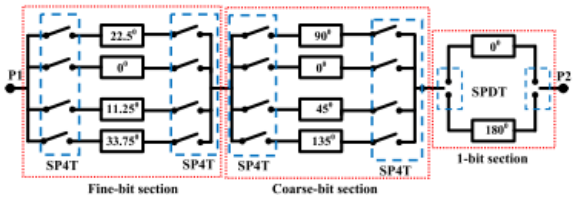


Figure 35. Schematic diagram of the 5-bit RF MEMS switched line phase shifter.

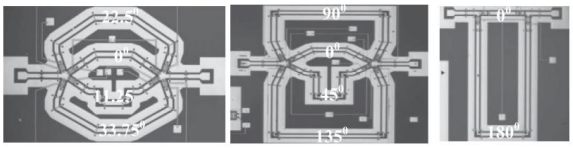


Figure 36. Microscopic images of the 5-bit phase shifter.

Three years later in 2018, Dey et al published a new paper with a revised design for the RF MEMS switch with improved switch reliability capable of more than 1 billion cycles at 85° C and 1 W of RF power [62]. Utilising these switches, Dey et al built 3 and 4-bit phase shifters capable of more than 400 million cycles at 85° C and 0.5 W of RF power. Figure 46 here shows an image of the 4-bit phase shifter using SP8T switches instead of SPST and SP4T switches as per the first design. They also changed to a DTML design rather than switched line. The

reduction in the number of switches goes a long way to explaining the improvement in the phase shifter reliability.

The switch modifications included a new robust cantilever design (a buckle-beam structure) and a new switch contact material, optimised for contact resistance, although the new material was not disclosed.

In a reliability comparison with other published papers, the authors claim superior performance for hot switching reliability as compared with 4 other researchers.

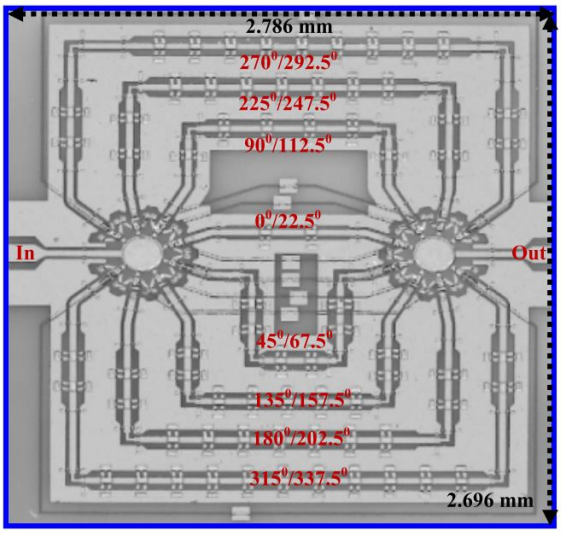


Figure 37. Microscopic image of 4-bit phase shifter.

A commercial example of a RF MEMS switch is from Analog Devices, the ADGM1004. It has an operating range of DC to 13 GHz, operating input power of 20 dBm, maximum power level of 33 dBm, insertion loss of 0.63 dB at 6 GHz, return loss of 17 dB and a switching time of 75 µs.

Analog Devices produce a chart of failures against the number of switch activations and operating power level, reproduced here in Figure 38. This shows, at 20 dBm, half of RF MEMS switches will have failed after 400,000 switches. Dropping the operating power level to 0 dBm will improve the reliability dramatically, half of RF MEMS switches will have failed after 4 billion switches.

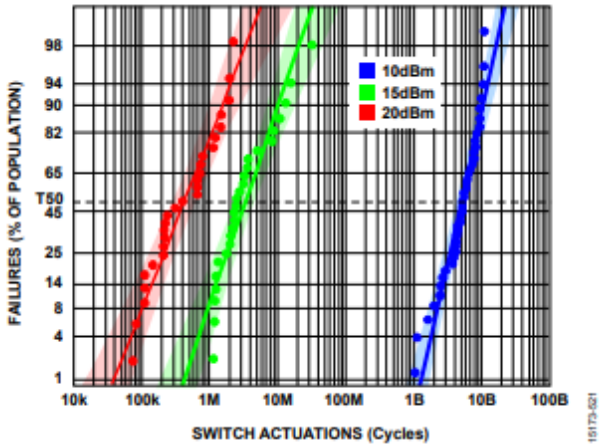


Figure 38. Hot switching probability distribution on Log Normal with 95% confidence interval.

Emerging MEMS manufacturers, such as Menlo Micro, have recently gained attention due to their advancements in packaging and reliability.

Historical supplier RadantMEMS did announce some of their reliability results. Testing at 20 dBm (100 mW) at X-band frequencies on a batch of 64 switches resulted in an 88% pass rate up to 100 billion cycles, with a median cycle-to-failure much greater than 1 trillion cycles. The longest recorded lifetimes exceeded 1.5 trillion switch cycles before the test was halted after 30 continuous months [63]. RadantMEMS has now been absorbed into Communications and Power Industries Inc.

Meno Microsystems has a RF MEMS switch (MM5140) available today that they claim is guaranteed for a minimum of 3 billion on off cycles.

2.7.2. Menlo Micro

Menlo Microsystems is a US start-up company spun out of General Electric after 16 years of MEMS development effort. They are solely focused on MEMS devices and claim to have solved the issues of reliability and durability.

They announced in May 2023 the production release of their MM5140 RF MEMS switch, with specifications as below.

This product has low insertion loss, high power handling capability and good linearity with an IP3 value of 90 dBm, integrated charge pump and SPI (Serial Peripheral Interface) controls along with reasonable port isolation. The switching is slower than a PIN diode (4-12 nanoseconds) or a silicon switch, (10 - 20 nanoseconds) however this is not a concern for this application but may be a concern if truly rapid scanning was required.

MM5140	Specification
Function	SP4T
Frequency range	DC to 8 GHz
RF Power	25 W (CW)
Insertion loss ON	0.5 dB @ 8 GHz
Isolation OFF	25 dB @ 6 GHz
Reliability	> 3 billion cycles
Price	USD$45 (100+ qty)
Package	5.2 x 4.2 mm LGA
Switching speed	<15 µs

Table 2. MM5140 specs.

Menlo Micro RF MEMS switches use an electrostatic actuation mechanism. This works by applying a voltage to create an electric field, which pulls the switch contacts together, enabling conduction. This approach offers key advantages, including extremely low power consumption and excellent isolation when in the off state. Unlike traditional RF MEMS switches that require external high-voltage biasing (e.g., 90V in early designs), Menlo Micro has integrated a low-voltage electrostatic drive making their switches practical for commercial applications. Alternative RF MEMS switch technologies include thermal actuation, which relies on Joule heating to expand or contract a microstructure to close the switch. While thermally actuated switches can offer high contact force and robustness against stiction, they suffer from higher power consumption and slower response times. Another alternative is magnetostatic actuation, which uses an external magnetic field to move the switch contacts. This method can provide reliable operation in harsh environments but typically requires additional magnetic components, increasing complexity.

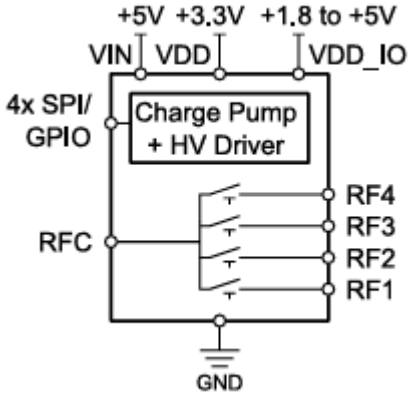


Figure 39. Block Diagram of MM5140.

An interesting feature of the MM5140 is the ability to operate each switch independently, such that both RF1 and RF2 can both be closed at the same time and as such create a path from port RF1 to port RF2, or any other combination.

Since 2017, Menlo Micro Inc. has offered packaged RF-MEMS switches suited to PCB-level TDUs, with device-dependent wideband operation (from DC–26 GHz), low insertion loss, high linearity, SMT packaging and in some devices, integrated drivers. Representative parts such as the RF switch MM5130 (SP4T, DC–26 GHz) and the loop-back switch MM5622 (2xDP3T, DC–20 GHz, 80 Gbps) illustrate the availability of off-the-shelf switch elements that enable compact, low-loss switched-line TDUs on standard PCB processes.

2.7.3. Menlo Micro Reliability

The manufacturer has published some data for switch reliability, see Figure 40, although it is not clear what the test conditions were, temperature, RF power etc.

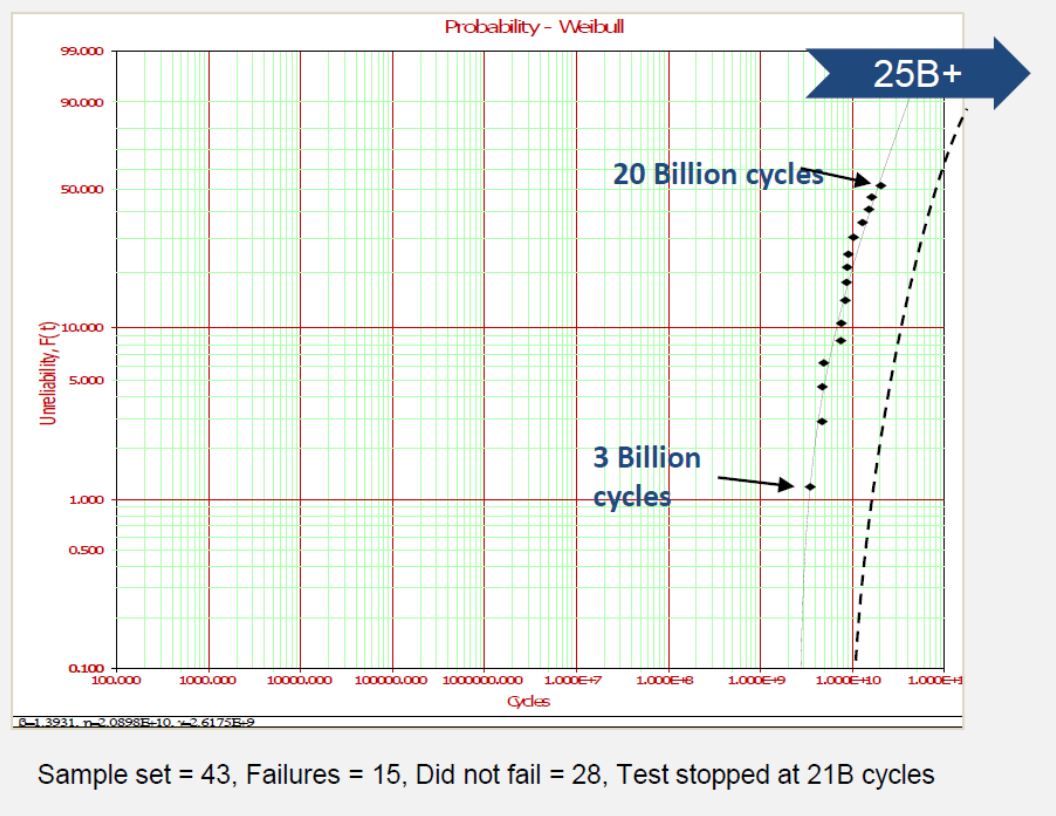


Figure 40. Menlo Micro switch reliability data.

From the Weibull probability data, several important reliability characteristics of the Menlo Micro RF MEMS switches can be inferred:

1. Extremely low failure rate at 3 billion cycles

- Only 1.1% of switches fail by 3 billion cycles, indicating high reliability in the early operational phase.
- This suggests low infant mortality (early-life failures), meaning the manufacturing process is well-controlled.

2. 10% failure rate by 10 billion cycles
   - A 10% failure probability at 10 billion cycles suggests a relatively slow degradation process.
   - This is typical of wear-out failure modes, likely related to contact resistance changes or surface oxidation.
3. Median failure at 20 billion cycles (50% at 20b cycles)
   - This means the characteristic lifetime (η) is around 20 billion cycles—half of the switches are expected to survive beyond this point.
   - This aligns with a Weibull shape factor (β > 1), meaning failures increase with aging rather than being purely random.

From this, it can be deduced that for a system that operates at a moderate switching rate (e.g., a few million cycles per year), failures would be rare over many years. If the switches are used in a high-switching-rate environment (e.g., a phased array scanning system adjusting thousands of times per second), the long-term reliability must be considered carefully.

The gradual increase in failure probability (10% at 10B, 50% at 20B) suggests that aging mechanisms like contact degradation or surface wear dominate. This is different from purely random failures, meaning lifetime predictions can be made with some confidence.

Menlo Micro claim that beam fatigue has been eliminated suggests that traditional mechanical stress-related MEMS failure (common in earlier RF MEMS designs) is no longer a limiting factor and instead contact reliability, material wear, or contamination may be the primary concerns.

This product was chosen as the RF MEMS switch for this research work.

2.8. Metrics

In addition to the normal metrics of insertion loss $(IL(dB) = -20\log|S21|)$ and return loss $(RL(dB) = -20\log|S11|)$, measuring and comparing TDUs makes use of group delay.

Group delay is a measurement, in seconds, for the time taken by each frequency component of a wideband signal to propagate through the device under test. Ideally the time delay is constant across the bandwidth of the signal otherwise the signal becomes distorted as different frequency components are delayed by different amounts. This is another way of saying the phase across the signal bandwidth needs to vary linearly with frequency, as per a true time delay and not as a true phase delay.

Group delay, τ_g, is defined

$$\tau_g = -\frac{d\phi}{d\omega}. \tag{2.13}$$

The group delay can be calculated as the negative frequency derivative of the phase of S21

$$\tau_g(\omega) = -\frac{d}{d\omega}\arg(S_{21}(\omega)). \tag{2.14}$$

There is also a common Figure of Merit (FOM) of the delay (in ps) divided by the loss (in dB) as a way to compare TDUs and acknowledge the importance of achieving a reasonable delay while not sacrificing signal levels.

2.9. MMIC Solutions

A natural question arises as to why a MMIC (Microwave Monolithic Integrated Circuit) is not used to build a TDU when there are plenty of time delay Integrated Circuits (ICs) available.

Both RF MEMS-based switched-line TDUs and MMIC CMOS TDUs can provide true time delay for phased array antennas and RF beamforming networks. However, their architectures, performance characteristics and commercial maturity differ significantly, so the most appropriate choice depends on the intended application.

RF MEMS TDUs excel in high-frequency, low-loss and high-power applications, making them well suitable for military, aerospace and precision radar systems. MMIC CMOS TDUs are cheaper, faster and highly scalable, making them well suited for commercial 5G, low-power beamforming and mass-market applications. If low insertion loss and high-power handling are critical, MEMS is preferred. If scalability, integration and fast switching are more important, CMOS MMICs are the better choice.

The following subsection defines the quantitative performance metrics used in this thesis to compare these two implementation approaches.

2.9.1. Performance Metrics

The relative performance of MEMS and MMIC TDU implementations can be quantified using several key metrics, defined here in Table 3.

Feature	RF MEMS-Based Switched-Line TDU	MMIC-Based Silicon CMOS TDU
Insertion Loss	Low (-0.2 to -1 dB per switch) but increases with frequency.	Higher (-3 to -6 dB per stage) due to lossy silicon substrate
Phase Accuracy	Excellent, due to mechanical precision of RF MEMS switches	Limited by transistor variability and parasitic capacitance
Power Handling	High (>1 W), suitable for high-power RF applications	Lower (≈10-100 mW), limited by silicon power dissipation
Switching Speed	Slow (10-100 µs) due to mechanical actuation	Fast (ns range) due to electronic switching
Frequency Range	From DC to millimetre frequencies	Typically, from low Gigahertz to 20 or 30 GHz
Delay Range	Long, 3,255 ps in reference [64]	Of the order of 10 – 400 ps
Linearity (IP3)	High (RF MEMS switches are passive, with near-zero distortion)	Moderate to low (active CMOS components introduce non-linearity)

Table 3. MMIC vs MEMS performance metrics.

In summary:

- RF MEMS switches exhibit very low insertion loss and excellent linearity, making them ideal for high-frequency and high-power applications.
- MMIC CMOS switches suffer from higher insertion loss due to silicon substrate loss but offer faster switching speeds and ease of integration.

2.9.2. Reliability and Lifetime

Feature	RF MEMS-Based Switched-Line TDU	MMIC-Based Silicon CMOS TDU
Mechanical Wear	Subject to fatigue and stiction (≈10^9 cycles)	No moving parts, long lifetime
Packaging	Requires hermetic sealing for long-term stability	Standard silicon chip packaging
Failure Modes	Stiction, charging effects, degradation of contact surfaces	Electrostatic discharge (ESD), transistor aging

Table 4. MMIC vs MEMS reliability and lifetime.

In summary: RF MEMS switches wear out over time due to mechanical movement, while CMOS MMICs have longer lifetimes but suffer from device degradation at high power.

2.9.3. 5. Commercial Viability and Scalability

Feature	RF MEMS-Based Switched-Line TDU	MMIC-Based Silicon CMOS TDU
Scalability	Limited by MEMS fabrication constraints, difficult to integrate many switches on-chip	Highly scalable, with many delay stages integrated on a single chip
Manufacturing Cost	Higher due to specialised MEMS processes and packaging	Lower due to well-established silicon foundry infrastructure
Adoption	Common in high-performance, low-loss RF applications (military, aerospace, satellite)	More common in commercial 5G, phased-array beamforming and consumer electronics

Table 5. MMIC vs MEMS commercial viability and scalability.

In summary:

- MMIC silicon CMOS TDUs are highly scalable and benefit from mass production in standard foundries.
- RF MEMS-based solutions remain more specialised but are preferred for low-loss, high-power and high-frequency applications**,** especially in aerospace and defence.

A recent publication reporting the performance of a 5-11 GHz true time delay in CMOS technology [65] included a table of the comparative performance of a number of MMIC true-time delay circuits and the table is copied here to give quantitative data in support of the comparison tables above.

Ref.	This work	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Tech	65nm CMOS	65nm CMOS	130nm CMOS	250nm SiGe	130nm CMOS	250nm SiGe	180nm CMOS	28nm CMOS
Structure	TTD (Low Pass LC in parallel)	TTD (LC+T-line)	TTD (trombone)	TTD (LC w/ varactor)	TTD (trombone)	TTD (LC w/ varactor+ Gm-RC)	TTD (Low Pass LC)	TTD (All Pass LC)
f_{RF} [GHz]	5-11	20-30	1-20	10-50	15-40	20-40	5-20	3-30
Maximum Delay[ps]	400	35.2	400	32.8	42	12.5	106	68.5
Resolution	1.54ps	0.56ps	5ps	cont	5.2ps	cont	3.3ps	4.9ps
Maximum Loss[dB]	41	12.3	45	25	14	-	38	13.5
Loss/Delay [dB/ps]	0.103	0.35	0.113	0.76	0.33	-	0.36	0.2
Delay/size [ps/ mm^2]	137 163(Core)	196(Core)	100	149(Core)	42	125(Core)	120	201(Core)
IP1dB (dBm)	11.2	6.5	2.5	15.5	8-10	18/13	-	6.2
DC power [mW]	passive	passive	2.6-6	passive	8.6-24.6	33	passive	passive
Chip area [mm^2]	2.91 / 2.46(core)	0.18(core)	4	0.22(core)	0.99	0.1(core)	0.88	0.34(core)

Table 6. Comparison of previous reported true-time delay circuits (Reprinted from reference [65]).

A few points to note:

- CMOS has a maximum frequency of 30 GHz. SiGe can go to 50 GHz.
- The maximum loss varies from 12.3 dB to 45 dB.
- The largest P1dB level for CMOS is 11.2 dBm.
- The maximum delay is 400 ps.
- The lowest frequency is 1 GHz.

2.9.4. Commercially Available Beamforming chips

There are a number of analogue beamforming ICs available now, mainly for the 5G market, in Ka, V and E-bands. Typically, these chips offer fixed phase delay and not true time delay and with limited phase delay, only 400° max, with few available in the 1 – 6 GHz band. See manufacturers such as Renesas, Qorvo, Analog Devices, Anokiwave and Sivers Semiconductors.

For the SatCom market there are several products suitable for X, Ku and Ka bands, however the latest commercial true time delay beamformer ICs have limited time delay range, typically less than 60 ps.

SatixFy (Farnborough UK) has introduced a digital beamforming (DBF) ASIC implementing true time delay (TTD) at Ku band for SATCOM terminals, demonstrating TTD in silicon DBF rather than as a passive MEMS TDU. This is significant for narrower-band SATCOM DBF modules but does not change the feasibility or motivation for PCB-level MEMS-switch TDUs at lower frequencies.

Anokiwave's (a division of Qorvo, USA) commercial DBFs are silicon beamformer ICs (phase/gain) at X-band and mmWave; there is no publicly listed TTD IC and no low-frequency MEMS TDU, so they are distinct from the passive TDU approach developed in this thesis.

Hence a packaged RF MEMS switch is an attractive option as a low cost, commercially available solution to the quest for a true delay unit for wideband phased arrays.

2.9.5. Commercially Available TDUs

Extensive market research reveals that there is only 1 true time delay unit available today and that is from API Weinschel, their model 984-1. It is a switched line design using electromechanical switches, relays, i.e., operating to 6 GHz, insertion loss of 4.3 dB and a maximum delay of 630° at 6 GHz.

There are no commercially available RF MEMS TDUs on the market today.

2.10. Practical Review and Emerging Directions

Replacing the phase shifters of a phased array with TDUs, forming a timed array, overcomes the issues introduced by frequency-dependent delays, enabling precise broadband beamforming without squint or distortion [3], [4]. Despite these advantages, TDUs remain underutilised in practice due to challenges in physical size, fabrication cost, long-term reliability and manufacturability. Photonic, MMIC and DMTL TDUs have each demonstrated specific strengths but suffer from trade-offs that limit their deployment [66], [67]. Photonic approaches require complex integration [68], [69]; MMIC-based solutions offer speed but suffer from insertion loss and limited power handling [70]; and DMTLs provide compactness and bandwidth at the cost of switch count and dispersion [21], [20], [24].

RF MEMS switches offer a compelling alternative, combining low insertion loss, high linearity and wide bandwidth with negligible static power consumption. Recent research has re-evaluated their potential in the context of mobile broadband, mmWave front ends and satellite payloads [6], [7], [8] and suggests that RF MEMS are eminently suitable as the building blocks for future beamforming modules and networks. However, further enhancements are required and ongoing research continues into new mechanical structures [71] (e.g. three-dimensional origami design), novel materials [72] (e.g. silicon-on-insulator), improved packaging [73] and long-term reliability [74]. These developments renew interest in MEMS-based TDUs as viable components in advanced RF systems.

Parallel advances in beamforming architectures have also expanded the design space. Joint phase-time arrays (JPTAs), for example, propose hybrid analogue front-ends that combine coarse TDU elements with fine-grained phase shifters for efficient beam control across frequency [75], [76]. These systems increasingly demand compact, wideband and low-loss TDU blocks compatible with low-cost PCB platforms.

Motivated by these trends and by the recent availability of a compact, reliable and commercially packaged RF MEMS switch, this work presents a practical, manufacturable TDU implementation.

3. Literature Review and Challenges

The development of RF MEMS-based TDUs has reached a turning point, transitioning from experimental prototypes to viable commercial solutions. Over the past three decades, MEMS TDUs have demonstrated low loss switching, high linearity and improved reliability, laying the groundwork for practical adoption in phased arrays. A key enabler of this shift is the recent emergence of commercially packaged RF MEMS switches, which now integrate self-contained charge pumps, eliminating the need for high-voltage external supplies and simplifying system integration. These advances address long-standing barriers such as substrate compatibility, packaging complexity and reliability concerns, opening the door for MEMS TDUs to move beyond research labs and into deployable RF systems.

This chapter reviews key academic contributions to MEMS-based TDUs, examining both the historical challenges and the technological breakthroughs that are now driving commercialisation. The review is structured into five thematic areas:

1. Early MEMS-based TDUs,
2. Substrate material considerations,
3. MEMS packaging and integration,
4. Half-wavelength resonance effects and
5. Long-delay implementations.

By framing the literature in this way, the chapter highlights the evolution of MEMS TDUs from bespoke research devices to scalable commercial components, setting the stage for their widespread adoption in next generation phased arrays.

3.1. Early Days: Foundations of MEMS-Based True Time Delay Units

The first reported proposal to build a switched line time delay unit using RF MEMS switches (or micromechanical membrane switches as they were called at the time) appeared in 1995 [77], by Goldsmith et al. However, it was just a proposal with a circuit simulation, no actual hardware was built.

In 1998, Barker and Rebeiz [21] reported the first wideband RF MEMS-based true-time delay phase shifters using distributed MEMS transmission lines (DMTL)**.** The design used coplanar waveguide transmission line fabricated on a quartz substrate with RF MEMS bridge capacitors placed periodically along the transmission line creating a slow-wave structure, giving the ability to continuously tune the phase velocity with a single control voltage. The

measured results demonstrated a 0–60 GHz TTD phase shifter with 2 dB loss at 60-GHz and with a maximum phase shift of 118°.

3.2. Substrates: Quartz, LCP, Alumina vs PCB-Based TDUs

The choice of substrate for a RF MEMS TDU is critical not only for the circuit's performance but also for determining the pathway from laboratory research to widespread adoption.

Many published reports of RF MEMS TDUs from 1998 to 2011 leveraged the advantages of lab-grade substrate materials, including quartz, alumina, high-resistivity silicon (HRS) and organic substrates such as liquid crystal polymer (LCP) and low-temperature co-fired ceramic (LTCC). These materials were selected for their low dielectric loss and high-frequency performance, often enabling monolithic designs, where the RF MEMS switches and delay lines were integrated onto a single substrate.

However, despite their superior electrical properties, these substrates posed significant challenges for scalability. While these early designs demonstrated the technical feasibility of MEMS-based TDUs, their reliance on high-performance but non-standard substrates severely limited mass production and commercialisation. The next phase of development focused on transitioning to more production-friendly solutions, albeit with new challenges related to packaging and integration.

3.2.1. Challenges with Lab-Grade Substrates

Early studies on LCP by Bairavasubramanian, R., et al. (2006) [78] and Chen M. J. et al. (2008) [79] highlighted integration difficulties with MEMS switches. They noted that LCP was prone to curling during processing due to temperature fluctuations and fabrication was complex, particularly in achieving precise metallisation and multilayer lamination while maintaining the intended transmission line characteristics.

Nordquist et al. (2006)] [80] designed and built a monolithic RF MEMS TDU on an alumina substrate but reported a very low fabrication yield of just 15%, meaning 85% of fabricated devices failed. While they presented the first 6-bit RF MEMS TDU operating from DC to 10 GHz with a maximum delay of 393 ps, the poor yield underscored the need for improved MEMS fabrication processes.

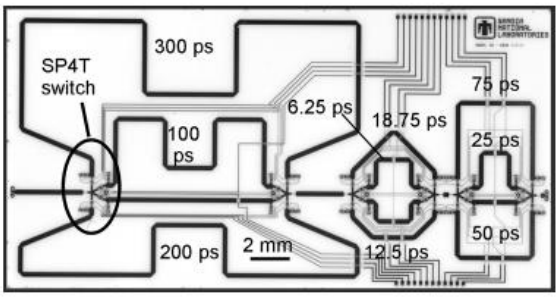


Figure 41. Optical micrograph of RF MEMS 6-bit TDU (27mm x 14mm).

Songbin Gong. et al. (2011) [81] used a quartz substrate to build a 60 GHz 2-bit RF MEMS TDU integrated with CPW transmission lines. The authors noted that while quartz provided excellent RF properties, its high fabrication cost and processing difficulties made it unlikely to become a mainstream commercial substrate for RF MEMS switches. Unlike silicon, which benefits from a well-established MEMS foundry ecosystem, quartz processing is more specialised and not widely supported by commercial fabs. This study demonstrated technical feasibility but did not suggest a clear pathway for commercial adoption.

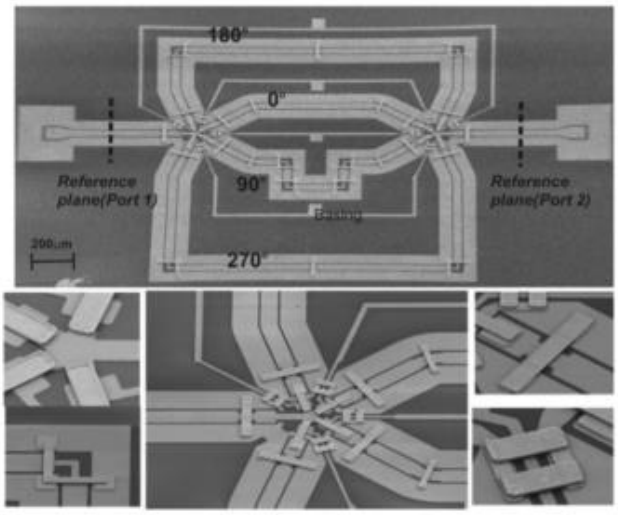


Figure 42. Scanning Electron Microscope images of the fabricated 2-bit V-band phase shifter.

3.2.2. Transition to PCB-Compatible Solutions

The transition toward PCB-compatible MEMS TDUs began in 2013 with the first reports of RF MEMS switches mounted on standard printed circuit boards (PCBs).

Du et al. (2013) [82] introduced hermetically sealed MEMS die switches mounted on a Rogers RO4350B PCB for a 5-bit phase shifter, operating from 1 GHz to 12 GHz and achieving a 348° phase shift. These commercial RF MEMS switches from RadantMEMS were packaged as hermetically sealed dies, requiring wire bonding for PCB connection and additional external control circuitry and high DC voltages for switch activation. However, the authors reported

poor isolation and excessive insertion loss due to bond-wire parasitics, which affected phase accuracy. They noted that reliance on commercial RF MEMS switch packaging limited their ability to optimise switch layouts for improved RF performance. Despite these challenges, the use of packaged RF MEMS devices represented a significant step toward practical MEMS-based phase shifters on PCBs, offering a more scalable solution compared to previous bare-die MEMS phase shifters.

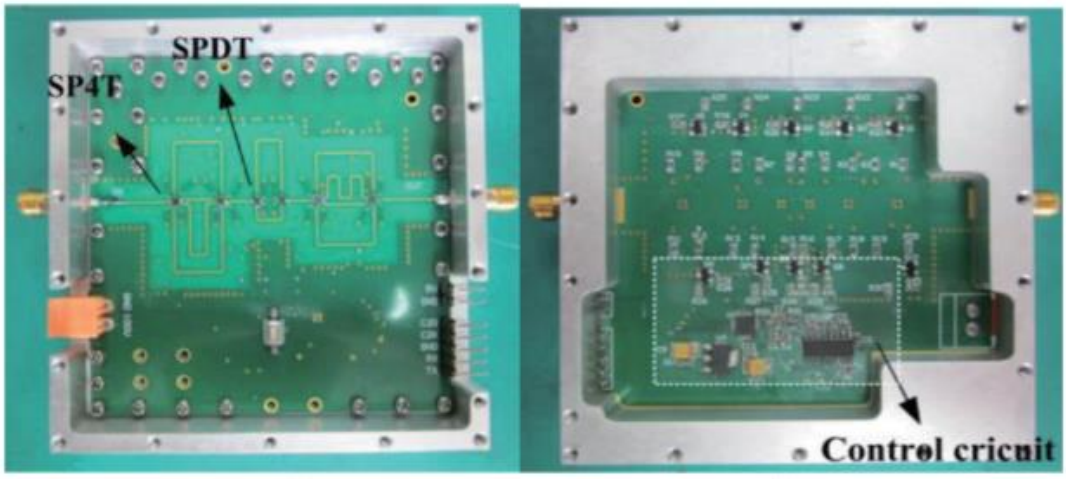


Figure 43. Photograph of 5-bit phase shifter, top and bottom.

Ibrahim et al. [83] further advanced this approach by integrating a fully packaged RF MEMS switch onto a Rogers RO6010 PCB, marking a shift toward production-friendly solutions. Their TDU operated over 1-5 GHz with 3-bit control, using conductor-backed CPW transmission lines and achieving a maximum delay of 49 ps. However, the authors commented on the difficulty of mounting the switches, which significantly impacted performance. The delay ripple was extreme at ±100 ps and the insertion loss was 7 dB, making the design potentially unusable.

Other researchers have persisted with hermitically sealed MEMS switches on PCBs. Yulin Huang et al (2015) [84] demonstrated a MEMS-based TDU with an insertion loss of just 0.89 dB for a modest phase delay of 75° at 2.7 GHz.

To the best of the author's knowledge, no published works report the fabrication of a functional UWB TDU using commercially available RF MEMS switches.

3.3. Packaged MEMS vs Hermetically Sealed Dies & Custom Integration

The integration of RF MEMS switches into TDUs has evolved significantly over the past three decades, transitioning from custom-fabricated MEMS requiring specialised foundries to commercially available packaged solutions. However, despite these advancements, a fully self-

contained PCB-based TDU using an off-the-shelf packaged RF MEMS switch has yet to be demonstrated.

3.3.1. Early Custom MEMS Designs – The Need for Foundries

Early work on MEMS-based TDUs, such as that by Nordquist et al. (2006) [80], relied on custom-designed MEMS switches, which required fabrication in dedicated foundries. These switches were monolithically integrated onto high-performance but non-standard substrates, such as alumina. While these designs demonstrated the potential for low-loss MEMS switching, they were not scalable. This reliance on proprietary fabrication, along with very low yields, significantly limited the adoption of MEMS-based TDUs beyond research environments.

3.3.2. Transition to Hermetically Sealed MEMS Dies

To improve practicality and scalability, researchers explored commercial MEMS switches, leading to the adoption of hermetically sealed MEMS dies. Du et al. (2013) [82] demonstrated a TDU using RadantMEMS hermetically sealed MEMS switches, mounted on a PCB. This marked a major step forward, allowing designers to integrate MEMS-based TDUs without requiring a dedicated MEMS foundry. However, these switches still required wire bonding, which introduced series inductance and parasitic effects that degraded phase accuracy and insertion loss. Additionally, external high-voltage DC control circuitry was still required, limiting ease of integration with low-voltage RF systems.

3.3.3. Toward Packaged RF MEMS Switches

The next step in integration was the use of surface-mount RF MEMS switches, eliminating the need for wire bonding. Ibrahim et al. (2014) [83] used an Analog Devices ADG1904 MEMS switch, mounted on a Rogers RO6010 PCB, to implement a 3-bit TDU operating over 1–5 GHz. The move toward a packaged MEMS switch was a significant improvement, reducing the handling complexity compared to bare-die MEMS switches. However, based on photographs (Figure 44) of the fabricated PCB, the design appears to still require multiple external wires for actuation, suggesting that the DC bias circuitry was not fully integrated within the package. Without an available datasheet for the ADG1904, it is unclear whether this switch had on-chip charge pumps to generate the required actuation voltage, or whether an external high-voltage supply was still necessary.

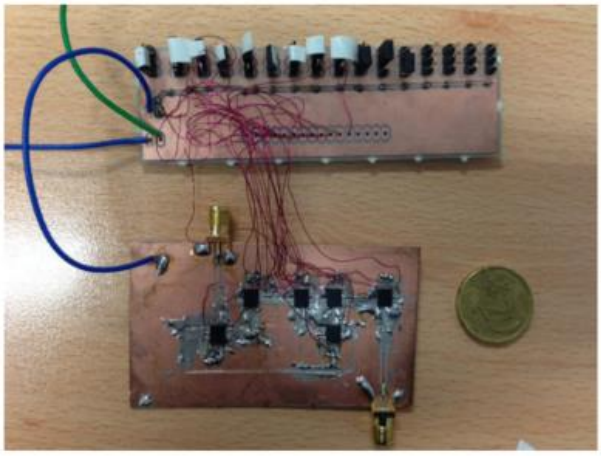


Figure 44. Fabricated switched line PCB.

3.3.4. The Current Gap: Fully Self-Contained MEMS-Based TDUs

Recent advancements in commercial RF MEMS switches have resulted in fully self-contained packages, where the DC actuation voltage generation is included within the package, allowing for direct integration into low-voltage RF systems. However, no published work to date has demonstrated a MEMS-based TDU using one of these fully self-contained switches. Most reported implementations still require external control voltage supplies, complicating PCB integration and limiting adoption in commercial RF systems.

Future work in MEMS-based TDUs should focus on demonstrating a practical, low-insertion-loss PCB-based TDU using fully packaged RF MEMS switches. This would bridge the gap between high-performance research prototypes and real-world deployable systems, enabling MEMS-based TDUs to be integrated into compact, low-power phased array architectures.

3.4. Half-Wavelength Resonance Effects in MEMS TDUs

Resonance in unused delay lines presents a well-documented challenge in switched-line TDUs, often degrading passband performance. This issue arises when delay lines that are switched out of the circuit— i.e., unused for a given delay step—resonate at frequencies where their physical length corresponds to a multiple of $\lambda/2$. These resonances can introduce unwanted signal interactions, affecting isolation, insertion loss and overall system performance. The problem becomes particularly severe in wideband and ultra-wideband TDUs, where multiple resonant conditions may fall within the operational frequency range.

To address this issue, researchers have investigated various suppression techniques, each with trade-offs in circuit complexity, insertion loss and bandwidth suitability.

3.4.1. Nordquist et al. (2006) – Dual-Switch Approach and Reference Line Tuning

Nordquist et al. (2006)] [80] proposed two distinct approaches to mitigate half-wavelength resonance in MEMS-based TDUs.

1. Dual-Switch MEMS Architecture

In their first approach, the researchers developed a dual-switch MEMS configuration, incorporating:

- A series switch to establish the transmission path.
- A shunt switch to ground unused delay lines.

By grounding the inactive delay lines, unwanted resonances were effectively suppressed, particularly in designs where broadside coupling between adjacent tracks was significant. However, this method increased the number of MEMS switches, leading to higher insertion loss. The trade-off was a more robust wideband response at the cost of additional switching complexity and loss.

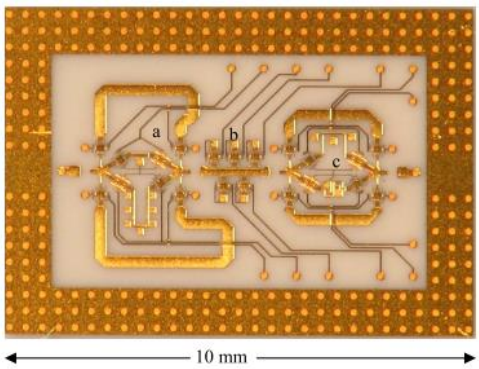


Figure 45. Optical micrograph of six-bit TDU with individual two-bit circuits labelled: (a) long, (b) short, (c) medium.

2. Reference Line Tuning for Resonance Suppression

In their second design, Nordquist et al. (2006) [85] eliminated the need for shunt grounding switches by modifying the reference delay line length. The approach relied on ensuring that all delay line lengths were chosen such that their resonant frequencies fell outside the desired operational band. This method worked effectively in narrowband applications, as it forced resonances out of band without additional switches.

However, this technique proved unsuitable for wideband TDUs, where it is difficult to position all resonances outside the passband. For very short delay lines, broadside coupling

remained difficult to mitigate and the researchers resorted to a distributed MEMS transmission line (DTML) approach to minimise unwanted signal interactions.

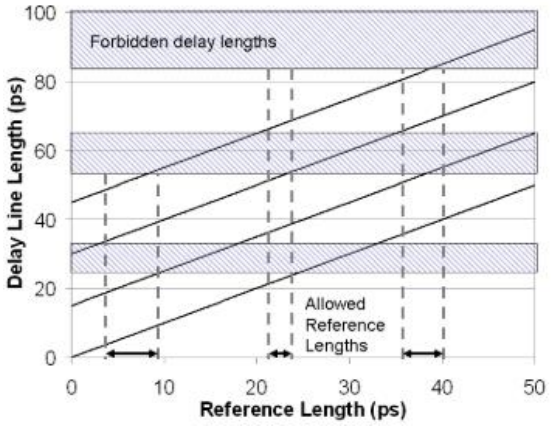


Figure 46. Graphical analysis of reference line length for a 15 ps four path time delay circuit. Shaded areas are forbidden. Vertical lines indicate windows of allowable lengths.

3.4.2. Yoon & Nam (2016) – Termination-Based Isolation Enhancement.

To further improve isolation in MEMS-switched TDUs, Yoon and Nam, (2016)] [86] introduced a termination-based method, designed to eliminate leakage signals from unused delay paths.

Their approach incorporated:

1. A main RF MEMS switch.
2. Additional switches placed in series with each signal path.
3. Termination resistors to dissipate energy from the unused switch port.

This ensured that, regardless of which delay path was active, the unused track was automatically terminated, preventing reflections and signal leakage. While this method significantly improved switch isolation, it required three switches per path, effectively tripling the switch count and doubling the number of active switches in circuit. Consequently, while isolation improved, insertion loss increased, highlighting the trade-off between isolation and signal attenuation. See Figure 48.

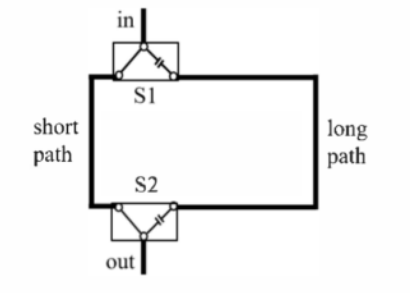


Figure 47. Conventional Switched Line.

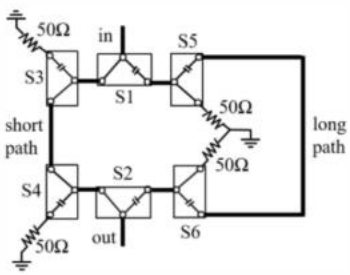


Figure 48. Proposed Switched Line using Cascaded Switches.

3.4.3. Impact on Future MEMS TDU Design

Switch port isolation remains a critical parameter in MEMS TDU design, as insufficient isolation can lead to resonance-induced phase errors, signal leakage and passband degradation. Various suppression techniques—shunt grounding, reference line tuning and termination switching—have been developed to mitigate these effects, yet each introduces trade-offs in insertion loss, circuit complexity and frequency bandwidth suitability.

As MEMS TDUs move toward commercial deployment, optimising switch topology to balance isolation, loss and manufacturability will remain a key challenge in wideband phased array applications. Future research may explore low loss switching networks, adaptive impedance tuning and alternative MEMS architectures to further improve port isolation while maintaining high efficiency. It is a topic of this research work.

3.5. Long-Delay MEMS-Based TDUs

For RF MEMS TDUs to be viable in ultra-wideband (UWB) large phased arrays, they must provide delay values spanning multiple wavelengths to enable beam steering over wide scan angles. For example, in a phased array with an aperture of 50 wavelengths, achieving a 60° scan in all directions requires a maximum TDU delay of approximately 60 wavelengths to compensate for the differential path lengths across the array. The challenge is to achieve such long delays in a cost-effective, compact design while minimising insertion loss, as a transmission line spanning 60 wavelengths inherently introduces significant signal attenuation.

3.5.1. Progress in Achieving Long Delays

Early MEMS-based TDUs demonstrated delays of approximately 393 ps (Nordquist et al., 2006)[80] which corresponds to a maximum delay of ≈4λ at 10 GHz**.** A decade later, Jin Lin (2016), [64] significantly advanced the state of the art by achieving a maximum delay of 31λ (3255 ps at 12 GHz), representing an 8-fold increase in absolute delay within 10 years. This

work demonstrated that long-delay MEMS TDUs are technically feasible, though challenges remain in optimising size, insertion loss and power requirements.

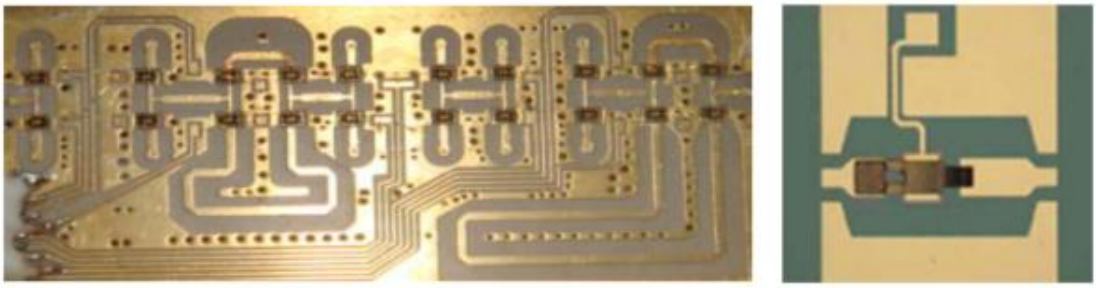


Figure 49. PCB Layout and MEMS cantilever switch.

Lin's design utilised 20 SPDT RF MEMS cantilever switches, integrated into a four-layer Rogers Duroid 5880 PCB. While achieving a substantial 31λ delay, the large number of switches resulted in a maximum insertion loss of 16 dB. Additionally, the RF MEMS switches were custom-fabricated, rather than off-the-shelf components, requiring an actuation voltage of 50–70 V. This higher voltage requirement compared to semiconductor switches may limit practical integration with low-voltage RF systems. Despite these challenges, Lin's work remains a landmark demonstration of the feasibility of multi-wavelength MEMS TDUs.

The physical size of Lin's TDU is unclear. The reported dimensions of 25 mm × 4 mm × 2.5 mm seem unrealistically small, especially considering the 31λ delay at 12 GHz. If accurate, this suggests extreme miniaturisation through the use of tightly wound or stacked delay lines, but further verification is needed.

3.5.2. Compact Design Considerations for Long-Delay TDUs

One of the major challenges in long-delay TDUs is physical size, as implementing delays of the order of tens of wavelengths requires extensive transmission lines. To address this, Yoon and Nam (2019) [70] proposed a multilayer PCB approach to minimise the footprint. Their design achieved a 1016 ps delay using silicon-based switches, confined within a 36.6 mm × 19.4 mm area by utilising a 7-layer PCB stack-up.

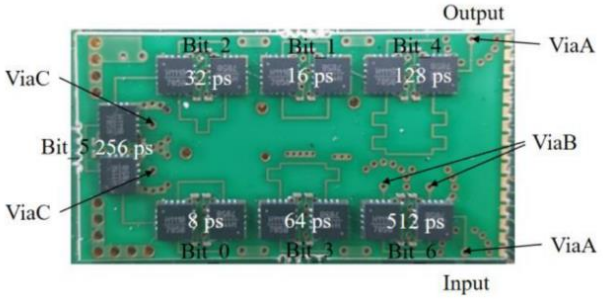


Figure 50. Fabricated TDU.

While Lin's work used a four-layer PCB, Yoon and Nam's study is distinct in its explicit focus on vertical integration for space savings. The use of additional PCB layers helped achieve a 34% reduction in area compared to a conventional single layer implementation.

Future research could explore similar multi-layered approaches for MEMS-based TDUs, allowing high delay values to be achieved while minimising physical footprint and transmission losses.

3.6. Summary of Limitations of Prior RF MEMS TDU Studies

Prior demonstrations of RF MEMS-based TDUs, while establishing technical feasibility, reveal recurring practical limitations that have impeded transition to manufacturable, wideband modules:

- **Substrate/process constraints.** Many prototypes rely on quartz, alumina, HRS silicon, LCP or LTCC to achieve low loss and high-frequency performance; however, these materials introduce cost and process complexity that limit scalability to volume production on standard PCB lines. Integration on LCP, for example, can be sensitive to multilayer lamination and metallization, and is prone to curl during processing.
- **Yield and reliability.** Early monolithic MEMS TDUs report low fabrication yields (e.g., ≈15% on alumina), with reliability concerns (stiction, packaging hermeticity, actuation voltage) that complicate adoption.
- **Packaging & integration.** Die-level MEMS parts (wire bonds, custom hermetic packages) add parasitics at switch-line interfaces and complicate assembly; robust, off-the-shelf packaged devices have historically been scarce, limiting PCB-level implementations at lower GHz.
- **Delay–loss and ripple trade-offs.** Long delay or many bits typically increase insertion loss and group-delay ripple, especially where matching at switch/termination interfaces is imperfect; these effects directly impact usable bandwidth and array calibration burden.
- **Control and driving constraints.** Many reported MEMS devices require high actuation voltages (circa 80-100V) and careful hot-switch management, increasing driver complexity at array scale; integrated low-voltage drivers were rarely available historically (now emerging in some packaged parts).
- **System-level implications.** The above limitations constrain bandwidth, size, manufacturability, and repeatability, which are critical for deployable timed arrays.

These themes align with the paper-by-paper “Limitations” listed in Appendix 2 and motivate the approach taken in this thesis to use commercially packaged RF MEMS switches and standard PCB processes to realise low-loss, wideband switched-line TDUs.

3.7. Conclusion

The evolution of MEMS-based TDUs has reached a pivotal stage, transitioning from custom-foundry designs to commercially available, packaged RF MEMS switches such as those from Menlo Micro. With these technologies now accessible, the focus must shift toward leveraging off-the-shelf RF MEMS switches to develop the next generation of deployable TDUs. Challenges such as substrate integration, resonance suppression and packaging optimisation have been addressed in research, paving the way for real-world implementation. Future innovation lies in hybrid architectures that combine MEMS with GaAs or Si-based switches to optimise performance, scalability and power consumption, ensuring MEMS-based TDUs become a practical and widespread solution in modern RF systems.

4. RF MEMS True Time Delay Unit for Wideband Phased Arrays

Existing true TDU designs for phased arrays face several critical limitations, including high insertion loss, excessive group delay ripple, limited broadband performance and practical integration challenges. Many prior RF MEMS-based TDU implementations relied on custom-fabricated MEMS switches, requiring high-voltage DC actuation and exhibiting significant parasitic effects due to wire bonding. Others, particularly those implemented using monolithic integration, suffered from high losses due to lossy semiconductor substrates. Moreover, hierarchical beamforming network designs using conventional switched-line TDUs often failed to optimise for quantisation effects, leading to structured phase errors that degraded beamforming accuracy and exacerbated sidelobe levels. To address these limitations, this work presents a novel RF MEMS-based switched-line TDU utilising commercially available packaged RF MEMS switches, eliminating the need for custom fabrication and simplifying system integration. The TDU employs coplanar waveguide transmission lines to mitigate dispersion and reduce insertion loss while maintaining a compact footprint.

A MATLAB-based simulation framework was developed to analyse quantisation induced sidelobe degradation, leading to an optimised TDU design that minimises structured phase errors and reduces peak sidelobe levels by to 2.75 dB compared to conventional uniform quantisation. The measured performance of the fabricated TDU confirms a low-loss, ultra-wideband delay response, achieving an average insertion loss of 1.5 dB with maximum loss of 3.09 dB, an overall mean absolute error of time delay error of just 18.4 ps and a delay-to-loss figure of merit (FoM) of 152.8 ps/dB, surpassing most prior works.

This chapter details the design methodology, simulation-driven optimisation, electromagnetic simulation validation and experimental characterisation of the developed TDU, demonstrating a practical, high-performance solution for next-generation wideband phased arrays.

4.1. Design Methodology (Theory & Parametric Exploration)

This section defines the key design parameters of the RF MEMS switched-line TDU, including control bit resolution, quantisation levels, transmission line characteristics and evaluates design trade-offs before electromagnetic simulation and fabrication.

4.1.1. TDU Specifications

The true TDU, the subject of this research, is designed to work with an 8-element linear antenna array covering an ultra-wideband frequency range of 0.4 GHz – 6 GHz, single polarisation and provide for a scan range of ±45°. Sidelobes should be down as low as possible,

target -20 dB. These specifications were chosen so that the TDU would interface with a tightly coupled array being designed and built by another team. The frequency band was selected to cover the popular license-free ISM bands with one antenna array and the scan range was chosen as a reasonable challenge for an ultra-wideband tightly coupled array at 6 GHz, to avoid grating lobes and excessive sidelobe degradation**.**

A typical definition of UWB is a signal bandwidth that exceeds the lesser of 500 MHz or 20% of the arithmetic centre frequency of operation. In this case the specification is for a signal bandwidth of 5.6 GHz, clearly much larger than 500 MHz so this research work can be defined as ultra-wideband.

The detailed specifications for the TDU follow:

- Frequency Range - The frequency range of operation is to be 400 MHz to 6 GHz, (i.e., 15:1) based on the proposed UWB array. This gives a centre frequency of 3.2 GHz with an operational bandwidth of ± 2.8 GHz, or 175%.
- Power and Insertion Loss - Given that the maximum transmit power in the ISM band is 4 watts EIRP (36 dBm), with an array gain of 9 dB, the total input power shouldn't exceed 27 dBm. Allowing for 3 dB of loss, this gives an input power level of 30 dBm, which is 125 mW of power per element and TDU. This does assume a uniform amplitude across the array. Allowing another 3 dB for a tapered amplitude profile, should that be required, gives a minimum power handling level for the TDU of 250 mW, 24 dBm.
- Time Delay Range - The time delay range of the TDU will be set by the spacing of the elements of the antenna array, the highest frequency of operation and the required scan angle. Using an array design of antenna spacing equal to half a wavelength at 6 GHz and a maximum scan angle of 45°, equation (2.1) gives an incremental delay of 59 ps between elements and a maximum delay of 413 ps on the 8^{th} element. (Note the first element has a delay of zero so the maximum delay is 7 times the incremental delay.) The time delay of 413 ps at 6 GHz is equivalent to 892° of phase shift, much more than a single wavelength and hence why a true phase shifter with a maximum range of 360° is unsuitable for this application.
- Digital Control Bits - 4 bits was selected as a good compromise between performance and complexity. Four bits with an 8-element array will give a maximum quantisation average sidelobe level of -18.6 dB and an RMS pointing error of 1.2°. The compromises and alternatives will be explored in subsequent sections.

- Switching Speed - Switching speed to not a feature of RF MEMS switches and fortunately is not critical for this research work. The state-of-the-art for RF MEMS switches appears to be a switching time of the order of 10 µs, while for PIN diodes a typical switch speed is 4-12 nanoseconds and a silicon switch has an on/off time and settling time of 10 - 20 nanoseconds.
- Size - Working on an element spacing of a half wavelength at 6 GHz, the area underneath each antenna element will be approximately 2.5 x 2.5 cm. While it would be ideal if the time delay unit could lie flat behind the array with each TDU taking up less than 2.5cm square, it seems more likely that the feeder network will be perpendicular to the array. Under this scenario size will be less of an issue as seeking a low cost solution is in preference to a small size.
- Reciprocal - A reciprocal phase shifter works in both directions, meaning the signal can propagate in either direction through the phase shifter and this is a requirement in this case as the phase shifter is to operate in both transmit and receive.

4.1.2. TDU Architecture

For the design of the TDU, a switched-line architecture was selected over alternatives such as DTML due to its inherent simplicity, ultra-broadband capability and ease of implementation. The switched-line approach enables precise, discrete time delays by selecting different physical transmission paths. A key motivation for this design is the opportunity to demonstrate the feasibility of commercially available RF MEMS switches, which offer low loss, high power handling, high isolation and near-zero power consumption compared to traditional electromechanical / semiconductor-based switches. Additionally, the switched-line TDU provides scalability for larger arrays and facilitates straightforward integration into existing PCB-based phased arrays.

Using the Menlo Micro MM5140 product, a 4-bit TDU can be designed as shown here in.

Figure 51.

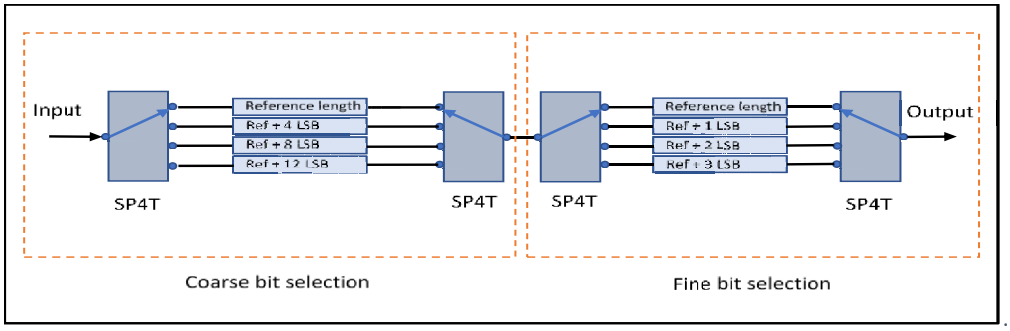


Figure 51. TDU Schematic.

The Menlo Micro RF MEMS switch is a single pole four throw (SP4T) switch and as such, four are required to give all 16 delay times associated with 4 control bits. Between 2 switches there are 4 transmission lines of different lengths. The shortest path is the reference length and is the straight through path with “zero” delay, i.e., the design time delay value is the delay in excess of the reference path. The other transmission lines are a set length longer than the reference line in order to delay the signal by the propagation time through the longer line length.

The full TDU is in 2 sections, a fine bit control and a coarse bit control section. The fine bit control incorporates delays of 1, 2 and 3 LSBs and the coarse bit control incorporates delays of 4, 8 and 12 LSBs.

The switch manufacturer, Menlo Micro, provides a lumped element model for their switch, shown here and they comment that the model gives good correlation with 2-port measured S-parameters up to 12 GHz. This lumped model was used for initial simulations and later proved optimistic when compared with the assembled board.

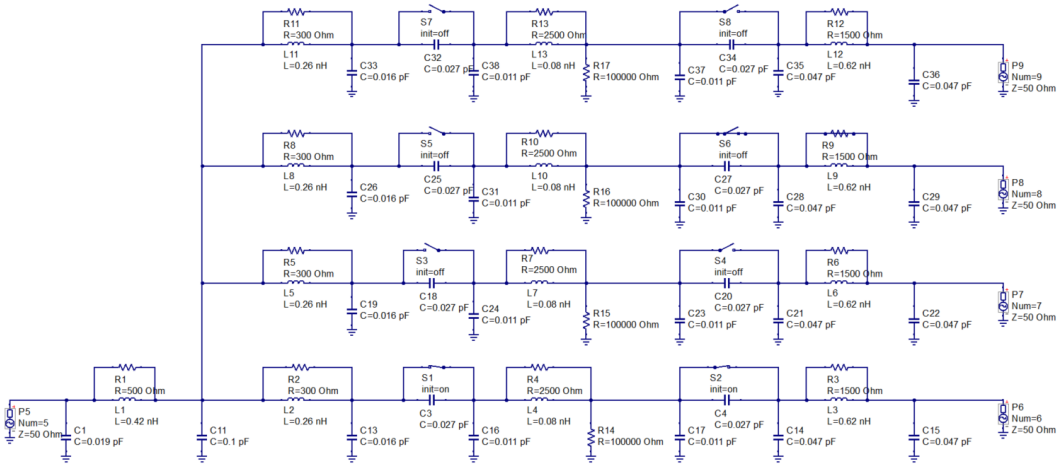


Figure 52. Lumped element model of MM5140.

The construction is really four single pole single throw switches (SPST) in parallel with a common bus connected to one side of each switch. Notice when a switch is off, there are two 0.027 pF capacitors in series and these are shorted out when a switch is on.

As a check of the model for the RF MENS switch and to check the results against the claim of the lumped element model producing results with a good correlation with measured performance, the circuit simulator ANSYS Circuit was used to compare results. The model simulation results are shown here with a copy of the published specs from the manufacturer’s datasheet.

Figure 53 shows the model return loss starting at 50 dB around DC, rising to 16 dB at 6 GHz. This is in line with the published specs showing 15 dB at 6 GHz although the measured performance is not as smooth as the model suggests.

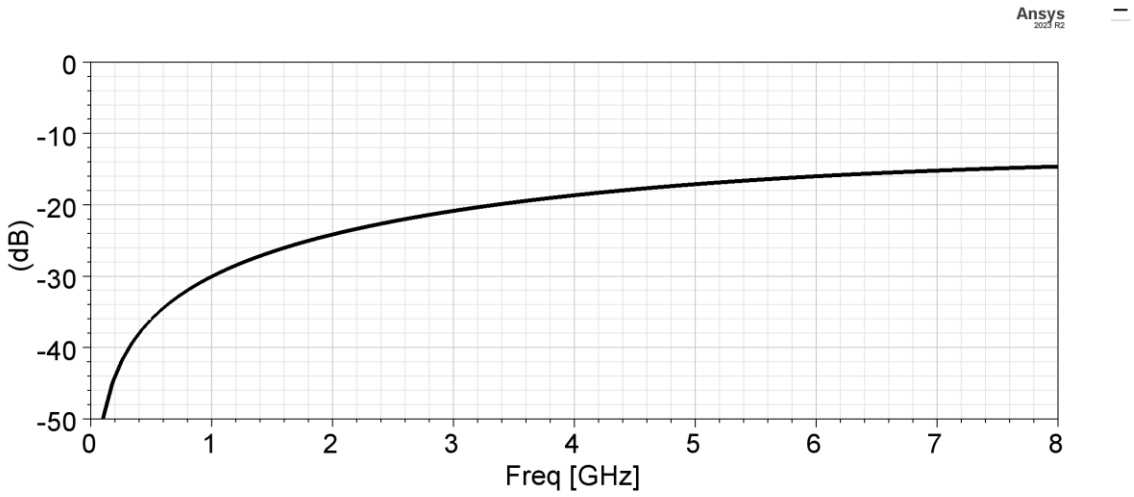


Figure 53. S11 (dB) for RF MEMS switch model.

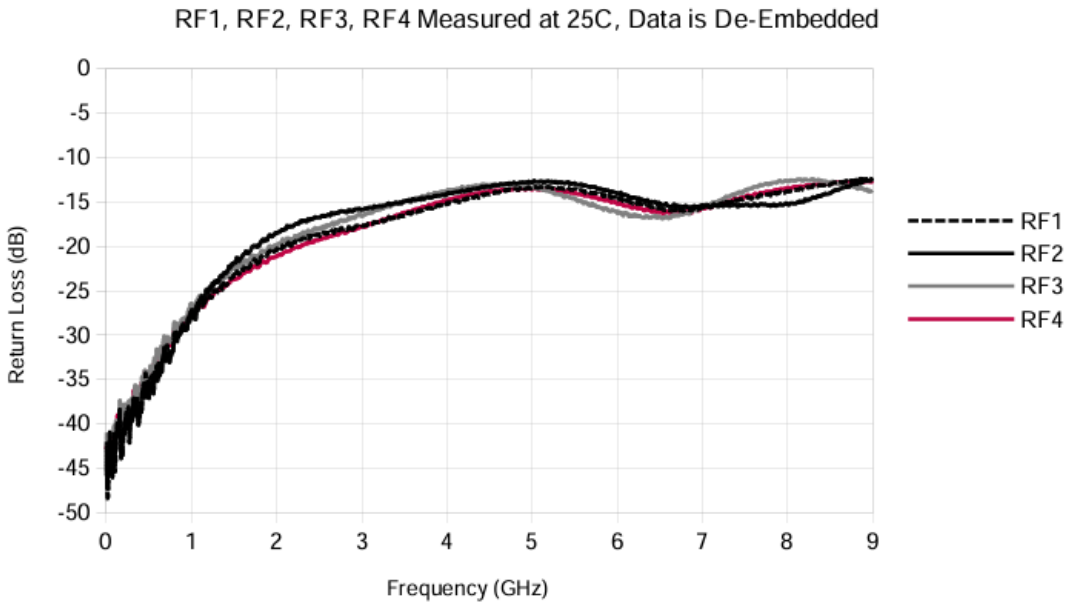


Figure 54. Measured Return loss (dB) for RF MEMS switch.

Similarly, the insertion loss from the model is 0.2 dB at 6 GHz compared with a measured insertion loss of 0.44 dB.

However, the model does give a greater isolation between ports, 34 dB, than actually measured at 26 dB, at 6 GHz.

The model group delay shows a good flat response of 22.5 ps, well past 6 GHz.

Building up a full Circuit model of the full TDU identified two practical problems that required solving, specifically:

1. The imperfect match on the input to the switch caused varying performance depending on which delay line was in circuit and
2. The delay lines not in circuit oscillated causing ringing in the group delay. This was mentioned as a potential issue in the paper by Nordquist et al, [80, 85].

Considering the first problem, the switch transformed the 50 Ω input impedance to a combination of resistance and reactance on its output pin, 54+j14 at 3.2 GHz, the middle of the frequency band. Launching into the delay line, this transforms to varying impedances depending on the length of the transmission line and so varies the amplitude and return loss performance of the TDU depending on the delay line length.

To overcome the mismatch on the switch input, a simple LC matching network was designed to move the transformed impedance to pure resistance and having the delay transmission line of the same characteristic impedance. Then the output impedances of the delay lines are all the same and will perform the same. In the design, the characteristic impedance of the delay lines is 54 Ω.

To solve the resonant delay lines, one solution is to terminate the unused lines when not in circuit and Nordquist employed this strategy in his first paper with custom RF MEMS switches that were both series and shunt. In his second paper, Nordquist proposed a scheme of adjusting the length of the reference line so as to ensure the resonant frequencies of the delay lines were all out of the frequency band of interest and they no longer terminated the unused lines. This had the added advantage of reducing the number of RF MEMS switches. However, this was not an option for this research work as the frequency band of operation is so wide. Nordquist also switched in capacitors on some lines to dampen oscillations. For this research work, the decision was to terminate the unused lines as a more certain method to stop any resonance.

The challenge is how to implement a termination on 3 lines and not disrupt the performance of the one delay line in circuit and to have control over the switching of the termination. Again, the SP4T RF MEMS switch provides an elegant solution.

As the Menlo Micro switch is made of 4 independent single switches in parallel, each with independent control, (see Figure 39) it is possible to mount a second switch in parallel with each SP4T switch in Figure 51 to switch in a termination resistor for the unused delay lines. One termination resistor per end is sufficient for 3 lines.

The full schematic of a single 2-bit TDU is shown here in Figure 55. Blocks U1, U2, U4 and U5 are the RF MEMS switches. The termination resistors are R1 and R1415, in parallel with a small capacitor for a better match. The shunt open circuit stub and series inductor form the LC matching network on each of the four delay lines.

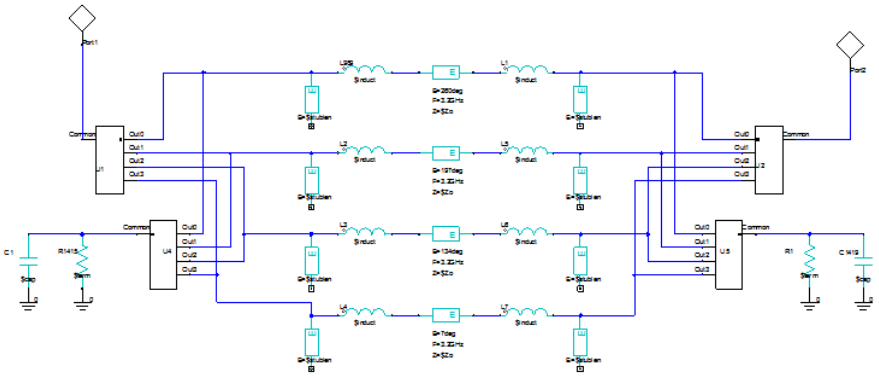


Figure 55. Schematic of 2-bit TDU.

The simulated performance is shown below for a single delay line. Figure 56 shows the return loss of a complete 2-bit TDU to be better than 20 dB across the band of interest with a characteristic ripple that does vary in shape depending on which delay line is in circuit.

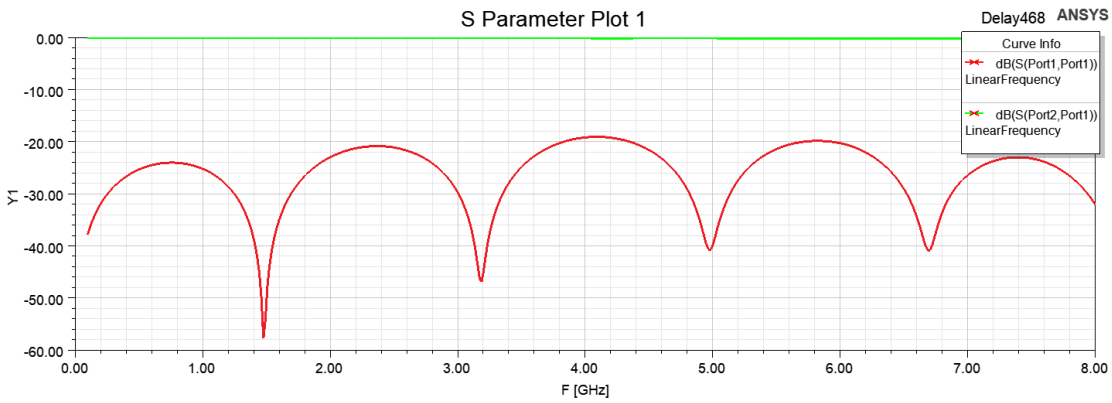


Figure 56. Return Loss (S11) 2-bit TDU.

The insertion loss (S21) is 0.2 dB at 6 GHz, as per Figure 57.

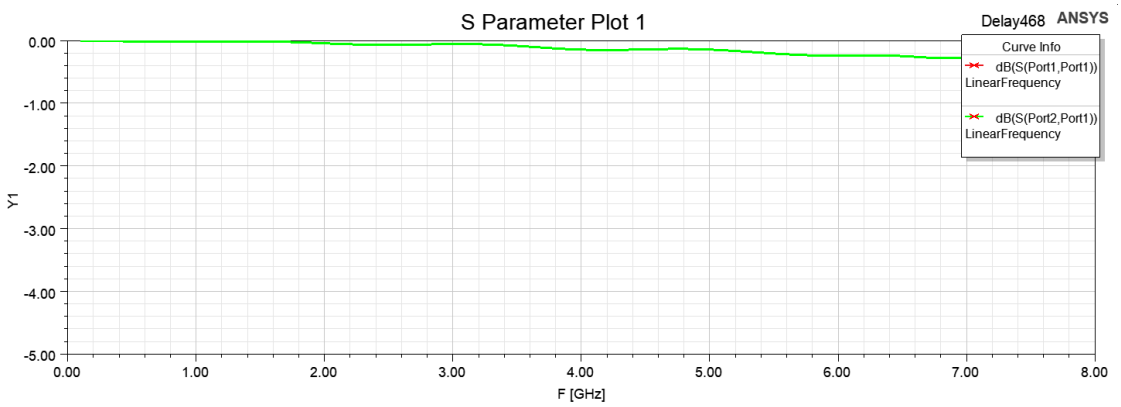


Figure 57. Insertion Loss (S21) 2-bit TDU.

The group delay is 290 ps, +/- 2 ps, up the 6 GHz. The ripple in the group delay does follow the return loss profile and the better the input match the better the group delay. See Figure 58.

Cascading two 2 bit delay units to form the design objective of a 4-bit TDU produces the return loss and group delay as shown in Figure 59 and Figure 60.

The return loss is better than 20 dB right across the band of interest. More ripple in now evident as 2 delay lines are now in series. The group delay has deteriorated and now has +/- 5 ps variation.

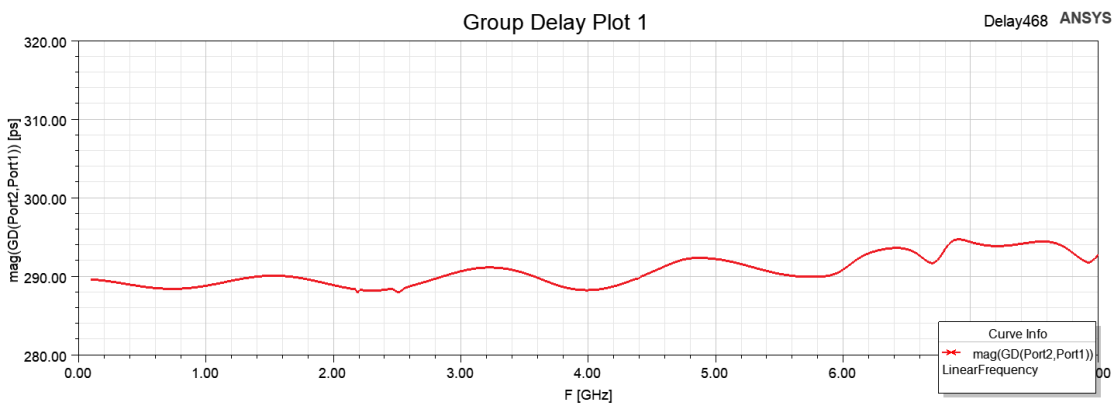


Figure 58. 2-bit TDU Group Delay.

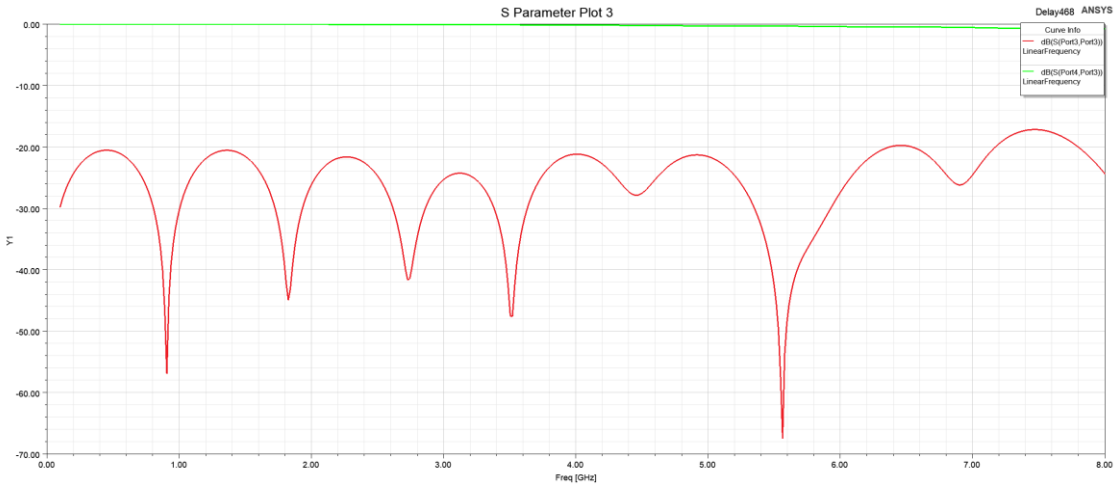


Figure 59. Return loss (S11) 4-bit TDU.

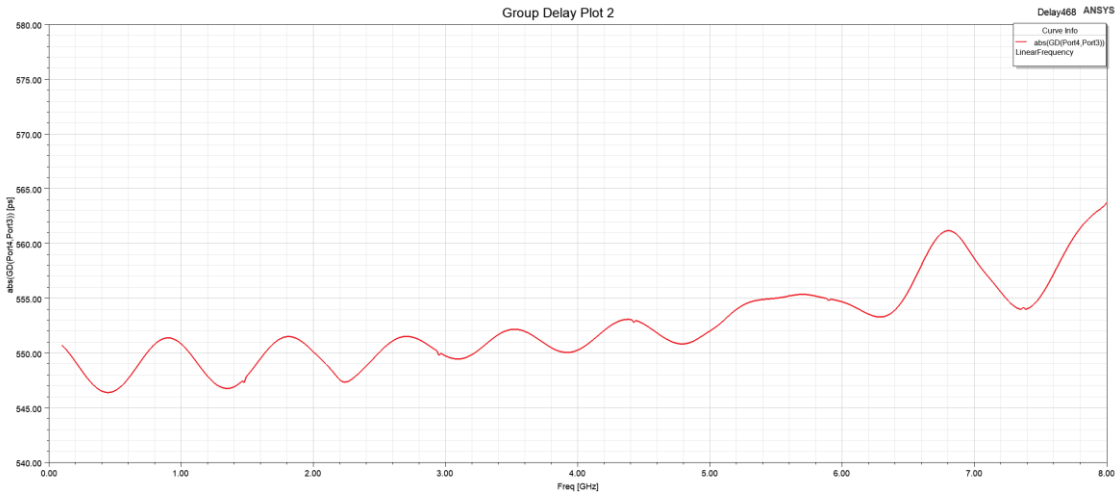


Figure 60. Group Delay 4-bit TDU, max delay.

4.1.3. Transmission Line Technology

An important decision in the design of the TDU is the selection of the appropriate transmission line technology, particularly when aiming for minimal dispersion and a consistent group delay. In this work, conductor backed coplanar waveguide (CBCPW) was chosen over microstrip as the transmission line medium due to its superior dispersion characteristics and enhanced design flexibility.

This was also the conclusion of an explicit investigation by Ibrahim into which was the most suitable transmission structure for RF MEMS switch TDUs [87].

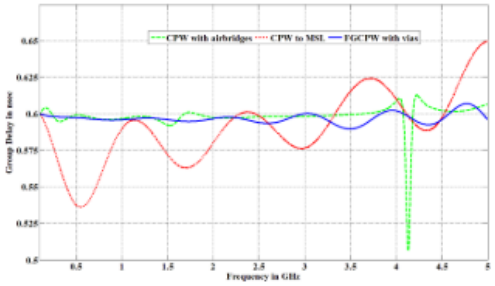


Figure 61. Simulated group delay for three different line structures.

Figure 61 shows their simulation results for microstrip (MSL), the red trace, coplanar waveguide (CPW), the green trace and finite grounded coplanar waveguide (FGCPW), the blue trace, which is the same as CBCPW.

The fundamental even mode of CPW is less dispersive than the fundamental mode in microstrip. This is especially true if the tracks are carefully designed with small gap widths [28]. CPW also has the practical advantage that it is a simple fabrication that more easily allows for the assembly of both series and shunt components.

However, CPW also presents certain challenges, particularly in terms of manufacturing tolerances and unwanted mode excitation, which are discussed later in this chapter.

4.1.4. Reduction of Dispersion and Group Delay Variation

The primary design objective for the TDU is to achieve a flat group delay response across the operational bandwidth of 0.4 GHz to 6 GHz and group delay is greatly affected by dispersion.

Dispersion refers to the frequency-dependent variation of phase velocity in a transmission medium. In a non-dispersive medium such as free space, phase velocity remains constant, meaning all frequency components of a signal travel at the same speed. However, in practical guided structures such as waveguides, microstrip lines and coplanar waveguides, phase velocity changes with frequency due to variations in effective permittivity and wave propagation characteristics. This variation causes different frequency components of a signal to propagate at different speeds, leading to pulse spreading and distortion, which can degrade signal fidelity in wideband applications.

The phase velocity v_p is given by

$$v_p = \frac{\omega}{\beta}, \tag{4.1}$$

where ω is the angular frequency and β is the phase constant. In microstrip and CPW transmission lines, phase velocity can increase or decrease depending on substrate permittivity and conductor geometry, making dispersion effects highly design dependent.

A closely related concept is group delay, which represents the rate of change of phase with respect to frequency and determines how different frequency components of a signal experience time delay. Group delay τ_g is defined as

$$\tau_g = -\frac{d\phi}{d\omega}, \tag{4.2}$$

where ϕ is the phase shift and ω is the angular frequency. Unlike phase velocity, which describes the propagation speed of a single frequency component, group delay quantifies the delay experienced by a modulated signal or pulse. In a dispersive transmission line, group delay varies with frequency, leading to signal distortion as different frequency components of the waveform arrive at different times.

In the context of TDUs, dispersion in the delay lines results in frequency-dependent delays, impacting phase accuracy and signal alignment across different frequencies. If dispersion is significant, signals at higher frequencies experience different delays compared to lower frequencies, causing phase distortion and potential beam pointing errors in phased array applications. This is particularly problematic in ultra-wideband TDUs, where time delay accuracy is critical. To mitigate these effects, careful selection of materials, impedance matching and delay line geometries is required to minimise dispersion and maintain consistent time delay performance across the operational bandwidth.

Early in the design process, full-wave electromagnetic simulations were conducted to analyse the group delay characteristics of different transmission line structures, including microstrip and CPW. The results demonstrated that CBCPW exhibits a flatter group delay response, whereas microstrip showed a slight but noticeable increase in group delay with frequency. Specifically, the microstrip line exhibited a rise of 5 ps with frequency over a total delay of 230 ps, which, although not excessive, could introduce unwanted phase variations in wideband applications. In contrast, CBCPW maintained a more stable group delay across the frequency range, reducing potential timing errors and ensuring better phase coherence in the TDU.

4.1.5. Lower Ohmic and Dielectric Losses

In a switched-line TDU, since different transmission lines of varying lengths are switched into the signal path, there will always be a variation in loss for the TDU with the delay value

selected. Short of consciously introducing extra loss in the shortest delay paths, this will always be the case. (As one example of a conscious effort to keep losses on all delay lines consistent see ref [60].) A downside of selecting CBCPW is that CBCPW is known to have greater losses than microstrip and this has been accepted as a necessary compromise for this research work to gain the benefit of the reduced dispersion. From published research [88] and simulation, the extra loss was calculated to be 0.02 dB/cm at 6 GHz, equal to an extra loss of 0.19 dB for the longest line.

4.1.6. Challenges of CPW: Manufacturing Tolerances and Mode Suppression

While CPW provides several advantages over microstrip, it also introduces manufacturing and design challenges that must be considered:

- **Tighter fabrication tolerances**: CPW requires precise gap and conductor width control to maintain the desired impedance. Any deviation in these dimensions can significantly alter the characteristic impedance and degrade performance. This imposes stricter requirements on PCB fabrication processes compared with microstrip, which is generally more forgiving in terms of width tolerances. For example, with CPW, a change in the gap of just 0.02 mm will change the line impedance by 8.6%, while with microstrip, the track width needs to change by 0.14 mm to have the same change in line impedance, i.e., microstrip is a factor of 7 times more forgiving with tolerances in this example.
- **Unwanted Mode Excitation**: CPW can suffer from the excitation of odd modes, also known as stripline modes, particularly in the presence of asymmetry or discontinuities in the layout [89]. These unwanted modes can interfere with the primary signal, leading to degraded performance.
- **Evanescent Wave Propagation**: Another concern with CBCPW is the potential for evanescent wave propagation in the dielectric between the top and bottom ground planes. This occurs due to differences in phase velocity between the air and the dielectric substrate, leading to unwanted energy leakage. This effect is more pronounced in CBCPW structures with finite ground planes, where the electric field can extend into the surrounding air.

Despite these challenges, the overall advantage of CBCPW with lower dispersion, on balance, made CBCPW the best choice for the switched-line wideband microwave TDU application.

4.1.7. Supressing Odd Modes

There are 2 well accepted methods to help suppress unwanted parasitic modes of propagation with CPW:

- Air bridges, a simple 3D structure of conductive material that bridges over the centre CPW track and connects the two ground planes on either side. Bond wires are a simple example.
- Vias from the top ground planes down to the lower ground plane so as to ensure that the ground planes are at the same potential for propagation of the desired, fundamental even mode.

For this research work, vias were used to ensure suppression of the unwanted modes of propagation. Extensive use of electromagnetic simulation (Ansys HFSS) was used to optimise the placement of vias by inspecting plots of electric field strength to ensure even mode propagation and to limit coupling of energy to other tracks.

Figure 62 is one example of an odd mode of propagation with unequal electric potential either side of the centre conductor of a CBCPW transmission line. The solution is to place vias to the ground plane below to achieve equal potential each side on the ground planes on each side of the centre track.

Figure 63 is an example of even mode propagation showing equal field strength either side of the centre track.

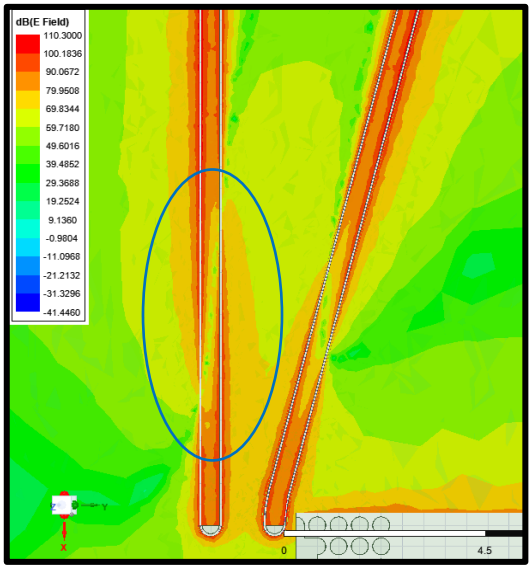


Figure 62. Example of CPW odd mode propagation, showing unequal field strength each side of the track.

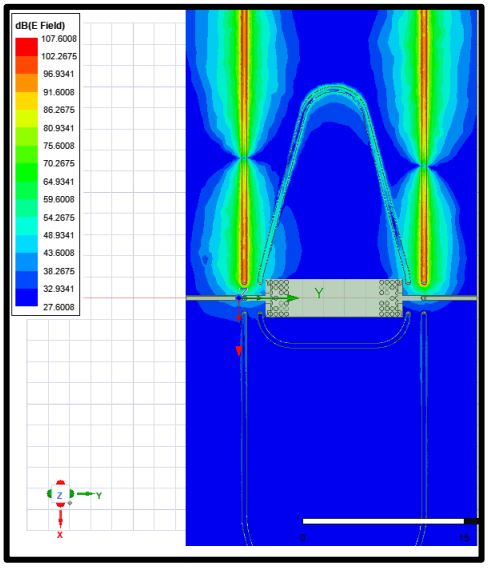


Figure 63. Example of even mode propagation.

One manifestation of the odd mode of propagation and the evanescent wave, is disturbances, or glitches on the group delay profile so it is paramount to supress unwanted modes.

Figure 64 is a good example of these unwanted glitches, showing 4 delay lines i.e., 4 delay values, each with a trace including glitches due to the odd mode propagating and a much cleaner trace when the odd mode has been supressed with vias and only the even mode is excited.

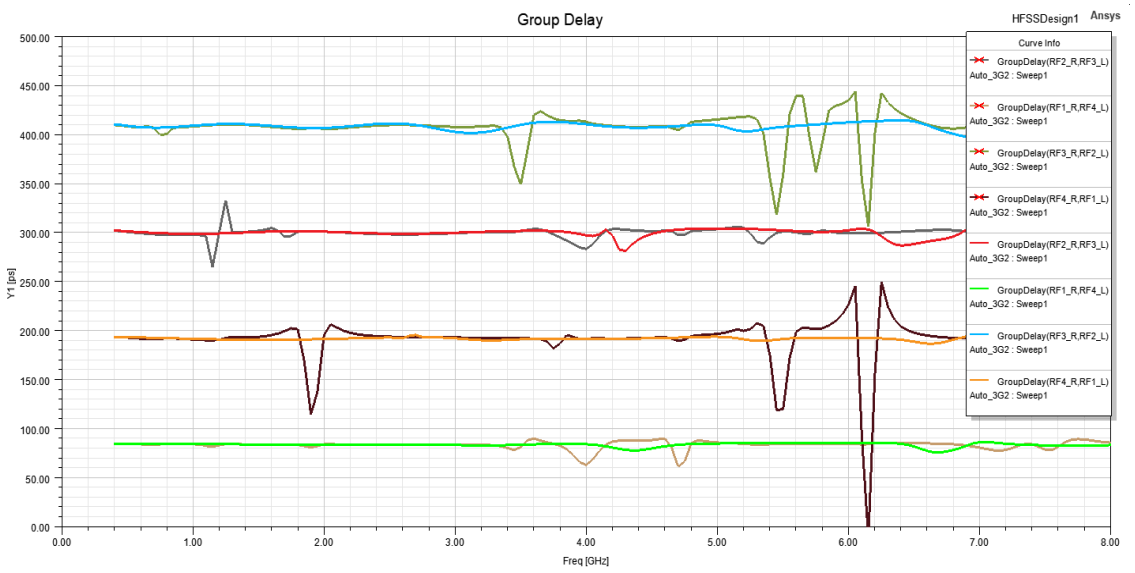


Figure 64. Examples of the effect of odd mode propagation on the group delay.

4.1.8. Unused Track Resonances

Another known phenomenon with switched line delays is half-wave resonance of unused tracks, i.e., those delay paths that are not switched into the transmission path and are idle, or unused. These can resonate at frequencies where the track length is a multiple of λ/2. If these tracks are excited by any means they can resonate and disturb the signal on the through path.

This characteristic was discussed in chapter 3.4 and reference [85] where the researchers speak about selecting a reference line length suitable to keep the resonances out of the wanted frequency band. Unfortunately, this is not an option for this research work as the delay times are too large as compared with the proposed scheme where delays of only 15 – 40 ps were required.

That said, the scheme of a very short reference line was investigated with the layout shown in Figure 65. The two footprints for the RF MEMS switches are shown with the pads for the LGA and the reference path is circled. The 3 delay lines are shown but not the input and output lines. These were problematic as they would have to pass under or over the delay lines in order to connect with the switches and as such this design was dropped. As well, it did not solve the problem of half-wave resonances which were still evident.

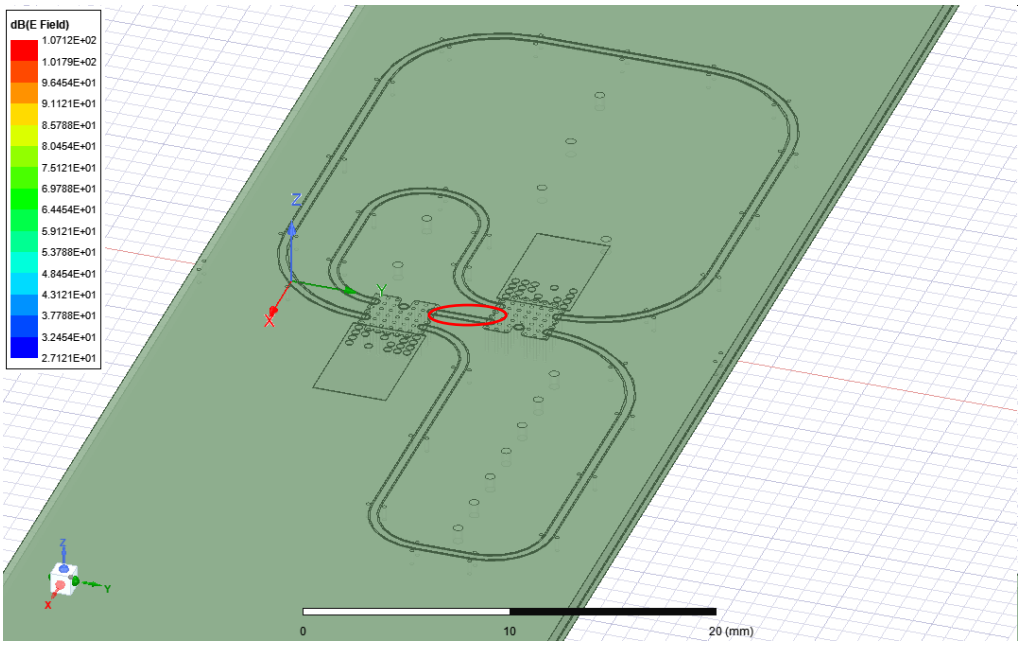


Figure 65. Example layout of PCB for short reference line (Zero delay line).

There are 2 mechanisms for exciting the unused tracks:

- Electromagnetic coupling from the used track to the unused track and
- Feedback through the RF MEMS switch, i.e., specified as the port isolation.

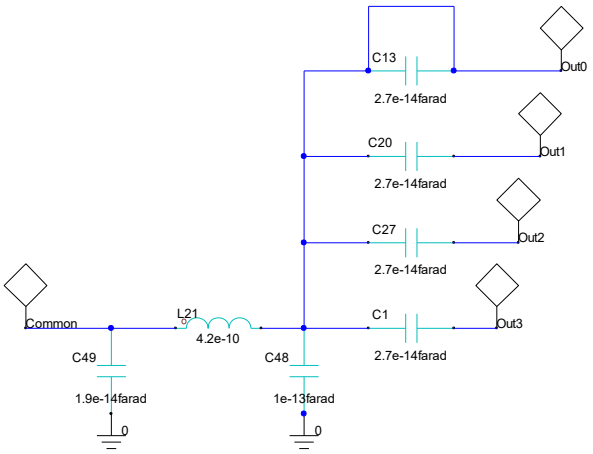


Figure 66. Block diagram of RF MEMS Switch.

To understand the switch feedback mechanism, consider the simplified switch block diagram in Figure 66. There is a small series capacitor feeding each output port from the common bus. When a switch is activated, the capacitor is shorted out and the input port is connected to that output port. There is also a path for the input signal to every other output port through the series capacitor. The capacitor is small in value, 0.0027 pF but still some energy can pass to the open ports. Ideally this is a very low level but in practice may be only 25 dB down and can excite the unused tracks.

As mentioned earlier, the strategy adopted to tackle this problem is to terminate each unused track to ground through a termination resistor at each end when not in use. Experiments revealed that only terminating a track at one end was not enough to remove all disturbances in the group delay from the half-wave resonances.

Figure 67 is an example of a group delay trace (magenta) with floating unused tracks, notice the glitches. The green trace shows the improvement when terminating the unused tracks.

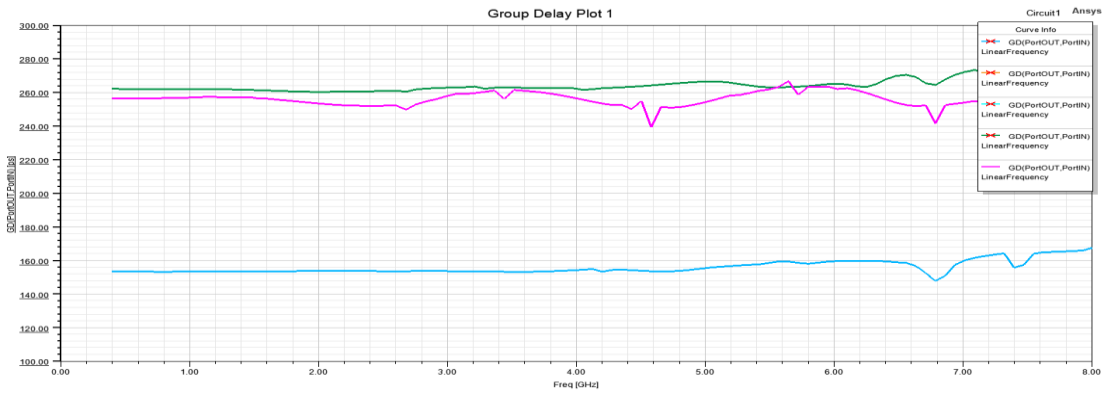


Figure 67. Example of glitches on group delay trace because of half-wave resonances.

Recall also the method proposed in chapter 3.4.2 where extra switches were inserted in-line to stop the feedback through the single switches. While this method did indeed significantly reduce the half-wave resonances, it tripled the number of switches and was discounted for this research work.

With many silicon switches, there is the option to use non-reflective switches, also called absorptive switches that internally terminate the ports that are switched out of circuit and consequently suppress any half-wave resonances. Unfortunately, current RF MEMS switches are fully reflective as they are open circuit when switched off and as such there is scope for half-wave resonances.

4.1.9. Shorting or terminating Unused Tracks

The proposition of this research work is to dampen or suppress any half-wave resonances of unused tracks by terminating each track when not in use. This is to be achieved by a second group of RF MEMS switches mounted directly beneath the delay transmission tracks and in parallel with the RF MEMS switches used for switching delay lines in and out of circuit.

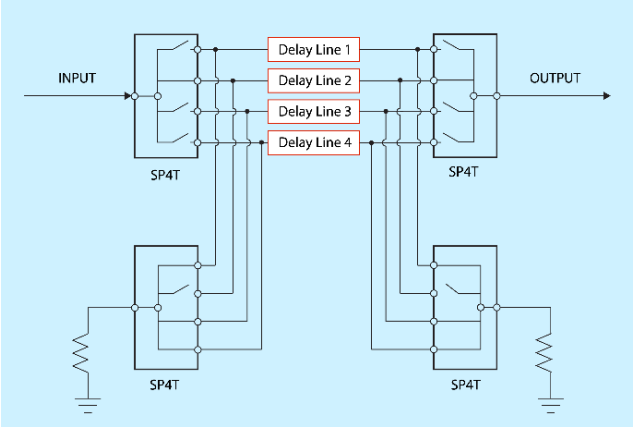


Figure 68. Terminating RF MEMS switch schematic.

Here the feature of the MM5140 switch to be able to control all 4 contacts independently is used to close 3 contacts at a time in a single SP4T switch.

The assembly of this arrangement requires a shorting pin at the end of each track, directly below the top RF MEMS switch, connecting to another RF MEMS switch on the bottom side of the PCB. This does require a manufacturing technology called Via in Pad (VIP) as the via is right in the middle of the pad for the LGA packages and this fabrication technology is not widely available.

One consequence of installing a via through the PCB is to effectively have a little antenna within the PCB which has the undesired effect of radiating energy into the substrate. Fortunately, terminating the tracks through this shorting via has the effect of stopping any radiation.

Figure 69 and Figure 70 show the energy on the top surface of the PCB, with the longest track switched into circuit, without the shorting vias terminated and with them terminated.

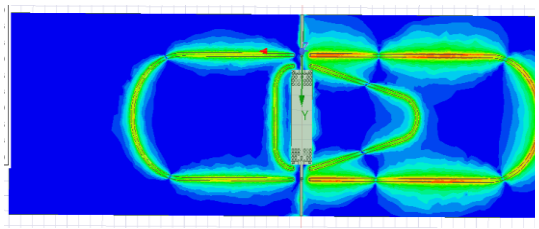


Figure 69. Electric field strength with shorting via not terminated.

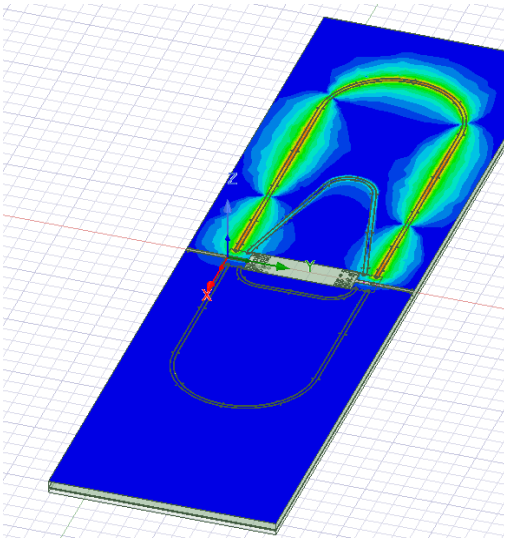


Figure 70. Electric field strength with shorting via terminated.

4.1.10. Matching Network

The MM5140 on its own has a reasonable input match to a 50 Ω transmission line, 12 dB to 15 dB up to 6 GHz, (see Figure 53.) and shown here on a Smith chart (zoomed in), in cyan. This was improved slightly with a simple "L" section of a series inductor and shunt capacitor to achieve the red trace which shows a slight improvement in the group delay ripple in simulations.

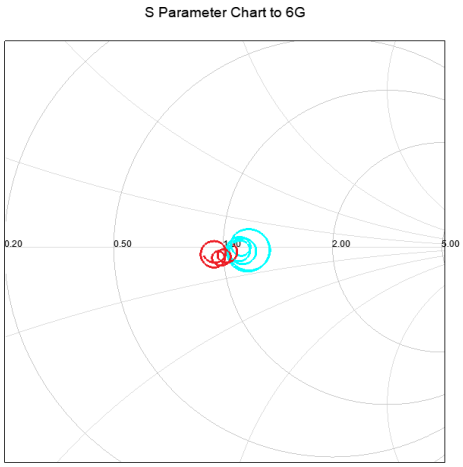


Figure 71. Input impedance of RF MEMS switch, native cyan and with matching network in red.

The importance of impedance matching will be discussed in much more detail in the results section 4.4.7.

4.1.11. System parameter Simulation

A full mathematical simulation was developed in MATLAB to analyse the performance of an 8-element linear array with half-wavelength element spacing at 6 GHz, where each element

was fed by an independently controlled TDU. The model was designed not only to evaluate array performance but also to systematically explore the interactions between key design variables, such as the number of control bits and quantisation levels and their impact on beamforming accuracy, sidelobe levels and pointing errors. Understanding these relationships was a key objective, providing insight into the trade-offs inherent in TDU-based time delay implementations. The TDUs were configured to achieve the required time delay for ±45° scanning, while a fixed Chebyshev gain profile was applied to ensure -20 dB sidelobes at boresight. This amplitude profile remained constant, as its effect primarily scaled the results without altering relative trends.

The level of -20 dB for the sidelobes was chosen as a balanced trade-off between being low enough to reveal any unwanted sidelobes introduced by quantisation effects, yet not so stringent as to be unattainable for an 8-element array. This level ensures that the analysis remains both meaningful and practical, capturing the impact of quantisation while reflecting realistic performance constraints inherent to small array configurations.

Of course, in practice, sidelobe control is critical for ensuring the efficiency and reliability of phased array systems, as excessive sidelobe levels can lead to unintended signal reception, interference and reduced system performance. In radar applications, high sidelobes increase susceptibility to clutter and jamming, reducing target detection accuracy and system sensitivity. In communication systems, such as satellite and 5G networks, poor sidelobe suppression results in unwanted interference with adjacent channels or networks, degrading signal quality and reducing spectral efficiency.

The MATLAB program evaluates multiple combinations of the following system parameters:

- Scan angle, from -45° to 0°, 30 steps.
- Number of TDU control bits i.e. the number of quantisation levels for the TDUs. Simulated 2 to 8 bits inclusive.
- The LSB quantisation value. Here the LSB was varied between TDUs as all TDUs do not have to achieve the same range of time delay. This option was introduced as a method to reduce sidelobe levels and will be discussed in greater detail in chapter 5.2.
- Frequency, from 0.4 GHz to 6 GHz, 50 steps

For each set of the system parameters, the simulated performance was compared to the ideal Array Factor (AF) performance to quantify beam pointing error, sidelobe level increases and any amplitude loss.

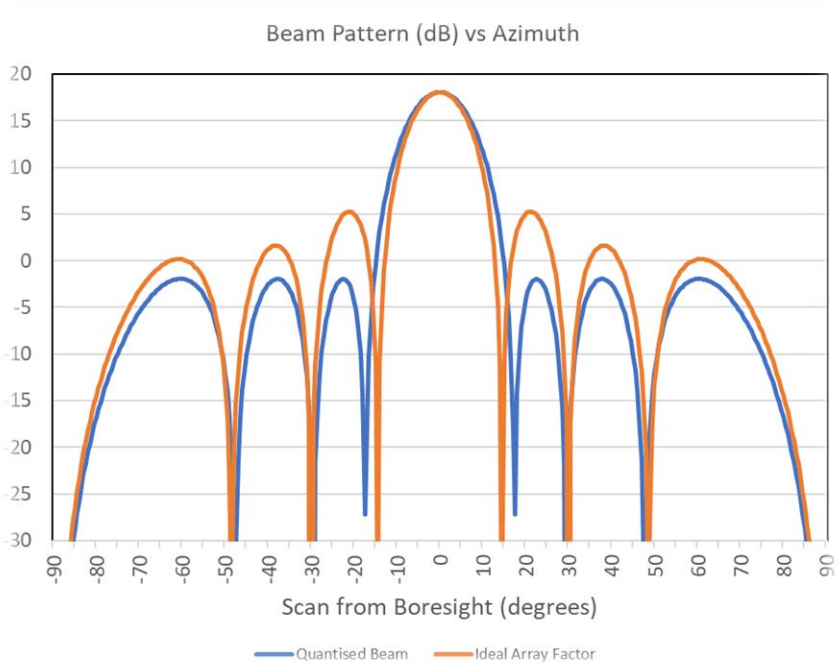


Figure 72. Reference beam pattern (AF Beam) vs array model with digital time delay units and amplitude profile.

Figure 72 shows the starting point with the reference beam pattern, the "Ideal Array Factor", for an eight-element linear array at 6 GHz and half wavelength element separation compared to the "Quantised Beam" which has the digital TDUs in series with each array element and is the subject of the investigation of the impact of varying the design parameters. The quantised beam shows the Chebyshev amplitude profile giving a slightly wider main beam and sidelobes down -20 dB so as to help reveal any imperfections that might be hidden by the normal -13 dB sidelobes of the ideal AF.

For comparison, Figure 73 shows a scan to -45° at 6 GHz. Note the broadening of the main lobe in the quantised beam.

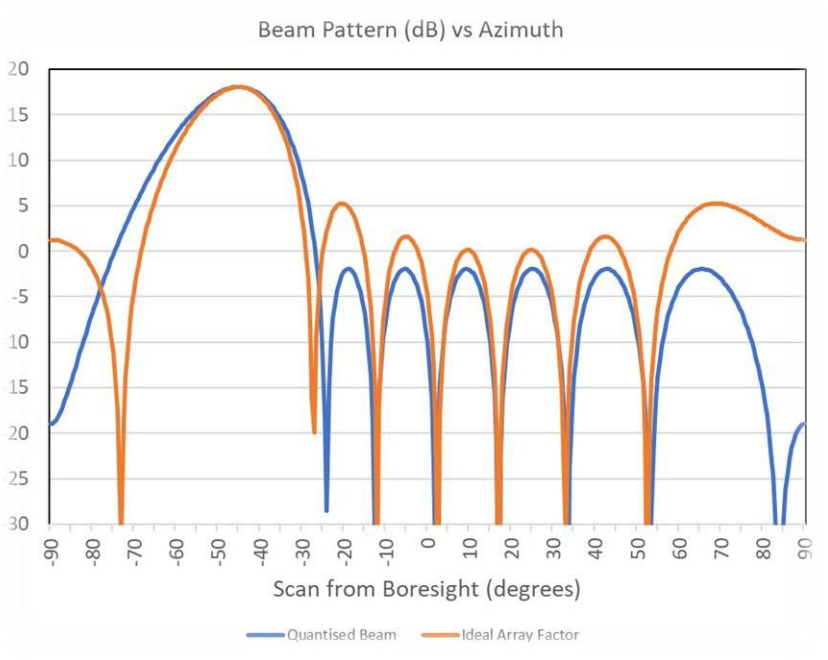


Figure 73. Beam scan 45° at 6 GHz.

In the case of the low frequencies, sidelobes are not always evident and so the simulation doesn't give any data for sidelobe levels under these circumstances. See Figure 74.

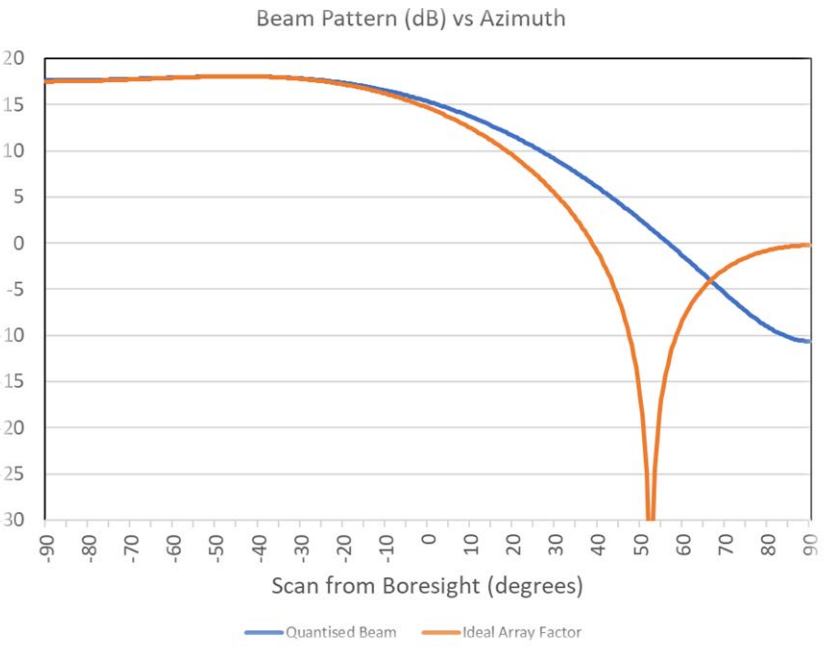


Figure 74. Beam scan -45° at 1 GHz.

The maximum time delay required is 413 ps, so if using 4 control bits, the least significant bit (LSB) is 27 ps, being one fifteenth of the maximum delay required.

Starting with each TDU exactly the same, the simulation gives the results in Table 7. The maximum values are the worst case for any frequency and any scan angle. The RMS and average values are across all scan angles and all frequencies.

Number of Control bits	Maximum pointing error (degrees)	RMS pointing error (degrees)	Max. QSLL (dB below beam peak)	Average QSLL (dB)	Max. amplitude error (dB)
2	93.4	26.612	-1.282	-4.575	-2.990
3	3.693	1.542	-3.853	-7.204	-0.603
4	1.993	0.852	-10.097	-12.991	-0.162
5	0.669	0.298	-14.229	-16.127	-0.025
6	0.362	0.166	-16.820	-17.959	-0.006
7	0.203	0.089	-18.318	-18.991	-0.001
8	0.124	0.053	-19.133	-19.497	-0.001

Table 7. Simulation results for all TDU the same.

As expected, the performance improves with an increasing number of control bits.

Starting with the pointing error, the quantised beam, (i.e., the beam formed by the quantised time delay units), oscillates about the true beam direction, under pointing (i.e., pointing less than the desired scan angle) and then over pointing as the beam is scanned. Obviously at some scan angles there is no pointing error. The RMS pointing angel error is the root mean square of all the errors over the 45° scan at all frequencies. The maximum pointing error is the exception and only occurs once or twice across the scan angle, always towards the edge of the scan range.

Notice that with 2 bits, the maximum pointing error is 93.4°. There is a peculiar beam pattern formed from 4 GHz to 6 GHz. See Figure 75 for an explanation. In this case the sidelobe is bigger than the main beam and hence it has been detected as the main beam, but 93.4° away from the desired angle.

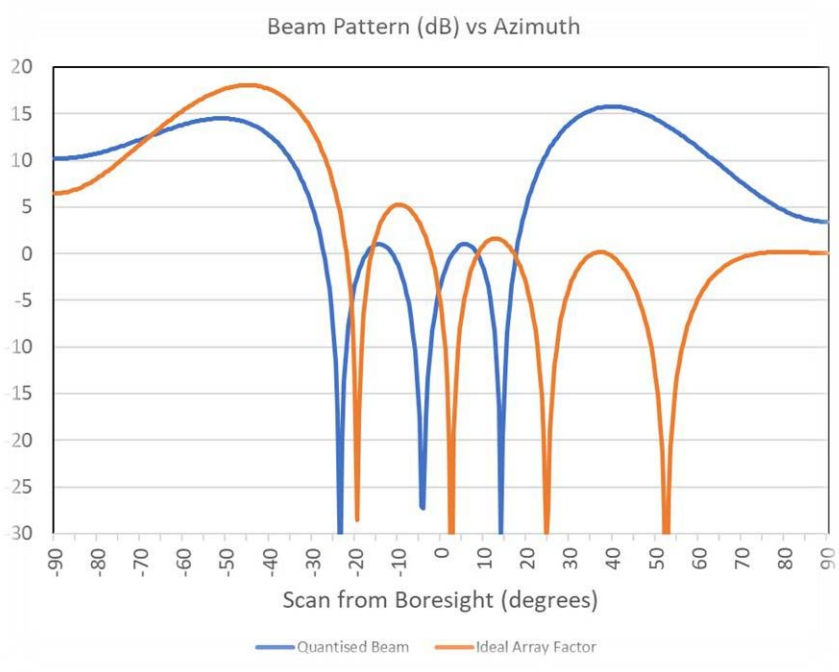


Figure 75. Beam pattern at 4 GHz and 2 control bits.

Figure 76 is a plot of every beam pointing error at every frequency and every scan angle with b = 4, four control bits. Notice how the error is independent of frequency and the worst-case pointing error only happens at 1 scan angle, 38.8° in this case.

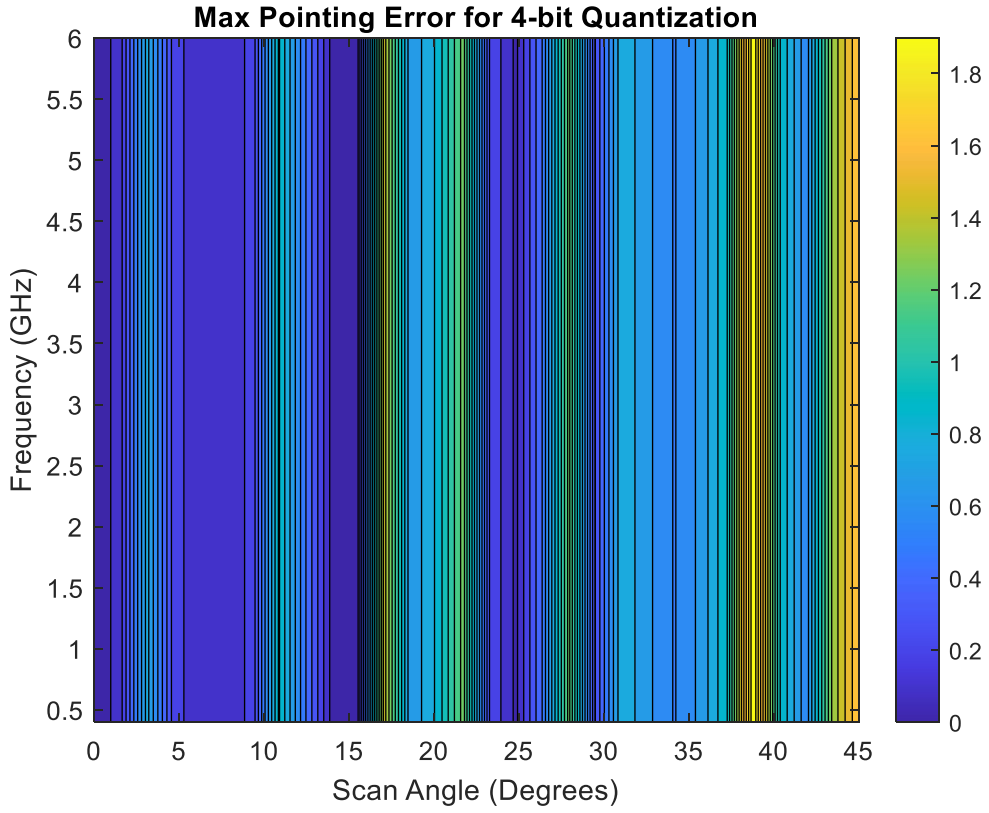


Figure 76. Display of the beam pointing error with b = 4 for every frequency and scan angle up to 45°.

Table 8 gives a comparison of the beam pointing error as derived from the simulation compared to the results of using equation (2.7). Ignoring b=2 for the reasons already discussed, the simulated results are slightly larger than the theory, however not unexpected as the equation is an approximation and with as N=8, this is a small array and statistically a small sample. Interestingly, if equation (2.6) had been used, where the phase error is taken as equal to the LSB, then the theoretical error values would double and then the simulation results would all be less than theory. Seems appropriate that the simulation results fall in the middle.

Bits	Simulated Error	Theoretical Error
2	93.400	4.436
3	3.693	2.216
4	1.993	1.108
5	0.669	0.554
6	0.362	0.277
7	0.203	0.138
8	0.124	0.069

Table 8. Beam pointing error (degrees) simulation results vs formula.

Next, considering the sidelobe level produced by having quantised time delay units, a typical profile of the QSLL is shown in Figure 77 for a scan of 0° to 45° at 6 GHz with 4 control bits and Figure 78 is a complete display of all QSLL levels for all frequencies and scan angles.

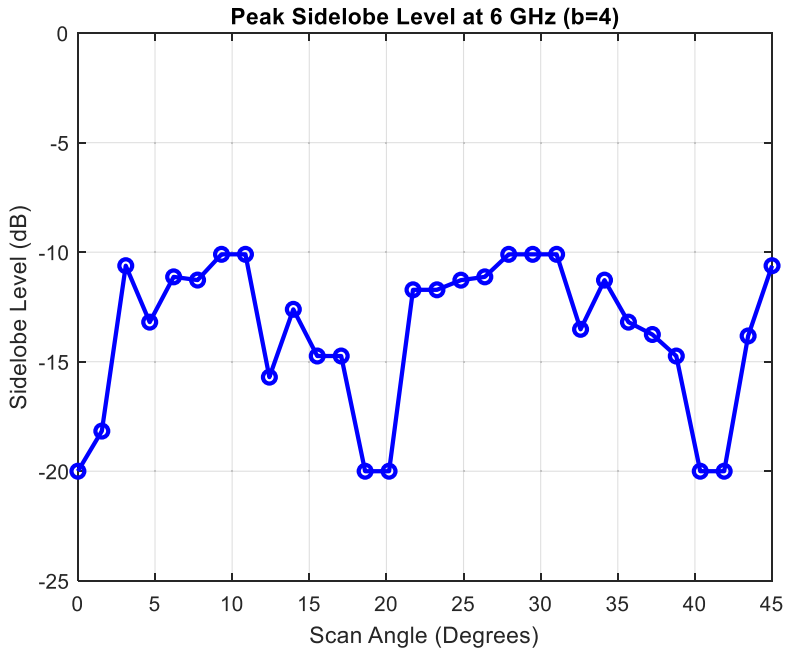


Figure 77. QSLL for 4 bits at 6 GHz.

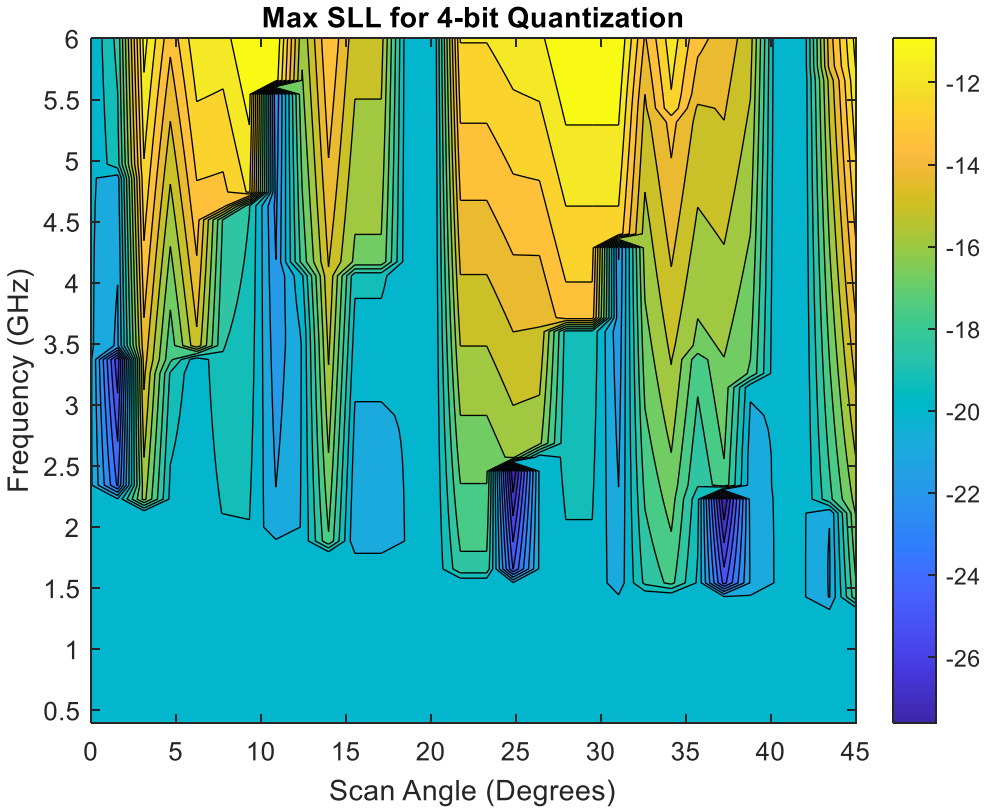


Figure 78. QSLL levels for all scan angles and frequencies with b = 4.

As expected, the profile follows the shape of Figure 77, with elevated sidelobes for most scan angles and at some scan angles the sidelobes are “perfect” in that they are as low as possible given the Chebyshev amplitude profile designed to achieve -20 dB sidelobes.

The sidelobes degrade with increasing frequency. The sidelobes are about 4 dB lower at 2 GHz as compared with 6 GHz, for both the average value and the worst case.

The simulation shows the sidelobes to be sensitive to the number of control bits with only - 3.8 dB peak sidelobes achieved with 3 control bits. Four control bits improves this to -10 dB but this is still high. Eight bits is required to get close to the floor of -20 dB.

Lastly, considering the amplitude error, see Figure 79. The profile of the amplitude error is similar to the QSLL profile in that at the same scan angles where the QSLL is -20 dB, the amplitude error is zero. The amplitude error is sensitive to frequency and at certain scan angles, although never to a large degree.

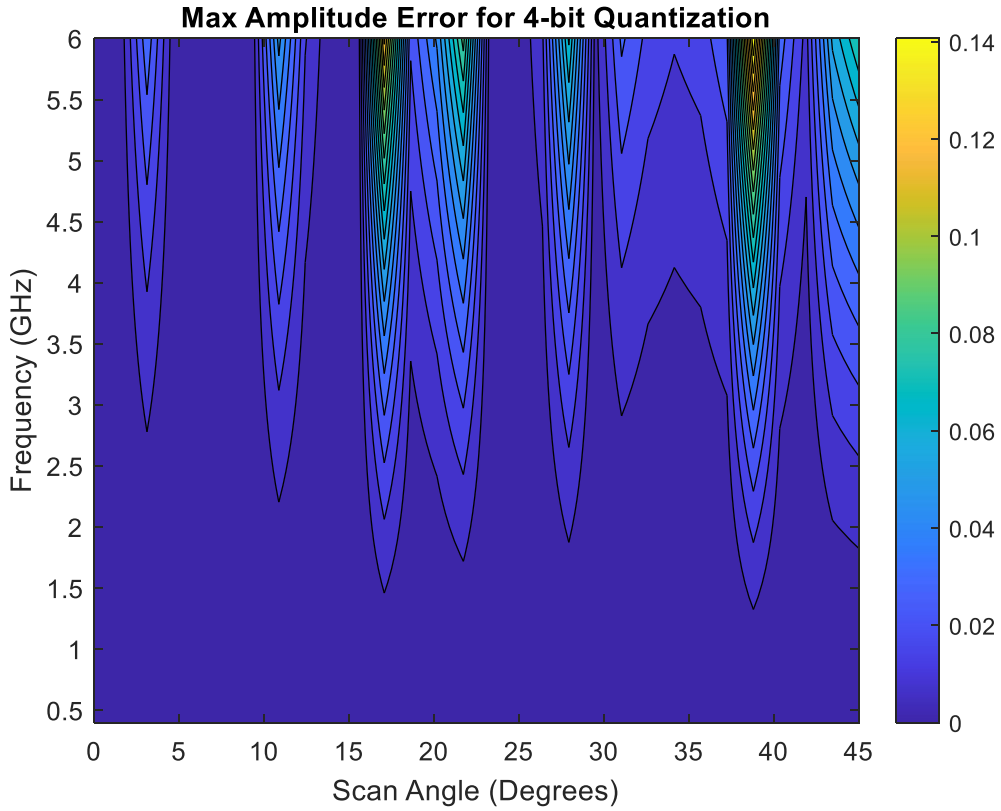


Figure 79. Amplitude error (dB) for all frequencies and scan angles with b = 4.

With 2 bits the error is nearly 3 dB, falling to practically zero with 8 bits.

Finally, a plot of the array factors for 0.4 GHz, 3.2 GHz and 6 GHz showing no beam squint at a scan of 45°. See Figure 80.

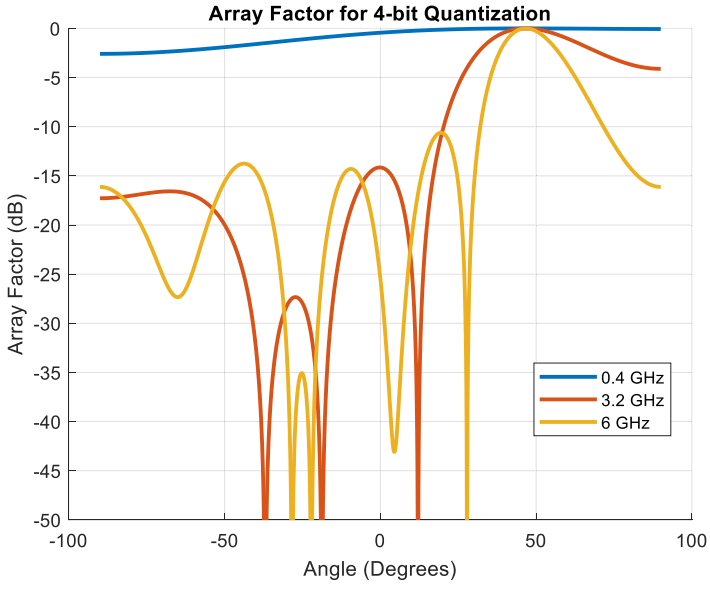


Figure 80. Array factors for 0.4 GHz, 3.2 GHz and 6 GHz with b = 4 and scanned to 45°.

In practice, it seems the question of acceptable sidelobes is the limiting factor in deciding the number of control bits to implement.

One new and efficient methodology for breaking up patterns of phase errors to help reduce sidelobes and grating lobes for no penalty is presented in chapter 5. This new technique has the added advantage of also reducing the real estate required for a BFN.

4.2. Fabrication and Practical Implementation

Bringing together the switched line architecture of Figure 51 and the termination strategy of Figure 68, a final PCB layout is shown here in Figure 81. The coarse bit selection is on the bottom and has the longer CBCPW tracks. The shortest track is the reference track. On the top is the fine bit selection. The pads for the RF MEMS switches are where the tracks converge, a total of 4 switches. Table 9 summarises the design lengths of each delay line. The input (shown on the bottom of the layout), output (at the top of the layout) and interconnect lines are designed to be 50 Ω, whereas the delay lines use 54 Ω to balance return loss across 0.4-6 GHz when cascaded with switch parasitics. Table 10 lists the CBCPW dimensions for the 50 Ω (Z1) and 54 Ω (Z2) tracks.

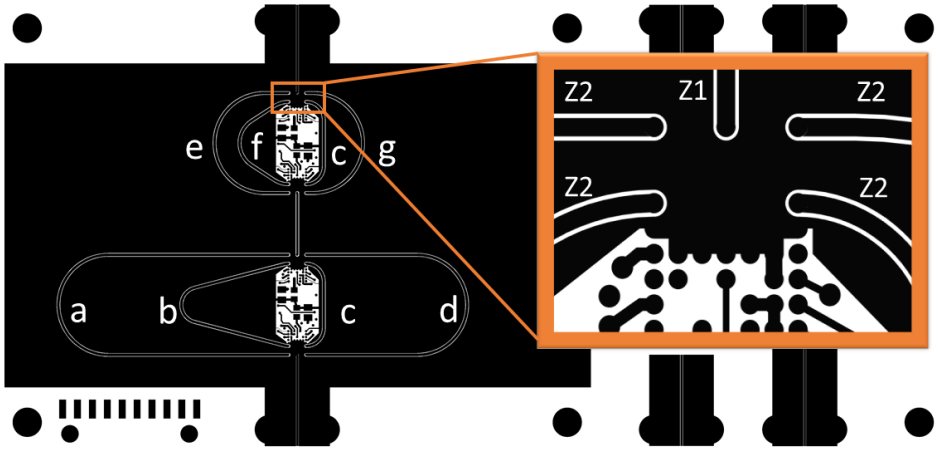


Figure 81. Final TDU PCB layout showing the 7 delay lines (a-g) and the tracks under the RF MEMS switch along with their characteristic impedances Z1 and Z2.

Delay Line	Length (mm)	Delay Line	Length (mm)	Delay Line	Length (mm)
a	88.14	d	64.57	f	23.32
b	41.00	e	35.10	g	29.21
c	17.43				

Table 9. Delay line design lengths.

Track	Impedance (Ω)	Track Width (mm)	Gap Width (mm)
Z1	50	0.43	0.10
Z2	54	0.39	0.12
RO4003C, h=0.508 mm, t=1 oz.			

Table 10. CBCPW track impedance and dimensions.

Shown in Figure 82 is the extent of the electric fields around each track if they are each excited. Note also the numerous vias running down the middle of each loop of delay line so as to minimise coupling of earth currents between tracks. The input and output lines are shown on the left and right of the looped delay lines.

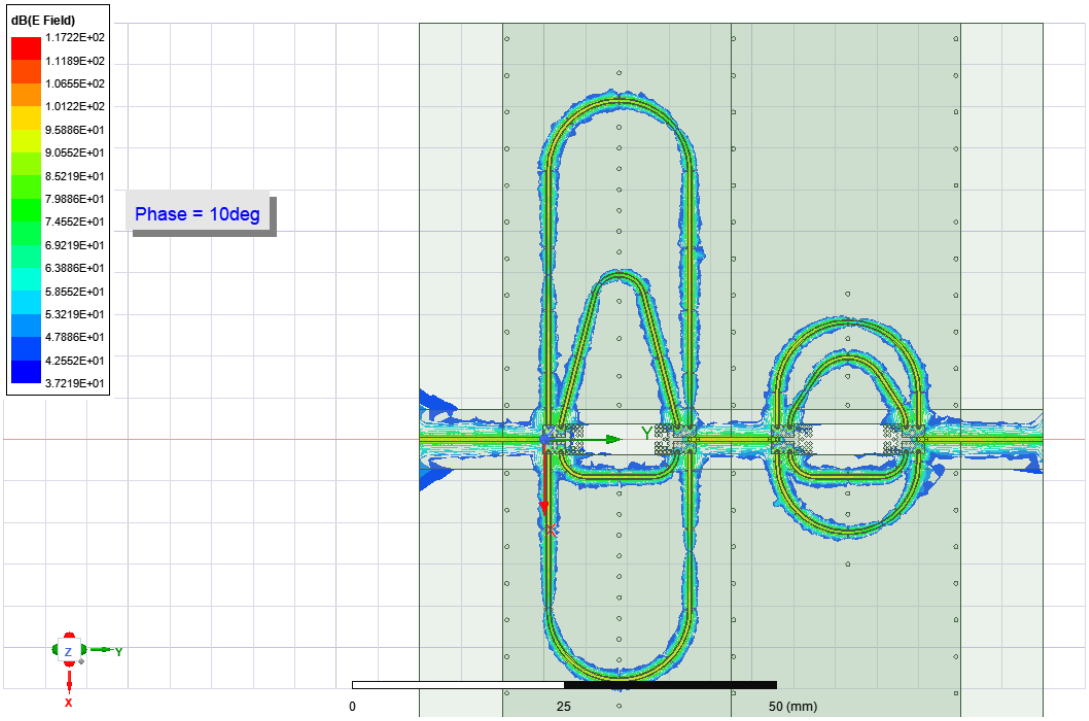
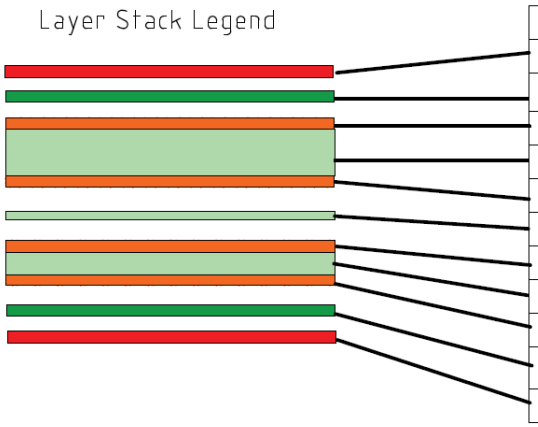


Figure 82. Simulation of electric fields around each delay line when in circuit.

The final design was for a 4-layer PCB with extra copper layers required to run all the power lines and control lines to each of the 8 RF MEMS switches. The layer stack is shown in Figure 83, showing the microwave dielectric substrate, Rogers RO4003 and an FR4 layer for the control / power tracks.

Each of the Rogers substrate and the FR4 board has 2 sides of copper (1 oz for the RO4003) and these were sandwiched together with a thin layer of prepreg.

Rogers RO4003 is a hydrocarbon ceramic laminate. It was chosen because it is readily available and can be fabricated using standard epoxy/glass (FR-4) processes. The FR4 not only provides 2 layers of copper, it also gives the finished PCB rigidity and strength as the RO4003 on its own would be too flexible.



Layer Name	Type	Material	Thickness (mm)
Top legend			
Top soldermask	Taiyo PSR 4000	LPI	0.0210
Layer 1		Copper	0.0350
Dielectric 1	RO4003	Core	0.5080
Layer 2		Copper	0.0350
Dielectric 2	High Tg FR4	Prepreg	0.1220
Layer 3		Copper	0.0350
Dielectric 3	High Tg FR4	Core	0.4750
Layer 4		Copper	0.0350
Bottom soldermask	Taiyo PSR 4000	LPI	0.0210
Bottom legend			

Figure 83. PCB Stack layout.

Figure 84 shows the detail of each of the four layers and Figure 85 is 3D depiction of some of the detail around the switches.

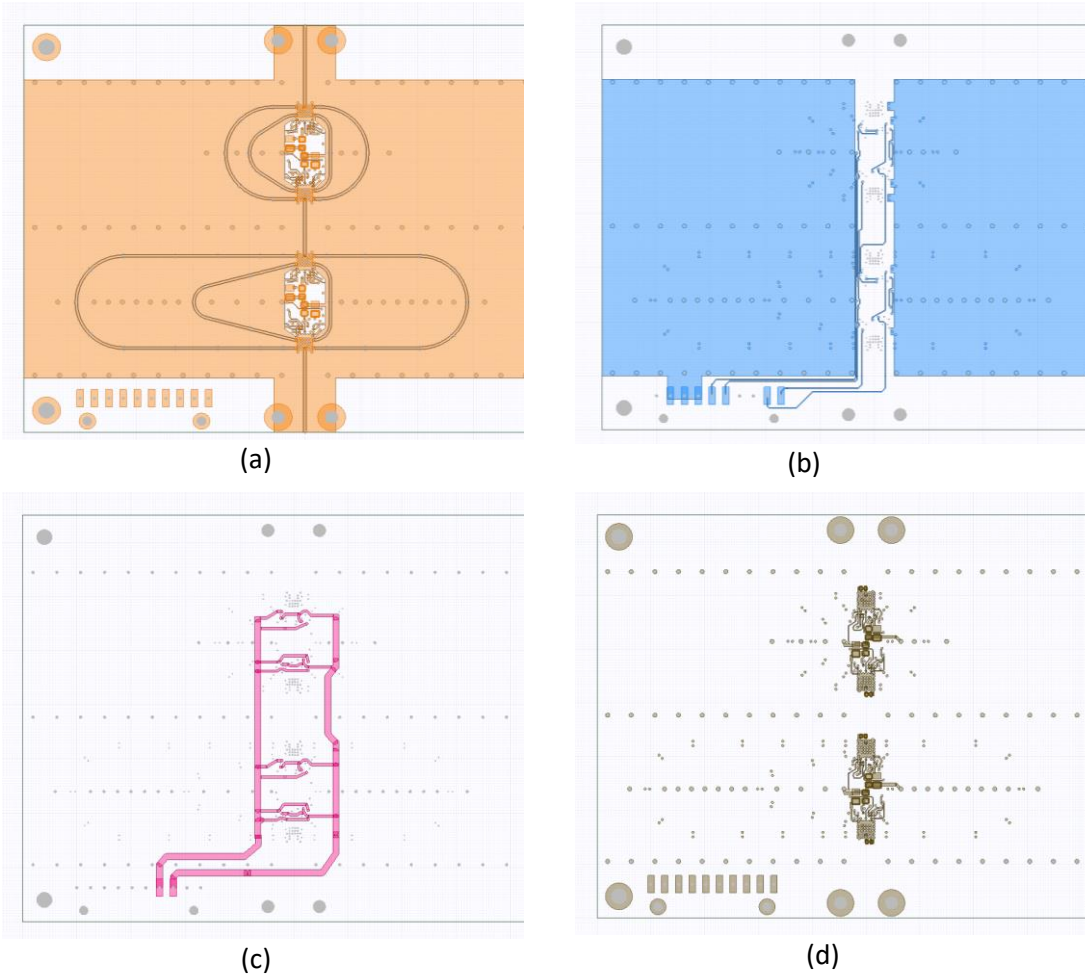


Figure 84. Four layers of PCB. (a) Top layer with CPW tracks. (b) Ground plane and control lines. (c) Power distribution. (d) Bottom layer showing terminating switches.

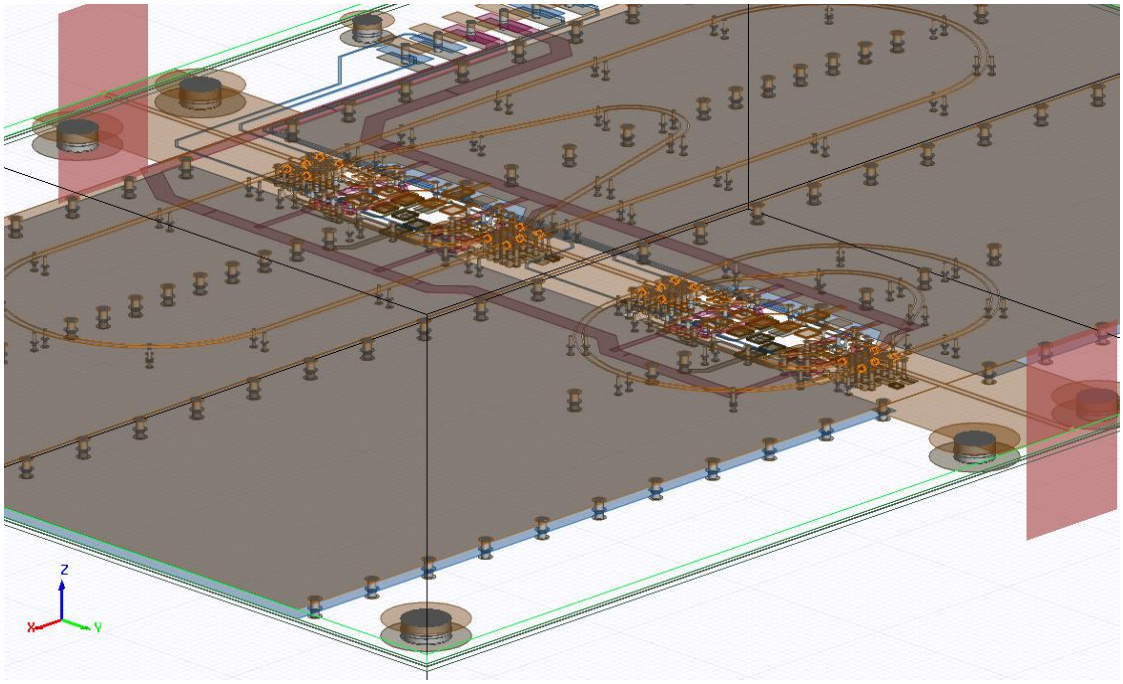


Figure 85. 3D depiction of PCB.

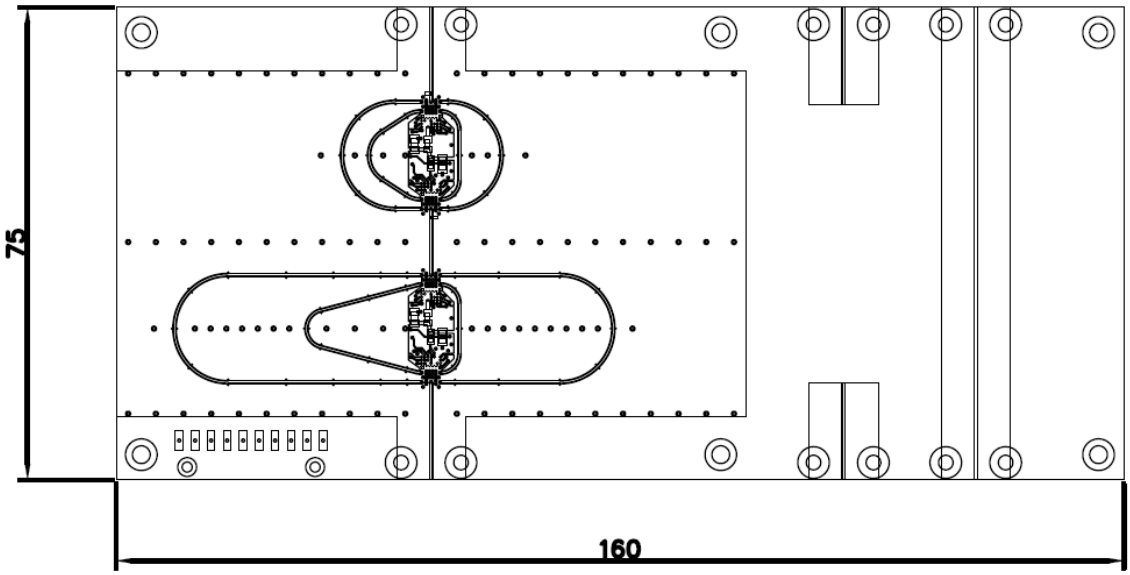


Figure 86. PCB outline drawing.

The final outline drawing is shown in Figure 86, showing the test tracks that were included; a straight-through 50 Ω line and 2 open circuit lines the same length as the input and output lines to the RF MEMS switches. These test tracks are necessary so as to be able to test for the actual impedance and dispersion performance of the final PCB and to be able to de-embed the performance of the TDU from the input and output tracks and SMA connectors.

4.2.1. Schematic

The final schematic diagram is shown here in Figure 87.

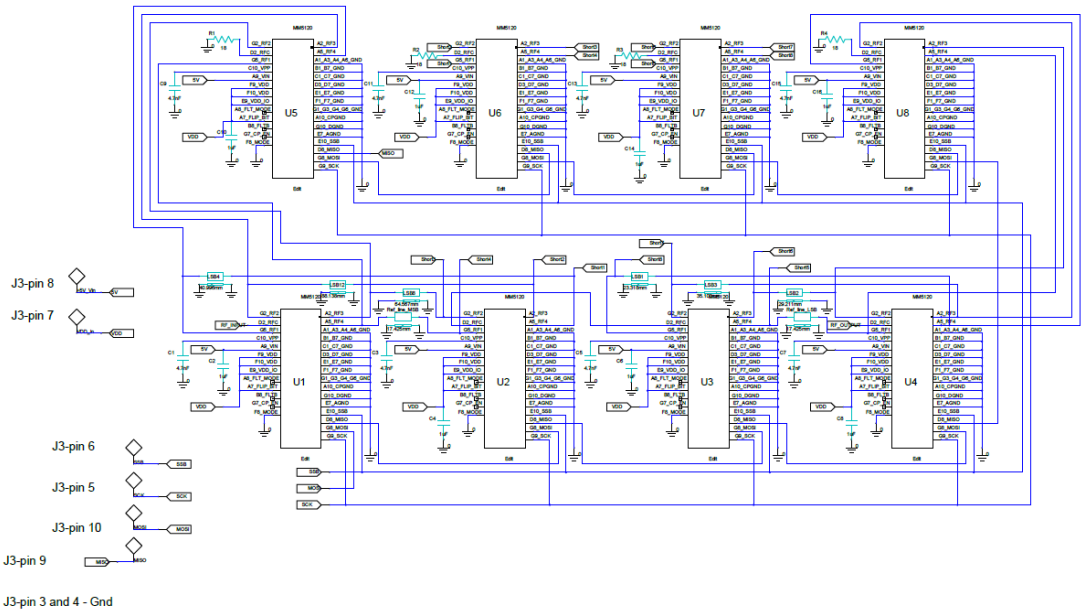


Figure 87. Final TDU Schematic.

4.2.2. Design for Manufacture (DFM)

Although fabrication is not the topic for this thesis, it consumed a lot of time and effort and is worth mentioning briefly just to highlight the fact that integration of RF MEMS switches and microwave transmission lines is not trivial and requires attention.

Really DFM means understanding the limitations of PCB manufacture and making sure that a design can actually be built.

In modern PCB manufacturing a commonly accepted tolerance for the accuracy of etching is ±0.002 inches (±2 mils or approximately ±50 micrometres). This means that for a designed trace width, the actual width after fabrication can vary by up to 2 mils above or below the specified dimension. Therefore, there is no point specifying a track width with greater precision than 2 mils or 0.05 mm. This can be a limitation with CPW as the gaps are very small and small discrepancies can change the line impedance significantly.

The placement of a via in a pad is a relatively new capability and not offered by every PCB manufacturer. There is a problem in that the via can suck away the solder from adhering to the pads on the IC, resulting in a dry joint.

Typically, a plated through hole (PTH) aspect ratio is 4:1, so for a 1.6mm PCB, the smallest via hole will be 0.4mm diameter, i.e., the hole can't be smaller because of the electroplating.

The aspect ratio for blind and buried vias is typically 1:1, so much larger than PTH, so limiting the size of blind and buried vias.

As an example of the tight tolerances, a change of just 0.025mm in the width of the CBCPW track, keeping the overall width of the track and gaps the same, results in a change in line impedance from 50 Ω to be 54 Ω and 0.025 is just half the manufacturing tolerance.

For this research work, the biggest challenge in manufacture was successfully soldering the RF MEMS switch LGA to the PCB. In the end this was done by hand as the automated process failed to solder all pads, either from too little solder paste or dips in the pads taking most of the solder paste. Initial prototypes had many dry joints, which were difficult to isolate as the suspicion was always that there were other faults when in fact it was just dry joints.

4.2.3. Reliability Calculation

Considering the TDU with four switches in series, the probability of the system working is the probability that all 4 switches remain operational. (Note that there no consideration of the four switches used to terminate the unused tracks as these would not be included in any final design, as will be discussed in the chapter on results.)

Using the data from section 2.7.3, the system reliability follows a series reliability model

$$P_{System} = P_{Switch}^4 . \tag{4.3}$$

- At 3 billion cycles, where $P_{Switch} = 98.9\% : \ then \ P_{System} = 0.989^4 = 95.7\%$
- At 10 billion cycles, $P_{Switch} = 90.0\% : \ then \ P_{System} = 0.9^4 = 65.6\%$
- At 20 billion cycles, $P_{Switch} = 50.0\% : \ then \ P_{System} = 0.5^4 = 6.25\%$

This means:

- At 3 billion cycles, the TDU has a 95.7% chance of still functioning correctly.
- At 10 billion cycles, there is a 34.4% probability of failure.
- By 20 billion cycles, failure is highly likely (only 6.25% probability of all 4 switches still working).

In conclusion, if the operational TDU use is to beyond 3 billion cycles, then there needs to be consideration for failure rates, either system-level redundancy or error correction techniques such as reconfigurable switching paths or bypass mechanisms, to help mitigate failure risks.

On the other hand, if switching cycles are infrequent (e.g., occasional reconfiguration in a phased array), then the RF MEMS lifetime is effectively very long, making it highly suitable for long-term deployment.

4.2.4. Finished Product

Below are photographs of the finished TDU PCB showing the looped CBCPW delay tacks on the top layer, the 4 RF MEMS switches (black ICs) on the top and bottom and the pin header (bottom left, top side) for the power and SPI control. The extra copper dimples are to balance the weight of copper on all layers to help stop warping.

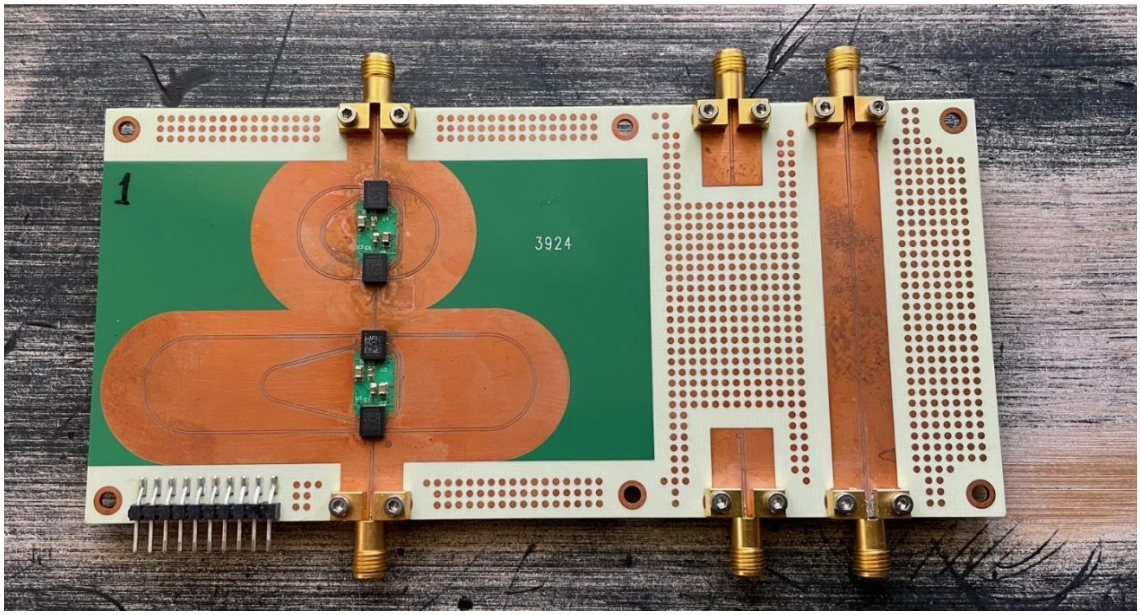


Figure 88. Finished PCB – Top Side, showing TDU and calibration tracks.

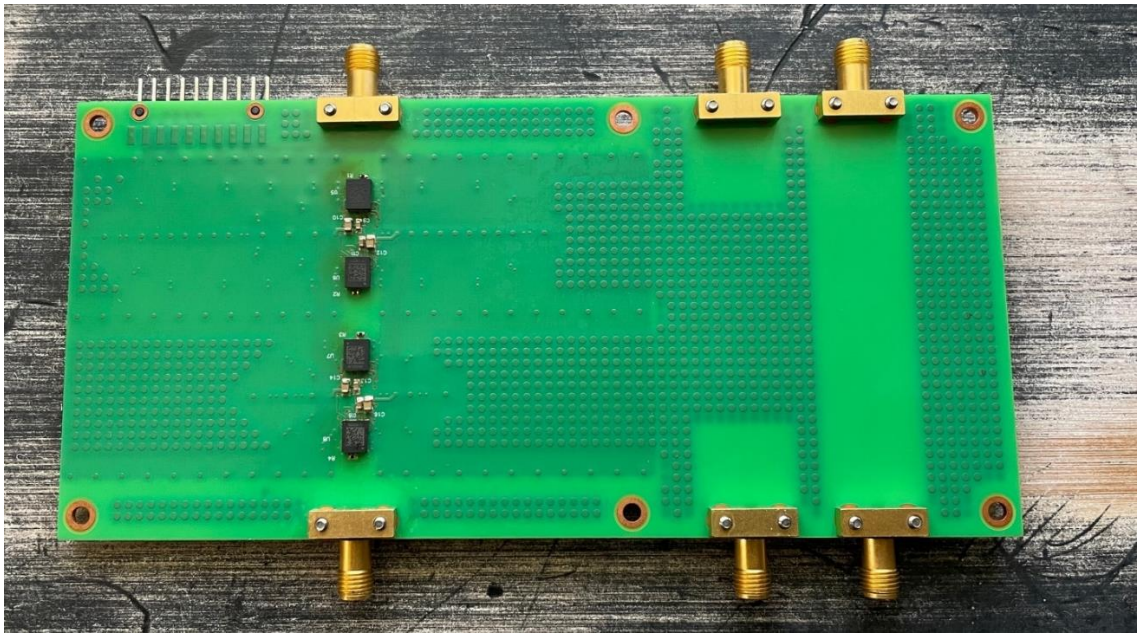


Figure 89. Finished PCB – Bottom side showing RF MEMS switches.

4.3. Electromagnetic Simulation and Analysis

Full TDU performance simulation was achieved by doing a co-simulation of the lumped element model for the RF MEMS switch along with a full EM (electromagnetic) simulation of the 4-layer PCB using Ansys “HFSS 3D Layout”.

The final schematic of the full co-simulation is shown in Figure 90. The block in the middle is the full EM simulation results for the PCB layout and the RF MEMS switches are the 8 blocks at the edges, modelled as a lumped elements as per Figure 52.

Ansys HFSS offers two different approaches to 3D EM simulations:

- HFSS FA3D - Fully Arbitrary 3D (also called MCAD – mechanical CAD).
- HFSS 3D Layout - 3D FEM (Finite Element Method) in layered structures, sometimes referred to as ECAD – electronic CAD.

The first, as the name suggests, is for any 3D structure and the second is specifically for structures in layers, such as a PCB. It understands pads and components etc.

Early simulations of the CBCPW design were done with HFSS FA3D and when it was time to add the control tracks for the final design, HFSS 3D Layout was used to route all the control lines and vias. Final EM simulations were in HFSS 3D Layout.

As would be expected, there was very little difference in comparing the EM simulation results of the two versions of HFSS.

One observation, it is not recommended to follow this workflow. HFSS 3D Layout is not a PCB layout tool, it has none of the sophistication of Synopsys, Mentor Graphics or Altium for example. There is no automatic routing or netlist checking. Fortunately, there were only a small number of control tacks to run for this research work but it took considerable time to manually place and check control lines. The preferred workflow would be to layout the PCB in Altium, or similar and then to pass to HFSS 3D Layout for the EM simulation.

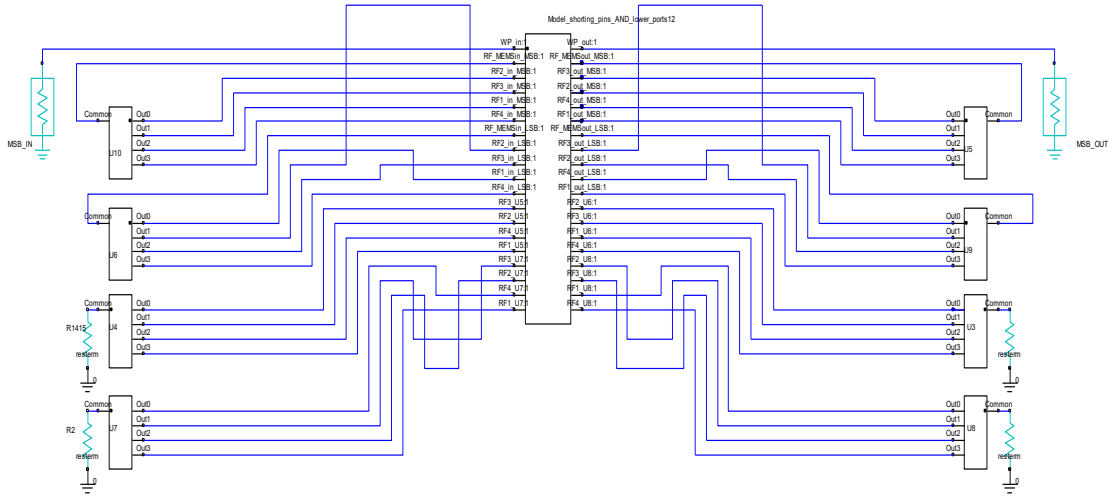


Figure 90. Schematic of co-simulation.

Figure 91 gives an example of the EM simulation for the completed PCB, including all the power and control lines, showing the electric field strength. The top layer (a) shows the excited tracks, the longest delay path and how the other tracks are not carrying energy. The ground plane (b) shows how well confined the energy is and that it is not coupling to the other tracks. Also of note is that the control lines are not coupling energy through the board. The next plot is the electric field strength inside the microwave substrate (c) and inside the FR4 substrate on the bottom (d).

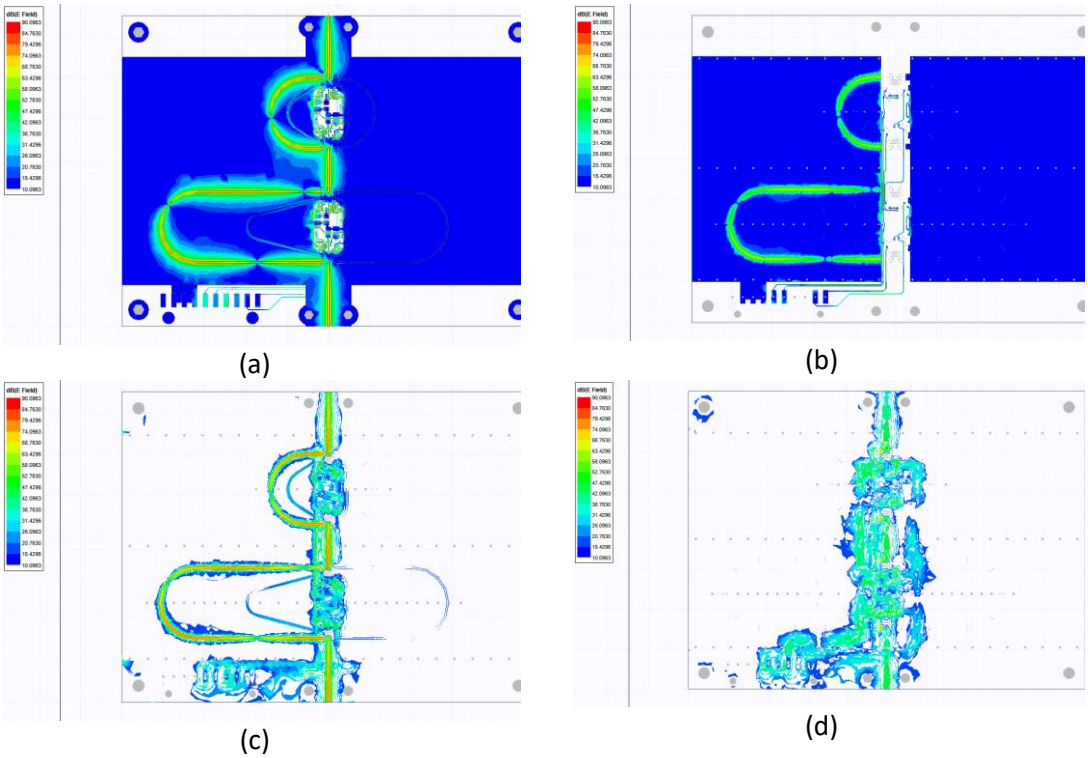


Figure 91. EM simulation of the electric field strength for each of the 4 layers of the PCB (a) Top layer, (b) ground plane, (c) microwave substrate and (d) the FR4 substrate.

4.3.1. Simulation Results

The following figures give the simulation results for the insertion loss ($-20\log|S21|$), the return loss ($-20\log|S11|$), the absolute group delay, i.e., the total group delay including the reference line and finally the relative group delay, i.e., the delay of each track in excess of the reference line.

4.3.1.1. S21 (dB)

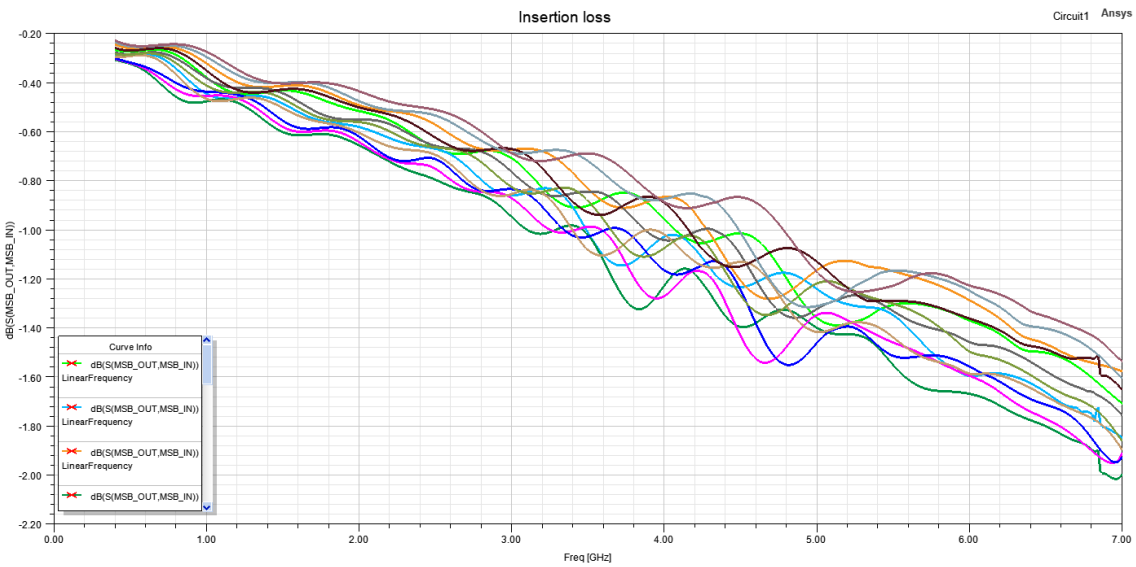


Figure 92. Simulation result S21 (dB).

The average insertion loss is 0.82 dB with a maximum loss of 1.68 dB, within the frequency band of operation. At 6 GHz the loss ranges from 1.21 dB to 1.68 dB, indicating that the difference in levels between zero delay and delay state 15 is expected to be just 0.47 dB. The simulation model for the switches indicated a loss per switch of 0.2 dB, (times 4,) giving a line loss range at 6 GHz of 0.41 dB to 0.88 dB.

4.3.1.2. S11 (dB)

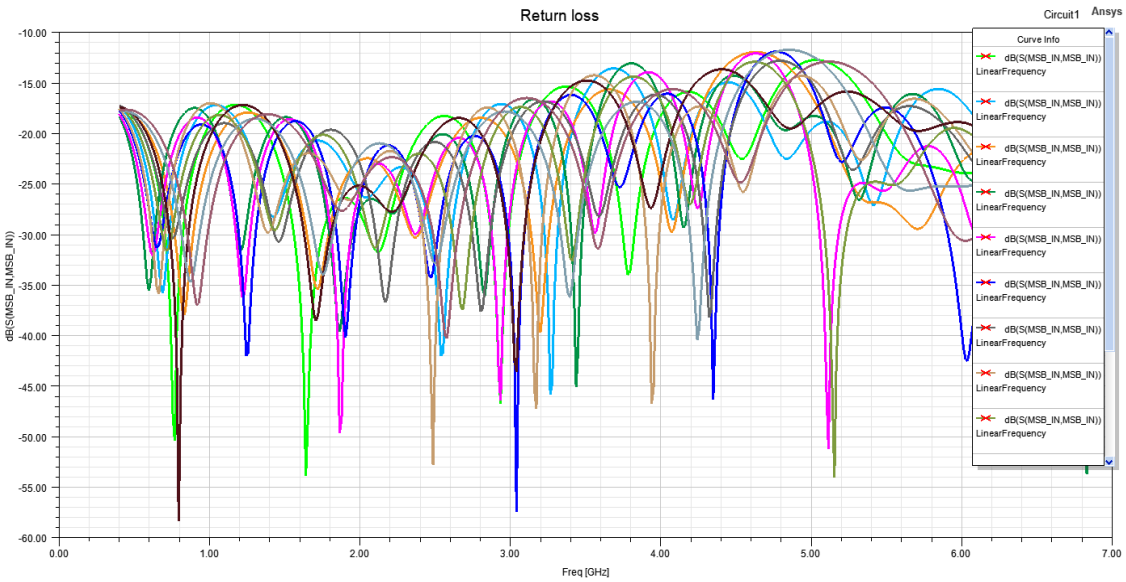


Figure 93. Simulation result S11(dB).

The return loss is acceptably all below 10 dB. That said, there is little margin for error as the worst case return loss is just 12 dB.

4.3.1.3. Group Delay (Absolute)

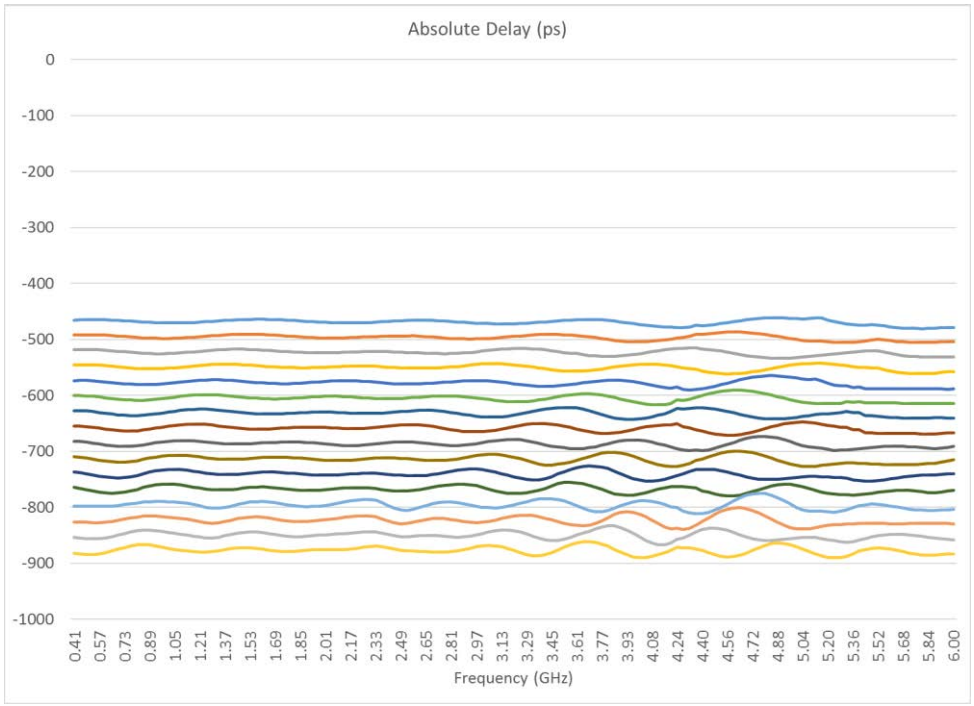


Figure 94. Simulation result absolute group delay (ps).

The absolute delay gives the total delay through all the reference lines and RF MEMS switches, just to indicate there is a considerable delay over and above the relative delay of the switched delay lines, shown below.

4.3.1.4. Relative Group Delay

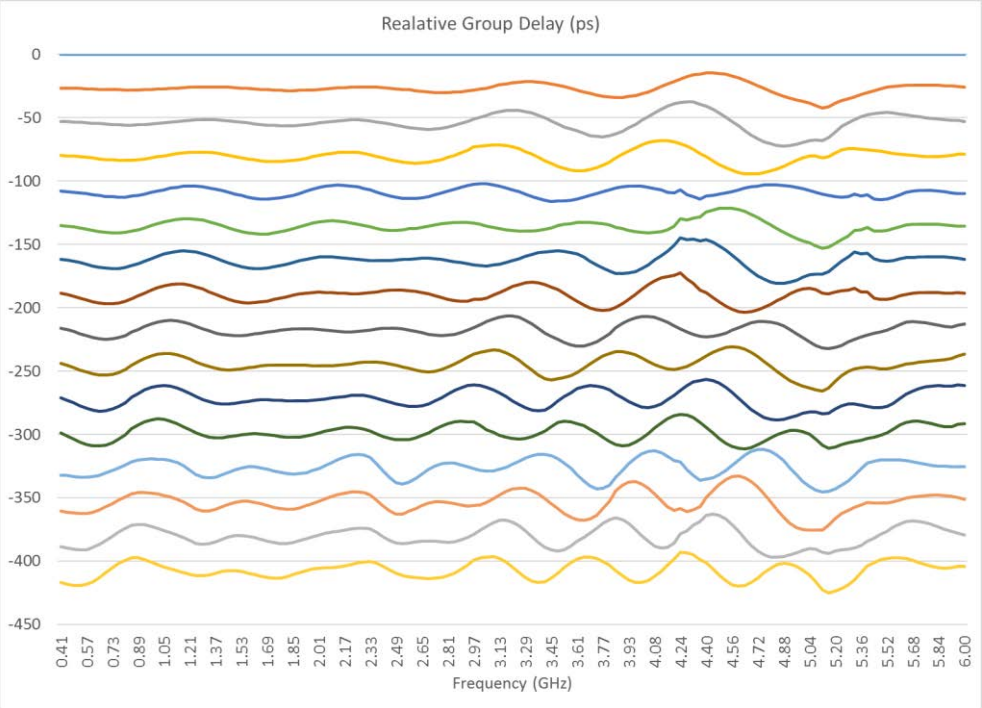


Figure 95. Simulation result group delay (ps).

To quantify the performance, the Mean Absolute Error (MAE) is used to measure the accuracy of the delay value and the standard deviation indicates the amount of ripple about the mean. The absolute value of the error is used as this avoids any reversion to zero because of positive and negative values,

$$MAE = \frac{1}{N}\sum_{i=1}^{N}\left| t_{simulated\_i} - t_{ideal} \right|, \tag{4.4}$$

where N is the sample size, $t_{simulated}$ is the simulated time delay and t_{ideal} is the ideal or design delay value.

MAE values for each delay step are given in Table 11.

Overall, for all values at all frequencies and all delay settings, the MAE is 5.56 ps with a standard deviation of 6.78 ps. This indicates a very small accuracy error over the full delay ranges and frequencies with a small ripple such that 95% of values are within +/- LSB/2 of the desired value, i.e., within 2 standard deviations of the desired delay value.

4.3.1.5. Summary

	Av delay (ps)	Target delay (ps)	MAE (ps)	Std dev delay	Average Loss (dB)	Max Loss (dB)	Std dev loss (dB)
1	-27.2	-27.5	3.3	4.87	0.66	1.15	0.31
2	-54.1	-55	5.3	7.19	0.69	1.22	0.32
3	-80.9	-82.5	4.7	5.74	0.71	1.25	0.33
4	-108.9	-110	3.2	3.69	0.74	1.31	0.35
5	-136.2	-137.5	4.2	5.49	0.76	1.29	0.34
6	-163.1	-165	5.6	6.84	0.79	1.36	0.35
7	-189.8	-192.5	5.4	6.09	0.81	1.39	0.36
8	-217.9	-220	5.0	5.83	0.84	1.46	0.36
9	-245.2	-247.5	5.7	7.05	0.86	1.50	0.36
10	-272.1	-275	6.4	7.40	0.88	1.60	0.37
11	-298.8	-302.5	5.9	6.45	0.91	1.59	0.38
12	-326.6	-330	7.0	7.69	0.95	1.56	0.40
13	-353.8	-357.5	7.4	8.67	0.97	1.60	0.40
14	-380.7	-385	7.3	8.09	0.99	1.67	0.40
15	-407.5	-412.5	7.1	7.06	1.02	1.67	0.41
Overall			5.56	6.78	0.82	1.68	0.38

Table 11. Simulation Results.

Note: Negative delay values indicate that the propagation time of the selected path is greater than that of the zero-delay reference path. The 'Overall' values represent the aggregate metrics computed across all delay states and frequencies.

4.4. Experimental Validation and Results

The results of the completed TDU are presented below, with de-embedding applied to remove the influence of input and output connectors and feed lines.

Measurements were taken with a Keysight Vector Network Analyser (VNA), model N5224.

The SOLT method was used for calibration. The Short-Open-Load-Through (SOLT) calibration method uses four known impedance conditions to remove measurement errors caused by system imperfections, such as cable losses, mismatch and leakage giving rise to more accurate S-parameter measurements.

1. Short Circuit (S) – Each port is terminated with a well-defined short circuit, allowing the VNA to establish a reference for phase and magnitude corrections.
2. Open Circuit (O) – The ports are left open, providing a complementary reference to the short circuit for determining capacitance and residual impedance effects.
3. Load (L) – A precision 50 Ω termination is used to define the system impedance and correct for mismatch errors.

4. Through (T) – A direct connection (or a well-characterised transmission path) between ports is measured to remove systematic transmission losses and phase delays from the test setup.

De-embedding is a post-measurement correction technique used to remove the effects of test fixtures, connectors and transmission lines from measured S-parameters, ensuring that only the Device Under Test (DUT) is characterised. The steps for de-embedding are;

1. The test transmission line and open circuit included on the TDU PCB are measured and characterised using the same SOLT calibration.
2. Using the measured S parameter data, an equivalent 2-port network model of the fixture is computed. (The fixture in this case is the input and output SMA connectors and the transmission lines leading in and out from the TDU.)
3. The S-matrix of the fixture is subtracted mathematically from the full measurement data using network de-embedding techniques i.e., T-matrix conversion, to isolate the DUT response.

De-embedding is critical for precise time delay measurements in TDUs, as even small connector discontinuities or mismatches can introduce significant phase and group delay errors. By properly de-embedding the input and output transitions, the measured results reflect the true performance of the RF MEMS-based delay lines.

The results are from the input pin on the first RF MEMS switch through to the output pin on the fourth RF MEMS switch.

4.4.1. Test Transmission Line

The TDU measurements began with the characterisation of a reference transmission line that was included on the same PCB to verify the expected impedance of the delay line geometry. The reference line was designed to provide a known 50 Ω path. When measured, the line exhibited a characteristic impedance of 55.5 Ω. The dominant source of this error was manufacturing tolerance rather than any difference in phase velocity from the design value. The track width measured 0.388 mm vs 0.43 mm (design), and the gap 0.134 mm vs 0.10 mm (design). See Figure 96. These differences account for the impedance shift. For this PCB, the delay line impedances deviate from the 50 Ω target by 11%, slightly outside typical 10% PCB tolerances for RF lines. The measured effective dielectric constant for the substrate was 2.174 compared to the design value of 2.166, a divergence of just 0.4% and certainly not the reason for the difference in impedances.

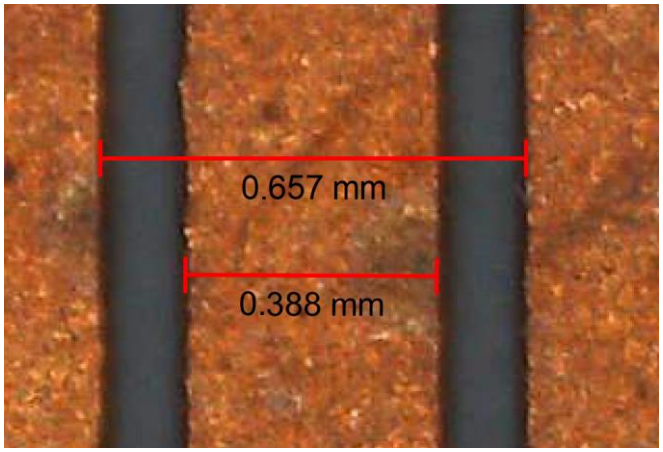


Figure 96. Microscopic view of the dimensions of the 50 Ω test track.

4.4.2. S21 Phase

The measured phase of S21 is shown in Figure 97 and shows good phase flatness across the desired band to 6 GHz and even out to 8 GHz. None of the measured phase traces intersect, indicating that phase accuracy remains within one LSB.

The phase of S21 for each delay state increases smoothly with frequency, indicating that the relative phase shift between different delay states remains consistent. This suggests that each switched delay path is well designed and exhibits a predictable delay response.

As none of the phase lines crossover, this suggests that there are no spurious resonances or unintended coupling between delay paths, that the switching is working as designed and that the physical length of delay lines are respectable. This confirmed the intended behavior of the switched-line topology and the consistent timing alignment of signals passing through each state.

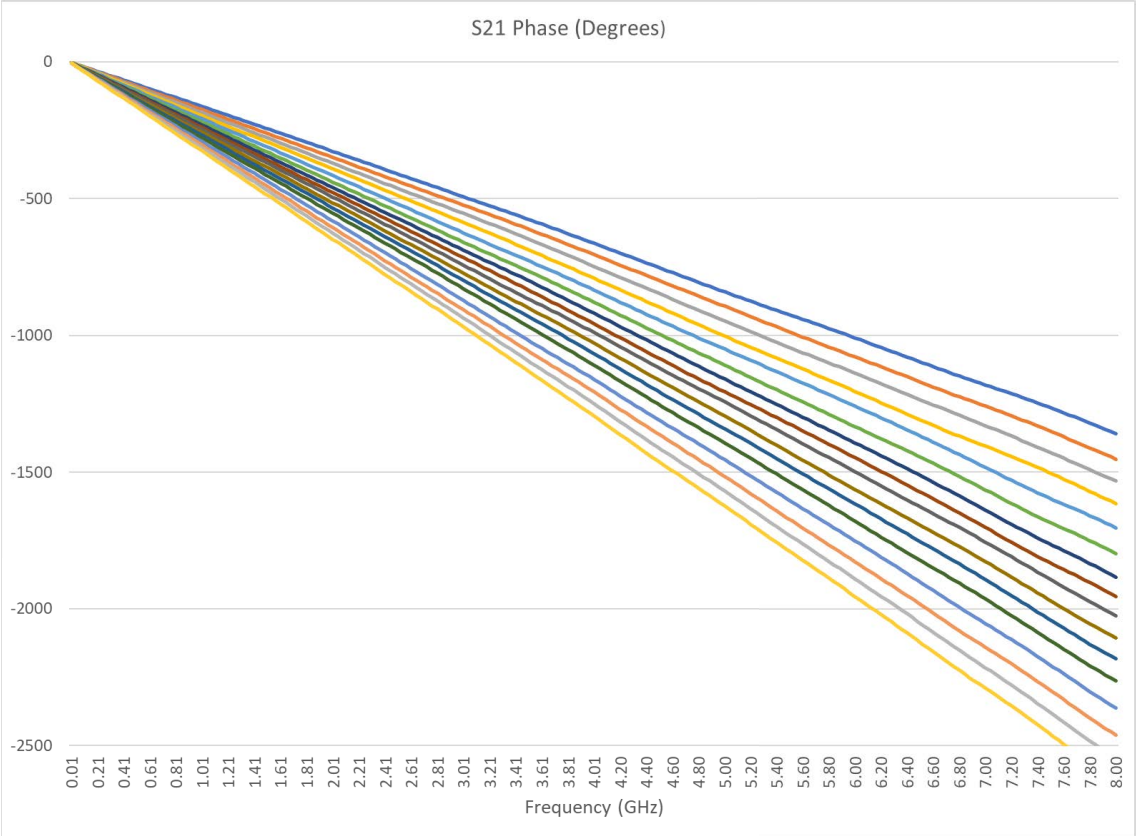


Figure 97. Measured S11 Phase (degrees).

As an alternative presentation and to show the accuracy of the phase shift as compared with the perfect values, see Figure 98 for a plot of the phase shift at 6 GHz. There is good agreement for the first 13 delay states, with all errors less than LSB/2. The maximum error is with delay state 15 and a phase error of 53.6° which is still less than the LSB phase shift value of 59.4°.

This does indicate that all the phase lines in S21 are dipping down at the higher frequency end of the band as they are all maintain a separation from their neighbour. Table 12 tabulates the results.

From these data, it would suggest that all delay lines are a little too long and all errors are negative, i.e., more delay than per the design values and these errors are cumulative. There seems to be some interaction for delay states 13 to 15. The LSB12 line has an error of 28.7° but this jumps to an error of 45.9° with the addition of the LSB1 line.

A comment about the delay through the RF MEMS switches. From the manufacturer's data, the group delay through a switch is 35 ps and flat so four switches in series will add 140 ps to the reference delay and as such is not part of the extra delay calculations.

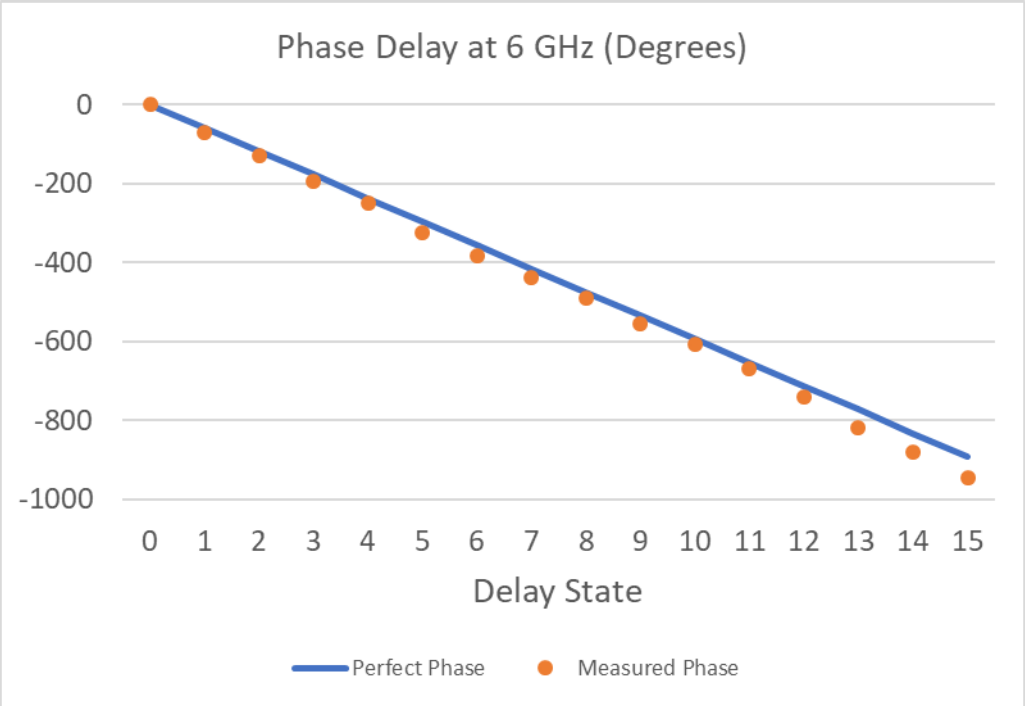


Figure 98. Display of the phase shift in degrees at 6 GHz of measured results against perfect values.

State	Target Delay (ps)	Phase at 6.0 GHz	Phase Shift Measured	Error (degrees)
0	0	0.0	0.0	
1	-27.5	-59.4	-69.7	-10.3
2	-55	-118.8	-128.8	-9.9
3	-82.5	-178.3	-195.4	-17.1
4	-110	-237.7	-249.5	-11.8
5	-137.5	-297.1	-324.4	-27.3
6	-165	-356.5	-383.9	-27.4
7	-192.5	-416.0	-437.8	-21.9
8	-220	-475.4	-489.3	-13.9
9	-247.5	-534.8	-554.3	-19.4
10	-275	-594.2	-606.7	-12.5
11	-302.5	-653.7	-670.0	-16.3
12	-330	-713.1	-741.8	-28.7
13	-357.5	-772.5	-818.4	-45.9
14	-385	-831.9	-880.8	-48.8
15	-412.5	-891.4	-944.9	-53.6

Table 12. Measured phase shift at 6 GHz against the perfect value for all delay states.

4.4.3. Group Delay

Of course, the phase of S21 is not the full story. The group delay is defined as the negative frequency derivative of the phase,

$$\tau_g(\omega) = -\frac{d}{d\omega}\arg(S_{21}(\omega)). \tag{4.5}$$

Even if the phase response curves are monotonic and well-separated, their slopes (which determine the group delay) can still intersect at certain frequencies and they do. See Figure 99. These traces are for the absolute delay from the input to the output, before calculating the delay relative to the zero delay of the reference paths. Figure 100 shows the relative delay for each delay state.

Looking first at the absolute delay, the delay is clean to about 3 GHz and then some ripple is apparent. A pattern is discernible. Take the first four delay traces. The dip in the group delay between 3 GHz and 5.5 GHz is very similar for all four. These four delays all pass through the reference line on the coarse bit delay section and only vary by the lines representing 1, 2 or 3 LSB delays in the fine bit delay section, indicating that it is the reference line on the coarse bit delay that is giving rise to the group delay dip.

Similarly, for the next four traces. They all have a similar dip in delay but a bit narrower in frequency, 3.5 GHz to 5 GHz. These all pass through the 4LSB delay line. It is the same story with the next four delays and the last four.

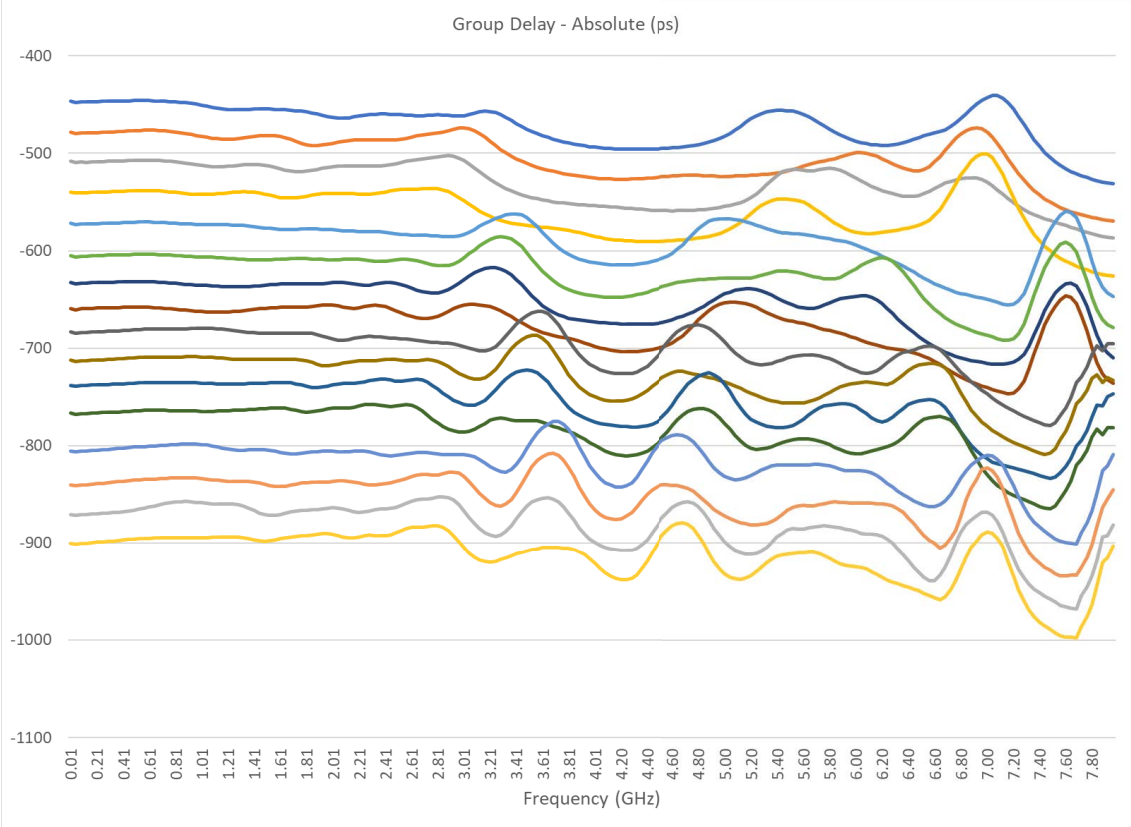


Figure 99. Measured Absolute Group Delay – all states, in picoseconds.

Again, the Mean Absolute Error (MAE) is used to measure the accuracy of the delay value and the standard deviation indicates the amount of ripple about the mean. The MAE values for each delay step are given in Table 13.

Overall, for all values at all frequencies and all delay settings, the MAE is 18.4 ps with a standard deviation of 13.3 ps.

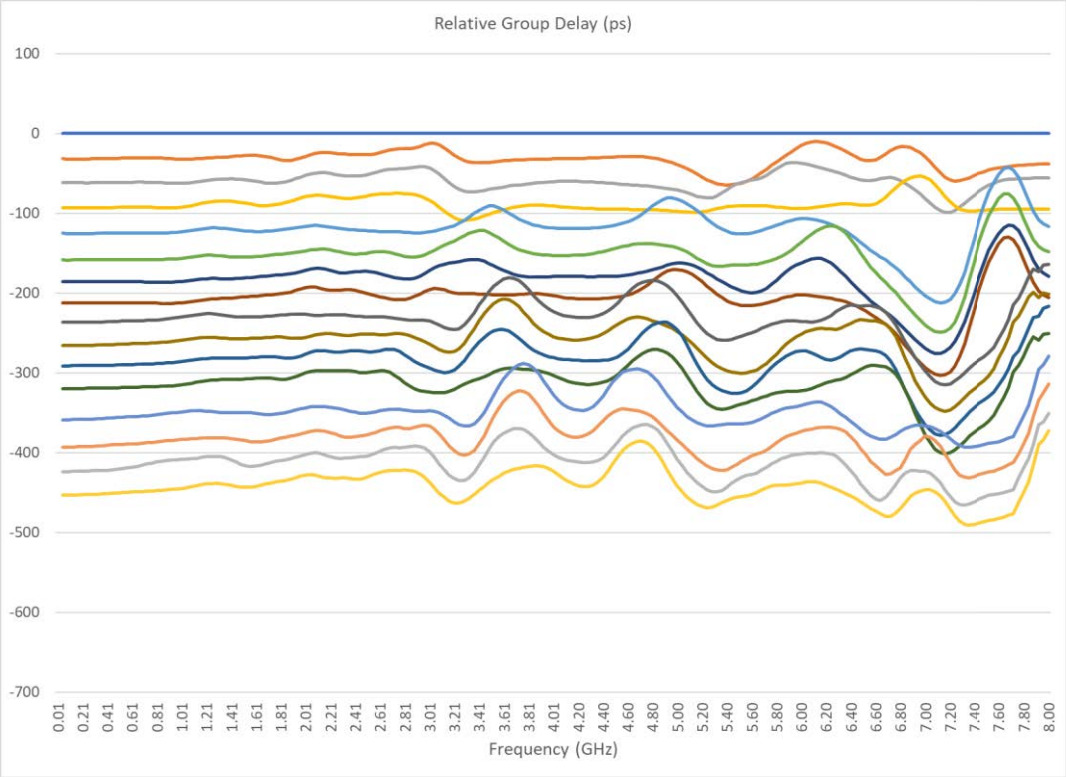


Figure 100. Group Delay relative to Reference path – all states.

Overall from the average delay values, it is evident that all the delay lines are a little too long giving slightly more delay than intended.

A box plot helps to show the distribution of the absolute errors. (Recall the red line in the box is the median not the mean so it is a bit different from the MAE values.) As is to be expected, the magnitude of the errors increases with the longer delays.

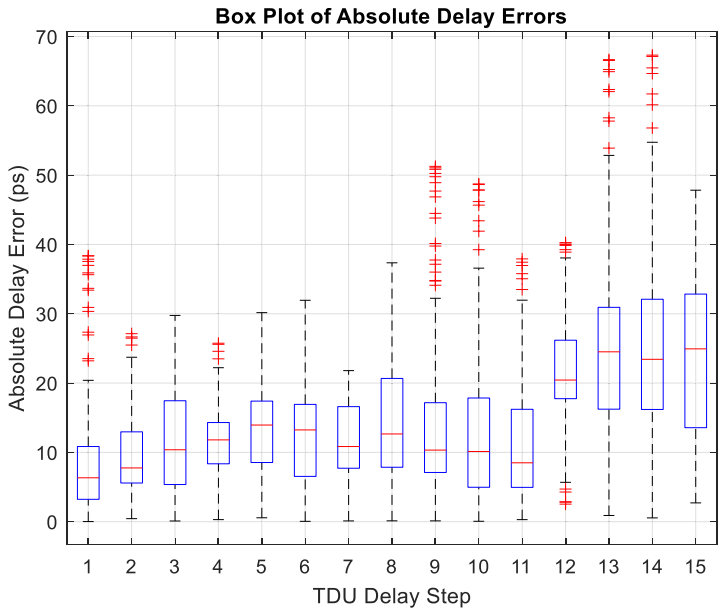


Figure 101. Box plot of the absolute errors for delay steps.

In comparison with the simulation results, the measured MAE is 18.4 ps in contrast to 5.56 ps for the simulation. This can largely be explained due to the slightly longer physical delay lines in the measured results.

The measured standard deviation of 13.3 ps is in contrast to 6.78 ps in the simulation and the reasons will be analysed in detail in Section 4.4.7.

4.4.4. S21

The measured insertion loss, including the reference lines, ranges from 2.3 dB to 3 dB at 6 GHz for all delay states and 3.09 dB is the worst case over all frequencies and all delay states. This variation in levels of 0.7 dB compares favourably with a value of 0.47 dB in the simulation. The manufacturer's measured S parameters for the MM5140 indicate a switch insertion loss of 0.44 dB at 6 GHz, so a total of 1.76 dB for four switches. This leaves the delay line losses ranging from 0.54 dB to 1.24 dB.

These values compare favourably with the simulated track losses of 0.41 dB to 0.88 dB, see Figure 92 and recall that the simulation assumed a switch loss of only 0.2 dB as distinct from reality of 0.44 dB.

The average insertion loss for all frequencies and all delay values is 1.5 dB with a standard deviation of 0.67 dB. The maximum loss at any frequency and any delay setting is 3.09 dB.

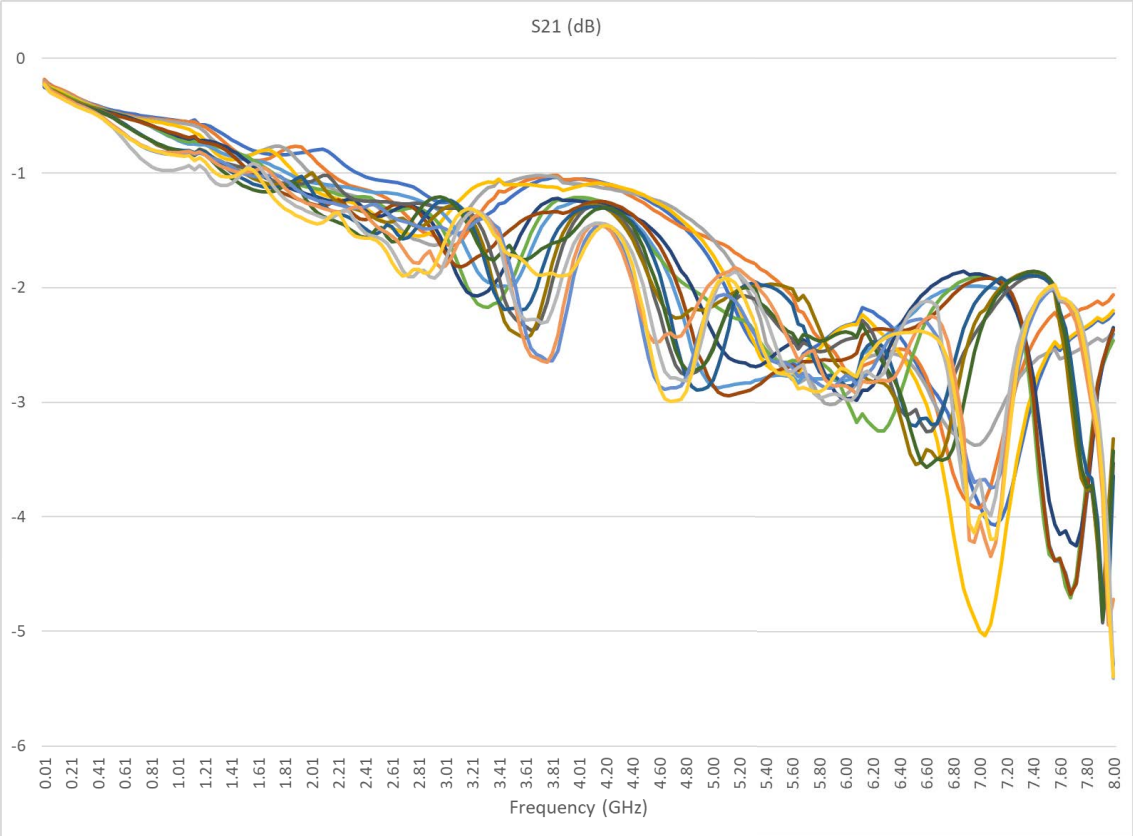


Figure 102. Measured S21 (dB) – Insertion Loss.

4.4.5. S11

The measured return loss remains better than 9 dB across the frequency band of interest but does not meet the design expectations of 12 dB derived in the simulation.

There is a strong correlation between return loss and group delay ripple as both phenomena originate from the same underlying cause, impedance mismatches and multiple small reflections at transitions between the RF MEMS switches and delay lines. Visually comparing the measured return loss and group delay response reveals that when the return loss is better than 15 dB, the group delay remains relatively smooth, indicating minimal phase perturbations due to multiple reflections. However, when return loss degrades to around 12 dB, noticeable variations in group delay begin to appear, though they remain within an acceptable range for many applications. This implies that a return loss threshold of approximately 15 dB is needed to sufficiently suppress group delay ripple, with 12 dB representing a marginal case where residual reflections still contribute to delay variation.

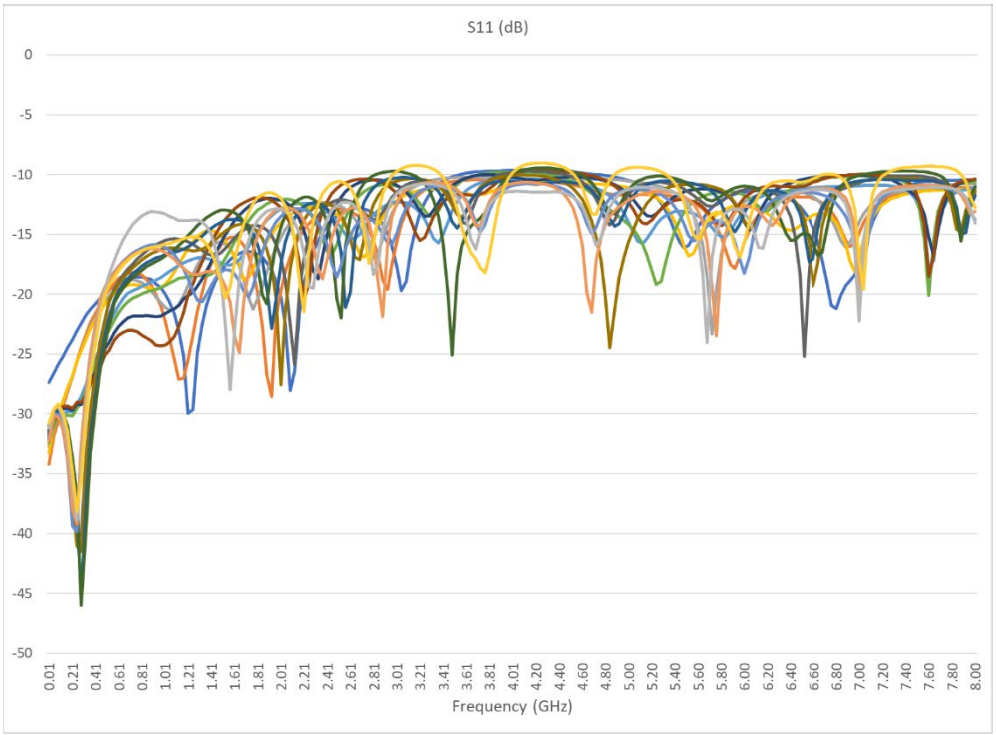


Figure 103. Measured S11 (dB).

The underlying causes of these differences between simulation and measurement are analysed in detail in the next Section where a refined multi-port switch model is shown to accurately explain all measured features.

4.4.6. Summary of Delay Performance

The table below tabulates the details of the group delay for each of the delay states.

State	Av Delay (ps)	Target Delay (ps)	MAE (ps)	Delay Std Dev	Av Loss (dB)	Max Loss (dB)	Loss Std Dev (dB)
0	0.0	0	0.0	0.0	1.243	2.68	0.63
1	-32.6	-27.5	8.9	10.1	1.22	2.73	0.52
2	-60.4	-55	8.9	8.5	1.30	3.02	0.66
3	-89.8	-82.5	10.1	6.9	1.31	2.77	0.61
4	-122.3	-110	12.9	8.5	1.54	2.87	0.76
5	-156.8	-137.5	19.6	7.6	1.49	2.97	0.66
6	-185.7	-165	21.1	8.2	1.50	2.97	0.68
7	-209.5	-192.5	16.7	10.1	1.54	2.94	0.72
8	-235.0	-220	14.8	8.8	1.55	2.76	0.66
9	-263.1	-247.5	15.4	9.3	1.51	2.75	0.58
10	-290.3	-275	15.3	8.5	1.56	2.89	0.64
11	-313.4	-302.5	12.9	10.7	1.54	2.72	0.58
12	-357.1	-330	25.7	9.9	1.68	2.89	0.72
13	-392.5	-357.5	34.2	11.5	1.64	2.86	0.63
14	-421.0	-385	35.6	12.0	1.70	2.98	0.64
15	-435.6	-412.5	23.6	16.2	1.70	2.99	0.67
Overall			18.4	13.3	1.52	3.09	0.68

Table 13. Summary table of TDU performance results.

4.4.7. Comparison with Simulation and Reconciliation

A key hypothesis of this research was that terminating unused delay tracks would eliminate half-wave resonances. Figure 104 shows a comparison of the group delay for delay state 15 (the longest delay path). There is a measurable benefit from terminating the unused tracks, the peak delay variation improves by approximately 25 ps at 4.7 GHz (nearly one LSB). However, the residual ripple with terminations remains 74 ps peak to peak, so the overall benefit is moderate. As shown later in this Section, this residual ripple originates from the shunt loading of the OFF-state switch ports rather than incomplete termination.

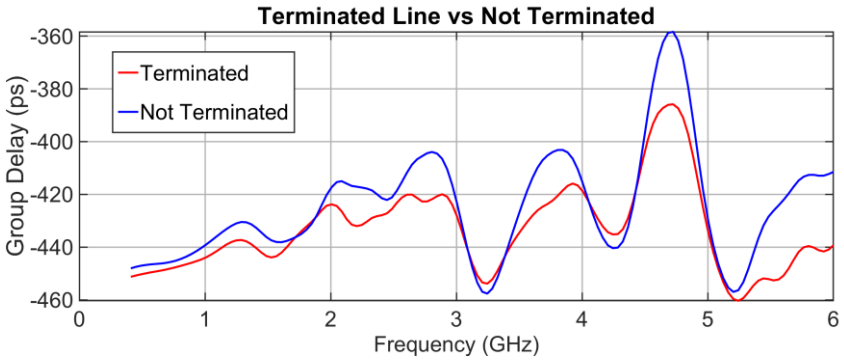


Figure 104. Comparison of group delay for terminated and unterminated unused delay lines for state 15 delay.

Other delay values exhibited similar, though smaller, improvements. For example, the zero delay shows a 7 ps improvement around one frequency.

Early circuit performance simulations, with unterminated unused tracks, indicated severe group delay distortions of up to 190 ps at frequencies equal to the resonant frequency of those unused tracks. As this delay variation is nearly seven times the LSB, the initial strategy was to terminate unused tracks to suppress resonances. However, the measured results suggest that with careful PCB layout, the impact of the unterminated tracks can be mitigated.

The conclusion is that with prudent use of grounding vias to suppress coupling between delay lines and the use of confined transmission line structures such as CBCPW, acceptable performance can be achieved without termination. In this implementation, better impedance matching would likely have delivered greater performance improvements than shunt terminations. These results highlight a key insight: while termination is a straightforward solution to suppress resonances, the root cause lies in electromagnetic coupling and reflection paths within the layout. In this work, the use of CBCPW, together with copper-filled vias connecting the top and bottom grounds, effectively reduced coupling between active and inactive delay lines by laterally confining the electromagnetic fields. This configuration forms a channelized structure in which the finite lower ground and via sidewalls prevent return-current

crossover and surface-wave propagation between neighbouring paths. These are well-established microwave design techniques [89]. The combined benefits of CBCPW geometry and grounding vias were confirmed by full-wave EM simulation. This suggests that careful electromagnetic design can serve as a viable alternative to termination in similar switched-line systems, simplifying the layout and reducing component count.

4.4.7.1. Simulation-measurement reconciliation.

A brief reconciliation explains the simulation to measurement gap.

The initial co-simulation used a lumped switch abstraction and published 2-port data for the switch which turned out to be too simplistic. Published 2-port S-parameters for multi-port devices are reduced under the assumption that all unused ports are terminated in the characteristic impedance Zo (typically 50 Ω). In this design, the unused MM5140 throws are connected to a coplanar line that continues into a shorting network implemented with a parallel MM5140. Consequently, the two-port representation of the active throw does not capture the port-environment-dependent loading present on the board. This discrepancy explains why the initial EM and 2-port co-simulation predicted substantially better return loss and insertion loss than those measured. That is to say, while the design of Figure 68 terminates each unused delay line to stop any resonances, the active delay line has the added shunt load of an open port on a parallel switch and this load is material to performance and cannot be neglected.

To resolve this, a compact reciprocal, passive 5-port macro was built for the MM5140 and embedded into the complete nodal model of the TDU so that each switch throw “sees” its actual board environment. The switch OFF state isn’t an open circuit. The MM5140 OFF path is essentially a capacitive ladder: big pad caps to ground on both pads (circa 300 fF) with a small series coupling cap between common to throw (12 fF), plus the common side is terminated in 50 Ω. It’s a π network and presents a very low impedance circuit to ground at 8 GHz.

Figure 105 shows the equivalent shunt admittance B(f) at the through-path tee, including the via connection, to the OFF-path termination switch. The extracted equivalent capacitance is about 600 fF at 0.4 GHz, roughly twice the nominal 300 fF pad capacitance of a single OFF port. This occurs due the short via linking the two switches. Without the via, the equivalent capacitance is about 450 fF. This additional shunt load exacerbates the passband ripple as observed in the measured results.

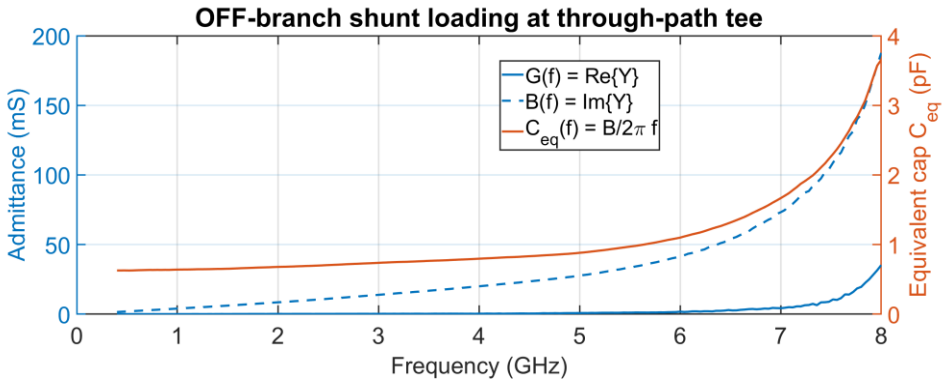


Figure 105. Equivalent shunt admittance (mS) at the through-path tee (includes via segment) and the equivalent capacitance (pF) of the load.

A sensitivity check was also performed by varying the dielectric loss tangent of the RO4003 substrate. Increasing tan δ from zero to values twenty times above the specified value affected only the insertion-loss slope (negatively) and return loss (positively), while the group-delay RMS ripple improved by a small amount of 4 ps. This confirms that dielectric loss degrades transmission magnitude but has negligible influence on the ripple, which instead arises from impedance discontinuities and OFF-path loading at the switch junctions.

With the 5-port macro and the full OFF-branch network included, the model closely tracks measurements: RMS errors of 2.5 dB (|S11|), 15° (∠S11), 1.1 dB (|S21|), 6° (∠S21), and 47 ps (group delay).

The strong, dispersive shunt admittance introduced by the loading of the OFF port of the parallel switch a) worsens the return-loss null structure, (b) adds excess insertion loss, and (c) produces the measured group-delay ripple peaks via multi-path internal reflections around the branch.

The systematic impedance bias of 55.5 Ω instead of 50 Ω is a secondary mechanism. This creates a per-junction reflection coefficient of order Γ = (Zc–Zo)/(Zc+Zo) ≈ 0.05 (-26.5 dB). With four switches and several line segments, these small discontinuities set a baseline ripple in S11/S21 and group delay, but they are not the dominant cause relative to the switch OFF-path shunt admittance.

Supplementary MATLAB analysis with the perfect-switch model confirms that the group-delay ripple increases by roughly 15 ps RMS when the delay-line impedance is varied from 50 Ω to 60 Ω, corresponding to a sensitivity of approximately 1.5 ps RMS per ohm of impedance deviation.

Using the corrected model to explore alternatives indicates that removing the parallel shorting switches and tightening interface matching can achieve return loss > 15 dB, insertion loss ≈ 0.9 dB at 6 GHz, and RMS group delay ripple ≈ 6.7 ps.

Figure 106 illustrates the corrected multiport model for the absolute delay state 0 over 0.4–6 GHz. The curve with the OFF-path shunt network (parallel switch plus termination) closely reproduces the measured group delay, while a hypothetical variant without the shunt shows the substantial ripple reduction achievable when the shorting network is eliminated. This isolates the OFF-path shunt as the dominant contributor to the observed ripple; layout-related reflections set only a smaller baseline.

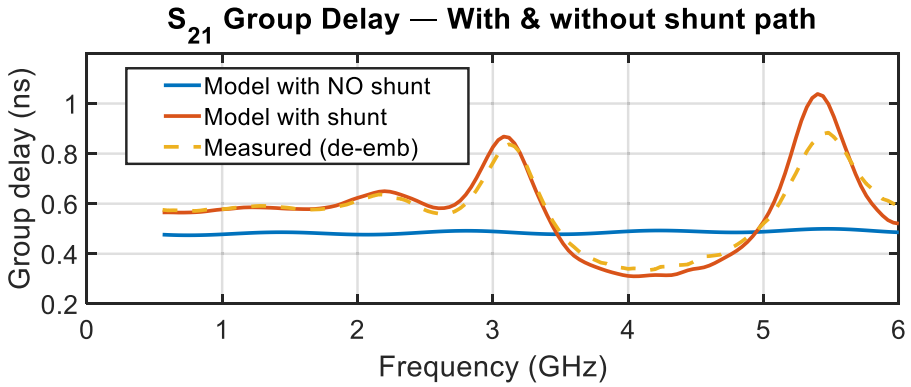


Figure 106. Group delay for state 0: measurement vs corrected multiport model with the OFF-path shunt, and a counterfactual model without the shunt. The corrected model aligns with measurement; removing the shunt predicts much lower ripple, isolating the OFF-path loading as the primary mechanism.

4.4.8. Comparison with State-of-the-Art

From the state-of-the-art papers discussed in chapter 3, four were selected for direct comparison with this research work. The four selected papers represent close comparisons, while not a direct comparison in that none is a PCB using commercially available RF MEMS switches, however they are close in technology. The other papers were considered too dissimilar as either the entire TDU, including transmission lines, switching elements and control circuits, was fabricated on a single silicon wafer, alumina or LCP substrate (monolithic integration) or used silicon or GaAs MMICs as switches, (not MEMS) none of which is the strategy of this research work.

Reference	[82]	[83]	[84]	[64]	This work
Year	2013	2014	2015	2016	2025
Technology	Packaged MEMS & PCB	Packaged MEMS & PCB	MEMS & PCB	MEMS & PCB	packaged MEMS & PCB
TX line technology	microstrip	FG CPW	microstrip	microstrip	FG CPW
Switch	MEMS	MEMS	MEMS	MEMS	MEMS
Frequency (GHz)	10	0 – 5	1.7 – 2.7	6 – 12	0.4 – 6
Bits	5	3	4	5	4
Max time delay (ps)	96	49	77	3255	472
Loss average (dB)	3.7	2.5		12	1.5
Loss maximum (dB)	3.2	7	0.9	16	3.09
Time error average (ps)	0.6				2.54
Time error max (ps) or std deviation		100			10.56
Return Loss	15	7	13.4	12	9
Loss per bit	0.64	2.333333	0.225	3.2	0.7725
FoM ps/dB loss	30.0	7.0	85.6	203.4	152.8

Table 14. Comparison of results with state-of-the-art.

To summarise the comparative works:

Ref [82] reports the first integration of packaged RF MEMS switches on a PCB in a switched-line TDU. The MEMS devices were hermetically sealed dies that required wire bonding, introducing parasitic losses.

The work in Ref [83] demonstrates the first LGA-packaged RF MEMS on a PCB. However, it exhibited over 100 ps of group delay ripple on a nominal 49 ps delay, indicating significant impedance and control issues.

The design in Ref [84] uses metal-contact MEMS in a hermetically sealed die mounted on a PCB, achieving 77 ps delay over a 1.7–2.7 GHz band. This design requires 90 V for actuation and suffers parasitic losses due to wire bonding.

The work in Ref [64] sets a high benchmark for broadband operation (6–12 GHz) with a delay of 3255 ps. However, the MEMS switches are custom and not commercially available, require 90 V activation and involve 20 switches with up to 16 dB insertion loss. Its FOM is 203 ps/dB but comes with considerable complexity.

The research work of this thesis achieves a Figure of Merit (FOM) of 152, a notable achievement given its reliance on commercially available RF MEMS switches without requiring a 90V activation voltage. This meets the original aims for the research work.

4.5. Observations of Finished Product

This work has presented the design, fabrication and experimental validation of a 4-bit switched-line true time delay unit (TDU) using commercially packaged RF MEMS switches and standard multilayer PCB processes. The prototype operates from 0.4 to 6 GHz with a maximum delay of 413 ps and a 4-bit resolution, achieving a figure of merit (FOM) of 152.8 ps/dB. Key performance metrics include average insertion loss of 1.5 dB and mean absolute delay error below 18.4 ps across all states.

The novelty of this work lies in its use of commercially available RF MEMS switches in a compact, manufacturable PCB implementation. Unlike prior designs that required custom dies, high-voltage switch actuation, or exotic substrates, this TDU leverages LGA-packaged RF MEMS switches and coplanar PCB technology to achieve high performance with low complexity.

Subsequent analysis using a corrected multiport switch model confirms that OFF-path termination–induced shunt loading is the dominant cause of the simulation–measurement gap. Incorporating this termination network into the model brings simulation and measurement into close agreement, with the remaining ripple explained by interface mismatch and minor layout reflections.

The findings show that high-performance TDUs can be achieved without custom fabrication, paving the way for deployable RF MEMS-based phased array systems. Such TDUs are essential for enabling beam squint-free, dispersion free wideband operation in advanced array systems, including those targeting 6G, satellite communication, radar and mobile platforms.

While the demonstrated prototype achieves its design objectives, opportunities remain for refinement. Reducing the footprint through multilayer or fractal delay-line geometries, improving impedance control via tighter process tolerances, and optimising junction matching could further enhance performance. The measured group-delay ripple originated primarily from the unnecessary termination of unused transmission paths. The revised multiport model in Section 4.4.7 showed that removing these terminations eliminates the associated shunt loading and substantially improves performance. These refinements represent practical extensions to the present TDU design, while broader system-level implications are discussed in Chapter 7.

5. Beamforming Network Optimisation

This chapter presents a novel methodology to optimise the design of BFNs for electronic scanned phased arrays. The approach addresses the critical need to reduce the physical real estate and improve phase accuracy. By introducing a variable delay range for TDUs within each layer of a multi-level, or hierarchical BFN, tailored to the specific positional requirements of each array element, this method departs from the conventional practice of using uniform TDU delay values across a layer. This novel profiling of TDU values saves physical space and reduces phase errors across the face of an array.

For example, with an 8-elemet array, the methodology saves 21.4% of space and improves the phase errors by 40%. In the case of a 128-element array, the technique saves up to 21% of physical space and reduces a 3.83° array phase error to 3.3°, an improvement of 13.7%, for an improvement in beam pointing accuracy of 0.16°. The TDU delay value profile reduces the least significant bit errors and disrupts quantisation error correlation, thereby reducing peak sidelobes and grating lobes and lowering average sidelobe levels. The pseudo-random nature of the phase errors delivers an 18 dB reduction in grating lobes for a large 256 x 256 antenna planar array.

A robust theoretical foundation is developed for this design framework and its effectiveness is validated through detailed examples involving both linear and planar arrays. The proposed technique is scalable and versatile, offering a promising solution for advancing the efficiency and accuracy of phased array systems in radar and communication applications.

5.1. Varying TDU Delay Values

Phased arrays offer significant benefits, particularly for electronic beam scanning, adaptive nulling and multi-beam operation [2]. As such, large aperture arrays have found extensive applications in radar, satellite communications and 5G cellular networks.

However, in practice, the reality of designing, manufacturing, controlling and maintaining large arrays where each array element is independently controlled is a complex and expensive exercise. Hence, considerable research has gone into reducing the cost, complexity, weight and size of electronically scanned phased arrays, such as tile vs slat designs [90] and modularisation with subarrays [91-93].

Other methods of reducing the size and complexity of phased arrays include irregular architectures such as thinned arrays, sparse and time-modulated arrays [94-96].

The use of parasitic elements instead of active elements has also been proposed to reduce complexity and cost [97] along with randomly feeding multiple antenna elements from a single phase shifter [98].

This chapter focuses on the BFN and proposes a novel method to reduce the size of a BFN with no compromise in performance.

TDUs are generally more expensive and occupy more space than phase shifters as they are required to provide significant time delays. The maximum delay is determined by the size of the array, the bandwidth and the maximum scan angle [5]. For example, a square array 50-wavelengths wide requires a TDU of approximately 60 wavelengths to achieve a 60° scan in all directions.

Using switched line TDUs, large delay values can become a physical challenge requiring significant real estate to be implemented. Hence researchers have proposed hierarchical structures, or otherwise known as multi-layer structures, in order to enhance design efficiencies and to reduce the number and size of TDUs required for a beamforming network [99, 100]. A typical hierarchical TDU-based BFN is illustrated in Figure 107.

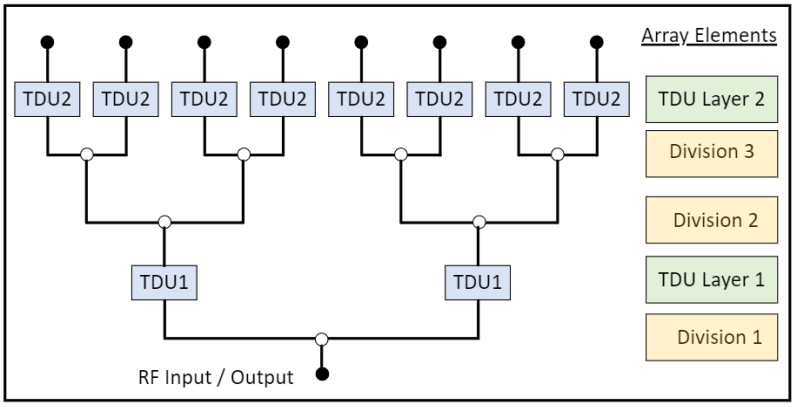


Figure 107. Hierarchical Beamforming Network showing Divisions and Layers.

The study in [101] formulates the optimisation as a binary integer linear program (ILP) that minimises a weighted sum of the total number of TDUs, bit count and RMS phase error with respective weighting of [1, 0.1, 0.001], which emphasises minimising TDU count. The allowable RMS phase error is set to 5°. The optimisation is solved using MATLAB's "intlinprog" routine with a branch-and-bound search. This identifies an architecture that meets phase-error limits at minimum cost and complexity. Readers seeking algorithmic details are referred to [101].

In this proposal, a further degree of design freedom is introduced to enhance TDU-based BFNs by varying the delay range of each TDU in a single layer. As far as the author knows, the open literature to date has only considered uniform TDU values in a single layer.

Introducing variations in the delay values of a single layer provides two potential benefits. It can save the space required to build the BFN as some TDUs reduce in value and hence size. Secondly, the phase errors can reduce and become less structured with less of a regular pattern thus reducing pointing errors and side lobe levels.

For this research work, linear integer programming was used, as per [101], to determine the optimum design variant with uniform TDU values in each layer and then to apply the proposed method of varying the TDU values in a single layer to quantify the benefits. The proposed shaping, or profiling of TDU values, is applicable for linear and rectangular planar arrays and is scalable in size.

This chapter details a design methodology to generate a profile of TDU values in a single layer of a hierarchical BFN to achieve the minimum delay value per individual TDU in a single layer, making 3 contributions to the state of the art:

- Physical space optimisation. The method introduces a specific approach to reduce the physical space required for beamforming networks by varying the time delay value of TDUs, which is not covered in the existing literature.
- Phase error reduction. The benefit of reducing array phase errors is a distinctive attribute that contributes to improving grating lobes and sidelobes.
- Scalability. The scalability of this approach to both linear and planar arrays and their applicability to various sizes and configurations is a strong point of differentiation.

The remaining chapter covers the theory and formulae along with practical examples for linear and planar arrays. Also included is a full wave simulation of a large linear array and a discussion of the results.

5.2. Eight-Element Linear Array Example

To explain the methodology, this section begins with the example of the 8-element linear array, the subject of this research work, before moving to the general theory and generic methodology.

First consider how one might vary the range of each time delay unit. The two time delay units on each end of the array need to be able achieve the full value of 413 ps, however the 2 units connected to the two middle array elements need only achieve a range of approximately half this range and those time delay units in between need to achieve a delay range in between the maximum of 413 ps and half that. Specifically, the range and LSB of each time delay unit is denoted in Table 15.

Time Delay Unit	Maximum delay (picoseconds)	LSB (picoseconds)
1 and 8	413	27.5
2 and 7	354	23.6
3 and 6	295	19.6
4 and 5	236	15.7

Table 15. TDU values for full range delay and LSB.

Using these values in the MATLAB simulation introduced in chapter 4.1.2, the performance results for the 8-element array are shown in Table 16.

Number of Control bits	Maximum pointing error (degrees)	RMS pointing error (degrees)	Max. QSLL (dB below beam peak)	Average QSLL (dB)	Max. amplitude error (dB)
2	12.759	5.981	-2.271	-14.096	-6.719
3	4.345	2.461	-7.950	-17.215	-0.935
4	2.352	1.186	-12.752	-18.635	-0.222
5	1.293	0.656	-16.426	-19.268	-0.065
6	0.597	0.221	-18.372	-19.671	-0.012
7	0.286	0.156	-19.053	-19.824	-0.004
8	0.183	0.084	-19.553	-19.921	-0.001

Table 16. Simulation results with varying TDU delay values.

The simulation conditions for Table 16 are identical to those used for the uniform-array results previously presented in Table 7 of Chapter 4 and should be interpreted on that basis. Specifically, the array is a uniform linear array with half-wavelength element spacing at 6 GHz. The frequency sweep spans 0.4 GHz to 6 GHz in 50 steps, and the scan angle varies from 0° to 45° in 30 steps. The number of control bits varies from 2 to 8. A fixed Chebyshev taper providing –20 dB sidelobes at boresight is applied and no additional windowing or amplitude modulation is used.

There are a couple of significant differences when compared with the results for all TDUs being uniform as shown in Table 7.

Firstly, the significant pointing error with 2 bits is gone and is more in-line with the trend of an increasing pointing error as the number of bits is reduced.

Overall, the pointing error has increased slightly for all values of control bits, increasing from a maximum of 2° to 2.35° with 4 bits for example, Figure 108. The overall performance

for all scan angles and frequencies is shown in Figure 109. As before, the pointing error is independent of the frequency, just subject to the scan angle.

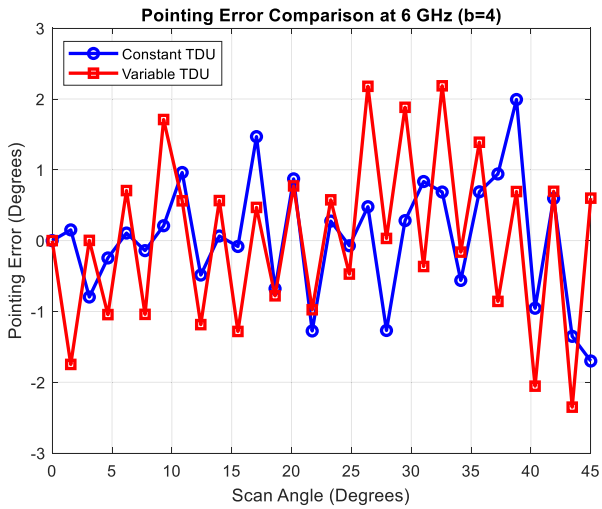


Figure 108. Beam pointing error for the TDUs having different LSB values compared to the reference case.

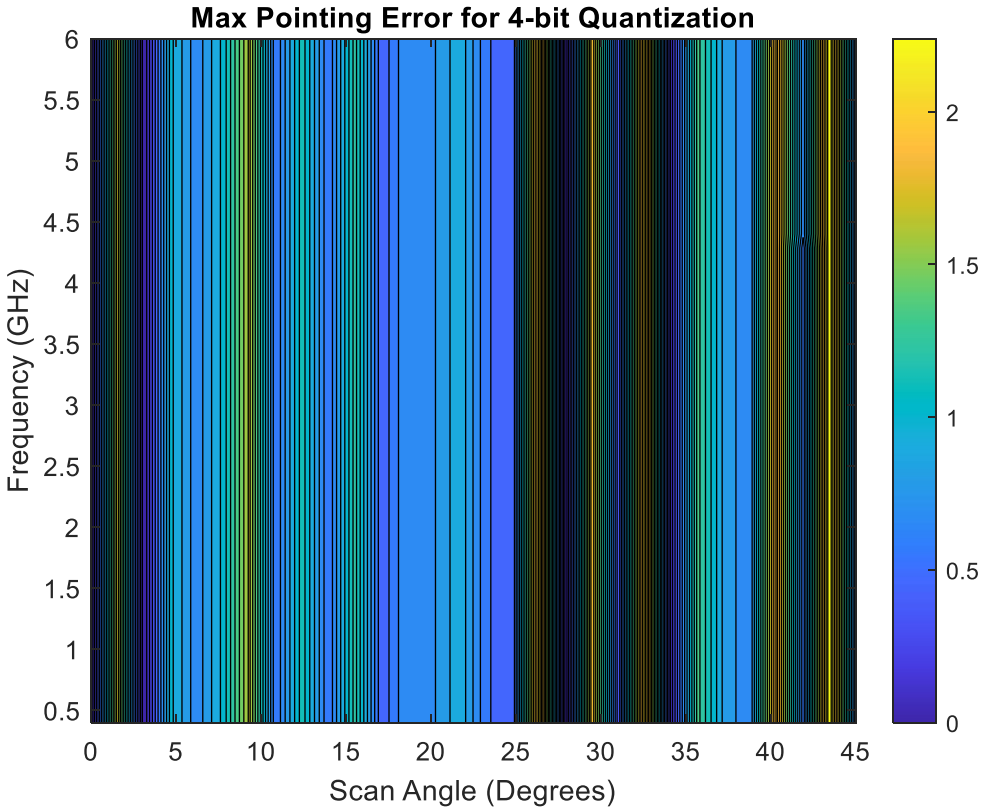


Figure 109. Maximum pointing error for 8-element array with varying TDU values.

The amplitude error also degraded slightly with this arrangement, degrading by -0.06dB with b = 4 for example. See Figure 110.

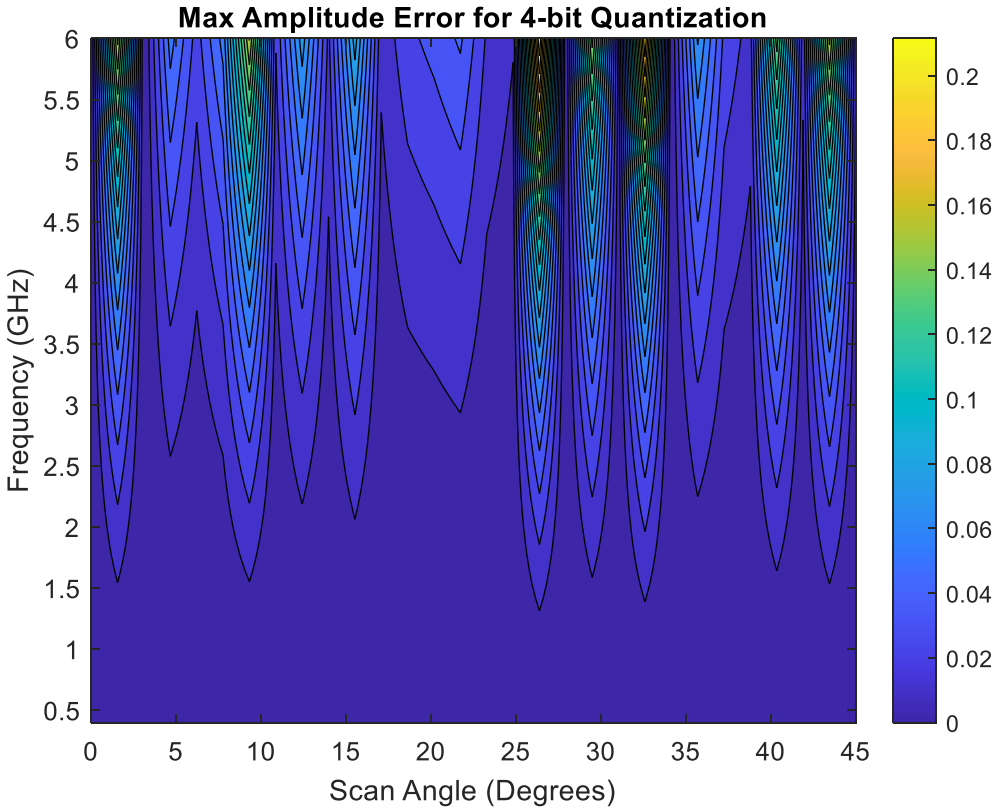


Figure 110. Amplitude error for 8-element array with varying TDU values, b = 4.

However, the average and maximum QSLL have significantly improved. The average QSLL has improved by 10 dB, 5.6 dB and 3.2 dB for b=3, 4 and 5 respectively. The peak QSLL has improved as well by 4.15 dB, 2.75 dB and 2.2 dB for b=3, 4 and 5 respectively.

Figure 111 shows a comparison of the QSLL for the case when all TDUs are uniform (as in Figure 77) and for the case when each TDU has an optimum maximum delay. It is clear that with the latter scheme, the QSLL is consistently lower, however only drops to -20 dB around boresight and not at any other scan angle. (This comparison is at 6 GHz with 4 bits.)

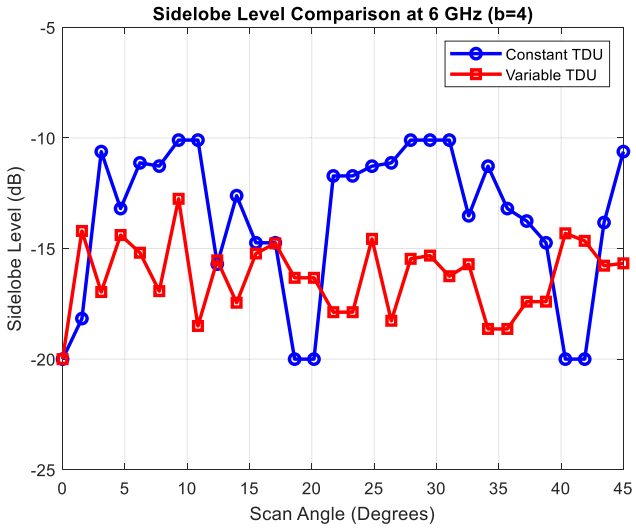


Figure 111. QSLL with different delay TDUs as compared with the QSLL when all TDUs are the same.

Overall, the complete performance of QSLL is shown in Figure 112.

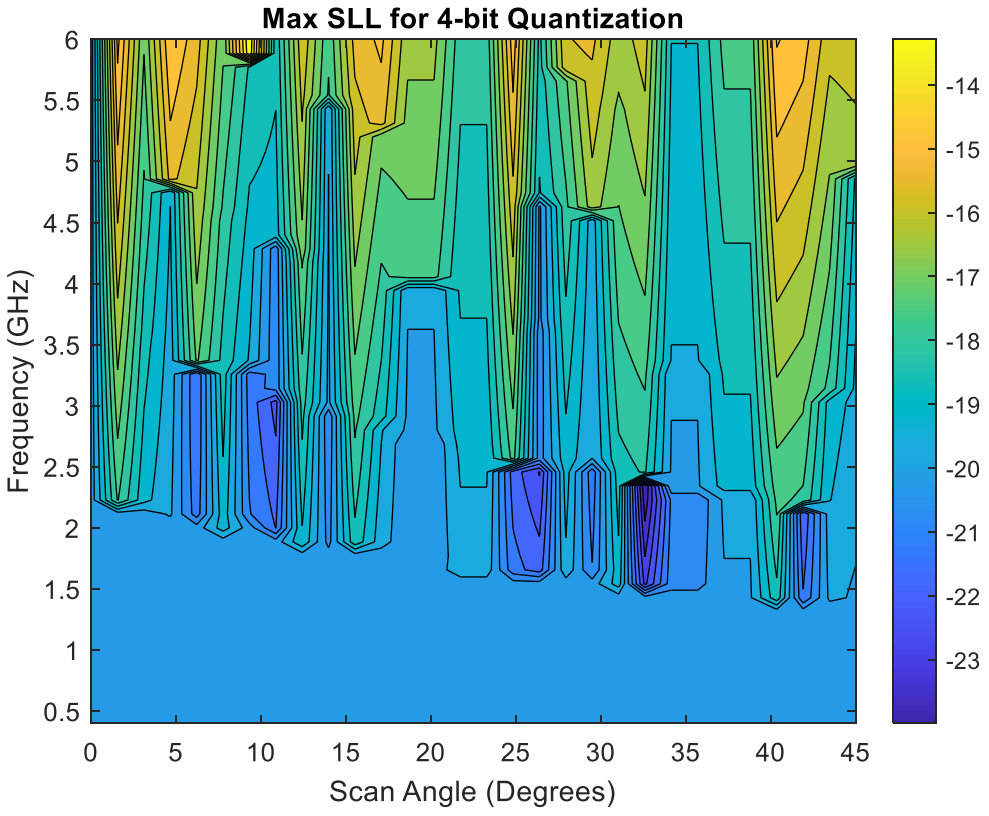


Figure 112. QSLL for 8-element array with varying TDU values with b = 4.

As the QSLL under this arrangement has an average of -18.6 dB, with 4 control bits, one may wonder if it is necessary to have an amplitude profile to produce -20 dB sidelobes.

The performance with an amplitude profile to produce -18dB sidelobes was simulated and interestingly the QSLL profile retains the same shape but simply lifts up by an average of 1.3 dB, so the amplitude profile across the array does have an impact on the QSLL.

Also simulated was the performance with uniform TDU delay values and -18 dB sidelobe amplitude profile giving a similar result but with less impact; the QSLL only degraded by 0.85 dB and at those scan angles where previously the QSLL dropped to -20 dB, now the QSLL only dropped to -18 dB.

It seems sensible to consider using TDUs of differing delay so as to gain the benefit of improved QSLL for no extra complexity, with a small penalty of degraded pointing error. This scheme has the added attraction of requiring less PCB area as the delay lines are shorter for the shorter delay TDU. This topic is explored is greater detail in the next section.

Really the question of how many control bits comes down to what pointing and sidelobe level can be tolerated. For this research work, 4 control bits was chosen as a reasonable compromise between the complexity of increasing the number of control bits and the performance of beam resolution (pointing error) and the sidelobe levels.

The explanation for the effect on performance of varying the TDU maximum delay values is evident in the histogram of the quantisation errors of a full scan from -45° to 45° at 6 GHz, shown in Figure 113. Clearly evident is the uniform probability of errors with the uniform TDU values and the Gaussian shape for the errors with varying TDU values, i.e., the distribution is “noise-like”, pseudo random.

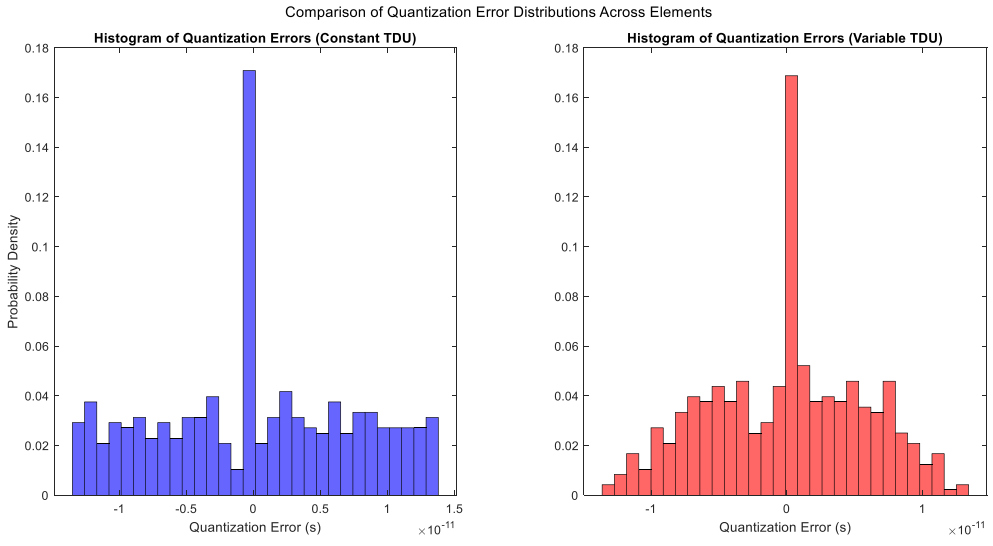


Figure 113. Quantisation errors for 8-element array (b = 4 at 6 GHz) for constant TDU values (left) and varying TDU values (right).

While the mean values for both are nearly the same at 0.2 and -0.05 ps respectively, the standard deviations are significantly different, with 7.3 ps for the uniform TDU version against 5.7 ps with the varying TDU version.

The regular periodic nature of the uniform TDUs generates highly correlated errors that give rise to the high peak sidelobes. The noise-like error distribution of the varying TDUs breaks up this correlation and somewhat smooths the sidelobes, as well as the main beam to some extent, which is why the pointing accuracy also degenerates. Finally, a plot of the error distribution per element for the two scenarios. See Figure 114. The box plot shows the median value as the red line in the middle of each box and the box encloses 50% of the values. The whiskers on each end show the extremes. Elements 1 and 8 are a little unusual in that for half the scan, (-45° to 0 and 0 to 45°) the error is zero, hence very concentrated errors in total. The red crosses show the extreme values in this case.

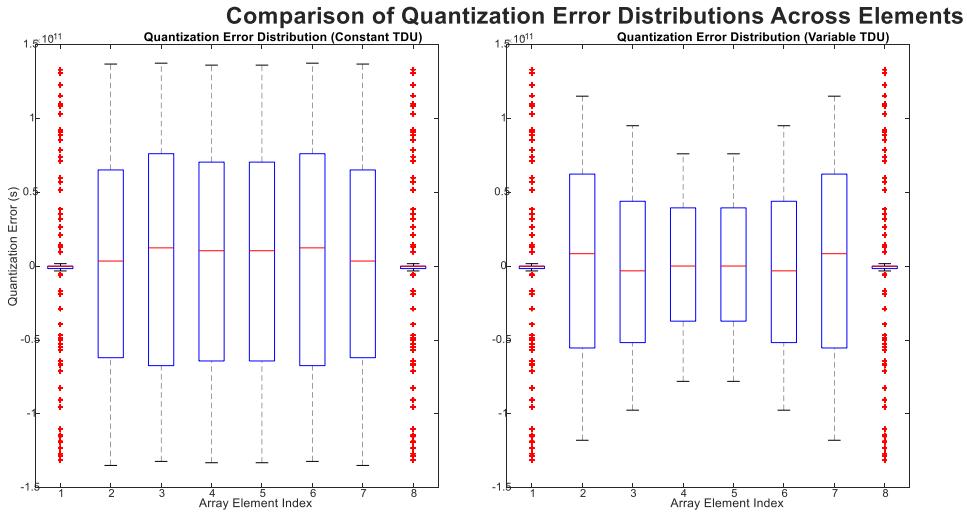


Figure 114. Quantisation error distribution per element for an 8-element array with uniform TDUs (left) and varying TDUs (right).

5.3. Theory

A significant benefit of using a hierarchical BFN design is the saving in real estate and the number of control bits required. For example, considering a 256 x 256 antenna array, the optimum BFN design across 3 layers saves 96% of the real estate and requires only half the number of control lines compared to a flat BFN design using a single layer of TDUs with uniform values per element. However, the lower layer TDUs of a hierarchical BFN are feeding widely spaced subarrays which introduces the risk of grating lobes.

In existing hierarchical TDU-based BFN designs, TDU values in each layer are generally the same, i.e. they are uniform in value. This, however, fails to capture the fact that the TDUs in

the center of an array do not need the full delay range of those TDUs at the edges. In this chapter, the approach leverages this practical insight by tailoring the TDU delay range within each layer to further enhance BFN performance. For a uniform linear or planar array, it is the TDUs at the edges that must swing from maximum to minimum delay whereas those in the middle need only swing around half the delay range. Here, the least-significant-bit (LSB) of centre TDUs is reduced while maintaining constant bit depth across the layer, to lower the quantisation resolution where full range is unnecessary. There is also the option to reduce the number of control bits for the central TDUs, which can be readily extended based on the design here.

This profile-based approach reduces the number of large quantisation errors and increases the number of small ones, thereby reshaping the distribution of errors across the array in a beneficial way**.** This logic is consistent with the observations in the previous Section and will be quantitatively developed throughout the following analysis.

Notation Consistency

Variables that vary across the antenna elements are expressed as functions of p, x and y (e.g., $r_n(p)$, $LSB_n(x,y)$), while layer indices n are treated as fixed parameters and indicated by subscripts. This convention distinguishes element-specific quantities from layer-specific parameters and is used consistently in both linear and planar array formulations.

5.3.1. Linear Array

The analysis begins by considering every possible design variant of a hierarchical BFN for a linear array.

Given a linear array with M elements, where M is a power of 2, the number of division levels D is,

$$D = \log_2 M \,. \tag{5.1}$$

Note that division level 1 is at the lowest level, furthest from the antenna radiating elements.

Let L denote the number of layers of TDUs. Each TDU layer may be placed on any division level from 1 to D and multiple layers may reside on different or the same levels, depending on the design requirements.

Let d_n denote the actual division level where there is a layer of TDUs and n is the number of the TDU layer and d_n is equal to the division level that incorporates the TDU layer of

number n. (For example, $d_2 = 4$ means that the second layer of TDUs in on the 4th division level.)

Next, the scanning details for each layer of TDUs is calculated from the size of each corresponding subarray, M_n. This is the number of array elements fed from the group of TDUs on layer n, fed from a single TDU on the layer *n*-1.

$$\begin{aligned} M_1 &= M \\ M_n &= \frac{M}{2^{d_{n-1}}}, \qquad \forall n \in \{2,....,L\}. \end{aligned} \tag{5.2}$$

The size of each subarray, in wavelengths, is given by h_n.

$$\begin{aligned} h_1 &= M_1 e_p \left(1 - \frac{1}{2^{d_1}}\right) \\ h_n &= M_n e_p \left(1 - \frac{1}{2^{(d_n - d_{n-1})}}\right), \qquad \forall n \in \{2,....,L\}, \end{aligned} \tag{5.3}$$

where e_p denotes the separation, or pitch, of antenna elements in wavelengths.

Considering the maximum scan angle $\theta_{\max}$, the scan distance for each subarray is given by

$$h_n^{scan} = h_n \sin\theta_{\max}. \tag{5.4}$$

The maximum delay $T^{\max}$ required at each TDU layer is calculated as the sum of any error from the TDU layer below, due to quantisation, plus the value necessary to achieve the scan required of the subarrays fed from that layer of TDUs.

$$\begin{aligned} T_1^{\max} &= \frac{h_1^{scan}}{c} \\ T_n^{\max} &= \frac{h_n^{scan}}{c} + T_{n-1}^{qe}, \qquad \forall n \in \{2,....,L\}, \end{aligned} \tag{5.5}$$

where T_{qe} is the quantisation error time delay.

The maximum LSB value of each TDU is simply the maximum delay divided by the number of bits controlling that TDU,

$$LSB_n^{\max} = \frac{T_n^{\max}}{2^{b_n} - 1}, \qquad \forall n \in \{1,....,L\}, \tag{5.6}$$

where b_n is the number of control bits for layer n.

The delay error from the TDU below can be calculated as half the value of the LSB of that layer. (This assumption is widely adopted in phased-array analysis; however, its limitations in hierarchical architectures will be examined in Chapter 6.)

The quantisation error values are

$$T_n^{qe} = \frac{LSB_n}{2}, \quad \forall n \in \{1,....,L\} \ . \tag{5.7}$$

This quantisation error accumulates through the hierarchy and plays a direct role in the final phase accuracy at the antenna elements.

5.3.1.1. TDU range profile across a layer

The calculation of the TDU delay values for each layer depends on the number of subarray elements formed by the TDUs at that layer and the number of array elements fed from a single TDU. Symmetry exists both within each subarray and across the complete array, since the array must steer symmetrically in both directions.

If each antenna element is indexed by p, a modified index p' is introduced to account for the subarray structure and to enforce symmetry about the centre of the array.

For each layer $\forall n \in \{1,....,L\}$, the delay profile is defined over subarrays of size M_n. The value of p'_n is computed as follows.

Let the local index r_n of antenna element p within its layer n subarray be

$$r_n(p) = (p-1) \bmod M_n, \quad \forall p \in \{1,....,M\}, \tag{5.8}$$

where $(.) \bmod$ is modular arithmetic.

The subarray resolution factor f_n is defined as:

$$f_n(p) = \lfloor r_n \cdot 2^{d_n - D} \rfloor, \quad \forall p \in \{1,....,M\}. \tag{5.9}$$

The floor function $\lfloor . \rfloor$ rounds a number to the nearest integer towards negative infinity.

Then the center-reflected subarray index p'_n is,

$$p'_n(p) = \max\left(f_n, 2^{d_n - d_{n-1}} - 1 - f_n\right), \quad \forall p \in \{1,....,M\}. \tag{5.10}$$

Note that $d_0 = 0$. For implementation or visualisation purposes, these expressions can alternatively be simplified by calculating the top half of the array and applying mirror symmetry.

Within each subarray, the TDU delay values decrease toward the centre. The step size, Δ, for each layer is calculated as

$$\Delta_1 = \frac{h_1^{scan}}{c \cdot \left(2^{d_1} - 1\right)}$$
$$\Delta_n = \frac{\Delta_{n-1}}{2^{d_n - d_{n-1}}} \quad , \; n \in \{2,....,L\}. \tag{5.11}$$

Combining the step size with p', the LSB value at each element $\forall p \in \{1,....,M\}$ for each layer $\forall n \in \{1,....,L\}$ are given recursively,

$$LSB_1(p) = \frac{\Delta_1 \cdot p'_1}{2^{b_1} - 1}, \qquad for \; n = 1$$
$$LSB_n(p) = \frac{\frac{1}{2} \cdot LSB_{n-1}(p) + \Delta_n \cdot p'_n}{2^{b_n} - 1}, \qquad \forall n \in \{2,....,L\}. \tag{5.12}$$

Introducing a delay profile within a layer reduces the maximum quantisation error at each TDU by lowering the LSB value toward the centre. Consequently, the next layer up in the BFN requires a smaller delay range, as it must only compensate for the reduced residual error passed up from the previous layer. This compression effect accumulates through the hierarchy, enabling space and error reductions.

It should be noted that this profiling opportunity exists only if the subarray contains at least four TDUs. When only two TDUs are present in a subarray, there is no scope for variation in the centre delay values. Therefore, a minimum of two division levels is required between adjacent TDU layers to enable profiling.

The value of the most significant bit (MSB) for each TDU is calculated as

$$MSB_n^p = \frac{2^{b_n}}{2} LSB_n^p,$$
$$\forall p \in \{1,....,M\} \quad and \quad \forall n \in \{1,....,L\}. \tag{5.13}$$

And the total TDU delay value for every TDU is

$$TDU_n^p = LSB_n^p \left(2^{b_n} - 1\right)$$
$$\forall p \in \{1,....,M\} \quad and \quad \forall n \in \{1,....,L\}. \tag{5.14}$$

Using the established formulae for the LSB delay values at each array element p in layer n, the number of TDUs required in the layer and their corresponding delay values can be determined.

There are 2^{d_n} TDUs in layer n.

Inspection of the LSB values reveals the delay range required across the layer.

As an example of the methodology, consider the design shown in Figure 115, which corresponds to variant 7390 from [101], identified as the optimal solution for a 128-element linear array at 30 GHz. The caption of Figure 115 shows the TDU delay values and control bits for the linear array with an element pitch of $\lambda/2$ for a maximum scan angle of ±60° from boresight.

A ±60° scan angle is commonly used in array antenna studies as it represents a challenging yet realistic test of array performance.

Figure 116 is a graph of the total delay value for each TDU on each of the 3 layers. On layer 1, there are 2 TDUs (i.e. 2^{d_1}) and because of the small count, there is no opportunity to apply profiling, each must provide the full required delay range. The graph for layer 2 (red) shows the step down in maximum delay value from 1020 ps to a minimum of 673.6 ps for the 32 TDUs on layer 2, division 5. Each TDU on layer 1 feeds 16 (i.e. $2^{d_2-d_1}$) TDUs on layer 2 and 64 (i.e. 2^{D-d_1}) array elements. The step down in value for each layer 2 TDU is calculated to achieve the maximum delay value required for the subarray of 64 array elements to be able to achieve the delay for the maximum scan angle.

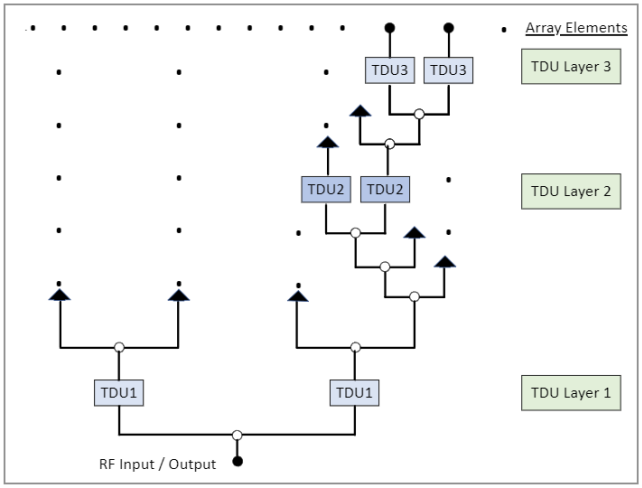


Figure 115. 128 linear array design, TDU1 has 2 bits and T_{LSB} =307.9 ps, TDU2 has 4 bits and T_{LSB} =68 ps and TDU3 has 6 bits and T_{LSB} =1.2 ps.

At each higher layer this same profiling approach is extended to calculate the maximum TDU delay value required across the subarray.

In this example there are 8 unique values on layer 2 and 16 unique values on layer 3. Since most of the performance benefit arises from the lower layers, a full set of unique values at the highest layer may not always be necessary in practical implementations.

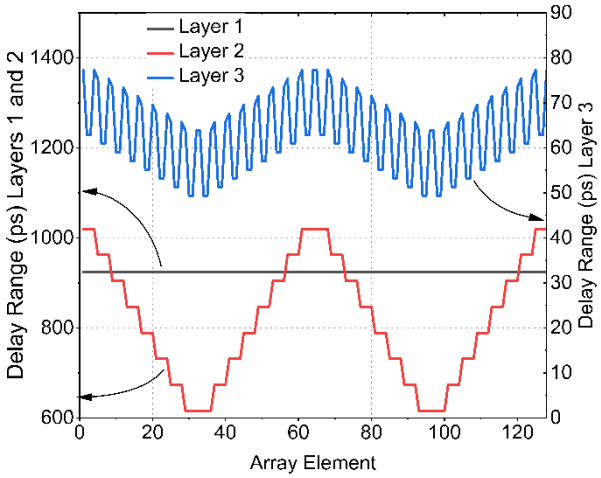


Figure 116. Graph of the TDU values on each of layers 1, 2 and 3 along the full length of the 128-element linear array with the design shown in Figure 115.

Varying the LSB delay values, as described here, reduces both the RMS phase error along the array and the physical area required to implement the TDUs.

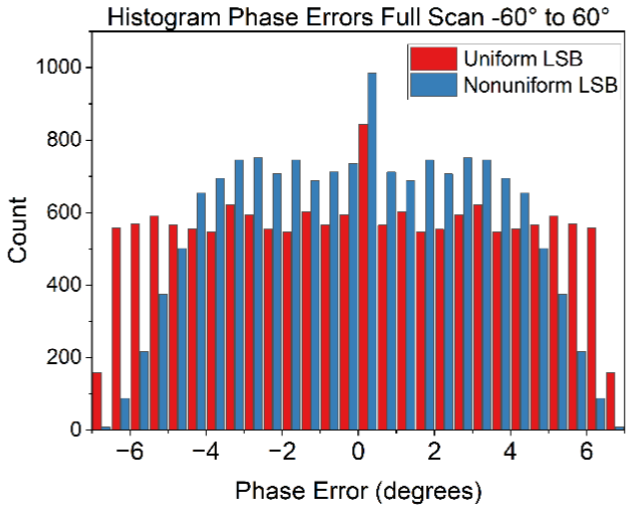


Figure 117. Combined histograms for the element phase errors for the 128-element linear array with the nonuniform TDUs and uniform TDUs for a full scan from -60° to 60°, showing many more smaller errors and fewer large errors for the nonuniform TDUs as compared with uniform TDUs.

This effect is illustrated in Figure 117, which shows the phase error occurrences for a full scan of the linear array from -60° to 60°. The uniform TDU case exhibits an even spread of phase error values, while the nonuniform case produces a distribution with many small errors

and fewer large deviations. This shift improves RMS phase error and results in better beamforming performance.

To calculate the resulting array phase error, note that it is governed entirely by the final layer of TDUs that provides the final correction after cumulative delays from earlier layers. The accuracy of this adjustment determines the deviation from the ideal delay at each antenna element and thus the resulting phase error. Assuming each element's delay error is uniformly distributed within ±½ LSB, the RMS error is equal to the standard deviation (σ) of the error, as the mean is zero and has been given by Mailloux [2] as,

$$\sigma = \frac{LSB}{2\sqrt{3}}. \tag{5.15}$$

Now that the LSB values of the TDUs have been varied, there is a range of LSB value errors. In principle, the overall variance could be calculated by a weighted sum of individual TDU variances, but this is unnecessarily complex. Because the LSB profile across the array is nearly linear, the square of the delay errors also varies slowly and approximately linearly.

This justifies using the arithmetic mean of LSB values as a direct estimate for RMS phase error, with negligible loss in accuracy (<0.0003%).

Then, the average TDU delay value is the midpoint between the delay at the edge and the delay at the minimum of the LSB range. This average value is then used in (5.15) to estimate the resulting phase error.

To estimate a TDU footprint, the method proposed in [5] is adopted. This method compares the area required for uniform versus varying delays and assumes TDUs are implemented on a PCB and occupy square unit cells of area a x a . The researchers proposed a scheme of a single length of line, equal to the delay required by the MSB, which occupies no more than half the unit area, leaving space for shorter delay lines.

If a PCB has a relative permittivity of 2, then 10 mm of line equals about 47 ps of delay. Working at 30 GHz, this equates to a unit cell of 3.5 mm x 3.5 mm, being half a wavelength square, allowing for an MSB line length of 10.5mm, equal to approximately 50 ps delay, such that the whole cell delivers a maximum delay of twice the MSB delay, giving a TDU of 100 ps delay in an area of 12.25 mm^2. This ratio is used consistently for all real estate calculations.

Since the schematic structure is unchanged, space savings arise solely from the reduced delay range requirements per TDU, particularly in lower layers.

Putting this all together, the application of the proposed method to the baseline 128-element linear array design (variant 7390, as per Figure 115) results in a 13.3% reduction in TDU footprint and a 13.7% improvement in RMS phase error, decreasing from 3.84° to 3.31°. This phase error reduction incurs no performance penalty and demonstrates a measurable gain in sidelobe suppression alongside significant space savings. Figure 118 shows the beam pattern for a –60° scan, comparing the case with and without the TDU delay profile. The overall array pattern remains largely unchanged, with no detrimental effects introduced, and the proposed method improves the response by a few decibels in certain regions. In particular, it suppresses a grating lobe near 30°, which corresponds to one of the grating lobes introduced by the periodic subarray structure formed by the first TDU layer. In this case, the array is divided into four 32-element subarrays spaced 16λ apart, resulting in the formation of 32 grating lobes. In a perfect array, these grating lobes would be perfectly cancelled due to the nulls in the array and subarray array factors. However, the partial visibility of the grating lobe at 30° arises from the degradation of these ideal nulls by quantisation errors. Although reduced in amplitude, the angular position and frequency-aligned behavior support its classification as a suppressed grating lobe rather than a conventional sidelobe.

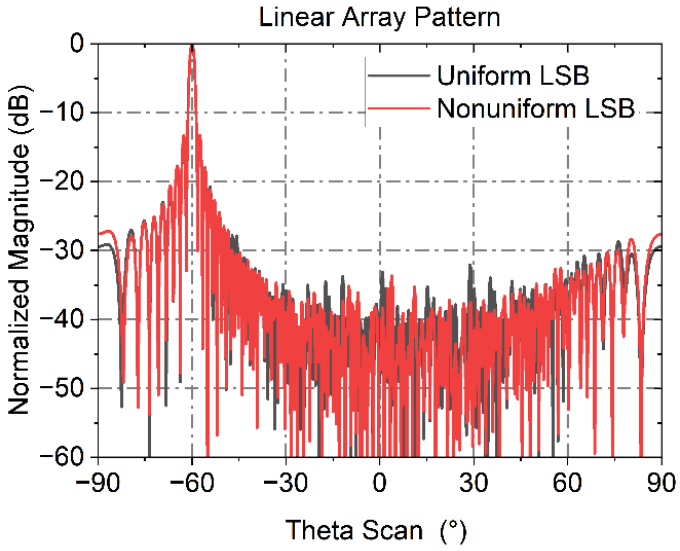


Figure 118. Array pattern for a 128-element linear array with constant TDU LSB values in a layer and varying TDU LSB values.

More importantly, introducing nonuniform TDU values changes the ILP-optimal solution itself. A revised configuration using 2, 6 and 5 bits on layers 1, 5 and 7, respectively meets the same phase error target with a 21% footprint reduction. This result shows that the proposed methodology both improves existing designs and enables new, more compact solutions that meet the same performance objectives.

All performance comparisons in this chapter use unity input amplitudes at each element, with no amplitude tapering or transmission line loss included. The observed improvements in sidelobe and grating lobe suppression are entirely attributable to the phase structure introduced by nonuniform TDU delays.

5.3.2. Planar Array

The core principles applied to linear arrays extend naturally to two-dimensional planar arrays. In such arrays, TDUs near the center require less delay than those at the periphery and this now holds in both the horizontal and vertical directions. As a result, the maximum delay values occur along all four edges of the array, decreasing progressively toward the centre. This creates a bowl-shaped TDU delay distribution, sometimes multiple adjoining bowls, depending on the number and placement of TDU layers across division levels.

In a 2D planar array, each division level subdivides the array by a factor of 4, unlike the binary division applied in linear arrays. If the total number of M is a power of 4, the number of division levels is given by,

$$D = \log_4 M \,. \tag{5.16}$$

The size of each subarray, in wavelengths, is derived from the linear array case but scaled appropriately to account for the maximum distance occurring along the diagonal of the square array elements,

$$\begin{aligned} h_1 &= M_1 e_p \sqrt{2}\left(1 - \frac{1}{d_1}\right) \\ h_n &= M_n e_p \sqrt{2}\left(1 - \frac{1}{2^{(d_n - d_{n-1})}}\right), \qquad \forall n \in \{2,....,L\}. \end{aligned} \tag{5.17}$$

To compute the maximum delay required on each TDU layer, each array element is indexed by its position (x, y) in a Cartesian coordinate system, where x and y are integer values representing the column and row numbers, respectively. Here both x and y are in the range $\forall x, y \in \{1,....,2^D\}$.

The TDU delay profiles for each element on each layer are computed by treating each array element as the intersection of a row and a column linear array. For an element at (x, y) the required delay is calculated from its position in both the row and the column and assigned the maximum of the two as the TDU delay for that position.

Using (5.8) to (5.12), the LSB values for the row and column linear arrays are calculated separately, substituting x and y for p and the planar TDU LSB value is given by,

$$LSB_n(x,y) = \max(LSB_n(x), LSB_n(y))$$
$$\forall x, y \in \{1,....,2^D\}, \qquad \forall n \in \{1,....,L\}. \tag{5.18}$$

The MSB values and total TDU delay values for the planar array elements are determined using the same method described in (5.13) and (5.14).

As an example, consider a 256 x 256 array, with L=3, $\theta_{\max} = 60°$ scanned across all azimuth directions. The array operates at 30 GHz with $\lambda/2$ element pitch.

Applying the integer linear programming method from [101] yields an optimal baseline configuration with TDUs on division levels 2, 6 and 8, and control bit depths of 2, 5 and 6, respectively. Applying the proposed nonuniform TDU profile to this baseline yields an 11.2% reduction in TDU footprint and a 6.5% improvement in RMS phase error.

More significantly, introducing nonuniform TDU values expands the design space, yielding 24 new candidate configurations that meet all design constraints. One such configuration, with TDUs on levels 4, 6 and 8 and bit depths of 3, 3 and 6, achieves a 29.9% reduction in space, a slight improvement in average sidelobe level (from –47.36 dB to –47.72 dB) and a 1.8% reduction in control lines, with only a 0.25% increase in the number of TDUs.

These results highlight that nonuniform TDU profiles not only reduce spatial and phase error overhead in existing designs, but also enable new, more compact solutions with improved sidelobe performance.

Because the top layer's LSB profile depends on both the profiles and control bit allocations of all underlying layers, it is not trivial to express the final phase error with a simple analytical formula. Instead, the final phase error is calculated exactly for each design variant of interest, of which only a small number are relevant.

To illustrate the complexity of a typical TDU delay profile in a large array, Figure 119 shows the maximum delay values of the TDUs on layer 2 for row 145 in the 256×256 planar array. The profile is neither linear nor uniformly stepped; rather, it varies nontrivially along the row due to the hierarchical structure, the influence of underlying TDU layers and the specific spatial location of each TDU. This nonuniform shaping of delay values is a deliberate feature of the proposed method and plays a key role in disrupting regular phase error patterns that would otherwise reinforce grating lobes.

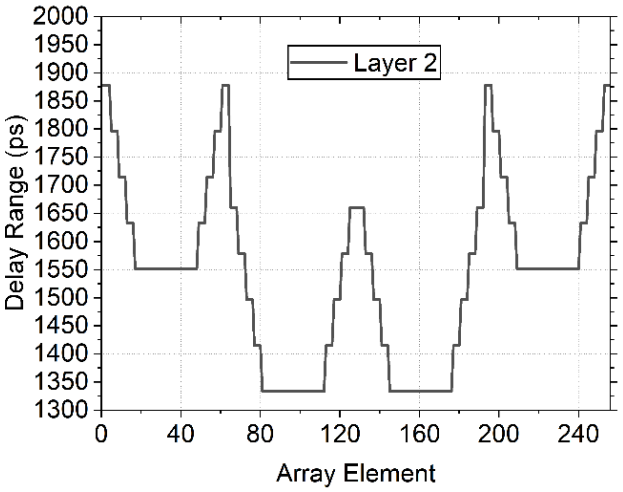


Figure 119. The TDU values for row 145 of a 256x256 planar array with varying TDU LSB values on layer 2.

While the reduction in RMS phase error from varying LSB values is modest, the corresponding redistribution of quantisation errors, with more small errors and fewer large ones, results in meaningful suppression of grating lobes. This improvement is not a product of randomness, but rather of breaking structured and repeating error patterns that promote sidelobe formation.

Figure 120 presents the close-in array factor in UV space for the baseline design from [101] which uses uniform TDU values in each layer. The main beam is steered to the scan direction $U = V = -0.61$. The prominent lobe near $U = V = -0.456$ closely matches the theoretical position of a grating lobe arising from the large subarray separation (32λ) introduced by the first TDU layer in both x and y directions. This periodic spacing gives rise to 46 grating lobes along the diagonal (U = V) for a 60° scan. These lobes are distributed across the visible region, but several are particularly apparent in the range between –0.4 and –0.5 due to quantisation-induced degradation of ideal array-level and subarray level nulls. Their spatial alignment with predicted grating lobe locations confirms their origin, distinguishing them from conventional sidelobes.

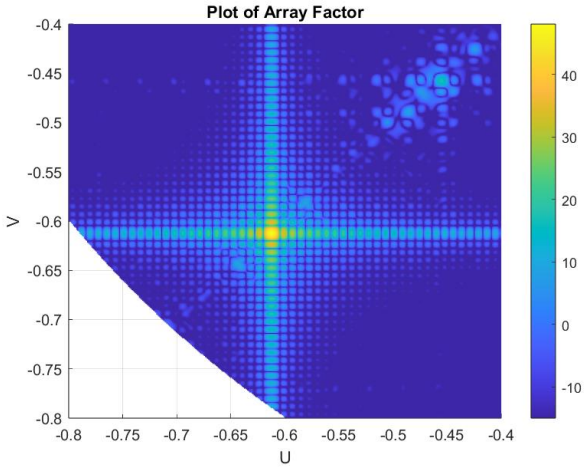


Figure 120. Array pattern plot for 256x256 array with constant TDU values in each layer highlighting the grating lobes.

After applying the proposed LSB variations across all layers, the grating lobe and adjacent sidelobes are suppressed. This is visually shown in Figure 121 and further quantified in Figure 122, which compares the diagonal array factor cut for uniform and nonuniform TDU configurations.

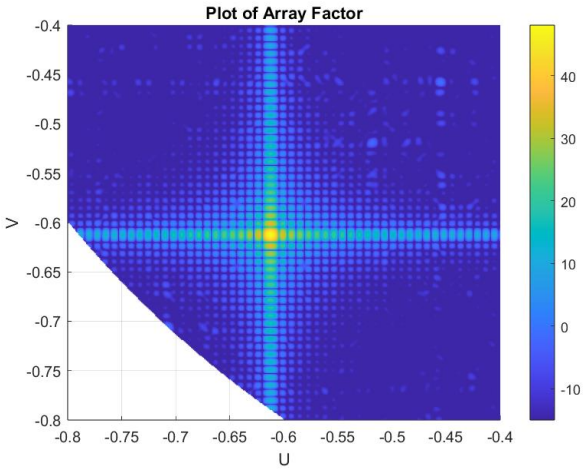


Figure 121. Array factor plot for 256x256 array with varying TDU values on each layer and lower grating lobes.

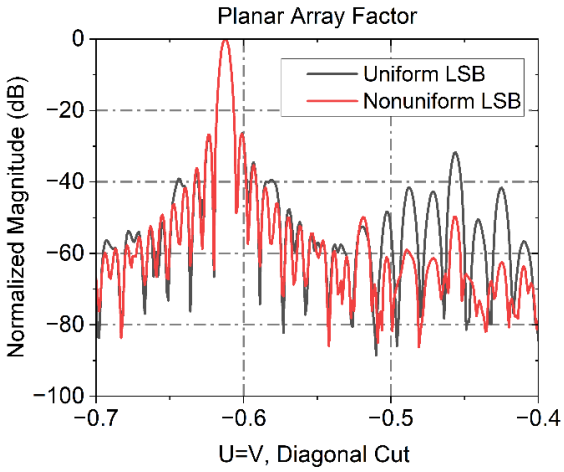


Figure 122. Array pattern plot for 256x256 planar array with comparison of uniform and nonuniform TDU values for a diagonal cut of U=V showing improvement to close-in grating lobes.

The primary grating lobe is reduced by 18.0 dB with some surrounding sidelobes are suppressed over 20 dB.

This example illustrates that even modest improvements in phase accuracy, when distributed in a less structured manner, can significantly improve grating lobe and sidelobe performance in large arrays. A more detailed analysis of this effect, including the underlying phase error distribution, is presented in the following section using full-wave simulation of a 16×16 array.

5.4. Verification Through Full Wave Simulation

To verify the performance of the proposed method in the presence of mutual coupling and practical antenna effects, a full-wave electromagnetic simulation was conducted using Ansys HFSS R2023 R2.1. A broadband 16×16 planar array was modelled with each element excited at constant amplitude and phase-shifted according to the proposed TDU configurations.

The array employs Vivaldi antennas as elements, designed using established techniques such as in [102]. As shown inFigure 123, each element is modeled as a perfect electric conductor on either side of a 16 mil Rogers 4003 laminate. Elements are fed via a central stripline within the substrate, with the taper defined by the exponential profile $y = 0.05e^{0.135z}$. The array pitch is 5 mm, corresponding to half a wavelength at 30 GHz.

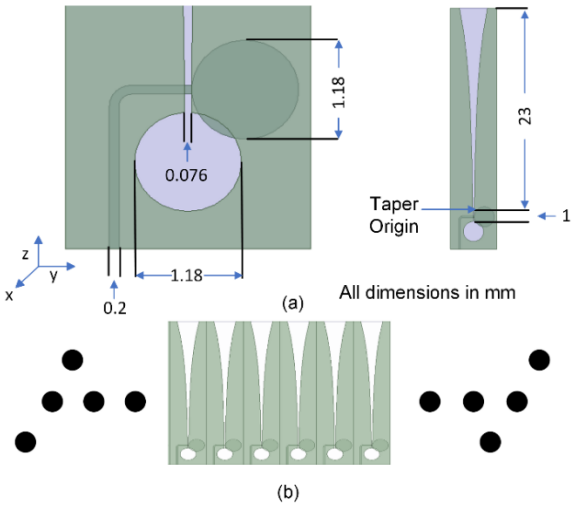


Figure 123. (a) Vivaldi element details and (b) section of 16x16 element planar array.

The beamforming network comprises two TDU layers, placed at division levels 2 and 4, with 2 and 6 control bits respectively. The maximum LSB time delays are 81.6 ps and 1.62 ps for layers 1 and 2.

Full-wave simulation confirms that both uniform and nonuniform TDU configurations support complete beam steering across the intended scan range. At 30 GHz and a 60° scan angle, both configurations achieve a gain of 29.4 dBi, with a VSWR of 2.2 measured at the corner element. This confirms that the aperture efficiency remains unchanged despite the modifications to the BFN.

A notable improvement is observed in sidelobe levels, with reductions of up to 11.3 dB when using nonuniform TDU values, as illustrated in Figure 124. In the uniform case, three prominent sidelobes appear, which are substantially suppressed under the nonuniform configuration.

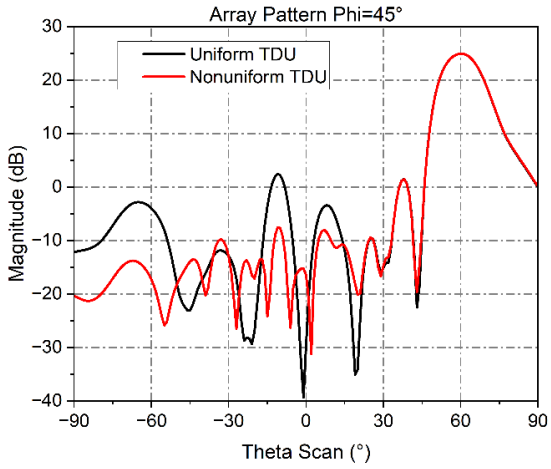


Figure 124. Full-wave simulation array pattern plot for 16x16 planar array with uniform and nonuniform TDU values at 30 GHz.

These results confirm that applying a tailored TDU LSB profile can improve both phase accuracy and sidelobe performance in practical antenna arrays.

Since the Vivaldi antenna is a broadband element, a further comparison was performed at 10 GHz using the same 16×16 array configuration with both uniform and nonuniform TDU values. See Figure 125. At this frequency, the array achieves a gain of 17.7 dBi, with a corner-element VSWR of 3.9 for both configurations.

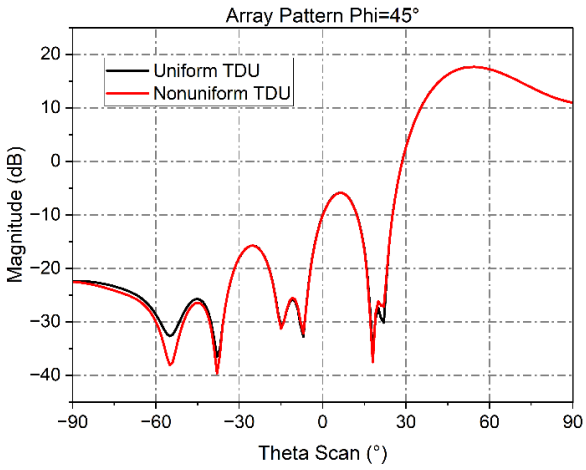


Figure 125. Full-wave simulation array pattern plot for 16x16 planar array with uniform and nonuniform TDU values at 10 GHz.

At 10 GHz, however, there is little observable suppression of grating lobes when using nonuniform TDU values. This is due to the shorter electrical element spacing, the elements are spaced at $\lambda/6$ and the subarrays are separated by $2\lambda/3$. Under these conditions, no grating lobes fall within the visible region and thus the benefits of quantisation error reduction do not manifest as sidelobe suppression in this case. Nonetheless, the space-saving advantages of the proposed TDU profile remain fully applicable across frequency.

5.5. Discussion

a) **Profiling Depth Benefit vs Benefit Trade-Off**

To satisfy typical phase error specifications, it is essential to include a layer of TDUs at the highest division level (closest to the antenna elements). Without this, multiple elements may share the same delay value, causing phase errors to grow unbounded with increasing scan angles.

A TDU layer at the first division level does not offer any scope for delay range variation. In contrast, delay profiling becomes increasingly effective in higher-level TDU layers where more elements are grouped. However, a minimum spacing of two division levels is required for meaningful profile variation.

b) **Dominant Impact of Lower TDU Layers**

The majority of the space-saving benefit arises from the lower TDU layers. In the 256x256 planar array example, layers 1 and 2 (division levels 2 and 6) account for 63% of the total space saving, while the remaining reduction is achieved by applying nonuniform TDU values to the top layer. Similarly, 16.7 dB of the total 18 dB grating lobe suppression results from applying nonuniform TDU values in just these two layers. This suggests that even partial profiling, limited to lower TDU layers, captures most of the benefit and offers a practical trade-off between complexity and performance. Designers of large-scale arrays may find this balance attractive, especially when facing constraints in fabrication, layout, or computational optimisation.

c) **Applicability to Irregular Array Topologies**

The proposed method extends to irregular arrays, including clustered, thinned, or sparse layouts, since the core principle still holds: elements near the array center require less delay range than those at the edges. Thus, the method is robust and adaptable across practical array architectures.

d) **Implementation Overhead and Design**

In the 256×256 array example, the number of distinct delays is 2 in layer 1, 16 in layer 2 and 32 in layer 3. With modern CAD tools and PCB manufacturing workflows, this level of variation presents little difficulty in layout or fabrication. Nonetheless, design teams must account for the added complexity during integration, particularly in large-scale or cost-sensitive systems.

5.6. Conclusion

This chapter presents a new methodology for optimising hierarchical beamforming networks by applying nonuniform delay profiles within TDU layers. A systematic approach is proposed for designing these delay profiles, tailored to the array structure, enabling meaningful reductions in both physical footprint and phase quantisation errors.

Beyond space and error savings, a central contribution of this work is the demonstrated suppression of grating lobes, achieved by reshaping the distribution of phase errors.

Numerical evaluation and full-wave electromagnetic simulations confirm that the proposed approach yields substantial improvements, including an 18.0 dB grating lobe reduction in a 256x256 planar array and a 29.9% space saving compared to the baseline configuration.

These results establish the effectiveness and practicality of the proposed method and position it as a scalable solution for advanced BFN design across a range of array sizes and configurations.

6. Practical Considerations for TDU Design

6.1. Impact of Quantisation Errors on TDU Sizing

As has been emphasised, TDUs can be expensive and increase in complexity as the number of control bits increases, so they tend to be used sparingly. The hierarchical architecture, also known as a multilevel BFN or “time delay in a corporate feed” [99], enables significant savings in physical space, cost, and interconnect complexity compared to a flat, single-layer design, especially for large arrays. To further reduce the size, complexity, and cost of the beamforming system, it is often desirable to limit the resolution (i.e., number of control bits or bit depth) of the TDUs. This introduces quantisation errors which must be carefully managed to avoid performance degradation, as noted by Miller in 1964 [29] and more recently by Haupt [103].

It is standard practice to assume that quantisation errors passed from one TDU layer to the next are bounded by half the least significant bit (LSB/2) of the lower layer [33], as was done in Chapter 5. This assumption, supported in classical phased array texts such as Mailloux [33] and commonly adopted in practical designs [101], [104], can however breakdown in hierarchical architectures. As TDU resolution decreases, quantisation errors grow. If the delay range of an upper-layer TDU is insufficient to accommodate both the ideal delay and the propagated error, the required delay may exceed the TDU's physical limits, causing truncation and introducing large phase errors that significantly degrade array performance.

Truncation is primarily a concern in large arrays with deeply layered TDUs, where errors accumulate across levels. The risk of truncation is highest near the design scan limits and when lower layers use coarse quantisation. Single-layer systems, by contrast, are immune to this issue.

6.2. Truncation Effects in Hierarchical TDUs

To demonstrate the practical consequences of truncation, consider a 128-element linear array, with λ/2 spacing, operating at 30 GHz with three TDU layers, each using uniform bit allocations per layer, as shown in Figure 126. (The same example as was used in section 5.3.1)

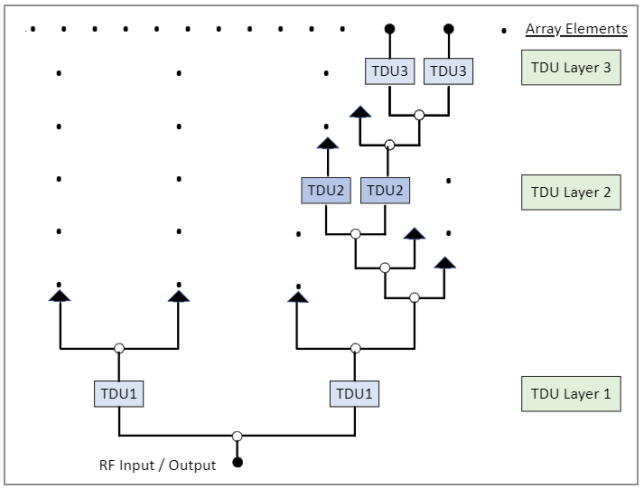


Figure 126. 128 linear array design, TDU1 has 2 bits and T_{LSB} =307.9 ps, TDU2 has 4 bits and T_{LSB} =68 ps and TDU3 has 6 bits and T_{LSB} =1.2 ps - 128 TDU in total.

Figure 127 is a visualisation of the array factor magnitude simulation for every scan angle from zero to 60°, with 10-bit control for each layer of TDUs, following the methods of Clenet et al. [105]. As expected, the quantisation error is negligible, and the array maintains excellent performance across the full scan range.

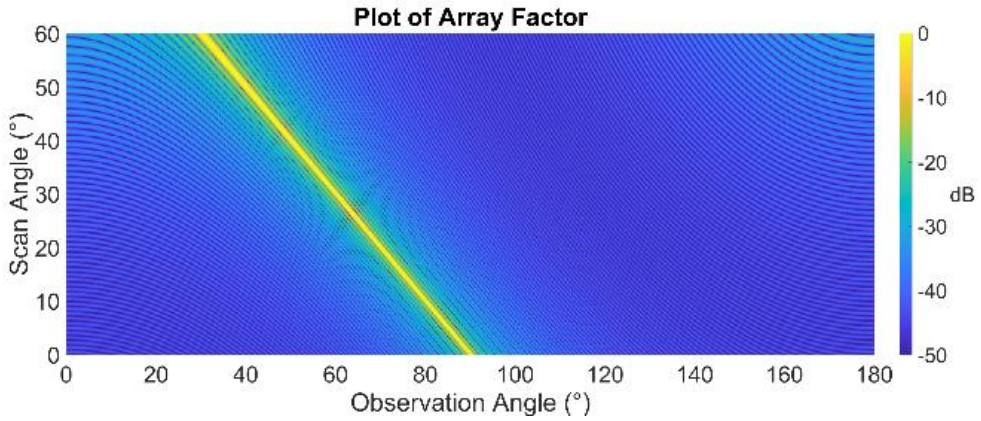


Figure 127. 128-element linear array, with 10 bit TDU control, scanned from zero to 60°.

Figure 128 shows the effect of reduced control resolution of 2, 4, and 6 bits on TDU layers 1, 2, and 3, respectively, as per Figure 126. No range limits are enforced, and the delay values are allowed to exceed the physical bounds of the TDU, that is, truncation is not yet applied. Despite the lower resolution, the performance remains acceptable. This indicates that quantisation error alone is manageable if the TDU can accommodate the full required delay.

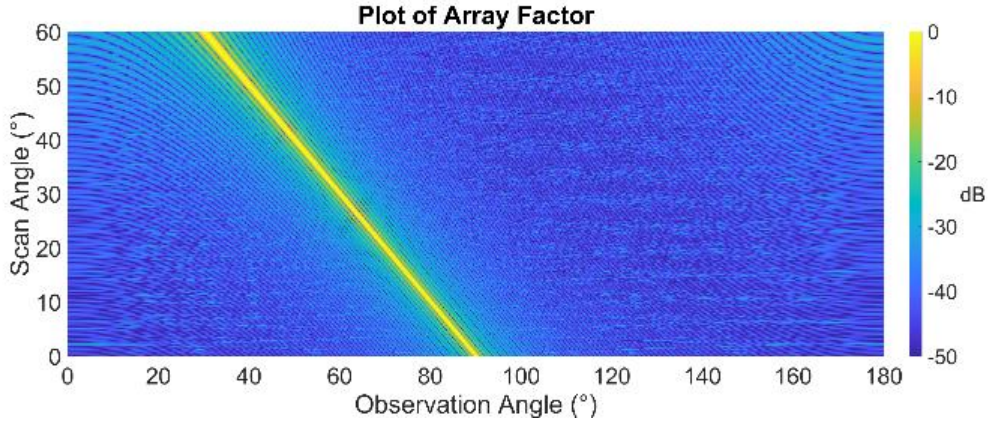


Figure 128. 128-element Linear array, with 2, 4 and 6 bit TDU control on layers 1, 2 and 3 respectively, scanned from zero to 60°.

However, Figure 129 enforces hard limits on the delay range of each TDU, based on the LSB and bit depth b (i.e., maximum delay range = $LSB \cdot \left(2^b - 1\right)$). For example, for TDU3 feeding element 44 on layer 3, at a scan angle of 60°, with 6-bit control, the maximum control word is 63, corresponding to a maximum delay of 63 × 1.227 = 77.3 ps. In this case, the ideal (perfect) delay requires a control word of 87, equating to 87 × 1.227 = 106.75 ps, which exceeds the physical range. The delay value is therefore truncated to the maximum control word of 63, introducing a time error of 30 ps and a corresponding phase error of 324° at 30 GHz. The resulting array factor shows a dramatic degradation, particularly at high scan angles, where sidelobes are significantly elevated. The next section quantifies this via the RMS phase error vs scan angle (Figure 135).

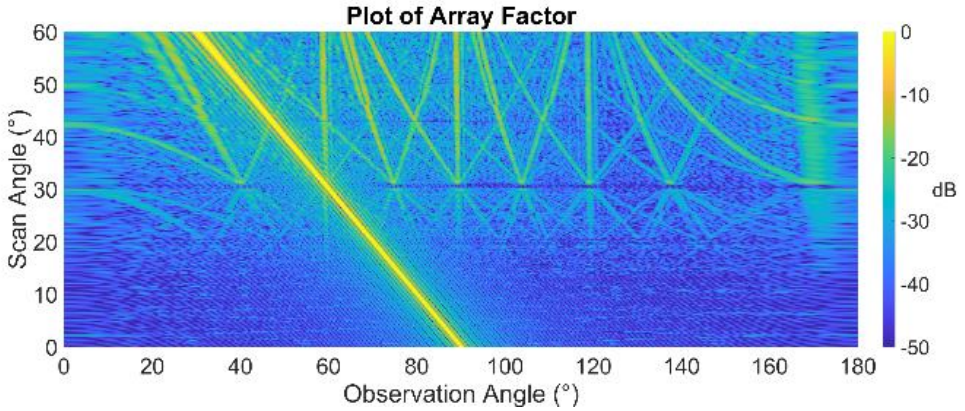


Figure 129. 128-element Linear array, with 2, 4 and 6 bit TDU control on layers 1, 2 and 3 respectively and with hard limited delay values, scanned from zero to 60°.

As a time-domain beamformer, the system's performance can also be analysed in the time domain by examining the energy pattern. Figure 130 shows the time-domain response of the 128-element linear array to a Gaussian input pulse with τ = 22 ps for both truncated and non-truncated scenarios. The truncated signal exhibits a slight timing shift of approximately 1.89 ps

and a slightly altered shape, including a reduction in amplitude. The correlation coefficient drops from 1.0 to 0.95.

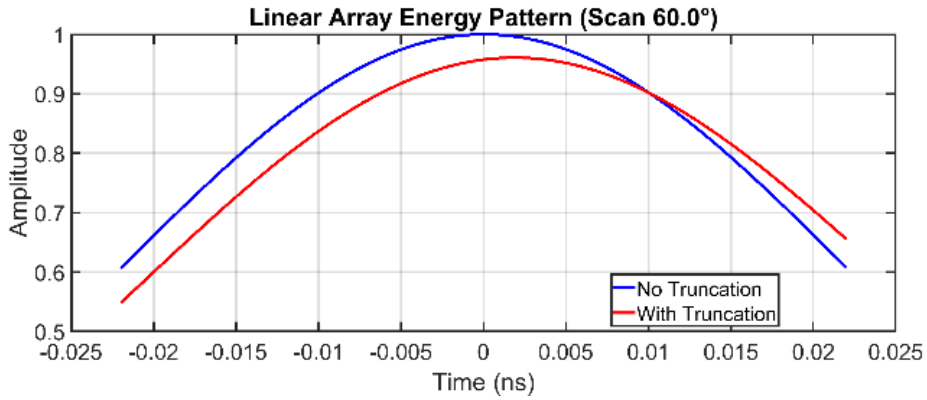


Figure 130. Time domain response of 128-element array to a Gaussian input pulse with truncation and without truncation.

The impact on sidelobe performance is highlighted in Figure 131. For a scan angle of -60°, the red trace shows the case with truncation, and the blue trace shows the same configuration without truncation. At an observation angle of 88.8°, nearly boresight for the main beam, the sidelobe level increases from –38.2 dB to –11.3 dB, a degradation of 26.9 dB caused solely by truncation.

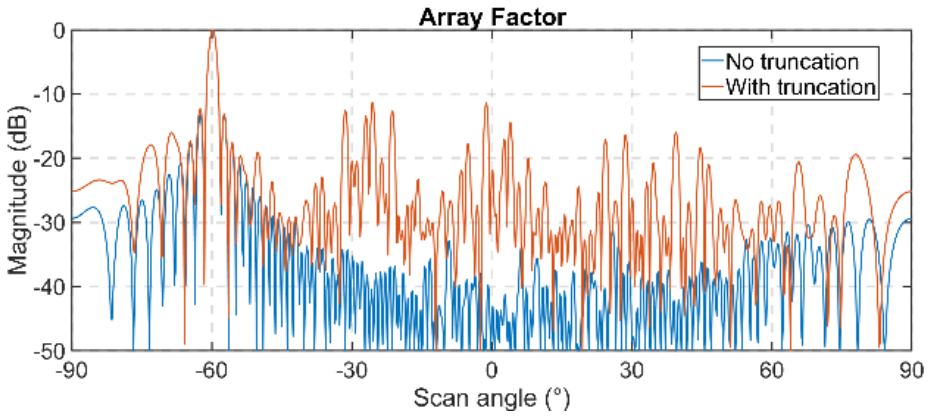


Figure 131. Array factor plot for a scan angle of 60°, blue trace with truncation and red trace with no truncation.

The cause of this effect lies in the layered subarray structure. Each TDU on layer 2 controls 4 array elements, forming 32 subarrays of 4 antennas. If adjacent TDUs on layer 2 are quantised to the same value, then up to 8 antennas at the output of layer 3 receive the same delay input. The edge-most antenna in that group may then require the capacity to accommodate an error delay value of up to a full LSB to avoid truncation.

Figure 132 tests the improvement of assuming a worst-case error of LSB from the previous layer. This prevents truncation and restores acceptable performance, though at the cost of a slight increase in RMS phase error due to the larger LSB used on layer 3. In this example, the

RMS phase error rises from 3.84° to 5.59°, a modest trade-off compared to the severe sidelobe degradation observed under truncation.

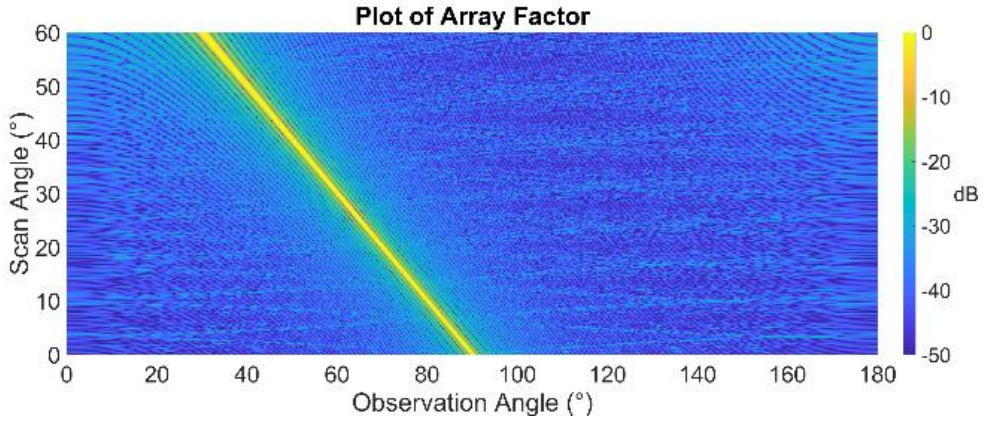
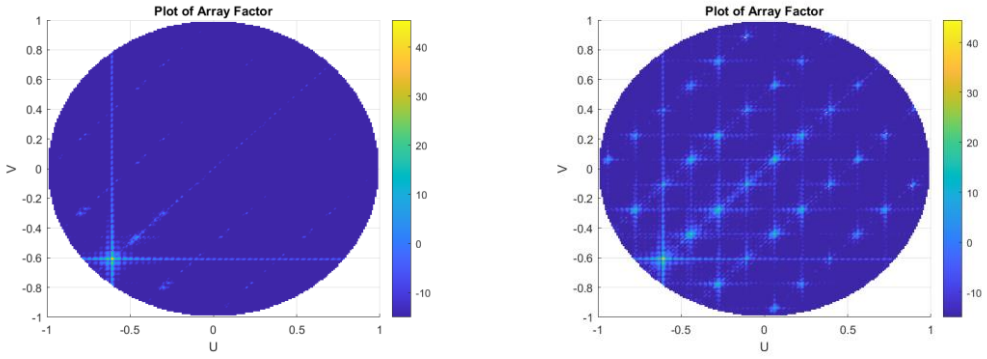


Figure 132. Performance with increased TDU values on layer 3 to include an error from layer 2 equal to LSB.

As an additional example of the importance of considering truncation effects, Figure 133(a) shows the UV plot of the array factor for a 256x256 planar array, operating at 30 GHz with half-wavelength element spacing, for a hierarchical BFN with 3 layers of TDUs at division levels 2, 6, and 8, with bit depths of 2, 5, and 6, respectively, scanned to θ=-60° and φ=-45°. No allowance for truncation has been made.

Figure 133(b) demonstrates the severe effect of truncating the delay values to their physical limits, where sidelobes increase by more than 20 dB in some regions. A potential solution to mitigate truncation effects is to increase the bit depth on layer 2 from 5 to 9, which restores performance to levels similar to those when truncation is not considered.



(a) (b)

Figure 133. UV array factor for 256 x 256 planar array with (a) no truncation and (b) with truncation.

These results demonstrate that conventional sizing practices based on LSB/2 are inadequate when resolution is low for a hierarchical BFN. The next section develops a theoretical framework for determining the minimum delay range required to avoid truncation while bounding phase error growth.

6.3. Theoretical Framework for Truncation-Aware TDU Sizing

To prevent truncation in hierarchical BFNs, each TDU must be sized not only to accommodate the ideal delay required for scan but also to absorb accumulated quantisation errors from lower layers. A scaling coefficient α is defined to represent the propagated error margin required at each layer. The LSB value for each layer can be defined as follows,

$$LSB_1 = \frac{1}{2^{b_1}-1}(\tau_1), \tag{6.1}$$

$$LSB_2 = \frac{1}{2^{b_2}-1}(\tau_2 + \alpha_1 LSB_1), \tag{6.2}$$

$$LSB_3 = \frac{1}{2^{b_3}-1}(\tau_3 + \alpha_2 LSB_2), \tag{6.3}$$

where, LSB_n and b_n denote the least significant bit size and the number of control bits respectively for layer n. The ideal time delay, τ_n, denotes the maximum scan delay required at layer n, computed by evaluating the delay profile for the subarray formed by the TDUs at that layer. It reflects the ideal (unquantised) delay needed to steer the subarray beam to the maximum scan angle of interest.

By recursive substitution, a closed-form expression can be derived for LSB_2, LSB_3 and a generic equation for n layers:

$$LSB_2 = \frac{1}{2^{b_2}-1}\left(\tau_2 + \frac{\alpha_1\tau_1}{2^{b_1}-1}\right) \tag{6.4}$$

$$LSB_3 = \frac{1}{2^{b_3}-1}\left(\tau_3 + \frac{\alpha_2}{2^{b_2}-1}\left(\tau_2 + \frac{\alpha_1\tau_1}{2^{b_1}-1}\right)\right) \tag{6.5}$$

$$LSB_n = \frac{\tau_n}{2^{b_n}-1} + \frac{\alpha_{n-1}\tau_{n-1}}{(2^{b_n}-1)(2^{b_{n-1}}-1)} + \frac{\alpha_{n-1}\alpha_{n-2}\tau_{n-2}}{(2^{b_n}-1)(2^{b_{n-1}}-1)(2^{b_{n-2}}-1)}\ldots\ldots\ldots \tag{6.6}$$

These expressions link the LSB size to the ideal scan delays, bit allocations, and error margins. As bits decrease, the value of α needs to rise above 0.5 to avoid truncation; at a low resolution, $\alpha \approx 1$ is required.

To apply this framework, designers should calculate the LSB values of each layer twice, once using $\alpha = 1$ and once using $\alpha = 0.5$, and compare the results. A large divergence signals

truncation risk. Adjustment of the bit values can then be used to achieve a convergence of values to within a margin of say 3%.

As an example of how these expressions perform, consider the design of Figure 126. A numerical model of the array was used to calculate the worst case delay range required on each layer for any scan angle. Then the model worked backwards to calculate the associated value of α, and then plotted α as a function of the number of control bits. See Figure 134 for a plot of α_2 as a function of b_2, for various values of b_3, keeping $b_1 = 2$. The graph highlights the dependency of α_2 on both b_2 and b_3. In all but one case, the value for b_2 is equal to $b_3 + 5$ in order to make $\alpha_2 = 0.5$ and avoid any truncation at any scan value.

The task of deciding between increasing b_2 or b_3 is not arbitrary as it is LSB_3 that ultimately sets the RMS phase error across the array. Hence it is the design task to ensure there are enough control bits on layer 3 to achieve the design RMS phase error and enough control bits on layer 2 to keep the propagated errors within the bounds of layer 3 TDUs.

From Figure 134 it can be seen that it is possible to avoid truncation if $b_3 = 2$ an $b_2 = 6$, however 2 control bits on layer 3 is unlikely to deliver an acceptable phase error profile. Keeping $b_3 = 6$, as per the original design, $b_2 = 11$ is necessary to achieve $\alpha_2 = 0.5$.

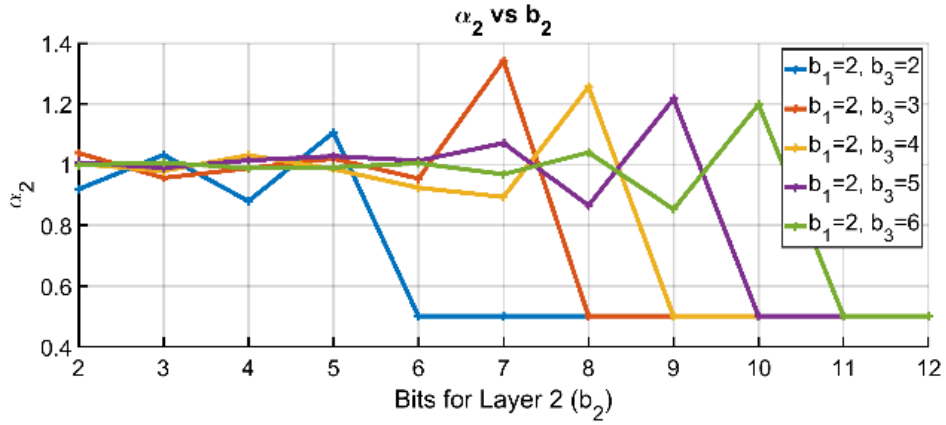


Figure 134. Plot of α_2 as a function of b_2 for various values of b_3, with $b_1 = 2$ and 3, for the 128-element array of Figure 126.

As an alternative to using a numerical model to search for the maximum delay values and then plotting alternatives as here, a simple calculation of what is required for the LSB values to converge to be less than 3% when calculated using $\alpha = 0.5$ and $\alpha = 1$ gives a good starting point for a design to avoid truncation.

It is useful to consider the RMS phase error of this example as it demonstrates the influence of the scan angle on the truncation problem. See Figure 135 for a plot of RMS phase error

versus scan angle for various values of b_2 with $b_1 = 2$ and $b_3 = 6$, as per the original design example. The plot shows that the truncation effects and phase error grow more severe as the scan angle approaches its limit. For example, with $b_2 = 7$, the RMS phase error remains flat and matches that of $b_2 = 10$ up to a 53° scan, before rising to 8° at a 60° scan demonstrating a possible compromise if moderate phase errors are tolerable at the maximum scan.

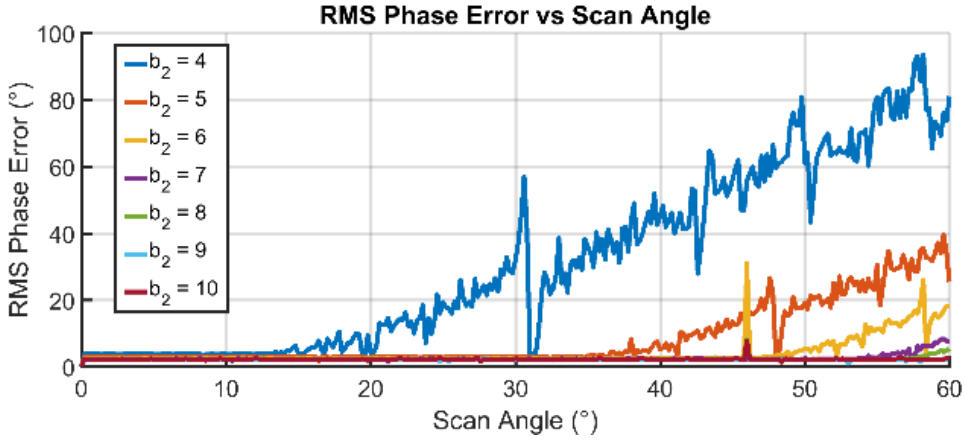


Figure 135. RMS phase error vs scan angle for the 128-element array of Figure 126 for different values of b_2 with $b_1 = 2$ and $b_3 = 6$.

An alternative design is to set $\alpha = 1$, keep the control bits as per Figure 126 and accept a slightly increased LSB_3, with the benefit of no truncation, as per Figure 132.

In summary for the example of Figure 126, the RMS phase error for different bit depths and α at a 60° scan are in Table 17, along with the maximum scan range for truncation free scanning with $\alpha = 0.5$. This clearly shows how staying with original bit depths of 2, 4, and 6 on layers 1, 2, and 3 results in truncation if scanned more than 15°. There is the option to increase α to 1 for no truncation with the current bit depth or keeping $\alpha = 0.5$ and increasing b_2 to a value of between 7 and 11.

b1, b2, b3	$\alpha_1 = 0.5$ $\alpha_2 = 0.5$	Max scan angle	$\alpha_1 = 0.5$ $\alpha_2 = 1$
10, 10, 10	0.751	60	0.135
8, 8, 8	2.30	57	0.58
6, 6, 6	12.06	34	2.88
4, 4, 4	45.10	23	21.19
2, 4, 6	81.06	15	5.59
2, 5, 6	25.44	37	3.8
2, 6, 6	12.06	47	2.88
2, 7, 6	7.73	53	2.54
2, 10, 6	2.47	60	2.24
2, 11, 6	1.99	60	2.18

Table 17. RMS phase error (°) max scan angle (°).

6.3.1. Design Implications and Recommendations

The results above demonstrate that truncation can become a dominant error source in hierarchical BFNs when lower-layer TDUs use low-resolution control. This effect must be carefully accounted for in any practical design. Because the final layer often has the smallest LSB, the quantisation error propagated from lower layers must remain within its delay range. This often requires allocating more control bits to the penultimate layer than to the top layer.

In practice, designers face a trade-off:

- increase the number of control bits in lower layers to ensure that the accumulated quantisation error remains within the LSB/2 margin for the final layer, or
- accept a smaller maximum scan angle before truncation occurs, or
- design the final layer(s) using an error margin of a full LSB (α = 1), while maintaining a low bit depth, which eliminates truncation but increases RMS phase error.

The recursive framework developed earlier allows designers to explore these trade-offs quantitatively. By computing the LSB values using (6.4) to (6.6) for both $\alpha = 1$ and $\alpha = 0.5$, the potential for truncation becomes immediately apparent and gives a mechanism to judge the effect of adjusting the number of control bits per layer. In this way, designers can ensure that upper-layer TDUs are not overrun by propagated errors. A useful design rule is to iteratively vary bit allocations until the two LSB calculations converge within a small threshold (e.g., 3%), indicating minimal truncation risk.

Simulation should be used to validate performance and confirm that the chosen architecture meets application-specific accuracy and scanning requirements.

These findings confirm that using α as a design variable enables practical trade-offs between bit resolution and phase errors while explicitly avoiding truncation. The approach can be directly applied during early stage BFN design.

6.4. Phase-Only Synthesis for Wide-Angle Beam Scanning: Probabilistic Considerations for TDU Design

Numerous metaheuristic and stochastic optimisation routines have been proposed for the synthesis of wide-angle scanning phased antenna arrays. However, each solution is unique. Running an optimisation routine multiple times will yield different results, even when the routine consistently converges. This poses a significant challenge for the practical design of TDUs, which must have the headroom to accommodate a broad range of optimised solutions.

This section examines the use of phase-only optimisation to mitigate sidelobe level (SLL) degradation in wide-angle beam scanning (WABS) arrays. Phase-only correction is attractive due to its simplicity and power efficiency compared to amplitude-phase optimisation. However, it introduces a fundamental design constraint: how much additional delay range must be incorporated into the TDU to ensure that optimised phase adjustments can be implemented across a wide scan range? This problem is approached probabilistically, determining the necessary TDU headroom in terms of standard deviations of phase deviation distributions.

This section quantifies the potential sidelobe reduction achievable with phase-only correction and determines the necessary TDU headroom for practical implementation.

6.4.1. The Challenge of Wide-Angle Beam Scanning

Increasing the scanning range of planar phased arrays is an ongoing area of research. Wide-angle scanning is often constrained by:

- Realised gain reduction at high scan angles.
- Degraded impedance matching due to mutual coupling effects and
- Scan blindness which occurs when the main beam cannot be effectively formed beyond a certain scan angle, particularly near endfire, due to the presence of a strongly coupled image beam that becomes indistinguishable from the main beam. This phenomenon sets a hard limit on the maximum achievable scan angle for a given array configuration.

The array radiation pattern is the product of the array factor and the element pattern, necessitating elements with a broad half-power beamwidth (HPBW) to support wide scanning.

6.4.2. Sidelobe Reduction Techniques

While aperture tapering with amplitude control is the most effective sidelobe reduction method, phase-only adjustment with uniform amplitude offers distinct benefits, including;

- Simplicity - fewer control points and fewer components, no need of unequal power dividers or power attenuators and,
- Power efficiency - power amplifiers are more efficient when driven hard so all PAs can operate at maximum efficiency.

These features make phase-only beamforming an attractive option for systems where size, weight, power and cost (SWaP-C) are critical factors, such as airborne radars, satellite communications and 5G base stations. While phase-only correction has limitations—such as reduced control over sidelobes compared to amplitude-phase optimisation—advancements in optimisation algorithms allow for near-optimal beamforming with minimal hardware overhead.

Phase-only synthesis introduces a trade-off between computational complexity and beamforming performance. Unlike amplitude-phase optimisation, which provides greater sidelobe suppression at the cost of increased hardware complexity, phase-only synthesis relies on numerical optimisation techniques to approximate the desired radiation pattern using constrained phase adjustments only. The complexity grows with the number of phase states and array size, making real-time adaptation challenging in resource-limited systems. However, precomputed phase distributions and lookup-table-based implementations can mitigate this issue, enabling efficient phase-only beamforming while maintaining a balance between performance and computational feasibility.

Another option for sidelobe reduction with any scanning array is the non-uniformly spaced array (NUSA) or aperiodic array, first introduced by R. F. Harrington [106] and later Ishimaru [107] developed an element spacing methodology for a Taylor equivalent performance in a NUSA, without amplitude tapering. However, aperiodic arrays do suffer from degraded SLL at wide scan angles, but optimisation techniques can be applied to improve sidelobe performance.

6.4.3. Phase-Only Synthesis for SLL Control

One of the earliest phase-only synthesis methods was proposed by DeFord [108] and later extended by Steyskal [109]. Later, Steyskal and Haupt [110] provided mathematical models for:

- Phase-only optimisation
- Combined amplitude-phase synthesis
- Null placement and subarray techniques

Recent contributions from M. Pour [111] have demonstrated that a 9-element array optimised using phase-only synthesis can achieve -30 dB SLL, showing the effectiveness of phase-only synthesis in modern array designs.

6.5. Hierarchical Beamforming Enhancements

In addition to phase-only optimisation techniques, hierarchical beamforming networks (BFNs) offer an inherent structural advantage that can be leveraged for sidelobe reduction without the need for iterative optimisation routines. Unlike pure phase-only synthesis, which requires precise control over each element's phase shift, hierarchical BFNs provide an additional degree of flexibility by controlling subarrays independently. A well-designed hierarchical BFN can achieve sidelobe level improvements of 2–4 dB, particularly at wide scan angles, through two key mechanisms: subarray beam steering adjustments and variable subarray spacing.

The first approach involves slightly modifying the scan angles assigned to each subarray, which can reduce grating lobes and distribute sidelobe energy more favourably across the angular spectrum. This technique has a negligible effect at broadside but simulations have demonstrated a 4 dB improvement in SLL at wider scan angles.

The second method of variable subarray spacing exploits the ability to slightly vary the spacing between subarrays, which introduces a structured amplitude-like tapering effect that contributes to an overall 2 dB reduction in sidelobes across the full scan range. These approaches are not optimisation-based but rather systematic design choices, making them attractive for real-world implementations where computational complexity is a concern.

While hierarchical beamforming networks are well-established in the literature, their use for passive sidelobe reduction in wide-angle scanning, without explicit optimisation, has not been widely documented. This suggests that the approach remains an underexplored yet effective method for achieving improved SLL performance in phased array systems.

6.5.1. Phase-Only Optimisation and Its Effect on SLL

A wide range of metaheuristic and evolutionary optimisation algorithms have been explored for phase-only sidelobe reduction in phased arrays. These include genetic algorithms (GA), particle swarm optimisation (PSO), differential evolution (DE) and simulated annealing

(SA), each offering different trade-offs between convergence speed, solution quality and computational complexity. Among these, PSO has gained popularity due to its ability to efficiently navigate large solution spaces while avoiding local minima. Unlike gradient-based approaches, PSO operates using a population of candidate solutions ("particles"), iteratively refining their phase values based on a balance of global and local search mechanisms. In the following results, PSO was employed to optimise the phase shifts of a 20-element linear array with half wavelength element spacing for wide-angle scanning, targeting consistent sidelobe suppression across various scan angles. The optimisation routine was run up to 1000 times, generating a statistical distribution of optimal phase solutions, which informs the required TDU design headroom for practical implementation.

Simulations of the 20-element periodic linear array show that phase-only optimisation can consistently achieve -16 dB SLL, regardless of scan angle. The first sidelobe remains stable even at scan angles as wide as 65° from boresight. Attempts to push below -17 dB SLL result in marginal improvements, but at the cost of increasing the first sidelobe level.

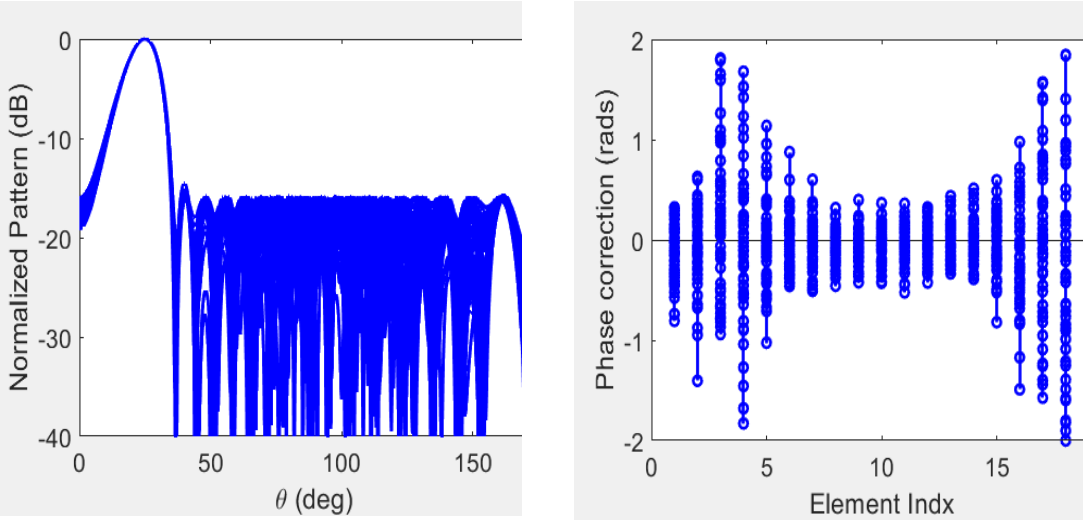


Figure 136. Plot of sidelobe levels and the phase shifter settings for the optimised solution after 200 runs.

Figure 136 is a plot of 200 optimisation solutions on top of each other and a plot of the phase shift value for each array element, above or below the perfect value for all solutions. The results demonstrate a consistent SLL better than -16 dB for all 200 optimisation solutions.

It is possible to introduce a small taper on the SLL levels, but this comes with a penalty: at 65° scans, the first sidelobe rises to -13 dB, while the SLL improves to -19 dB at the edge of the scan plot. See Figure 137.

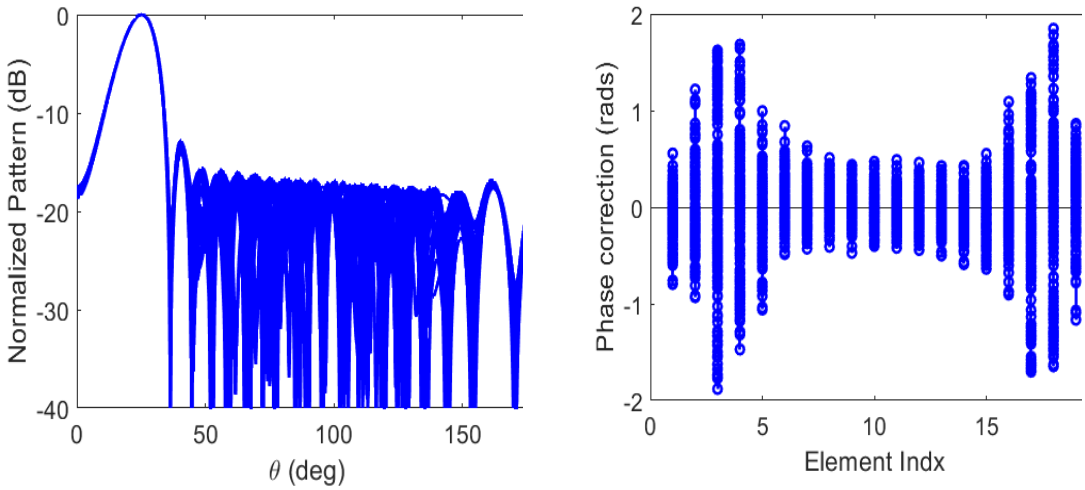


Figure 137. Plots of optimisation solutions with a slight SLL taper with the phase correction for each solution.

These exercises demonstrate that it is possible to achieve a SLL improvement of 2.8 dB by phase only adjustment for a wide angle scan, being the difference between the normal SLL of - 13.2 dB and the value here of -16 dB.

6.5.2. Statistical Distribution of Phase Deviations

A key challenge is determining the extra phase range, or headroom, required in each TDU to accommodate the spread of optimised phase shifts across multiple optimisation runs. Simulation results from 1000 optimisation runs of a 20-element linear array reveal that:

- The outermost phase shifters experience the largest deviations from the standard progressive phase shift.
- The standard deviation of required additional phase shift, in radians, for the first 10 elements (left to right) is in Table 18. The other elements 11 to 20 are the mirror image elements 1 to 10.

Element	Standard Deviation (Radians)
1	0.377
2	0.597
3	0.833
4	0.784
5	0.430
6	0.267
7	0.210
8	0.192
9	0.179
10	0.175

Table 18. Standard deviation of the required additional phase shift, in radians, for the first 10 elements.

Each value in Table 18 therefore represents the standard deviation of the additional phase shift required for a single TDU position along the array, calculated over all optimisation runs. The variation in these values across elements captures how the required headroom changes from element to element along the array.

This shows that outer phase shifters require significantly greater headroom than inner elements.

It is also the case that the performance degradation may be acceptable if only the outer 4 phase shifters at each end are used to optimise the sidelobe levels, as shown in Figure 138 where the blue trace is the solution with adjustment to all 20 phase shifters and the red trace is the performance with just 8 phase shifters optimised.

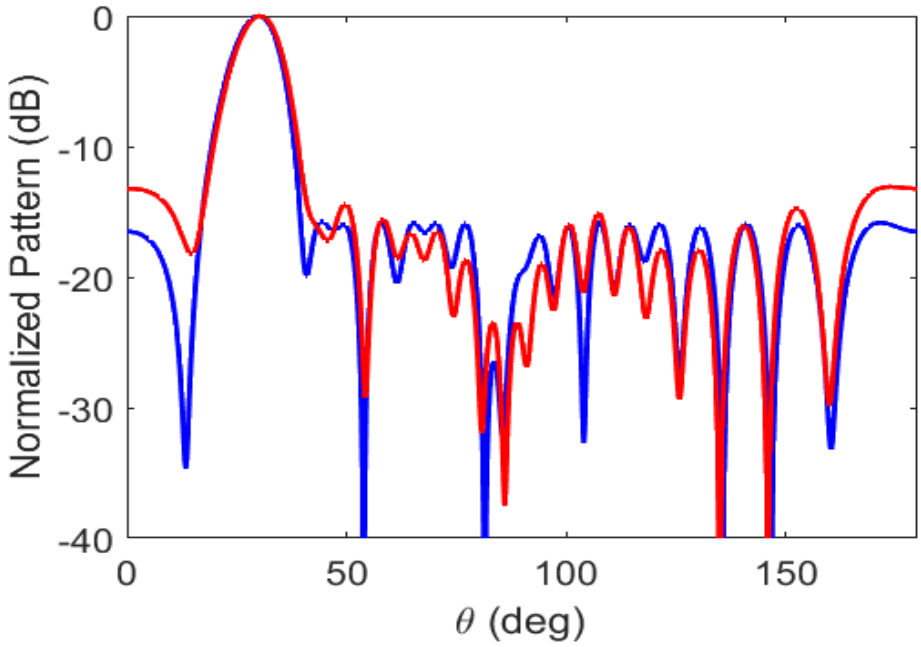


Figure 138. Comparison of the two optimised solutions, blue with 20 phase shifters adjusted and red with just the outer four phase shifters adjusted.

6.5.3. Verifying Gaussian Distribution

To determine how much additional phase capacity is required in the TDU, the data must be analysed for normality (Gaussian distribution). In this case the best-accepted method for verifying normality is the Q-Q Plot Inspection, as many of the other methods (e.g., Shapiro-Wilk Anderson-Darling) are very sensitive and reject normality if there is a slight tail deviation, even though the core distribution is normal. For practical design purposes, where 98% of the data follows normality, it's reasonable to assume a Gaussian model. See Figure 139 showing the data plotted against the ideal normal distribution, for the first 6 array elements, showing excellent agreement, except for some of the tails. Given that only circa 10 values deviate from ideal, 990 (99%) align well with ideal values.

It should be noted that this Gaussian distribution describes the variation in the extra delay required for a single TDU position over the 1000 optimisation runs, not the variation along the array. The two distributions - spatial variation across elements and statistical variation of a single element's required phase - are distinct. The latter defines the standard deviation σ used in the following design recommendations.

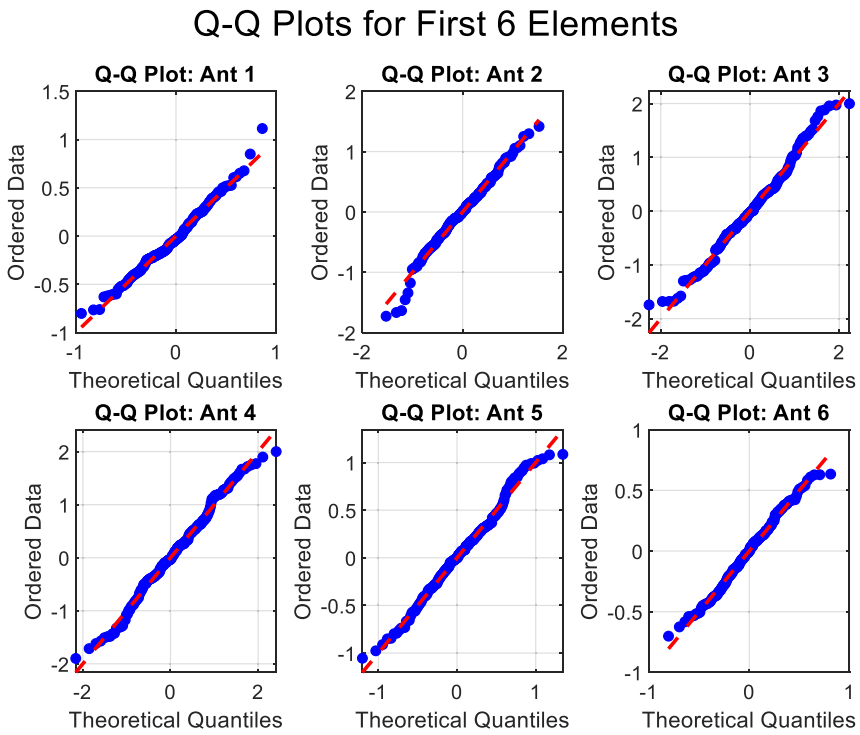


Figure 139. Q-Q plots of the first 6 array elements for the additional phase capacity that is required for the optimised solutions.

Now that normality is confirmed, the extra phase headroom can be defined in terms of standard deviations, σ:

- 1σ (68%) → Ensures sufficient TDU range for 68% of optimisation cases.
- 2σ (95%) → Covers 95% of cases.
- 3σ (99.7%) → Guarantees sufficient range in nearly all cases.

6.5.4. Practical Recommendation for TDU Design

For practical TDU design, a phase shift range of at least 2σ should be incorporated into the hardware to accommodate 95% of optimisation cases. The recommendation of 2σ coverage is a common engineering practice and a reasonable trade-off between performance, cost and manufacturability. In this case, if a design calls for a value greater than 2σ, there is always the option to run the optimisation routine again with every chance (95%) of calculating a value within the 2σ range. Any high-precision applications, such as deep-space communication or high-resolution synthetic aperture radar (SAR), may opt for a more conservative 3σ margin.

Given the observed data:

- The maximum σ at the outer elements is ≈0.8 radians.
- 2σ coverage suggests a phase headroom of ≈1.6 radians at the outer elements.

Thus, a TDU design with at least 1.6 radians of extra phase range for the outer elements is recommended for robust sidelobe control, ensuring that phase-only optimisation remains effective across the full scan range.

6.6. Conclusion

This chapter presents two distinct contributions to the field of TDU-based BFNs, each addressing key challenges quantisation effects and practical implementation strategies.

Addressing Truncation Errors Due to Quantisation Effects

This work identifies and analyses the often-overlooked issue of truncation errors in hierarchical BFN designs, where quantisation effects can lead to unexpected and severe performance degradation. Conventional methods assume that the error passed from one TDU layer to the next is limited to half the LSB of the lower layer. However, this assumption fails when quantisation errors accumulate, potentially causing delay values to exceed the available range of a TDU, leading to truncation. A theoretical framework is presented to accurately quantify and mitigate these effects by appropriately sizing TDUs. The proposed correction method ensures that the upper-layer TDUs are dimensioned to accommodate the full quantisation error, avoiding performance degradation due to truncation. The findings underscore the importance of properly accounting for these errors in practical phased array design.

Practical Considerations for TDU Sizing in Phase-Only Optimisation

A probabilistic analysis of phase-only optimisation for wide-angle beam scanning arrays has been conducted to determine the necessary TDU delay range. Phase-only synthesis methods offer advantages in power efficiency and implementation simplicity but introduce constraints in terms of required phase shift adjustments. The study demonstrates that optimised phase settings vary significantly across multiple runs of the same optimisation routine, necessitating additional delay range in TDUs to accommodate these variations. By analysing the statistical distribution of phase deviation across optimisation runs, a design rule is proposed to ensure that TDUs provide sufficient headroom for phase adjustments without excessive over-dimensioning. This practical guideline helps engineers balance sidelobe control with the physical constraints of TDUs in large-scale phased array applications.

Collectively, these contributions advance the understanding and implementation of TDU-based beamforming networks, addressing both theoretical and practical challenges. The proposed methodologies offer tangible benefits in terms of efficiency, performance and scalability, making them valuable tools for future phased array system development.

7. Conclusion

This thesis has presented a significant advancement in the use of commercially available RF MEMS switches for the realisation of switched-line true TDUs. This approach offers a practical and commercially viable solution for a wide range of phased array beamforming networks, demonstrating its adaptability and effectiveness in various applications. The work conducted here represents an essential step forward in the development of RF MEMS-based TDUs, addressing key historical challenges and demonstrating novel contributions to the field.

7.1. Framing the Contribution in MEMS TDU Development

The evolution of RF MEMS-based TDUs has been a long and challenging process. The first proposal of a RF MEMS-switched delay line was reported in 1995 [77], but it was purely theoretical and never experimentally validated. The first practical implementation by Norquist [80] introduced a 6-bit MEMS delay circuit, but with only a 15% yield, it was never viable as a commercial solution. The introduction of commercially available RF MEMS switches to the design of a TDU by Ibrahim [83] marked a turning point, yet the excessive group delay ripple of over 100 ps rendered it impractical for phased array applications. Lin [64] demonstrated an impressive 3255 ps delay, but their approach relied on custom MEMS devices with substantial insertion losses reaching 16 dB and requiring an external high-voltage source for actuation.

This thesis builds upon these developments by demonstrating a novel approach that eliminates the need for custom MEMS fabrication or external high-voltage actuation sources while maintaining very attractive performance. While Lin achieved a higher figure of merit (FOM) in terms of delay-to-loss ratio, their approach relied on custom MEMS technology, limiting accessibility. In contrast, the work presented here achieves the highest FOM reported for RF MEMS-based TDUs implemented with commercially available switches on a PCB, establishing a new benchmark in practical MEMS TDU design and contributing to the collective knowledge of the microwave community.

7.2. Technical Contributions and Findings

7.2.1. Shunt RF MEMS switches for Suppressing Half-Wave Resonance

One of the key investigations in this work was the application of shunt RF MEMS switches to terminate unused switched delay lines to suppress half-wave resonances. Although this technique ultimately yielded minimal benefit in practical measurements, the findings contribute to the broader understanding of resonance suppression mechanisms. By thoroughly examining the limitations and trade-offs, this study provides valuable insight for future researchers exploring alternative mitigation strategies. While the approach did not achieve the

expected improvements, its documentation and analysis serve as an important resource for the field.

7.2.2. Measured Performance and Future Enhancements

Further refinements in impedance matching and optimisation of transmission line structures have the potential to improve insertion loss and delay accuracy. The methodologies developed in this work lay a strong foundation for future enhancements while demonstrating the feasibility of commercially available RF MEMS switches for phased array applications.

7.3. Novel Contributions in Beamforming Network Optimisation

In addition to the fundamental contributions to RF MEMS-based TDUs, this work has introduced three novel methodologies in beamforming network optimisation, as detailed in chapters 5 and 6:

7.3.1. Varying Delay Values in TDUs for Space and Performance Optimisation:

A novel approach to optimising beamforming networks by varying TDU delay values within a single layer was proposed. This method reduces required PCB space by up to 13.3% and improves sidelobe suppression, demonstrating a 25.9 dB reduction in grating lobes. No prior work has reported this approach, making it a significant contribution to phased array design.

7.3.2. Addressing Truncation Errors Due to Quantisation Effects:

A rigorous analysis of quantisation-induced truncation errors in hierarchical beamforming networks was conducted, revealing that conventional design assumptions fail to account for cumulative quantisation effects. This study introduces a correction framework to mitigate truncation-induced performance degradation, a topic often overlooked in the literature.

7.3.3. Practical Guidelines for TDU Sizing in Phase-Only Sidelobe Minimisation:

A probabilistic analysis of phase-only synthesis for wide-angle beam scanning was performed, leading to new insights into the required TDU delay range. This study provides practical design rules that help balance sidelobe control with physical constraints, ensuring that TDUs are neither excessively over-dimensioned nor inadequately provisioned.

7.4. Future Work

The work presented in this thesis establishes a foundation for compact, wideband hierarchical beamforming networks using MEMS-based true time delay units. Several research directions can extend these findings.

First, the hierarchical architecture introduced in Chapter 5 could be expanded to include variable bit depth as an additional optimisation dimension, allowing trade-offs between

quantisation resolution, circuit complexity, and physical area. Extending the framework to arrays where the number of elements is not a power of two (for linear) or four (for planar) would generalise the applicability of the proposed method.

Second, the truncation analysis and α-scaling framework developed in Chapter 6 could be integrated into a higher-level optimisation routine that simultaneously selects the placement of TDUs and bit allocations to avoid truncation. Such an approach could employ machine learning or hybrid optimisation techniques to identify architectures that balance phase accuracy, delay range, and implementation cost.

Finally, the phase-only synthesis examined in Sections 6.4 and 6.5 could be expanded into a more comprehensive framework incorporating hybrid or partially adaptive arrays. Combining true time delay with limited phase control (JPTA) offers a path toward fine-grain, wide-scan beam steering with reduced bit depth and hardware complexity.

These extensions would further enhance the practicality and scalability of hierarchical beamforming networks for next-generation wideband array systems.

7.5. Final Remarks

This thesis has provided a comprehensive investigation into RF MEMS-based switched-line TDUs, demonstrating their viability using commercially available components while addressing key challenges in beamforming network design. The findings contribute to both theoretical advancements and practical implementation strategies, offering insights that can guide future research in the field. While there is still room for performance improvements through refined matching techniques, the work presented here establishes a strong foundation for further innovation in true time delay beamforming systems.

8. Appendix 1

Simple model to explain inherent narrow bandwidth of a linear phased array antenna.

The limitation is primarily signal dispersion. As the size or area of the array becomes larger, the time difference in the time of arrival of the signal on one end of the array compared to the arrival at the far end increases. If the time difference is so great that the received signals are in fact two different data symbols, there will be inter-symbol interference (ISI) in the combined output from the array after all the individual element signals are combined in the beam forming network. The phase shifters can adjust for a difference of 1 wavelength but no more as a phase shifter only has a range of 360 °. So the time difference between the array edges sets the minimum symbol period.

A simple formula can be constructed to model this as the data rate is the inverse of the period of the minimum time delay between the arrival of a single data symbol at the two ends of the linear array,

$$Signal\_bandwidth(N) = \left(\frac{c}{0.99(\lambda(1+\sin(\theta)Ne_p))} \right), \tag{8.1}$$

where λ is the wavelength, θ is the scan angle, N is the number of array elements in a linear array and e_p is the element pitch in wavelengths.

The factor of 0.99 is chosen such that the wanted to unwanted signal is 20 dB down.

The factor of one inside the denominator brackets accounts for a maximum of a 1 wavelength phase shift.

Plotting this function for different scan angles and increasing N will reveal the inherent narrow bandwidth of a phased array.

As an example, Figure 140 shows the plot at 3 GHz, 45° scan, and half-wavelength element spacing, illustrating the inherent bandwidth limitation of a linear phased array imposed by time-of-arrival dispersion across the array aperture and the finite range of a phase shifter. As the number of elements increases, the differential path delay between signals arriving at opposite edges of the array grows, eventually becoming comparable to the symbol period of the transmitted data. When this occurs, successive symbols overlap in time at the beamformer output, resulting in inter-symbol interference that limits the maximum achievable data rate. The example shows that at 10 elements the array supports data rates of about 350 Mbps,

falling rapidly to around 100 Mbps at 80 elements and flattening near 40 Mbps beyond 200 elements. This trend highlights that larger apertures provide improved angular resolution but inherently narrower signal bandwidths, set by the permissible delay difference between array edges at the design scan angle and the maximum available phase range of 360°.

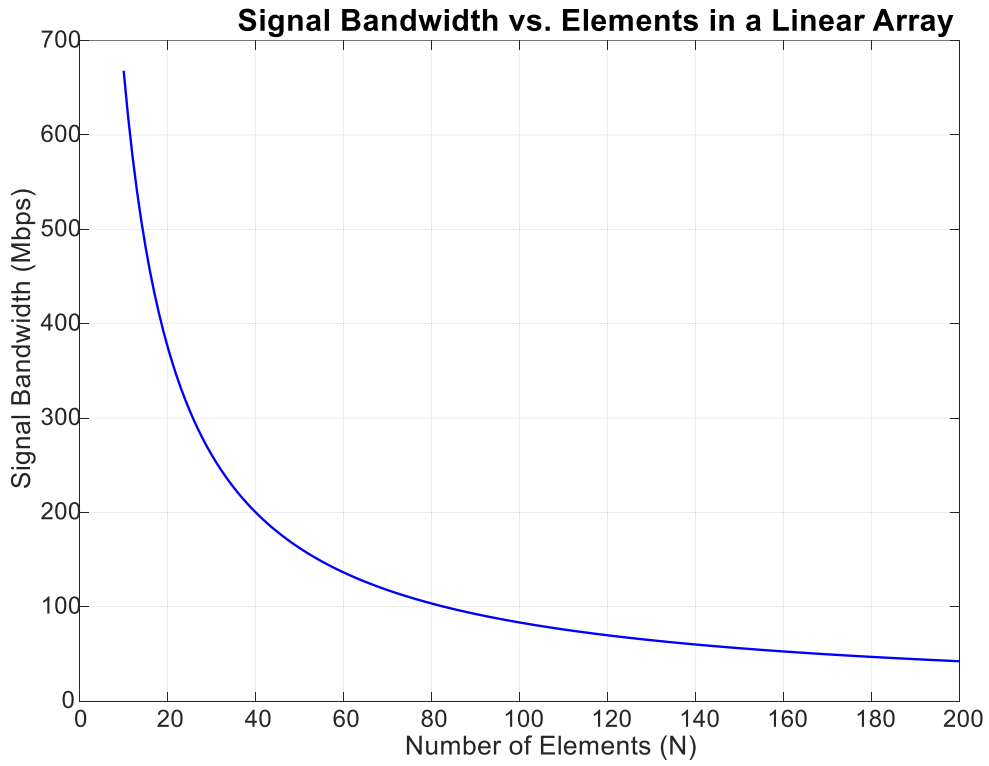


Figure 140. Plot of signal bandwidth vs the size of a linear array, at 3 GHz, 45° scan angle and half wavelength element spacing.

9. Appendix 2

Summary Table of Key Papers

Paper	Approach	Frequency Range (GHz)	Delay/Phase Control	Insertion Loss	Key Advantages	Limitations
RF MEMS-Based Dual-Frequency Phase Shifter on LCP (Bairavasubramanian et al.) [78]	First MEMS phase shifter on flexible liquid crystal polymer substrate	14	337.5° maximum phase shift	0.24 dB per bit	Monolithic MEMS integration, low insertion loss	The LCP substrate is non-trivial
A DC to 10-GHz 6-bit RF MEMS time delay circuit [C. D. Nordquist et al. (2006)] [80]	First demonstration of a six-bit RF MEMS time delay circuit	DC to 10	393.75 picoseconds, fine resolution 22.5° per bit	Max 2.5 dB, 0.42 dB per bit	Series/shunt RF MEMS switches	Alumina substrate, very low yield 15%
2.5.1.3. Ku-Band Six-Bit RF MEMS Time Delay Network [C. D. Nordquist et al. (2008)] [59]	six-bit RF MEMS time delay circuit using capacitively loaded lines for the 2 least significant bits	DC to 18	60 ps delay	Max 2.7 dB, 0.45 dB/bit	Avoids resonances by adjusting reference line length	Alumina substrate

Paper	Approach	Frequency Range (GHz)	Delay/Phase Control	Insertion Loss	Key Advantages	Limitations
2.5.1.4. Thin-film LCP amplitude compensated long time delay circuit [M. J. Chen et al. (2008)] [60]	amplitude-compensated long-time delay circuit on a multilayer liquid crystal polymer substrate	DC to 10	600 ps	3.9 dB +/-0.4 dB for all delays, 1.95 dB/bit	Consistent loss with any delay	Fabrication complexity, LCP substrate
60 GHz 2-bit Switched-Line Phase Shifter Using SP4T RF MEMS switches (Gong et al.) [81]	SP4T RF MEMS switches integrated in coplanar waveguide layout	55-65	90°, 180°, 270° phase shifts	-2.5 dB	Low insertion loss, high phase accuracy	High actuation voltage and quartz substrate
X-band 5-bit Switched-Line Phase Shifter Using RF MEMS Multi throw Switches (Du et al.) [82]	First integration of packaged RF MEMS multi throw switches in a switched-line phase shifter	8 - 12	348°maximum phase shift	-3.1 dB (average)	First packaged MEMS in switched-line phase shifter on PCB	Bonding-wire parasitics introduce additional loss
Wideband Switched Delay Line Using RF MEMS switches (Ibrahim et al.) [83]	RF MEMS switches integrated into coplanar waveguide delay lines	0 - 5	7 ps resolution delay tuning, 49 ps total delay	< -1 dB	Fine delay tuning, wideband operation	Excessive group delay ripple

Paper	Approach	Frequency Range (GHz)	Delay/Phase Control	Insertion Loss	Key Advantages	Limitations
Wideband RF MEMS switched Delay Lines with High Phase Linearity (Ibrahim et al.) [87]	Comparison of microstrip, CPW and FGCPW delay lines for high phase linearity	0 - 5	600 ps maximum delay with 10 ps and 50 ps tuning steps	0.75 dB	High phase linearity, minimal delay deviation	Only simulation results, no measured results.
4-bit Switched-Line Phase Shifter Based on RF MEMS switches (Huang et al.) [84]	Metal-contact RF MEMS switches in a microstrip-based 4-bit phase shifter	1.7-2.7	75° maximum phase shift	0.89 dB maximum	High phase accuracy, low insertion loss	Requires 90 V actuation, slight increase in size
Avoidance of Off-Switch Resonance in True Time Delay Line (Yoon & Nam) [86]	Cascaded SPDT switch true time delay for resonance suppression	1 - 7	270 ps maximum delay	Not explicitly stated, but lower than conventional designs	Removes unwanted resonance, improves group delay	Increased circuit complexity due to additional switches
5-bit RF MEMS switch Time Delay Line Shifter (Lin et al.) [64]	RF MEMS cantilever switches in a multilayer PCB time delay network	6 - 12	3255 ps maximum delay	-8 to -16 dB	Long delay values, high phase accuracy	High insertion loss due to large number of RF MEMS switches

Paper	Approach	Frequency Range (GHz)	Delay/Phase Control	Insertion Loss	Key Advantages	Limitations
7-Bit Multilayer True-Time Delay up to 1016 ps for Wideband Phased Array Antenna (Yoon & Nam) [70]	Multilayer PCB true time delay unit with optimised via structures	1 - 7	1016 ps maximum delay	< 3 dB across all delay states	Compact stacked PCB design, consistent impedance matching	Fabrication complexity due to multilayer PCB alignment

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