The Development and Applications of a Dual-Band, 8x8 MIMO Testbed with Digital IF and DDFS

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ABSTRACT

This paper describes the development of a very flexible multi-antenna testbed built on 5 PCBs. The FOM testbed (FOM, Flyable OFDM MIMO) was built with off-the-shelf components and can be configured with any number of antennas at the transmitter and receiver with a maximum of eight antennas on each side. The FOM testbed is dual-band with the two carrier frequencies at 2.44GHz and 5.245GHz and a bandwidth of 25MHz. It implements a digital IF scheme to mitigate I/Q mismatch and a DDFS for fast channel hopping. Such a flexible testbed becomes essential for evaluating various communication schemes for broadband applications. Theoretical studies and simulation can be validated on this testbed in a real-world environment with a real wireless channel and hardware impairments. A powerful GUI was developed for the operation of the FOM testbed. The architecture of the FOM testbed and the details of the circuits implemented on the individual PCBs are presented. The calibration process of the FOM testbed is discussed. Finally, possible applications such as MIMO transmissions or cognitive radio are discussed.

I. INTRODUCTION

The increasing need for higher data-rates in wireless communication applications drives the development of more complex systems. Wireless applications such as video conferencing, multimedia networks or browsing the internet are typical high data-rate applications. The development of such high data-rate and reliable wireless links is a challenging proposition to the wireless communication community. New system architectures and system theories are developed and tested in order to provide the higher data rates. The testing often ends with a simulation based on models i.e. wireless channel models. But for today's complex wireless communication systems, the validation with a simulation is often not effectual. The validation needs to be done in a real-world environment as in a testbed. Only a testbed shows all the effects of an actual implementation. Building a testbed is an intermediate step before committing algorithms to silicon. It is costly in a time and money sense but if it is built flexible enough, it can be used for many different wireless communication applications.

This FOM testbed is the 4th generation of wireless tetsbeds developed at UCLA [1]. It is a highly configurable, multi-antenna research testbed built with off-the-shelf components. The dual-band FOM testbed is built on 5 PCBs (Printed Circuit Boards). The PCBs are designed to fit into a 6u, CPCI (Compact PCI) chassis (Figure 1). This small form factor allows to easily deploy the FOM testbed in the field or even airborne (flyable). The chassis holds the PCBs for the FOM testbed and a CPU board to run the operating system. The antennas, mounted on top of the chassis, are movable in 2 dimensions. The power supply for the FOM testbed is a single 12V source (car battery) which is well suited for field measurements. The FOM testbed has an interface to a realtime and non-realtime platform. In the realtime case, the modulation and demodulation are performed in realtime on an FPGA/DSP platform. In the non-realtime case, the modulation and demodulation are performed offline on a PC. Implementing the realtime FPGA/DSP platform is conducted at a startup company. The FOM testbed was designed for MIMO-OFDM (Multiple Input Multiple Output Orthogonal Frequency Division Multiplexing) applications [2][3] but any other modulation scheme can be used as long as it conforms to the hardware specification. With an implemented DDFS (Direct Digital Frequency Synthesis), the channel at RF frequency can be changed at a speed in sub-microseconds. The implemented digital IF (intermediate Frequency) scheme helps to mitigate I/Q mismatch [4]. Any combination of transmitters and receivers can be used to operate in SISO (Single Input Single Output) mode, MIMO (Multiple Input Multiple Output) mode, SIMO (Single Input Multiple Output) mode for diversity combining or MISO (Multiple Input Single Output) mode for beamforming at the transmitter. Even smart systems such as cognitive radios [5] can be implemented on the FOM testbed. This gives the researcher the unique ability to test and evaluate numerous different communication system on a single testbed; the FOM testbed. In the following, the FOM system architecture and the frequency plan are presented. The implemented baseband and RF front-end hardware are discussed with detailed information. Also the calibration process and special features such as the digital IF and the DDFS are explained.

The remainder of the paper is organized as follows. Section II shows the specification, the frequency plan and the high level architecture of the FOM testbed. In section III, the PCBs of the FOM testbed are discussed. Section IV explains the

calibration process. In section V, some possible applications of the FOM testbed are presented. The paper concludes in section VI.

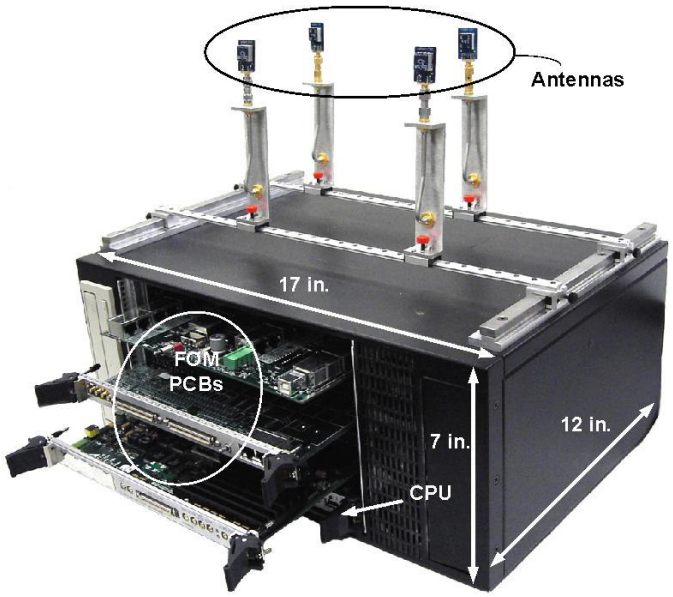

Figure 1 FOM testbed in CPCI chassis

II. SYSTEM OVERVIEW

The first step in developing the FOM testbed is to specify its parameters. Based on these specifications, the frequency plan is designed. The frequency plan shows how the up-conversion and down-conversion in the transmitter and receiver RF front-end respectively is done in the frequency domain. Then, the high-level architecture of the FOM testbed can be devised. These 3 steps are presented in the following.

A. *Specification*

The specifications are listed in Table 1.

Table 1 FOM testbed specification

Radio Architecture	Heterodyne with digital IF
System Setup	Anything from 1x1 to 8x8
Carrier Frequency	2.44GHz and 5.245GHz
RF Front-End Bandwidth	2.44GHz band: 80MHz 5.245GHz band: 195MHz
Signal Bandwidth	25MHz
Band Re-Tuning Time	< 100ns (DDFS)
Indoor Coverage Range	1m to 30m
Outdoor Coverage Range	1m to 50m
TCXO Temperature Stability	< 1ppm
Local Oscillator Phase Noise	-100dBc @ 100kHz frequency offset
Form Factor	Compact PCI (CPCI)

B. *Frequency Plan*

The frequency plan is a crucial and important step in any RF design [6]. The two carrier frequencies are given by the specifications (Table 1). The 2.44GHz carrier frequency lies in the ISM-2 band (Industrial, Scientific and Medical). The ISM-2 band covers a frequency range from 2,400MHz to 2,483.5MHz. The FOM testbed is using this band from 2,400MHz to 2,480MHz; a range of 80MHz bandwidth. The 5.245GHz carrier frequency lies almost in the center between the UNI-I and UNI-II band (Unlicensed National Information Infrastructure Band). The UNI-I band covers a frequency range from 5,150MHz to 5,250MHz and the UNI-II band from 5,250MHz to 5,350MHz. The FOM testbed is using this combined band from 5,150MHz to 5,345MHz; a range of 195MHz bandwidth. The choice of the IF frequency is mainly driven by the availability of off-the-shelf components [6]. Besides gain stages, mixers and other RF blocks, most important is to find commercially available band-pass filters for the desired IF frequency and the given bandwidth. For the FOM tetsbed, a band-pass filter designed for the Korean PCS band was chosen. Choosing the Korean PCS band as the IF for the FOM testbed brings the additional advantage of minimizing interference at IF since the FOM testbed will be deployed in the United States and the PCS band in the United States is located at higher frequencies. The digital IF (DIF) frequency was chosen based on available D/A and A/D converter speeds at the transmitter and receiver side respectively. The frequency plan of the FOM transceiver is depicted in Figure 2. The LO4 signal is twice the frequency of the LO1 signal and thus can be easily generated with a frequency doubler circuit.

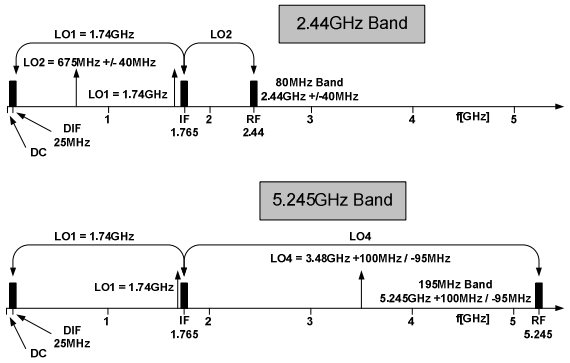

Figure 2 FOM frequency plan

Both bands are implemented with a 2-step up- and down-conversion process. At the transmitter side, starting at the digital IF frequency of 25MHz, the signals get up-converted to the IF frequency of 1.765GHz. Then, a second up-conversion step transforms the signal to the carrier frequency of 2.44GHz or 5.245GHz. The IF is intentionally chosen to be the same in both bands. This eases the search for components and reduces the overall complexity of the design. The frequency of the LO signal (Local Oscillator) for the first up-conversion step is 1.74GHz (LO1). Adding the 1.74GHz LO frequency to the digital IF frequency of 25MHz results in the IF frequency of 1.765 GHz. The LO2 signal for the second up-conversion step in the 2.44GHz band has a frequency of 675MHz ±40MHz. This LO2 signal is generated with the help of a DDFS, which allows to sweep across the available band of 80MHz. The LO4 signal for the second up-conversion step in the 5.245GHz band has a frequency of 3.48GHz (+100MHz/–95MHz). This LO4 signal is also generated with the help of a DDFS in order to sweep across the available band of 195MHz. The inverse process is implemented at the receiver side. IF and DIF frequencies are matched on the transmitter and receiver. This eases the design and also allows calibration of the FOM testbed at different frequencies as discussed in section IV.

C. High Level Architecture

The high level architecture of the FOM testbed is shown in Figure 3 with the transmitter on the left and the receiver on the right side. The FOM testbed consists of 5 PCBs: on the transmitter side the Tx_DIF (Transmitter Digital IF) and Tx_RF (Transmitter Radio Frequency) PCBs, on the receiver side the Rx_RF and Rx_DIF PCBs and the CIP (Control, I^2C, Programming) PCB.

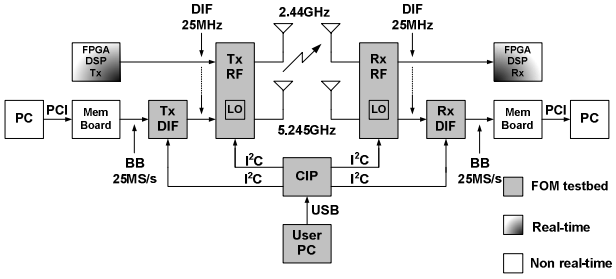

Figure 3 FOM high level architecture

Starting at the transmitter side, the baseband signal feeding the Transmitter RF can be supplied from two sources. One is the FPGA/DSP Tx platform, the other is the chain consisting of a PC, a Memory Board and the Tx_DIF PCB. The FPGA/DSP platform executes the needed baseband processing in realtime at the transmitter and receiver side. It generates and modulates the data to be transmitted over the air and digitally up-converts the data stream to the digital IF frequency of 25MHz. After a D/A conversion, the analog signal is forwarded to the Tx_RF PCB. This powerful FPGA/DSP platform enables realtime operation with the FOM testbed. In the non-realtime case, the data to be sent over the air is generated offline on a PC. The PC then sends the generated and modulated samples to a commercially available PCI based Memory Board. The Memory Board forwards the samples realtime at a speed of 25MS/s to the Tx_DIF PCB. The Tx_DIF PCB digitally up-converts the samples to the digital IF frequency of 25MHz and D/A converts them into an analog signal. The analog signal connects to the Tx_RF PCB. The Tx_RF PCB basically implements the frequency plan shown in Figure 2. It takes in the analog signal at a digital IF frequency of 25MHz and up-converts it in a first step to the IF of 1.765GHz. It then splits the signal at IF and up-converts the signal in a second step either to the carrier frequency of 2.44GHz or 5.245GHz, depending on which band the user chooses to use. Also implemented on the Tx_RF PCB is the generation of the LO (Local Oscillator) signals for the up-conversion.

At the receiver side, the inverse process is implemented. The Rx_RF PCB down-converts the received signal from the antennas (2.44GHz or 5.245GHz band) to an IF frequency of 1.765GHz. In a second down-conversion step, the signal is transformed to the digital IF frequency of 25MHz. Also implemented on the Rx_RF PCB is the generation of the LO signals for the down-conversion. In the realtime case, the digital IF signal is passed onto the FPGA/DSP Rx platform which first samples the signal at a speed of 100MS/s. It then digitally down-converts it to baseband and demodulates the signal. In the non-realtime case, the signal connects to the Rx_DIF PCB which digitizes it at a sampling rate of 100MS/s. The samples are then digitally down-converted and forwarded in realtime to the Memory Board at a rate of 25MS/s. The Memory Board passes the samples on to the PC which does the offline demodulation of the received signal. The non-realtime setup with the Memory Boards allows for 140ms of realtime transmission over the air.

The last block in Figure 3 is the CIP PCB. The CIP PCB is the heart of the FOM testbed. It implements the communication from the User PC to all the PCBs and back through an USB and I^2C bus (Inter Integrated Circuit). It also distributes the clock and controlling information to all the PCBs. In addition, it programs the FPGAs (Field Programmable Gate Array) on all the PCBs which are used for controlling purposes.

The five gray shaded blocks in Figure 3 are each implemented on a CPCI (Compact PCI) sized PCB with off-the-shelf components. Each PCB implements two transmitter or receiver data streams. For each transmitter or receiver chain there is a 2.44GHz band and 5.245GHz band implemented. The CIP PCB is designed to control up to an 8 transmitter and 8 receiver architecture. Table 2 shows how many PCBs are needed for some common setups. In the largest setup, a total of 17PCBs are in the FOM testbed. The operation of such a complex system calls for a very powerful GUI (Graphical User Interface) which helps to control the testbed. A very flexible GUI has been implemented based on C++.

Table 2 FOM setups (number of PCBs)

Setup	Tx_DIF	Tx_RF	Rx_DIF	Rx_RF	CIP
1x1	1	1	1	1	1
1x2	1	1	1	1	1
2x2	1	1	1	1	1
4x4	2	2	2	2	1
8x8	4	4	4	4	1

III. FOM PCBs

This section describes in more details the 5 PCBs.

A. Tx_DIF PCB

The Tx_DIF PCB is the interface PCB between the baseband, digital signals from the Memory Board and the analog, digital IF signals to the Tx_RF PCB (Figure 3).

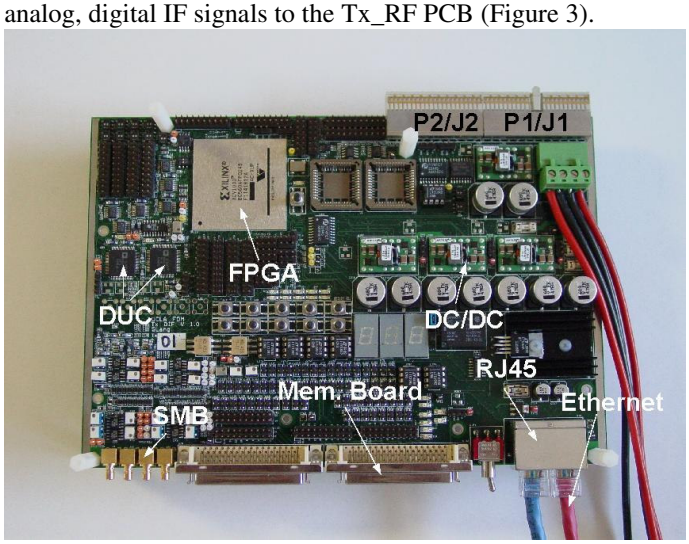

Figure 4 Photo of the Tx_DIF PCB

The basic functionality is to transform the digital input data samples from the Memory Board to an analog output signal at a

digital IF frequency of 25MHz. The Tx_DIF PCB implements the needed functionality for two transmitter data streams. In total, 1549 individual components are implemented on the 8 layer Tx_DIF PCB (Figure 4). A more detailed block diagram of the Tx_DIF architecture (one data stream) is depicted in Figure 5.

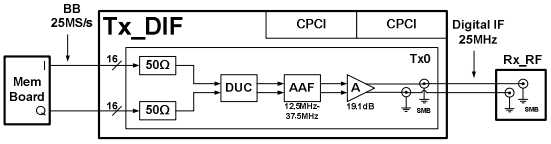

Figure 5 Tx_DIF architecture

The two 16bit I/Q data streams from the Memory Board are terminated in the 50Ω block. The digital up-converter (DUC) digitally up-converts the data stream to the digital IF frequency of 25MHz. The DUC block also includes the D/A converter. Following the DUC block is the anti-aliasing filter (AAF) to remove the frequency replicas from the D/A conversion and a gain stage A.

B. Tx_RF PCB

The Tx_RF PCB is the interface PCB between the analog signal at the digital IF frequency of 25MHz from the Tx_DIF PCB and the antennas (Figure 3). The basic functionality is to up-convert the analog input signal to the carrier frequencies of 2.44GHz and 5.245GHz. The Tx_RF PCB implements the needed functionality for two transmitter data streams. In total, 2118 individual components are implemented on the 10 layer Tx_RF PCB. The high level architecture of the Tx_RF PCB (one data stream) is depicted in Figure 6:

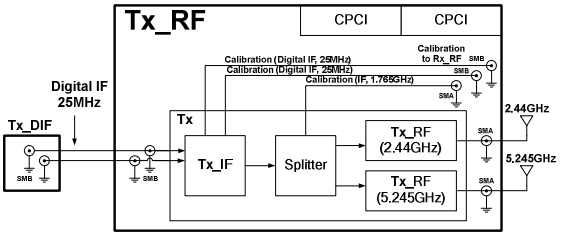

Figure 6 Tx_RF high level architecture

The Tx_IF block implements the up-conversion from the digital IF frequency of 25MHz to the IF frequency of 1.765GHz. The following splitter splits the signals to the two RF blocks which implement the final up-conversion to the carrier frequency of 2.44GHz and 5.245GHz. The Tx_IF and Tx_RF blocks are discussed in more details next.

In Figure 7, the Tx_IF block is shown in more details. The digital IF signals are amplified and filtered before connected to the Mixer M which up-converts the signal to the IF frequency of 1.765GHz. The Mixer M is driven by the LO1 signal. The output of the mixer is filtered with a SAW filter (Surface Acoustic Wave) and amplified before passed on to the splitter block. For calibration, the digital IF signal is taped out in front of the Mixer M and provided to the Rx_RF PCB.

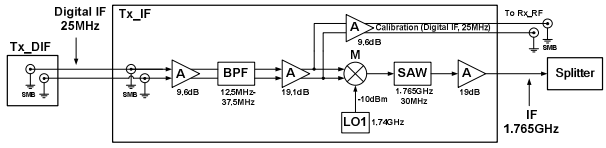

Figure 7 Tx_IF block diagram

The detailed block diagram of the Tx_RF blocks is shown in Figure 8. The top part of the figure shows the 2.44GHz and the bottom part the 5.245GHz block. The two RF chains are very similar. The switch at the input and output of the Tx_RF block facilitates to enable or disable the RF chain. The IF input signal from the splitter is amplified, filtered and then connected to the Mixer M1/M2. The Mixer M1/M2 up-converts the IF signal to the RF frequency of 2.44GHz and 5.245GHz respectively. The Mixer M1/M2 are driven by the LO2 and LO4 signals respectively. The signal at the output of the mixer is then again amplified and filtered. The power amplifier (PA) is driving the antenna. With the help of the variable attenuator, the transmit power can be set over a 31dB range in ½ dB steps. The antenna is connected to the Rx_RF PCB which implements the Tx/Rx switch. With this setup, a Tx_RF PCB and a Rx_RF PCB can be combined to a 2x2 transceiver. The power detector (PD) measures the power at the output of the Tx_RF PCB and reports it to the user via the I^2C bus. This helps to monitor the transmitted signal power.

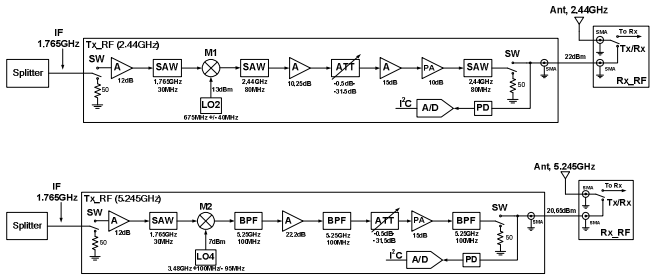

Figure 8 Tx_RF block diagram (2.44GHz and 5.245GHz)

The last block implemented on the Tx_RF PCB is the generation of the local oscillator signals. A block diagram is depicted in Figure 9. The DDFS generates digital sine- and cosine waveforms and the D/A converter converts it to the analog signal I and Q with a frequency ω_{DDFS} and an amplitude A. The following anti aliasing filter (AAF) removes replicas from the D/A conversion in the DDFS block. The I/Q signals are then forwarded to the I/Q modulator which modulates the I/Q signals with the local oscillator signals LO2'($\omega_{LO2'}$) and LO4'($\omega_{LO4'}$). The local oscillator LO2' and LO4' are fixed LO signals at a frequency of 675MH and 3.48GHz respectively. After I/Q modulation, the variable local oscillator signals LO2 and LO4 are available at the output.

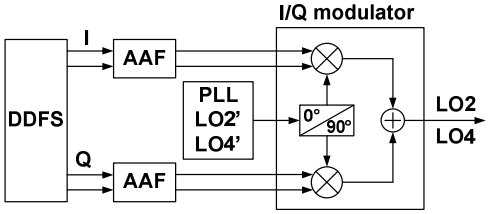

Figure 9 LO generation

The I/Q signals from the DDFS can be applied to the I/Q modulator in two different ways:

1) $I = A \cdot \cos(\omega_{DDFS} \cdot t) \qquad Q = A \cdot \sin(\omega_{DDFS} \cdot t)$

$LO2/LO4 = I \cdot \cos(\omega_{LO2'/LO4'} \cdot t) + Q \cdot \sin(\omega_{LO2'/LO4'} \cdot t)$

$LO2/LO4 = A \cdot \cos((\omega_{LO2'/LO4'} - \omega_{DDFS}) \cdot t) \qquad LSB$

2) $I = A \cdot \sin(\omega_{DDFS} \cdot t) \qquad Q = A \cdot \cos(\omega_{DDFS} \cdot t)$

$LO2/LO4 = I \cdot \cos(\omega_{LO2'/LO4'} \cdot t) + Q \cdot \sin(\omega_{LO2'/LO4'} \cdot t)$

$LO2/LO4 = A \cdot \sin((\omega_{LO2'/LO4'} + \omega_{DDFS}) \cdot t) \qquad USB$

Depending on how the I/Q signals are applied to the I/Q modulator, the Lower Side Band (LSB) or Upper Side Band (USB) frequencies are generated. Thus, the LO signal can be tuned over a bandwidth of twice the frequency ω_{DDFS} of the I/Q signals.

C. Rx_RF PCB

The Rx_RF PCB is the interface PCB between the analog signal received by the antenna at the RF frequency and the Rx_DIF PCB at the digital IF frequency of 25MHz (Figure 3). The basic functionality is to down-convert the analog input signal to the digital IF frequency of 25MHz. The Rx_RF PCB implements the needed functionality for two receiver data streams. In total, 2475 individual components are implemented on the Rx_RF PCB. The high level architecture of the Rx_RF PCB (one data stream) is depicted in Figure 10:

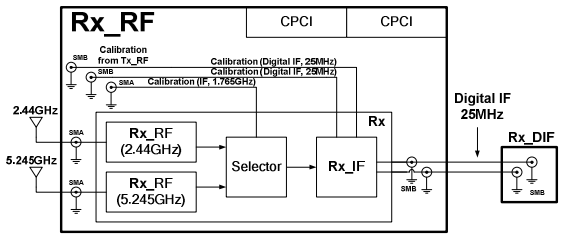

Figure 10 Rx_RF high level architecture

The Rx_RF block implements the down-conversion from the RF frequency to the IF frequency of 1.765GHz. The following selector selects the signal from one of the two Rx_RF chains and forwards it to the Rx_IF block for the final down-conversion to the digital IF frequency of 25MHz. The Rx_RF and Rx_IF blocks are discussed in more details next.

The detailed block diagram of the Rx_RF blocks are shown in Figure 11. The top part of the figure shows the 2.44GHz and the bottom part the 5.245GHz block. The two RF chains are very similar. The RF input signal from the antenna is amplified and filtered and then connected to the Mixer M3/M4. The Mixer M3/M4 down-convert the RF signal to the IF frequency of 1.765GHz. The Mixers M3/M4 are driven by the LO2 and LO4 signals respectively. The signal at the output of the mixer is then again amplified and filtered and passed onto the selector. The received signal strength indicator (RSSI) monitors the received signal power and controls the gain of the LNA block. In case of a high input power, the LNA block can be shorted and a possible damage to the LNA block can be prevented.

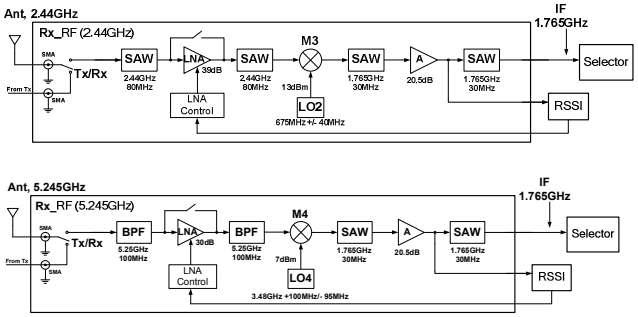

Figure 11 Rx_RF block diagram (2.44GHz and 5.245GHz)

In Figure 12, the Rx_IF block is shown in more details. The IF signals are amplified and filtered before connected to a power splitter. The power splitter splits the IF signal in one signal for noise figure measurement and the actual signal of interest. The Mixer M5 does the down-conversion to the digital IF of 25MHz. The Mixer M5 is driven by the LO1 signal. The output of the mixer is filtered and amplified before passed on to the Rx_DIF PCB. The two VGAs (Variable Gain Amplifiers), the A/D and D/A converters and the FPGA implement an AGC (Automatic Gain Control) loop to compensate for the path loss between the transmitter and receiver. The selector after the mixer M5 can, besides the data signal, select the calibration signal from the Tx_DIF PCB as the input signal. The LO generation is implemented similarly as on the Tx_RF PCB. For the 2.44GHz/5.245GHz receiver, the achieved noise figure is 5.8dB/5.1dB, the IIP3 is -11dBm/-14.7dBm and the sensitivity is -84.3dBm/-85dBm.

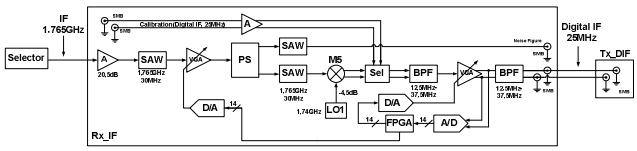

Figure 12 Rx_IF block diagram

D. Rx_DIF PCB

The Rx_DIF PCB is the interface PCB between the digital IF analog signal from the Rx_RF PCB and the baseband, digital signals to the Memory Boards (Figure 3). The basic functionality is to sample the analog input signal at the digital IF frequency of 25MHz, to digitally down-convert the signal and to forward the data to the Memory Board. The Rx_DIF PCB implements the needed functionality for two receiver data streams. In total, 1515 individual components are implemented on the Rx_DIF PCB. A more detailed block diagram of the Rx_DIF PCB (one data stream) is depicted in Figure 13:

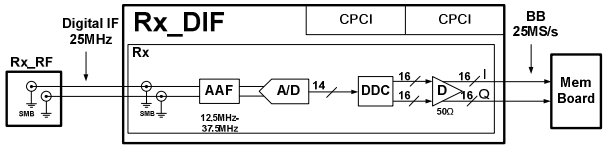

Figure 13 Rx_DIF architecture

The input signal from the Rx_RF PCB is first filtered and then A/D converted at a speed of 100MS/s. The following digital down converter (DDC) down-converts the signal to baseband and forwards it through a driver D to the Memory board.

E. CIP PCB

The CIP PCB interfaces on one side with the user via a USB connection to the GUI and on the other side to the FOM testbed. The CIP PCB distributes all the signals such as the clock signal based on a TCXO (Temperature Compensated Crystal Oscillator), the I^2C bus, FPGA programming signals, trigger etc. to all the PCBs in the FOM testbed (Figure 3). The interface to each PCB from the CIP PCB are two Ethernet Cat5e cables with a total of 16 wires. The Ethernet cables connect via an RJ45 duo connector. The controlling on the CIP PCB is implemented with an USB microcontroller. The CIP PCB is able to support a maximum of an 8 transmitter and 8 receiver setup. In total, 1349 individual components are implemented on the 8 layer CIP PCB. A photo of the CIP PCB is shown in Figure 14:

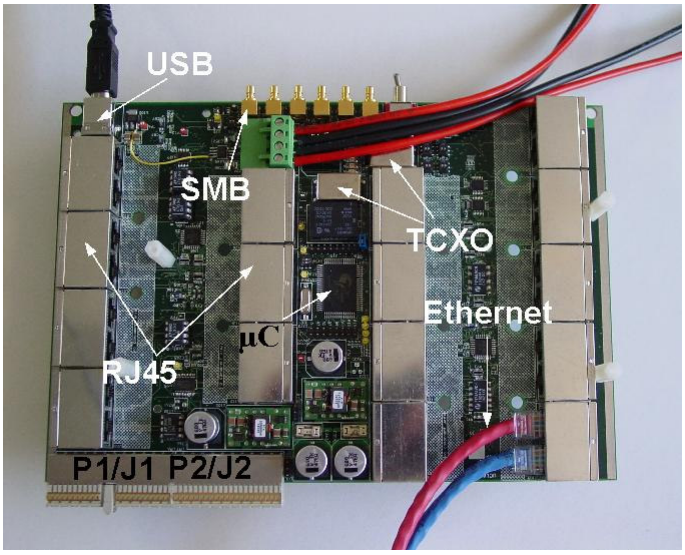

Figure 14 Photo of the CIP PCB

IV. CALIBRATION AND WIRELESS MEASUREMENT

After building the FOM testbed, it must be calibrated before deploying it in the field. The calibration gives a baseline of the performance of the testbed in comparison with theory. If there is a disagreement between measurement and theory, which can not be explained as artifacts from a real hardware setup, solutions in hard- and software need to be developed and implemented. A possible calibration metric is to measure the symbol error rates vs. input signal to noise ratio and compare it with theory. The FOM testbed has several calibration links as shown in Figure 15. This facilitates to calibrate the FOM testbed in a stepwise manner, starting at baseband and progressing towards RF.

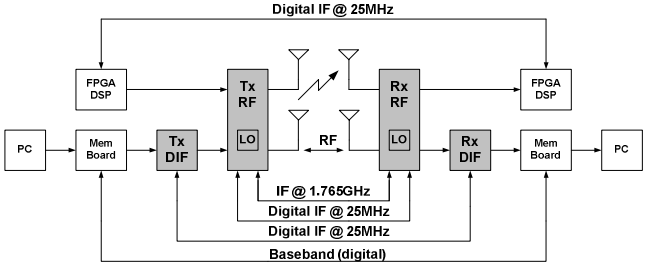

Figure 15 FOM calibration links

V. APPLICATIONS

There are many applications which can be implemented and tested on the multi-antenna FOM testbed. Besides MIMO systems, also smart radios such as cognitive radios [5] can be implemented as shown in Figure 16. In a cognitive radio setup, a transceiver scans for spectral white space and re-tunes the transmit spectrum to this location to minimize interference. The re-tuning can be done fast with the implemented DDFS in the FOM testbed.

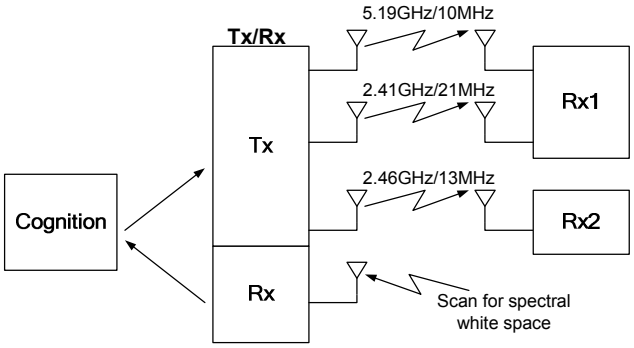

Figure 16 Cognitive Radio

VI. CONCLUSION

A very flexible MIMO testbed has been built and is described. The hardware development is shown in details and the calibration is discussed. Some possible applications of the FOM testbed are presented.

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