A Robust and Low-Complexity Timing Synchronization Algorithm for ADSRC System

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Abstract

In this paper, a robust, low-complexity timing synchronization algorithm suitable for 5.9 GHz Dedicated Short Range Communications (DSRC) system is proposed. The proposed method uses cross-correlation technique to detect the starting point of both a short training symbol and the guard interval of the first long training symbol. This allows the proposed algorithm to have low-complex architecture. Compared to the scheme proposed by Chang and Kelly, the proposed algorithm attains considerably higher timing synchronization performance and significantly reduced computational complexity. Simulation results show that the proposed algorithm is robust and efficient in high-mobility environments and low signal-to-noise ratio (SNR) conditions.

Index Terms – orthogonal frequency division multiplexing,, dedicated short range communication, timing synchronization, cross-correlation method.

1. Introduction

5.9 GHz Dedicated Short Range Communications (DSRC) is a short to medium range communications service that supports both public safety and private operations in roadside to vehicle and vehicle to vehicle communication environments. DSRC provides very high data transfer rates in circumstances where minimizing latency in the communication link and isolating relatively small communication zones are important. In North America, 5.9 GHz DSRC has been standardized as ASTM E 2213-03, shortly called ADSRC [1].

The ADSRC standard is the extension of IEEE 802.11. The physical layer (PHY) is adapted from IEEE 802.11a PHY, which is based on orthogonal frequency division multiplexing (OFDM) technology. Table 1 summarizes the key parameters of ADSRC's physical layer. ADSRC can operate with data payload capabilities of 3, 4.5, 6, 9, 12, 18, 24, and 27 Mbps. In addition, ADSRC can support a very high data rate, which can be up to 54 Mbps, when 20-Mhz bandwidth is used. The system uses 52 subcarriers, modulated using binary or quadrature phase shift keying (BPSK/QPSK), 16-quadrature amplitude modulation (16-QAM), or 64-quadrature amplitude modulation (64-QAM). Forward error correction coding is used with a coding rate of 1/2, 2/3, or 3/4.

OFDM has some advantages due to its capability to combat multi-path fading and high spectral efficiency [2]. However, OFDM is very sensitive to synchronization errors [3]. Since the vehicle in ADSRC system can reach the speed up to 120 mph, this makes the effect of Doppler spread become more severe. The Doppler spread associated with the multi-path propagation affects the synchronization performance. Therefore, ADSRC system needs a robust timing synchronization algorithm. In addition, for efficient hardware implementation, it is desirable that the timing synchronization scheme for ADSRC has low-complexity architecture.

Table 1. Key parameters of ADSRC's PHY

Signal Bandwidth B (MHz)	10
Data Rate (Mbps)	3, 4.5, 6, 9, 12, 18, 24, 27
Modulation	BPSK, QPSK,16-QAM, 64-QAM
Code Rate	1/2, 2/3, 3/4
OFDM Symbol Duration (μs)	8
Guard Interval (μs)	1.6
	10 , 20
Subcarrier Spacing (KHz)	156.25
Number of Pilot Tones	4
Number of Subcarriers	52

In this paper, a robust and low-complexity timing synchronization scheme for ADSRC system is proposed. It includes two steps. Firstly, the cross-correlation technique is used to detect the starting point of a short

training symbol. Then, the guard interval of the first long training symbol is found by applying the same cross-correlation function with the step size of 16. Therefore, timing synchronization can be achieved rapidly. The simulation results show that the proposed algorithm has good performances in high-mobility environments and low SNR conditions.

The rest of this paper is organized as follows. In section 2, the ADSRC system model is presented. After that, the proposed timing synchronization algorithm is given in section 3. Section 4 presents simulation results and analyses of the proposed algorithm. Finally, section 5 ends with conclusions.

2. ADSRC system model

Similar to WLAN 802.11a system, each ADSRC frame also has 3 fields: Preamble, Signal and Data as shown in figure 1. Preamble field includes 10 identical short training symbols and 2 identical long training symbols. Each short training symbol has 16 samples. Each long training symbol has 64 samples. The time interval between successive samples is 0.1μs.

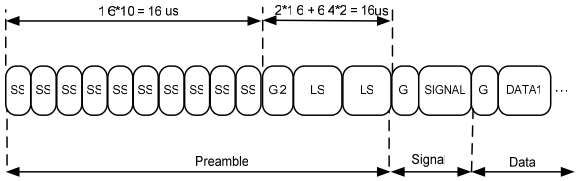

Figure 1. Frame format of ADSRC system.

Preamble is used for packet detection, Automatic Gain Control (AGC), carrier frequency offset estimation, symbol timing synchronization and channel estimation. The signal field's bits are BPSK-modulated. It contains the RATE and LENGTH information of the packet.

Figure 2 shows the block diagram of the baseband ADSRC system. In Signal Generation block, RATE and LENGTH parameters are encoded with a forward error correction (FEC) encoder, punctured and interleaved with an interleaver. After that, the interleaved data are BPSK-modulated and inserted by 4 pilot tones. The IFFT block generates an OFDM symbol which includes 64 data samples. To avoid intersymbol interference (ISI), a guard

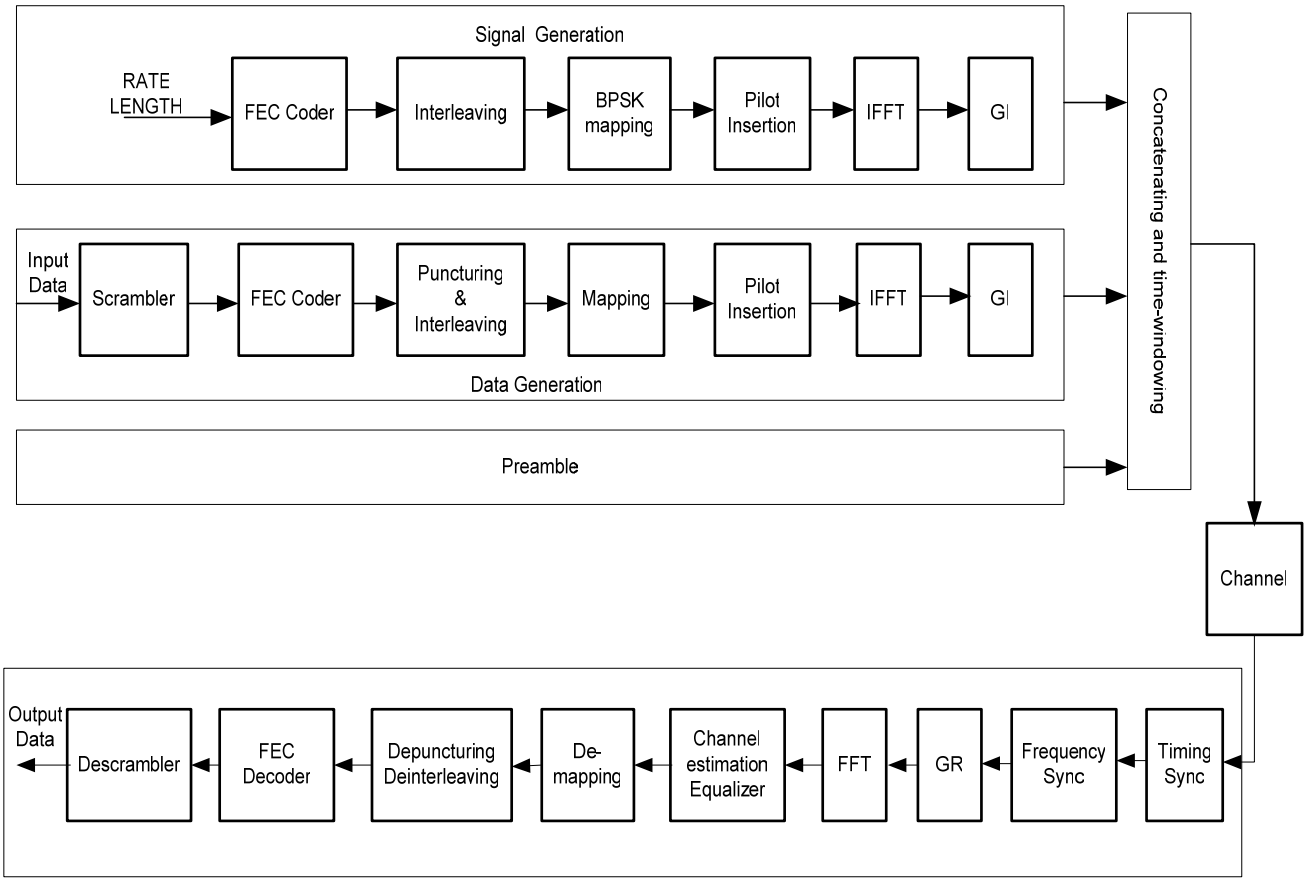

Figure 2. ADSRC Baseband Simulation Model

interval is added into this OFDM symbol. Guard interval comprises 16 data samples, which are the last 16 samples of useful data part. In Data Generation block, the input data is scrambled first. Then, like Signal Generation block, data are also encoded, punctured, and interleaved. Based on the RATE parameter in Signal field, data are modulated by using BPSK, QPSK, QAM16, or QAM64 technique. The remaining parts of this block work in the same manner as those of Signal Generation block.

An ADSRC frame is formed by concatenating three sub-frames: preamble, signal, and data. The boundaries are shaped by a time-windowing function in order to smooth transitions. The transmitted signal travels through the high-mobility channel. In this paper, the channel parameters of outdoor urban/suburban environment provided by Joint Technical Committee (JTC) are used for the ADSRC system [4]. Table 2 shows these parameters.

Table 2. Channel Parameters

Tap	Channel A (rms Delay Spread = 0.4μs)		Channel B (rms Delay Spread = 12 μs)	
	Relative Delay (ns)	Average Power (db)	Relative Delay (ns)	Average Power (db)
1	0	-1.6	0	-2.5
2	100	-5.1	300	0
3	200	0	8900	-12.8
4	500	-7.6	12900	-10
5	1200	-6.9	17100	-25.2
6	1600	-27.6	20000	-16

At the receiver, the timing offset and frequency offset in the received signal is adjusted in timing and frequency synchronization block. Next, Guard Removal (GR) block removes guard interval data and the OFDM symbols are converted to parallel data by FFT block. Based on two long training symbols and pilot tones, the channel estimation and equalizer block improve the system performance. The equalized data continued to be demodulated, depunctured, deinterleavered and decoded. Finally, output data are obtained after descrambler finishes processing the decoded data.

3. Proposed timing synchronization scheme

A variety of timing synchronization algorithms have been developed for the applications of OFDM-based systems [5]-[11]. In [5], a timing metric, which is the ratio between the correlation function to the received signal energy, is used to find the symbol timing. In [6], a Maximum Likelihood (ML) timing synchronization estimator is proposed. The robustness of these algorithms depends on the SNR estimation, which is usually inaccurate in high-mobility and multipath fading environments. In [7], a new timing synchronization which includes fine and coarse estimation steps is proposed. However, it requires a high-complexity architecture, particularly in coarse estimation block. Similar to [5] and [6], the accuracy of the algorithm in [7] also relies on the SNR estimation.

In this paper, a robust and low-complexity scheme for timing synchronization suitable for ADSRC systems is proposed. After Automatic Gain Control (AGC) and signal detection are done completely, the proposed timing synchronization scheme starts at an unknown position of the preamble. For example, the scheme is initialized at the 7^{th} sample of the 7^{th} symbol as shown in figure 3. The proposed algorithm takes two steps:

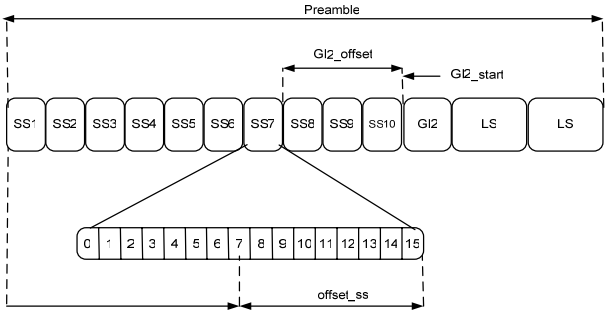

Figure 3. The proposed algorithm begins at the arbitrary point in Preamble field of an ADSRC frame.

Step 1: Detect the starting point of a short training symbol based on the cross-correlation function $R_1(n)$ between the received signal r(n) and the short training signal $r_s(k)$ which is known at both receiver and transmitter :

$$R_1(n) = \left| \sum_{k=0}^{15} r(n+k) r_s^*(k) \right|, \; 0 \le n \le 15 \qquad (1)$$

$$\text{offset-ss} = \arg \max_{0 \le n \le 15} \{ R_1(n) \}, \qquad (2)$$

where offset-ss is the timing offset of a short training symbol. Because one short training symbol has the period of 16 samples, the offset of a short training symbol is found when $R_1(n)$ is evaluated in 16 consecutive samples. As a result, the starting point of a short training symbol is detected.

Step 2: Detect the starting point of GI2:

$$R_2(m) = \left| \sum_{k=0}^{15} r(k+m) r_s^*(k) \right|, \qquad (3)$$

$$m = 0, 16, 32, 48, \ldots$$

$$GI2 - \text{offset} = \arg \max_{m} \{ R_2(m) < \theta \}. \qquad (4)$$

After step 1 is finished completely, the exact timing position of a short training symbol is found. However, how may short training symbols left in the given frame are still unknown. Therefore, the purpose of step 2 is to

find the starting point of the guar interval (GI2) of the first long training symbol.

The $R_2(m)$ calculates the cross-correlation value between the r(n) and $r_s(n)$. However, the argument m of $R_2(m)$ does not increase consecutively. Instead, m increases with step size of 16. Therefore, $R_2(m)$ has the plateau form in the short symbol region. When received signal is within the guard interval region of long symbol, $R_2(m)$ decreases sharply. A threshold θ is used to detect the starting point of guard interval in the received signal.

The architecture of the proposed algorithm is shown in figure 4.

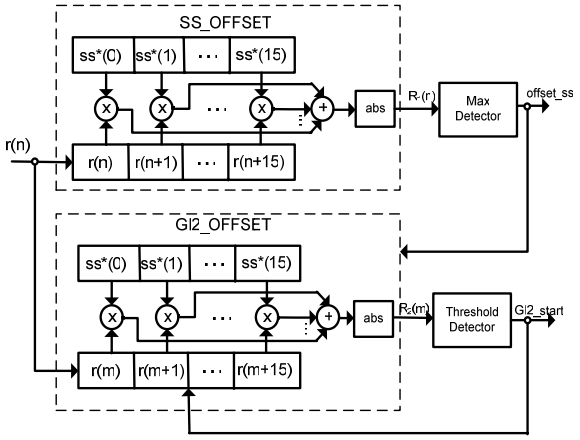

Figure 4. The architecture of the proposed scheme

Because both $R_1(n)$ and $R_2(m)$ use the same cross-correlation function, the structure of proposed scheme can be further simplified as shown in figure 5. This makes the proposed scheme become low-complexity.

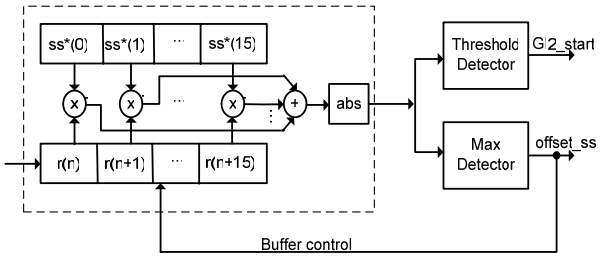

Figure 5. The low-complexity architecture of the proposed algorithm

4. Simulation results and analyses

The figure 6 and figure 7 show the curves $R_1(n)$ and $R_2(m)$ in the environment which has E_bN_o = 5 db and velocity of 120 mph. $R_1(n)$ curve reaches its maximum peak when n = 12. It means that the starting point of the short symbol is found at the 12^{th} sample of the received signal. $R_2(m)$ has a quite plateau form when m is within from 1 to 6. However, $R_2(m)$ decreases sharply when n =7, which indicates the starting point of the GI2.

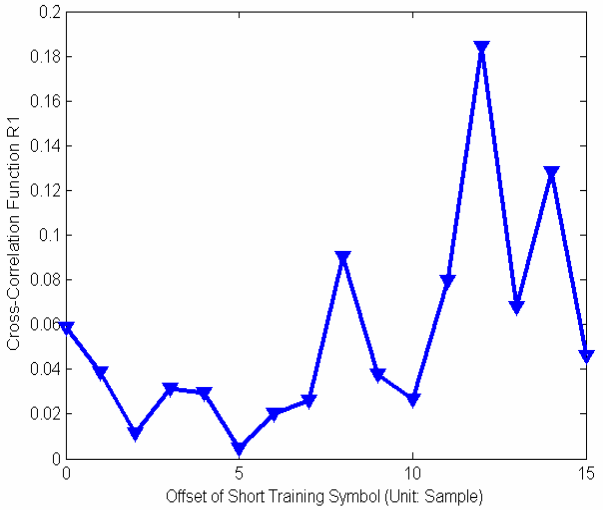

Figure 6. $R_1(n)$ reached the maximum peak when n = 12

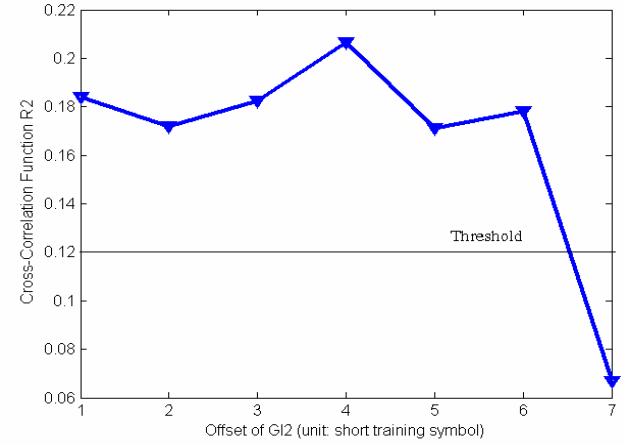

Figure 7. $R_2(m)$ is lower the threshold value Ω when m =7.

Synchronization Error Rate (SER) parameter is used to evaluate performance of the proposed algorithm. The Fig. 8 shows SER curves of the proposed approach and the Chang and Kelly algorithm in [7] when the vehicle moves at the velocity of 63 mph. Similarly, figure 9 illustrates the SER of these algorithms at the speed of 120 mph. Channel A is used in the experiments of figure 8 and figure 9. In channel B which has the delay spread (4μs) larger than the guard interval (1.6μs) of ADSRC system, the proposed scheme also shows its good performance as shown in figure 10.

The SER of the Chang and Kelly algorithm [7] is high compared to that of the proposed algorithm since SNR estimation of Chang and Kelly algorithm is usually inaccurate, particularly in high-mobility environments. Moreover, the accuracy of Chang and Kelly algorithm also depends on the received signal energy which is fluctuated in high-mobility and multi-fading conditions.

In addition to its robustness, the proposed algorithm

also has low-complexity architecture. The proposed architecture in figure 5 only needs 16 2-input multipliers, 15 2-input adders for hardware implementation. In Chang and Kelly algorithm, the timing synchronization is performed by the following equations [7]:

$$T_{fine-offset} = \arg \max_{0 \le n \le N-1} \left(\sum_{m=0}^{N-1} \left| \sum_{k=0}^{N_s-1} x(n+16m+k).SS^*(k) \right| \right) \quad (5)$$

$$f_{ML}(n) = \left| \sum_{k=0}^{N_t} x^*(n+k)x(n+k+N_s) \right| - \frac{1}{2}.\frac{\sigma_s^2}{\sigma_s^2+\sigma_n^2} \sum_{k=0}^{N_t} \left[|x(n+k)|^2 + |x(n+k+N_s)|^2 \right] \quad (6)$$

$$N_{reg} = \left\lfloor \frac{\min \left\{ \arg_n \left[f_{ML,norm}(n) < Thr \right] \right\}}{L_b} \right\rfloor \quad (7)$$

The number of 2-input multipliers and 2-input adders in (5) are at least 16 and 15, respectively. In (6), 16 2-input multipliers and 32 2-input adders are required. Therefore, Chang and Kelly algorithm needs at least 32 2-input multipliers and 48 2-input adders. Table 3 summarizes the computational complexity of the proposed algorithm and Chang and Kelly algorithm. It demonstrates that the proposed algorithm has low-complexity architecture.

Table 3. Computational complexity

	Proposed Algorithm	Chang and Kelly Algorithm
2-input multipliers	16	> 32
2-input adder	15	> 48

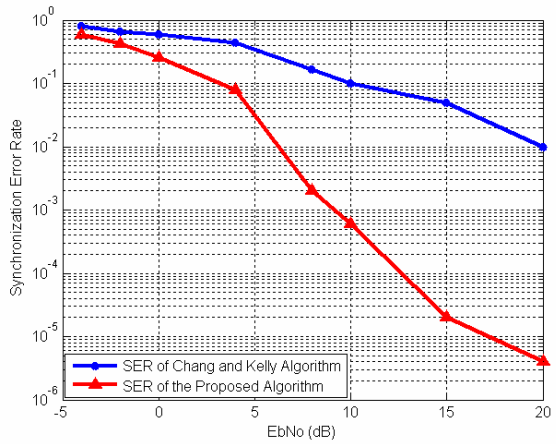

Figure 8. SER curves at the velocity of 63 mph, channel A

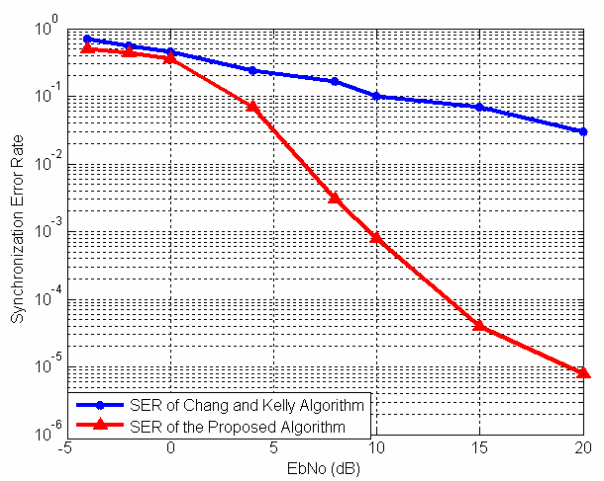

Figure 9. SER curves at the velocity of 120 mph, channel A

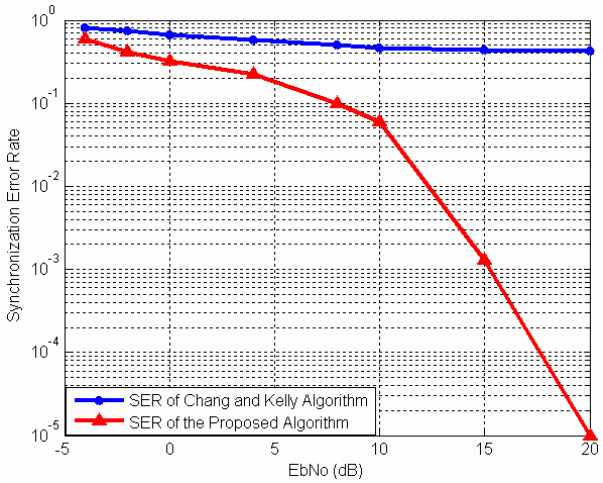

Figure 10. SER curves at the velocity of 120 mph, channel B

5. Conclusions

A robust and low-complexity timing synchronization algorithm suitable for ADSRC system was proposed. The proposed method uses cross-correlation technique to detect the starting point of a short training symbol. Guard interval's starting position of long training symbol is then found by applying the same technique. The advantages of the proposed scheme include its low-complexity architecture and its robustness in high-mobility environments and low SNR conditions.

6. Acknowledgement

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