Simulating and Designing RF Transmitter for Small Satellites

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Abstract

This paper discusses the simulation and the design of an RF transmitter for small satellites operating in the commercial S- band (2.2 - 2.29 GHz) with a data rate of 8 Mbps. In such systems, modeling frequency-dependent nonlinear characteristics of complex analog blocks and subsystems is critical for enabling efficient verification of mixed-signal system designs. In order to provide efficient and accurate simulation for the transmitter circuits, simple macromodels for weakly nonlinear mixer and power amplifier are used in the system simulation. Also, we introduce the noise in several circuits (frequency synthesizer, crystal oscillator, power amplifier, mixer,…) and we demonstrate their effect on the noise performance system. In the simulation we consider features of components and technologies commercially available.

1. Introduction

The increasing demand for small satellites communication systems has greatly expanded the need for algorithms and system-level simulation that are both efficient and accurate when applied to RF communication circuits. The respect of technical specifications of future systems requires important efforts in the integrated circuits technologies, RF circuits and algorithms of conception. The increase of electronic functions to integrate in a satellite RF systems is accompanied by the increase of electric consumption and the improvement of commutation speed. Circuit designers become very appre-ciative to know a design methodology that includes efficient exploration of system-level architectures before detailed circuit implementation. Today's transmitter subsystem in earth imaging microsatellite systems demand higher communication quality, higher data rates to be capable to transmit pictures or data with a quality quite appropriate, higher frequency operation and more channels per unit bandwidth. Low power consumption and small size are required for this equipment. In this module, modeling frequency-dependent nonlinear characteristics of complex analog blocks and subsystems is critical for enabling efficient verification of mixed-signal system designs. It's well know that the mixer and the power amplifier are considered, respectively, as time-varying systems because its function involves frequency translation and when there is a large signal in an adjacent channel [1]. For the transmitter simple macro-models for weakly nonlinear mixer and power amplifier are used to achieve efficient and accurate system simulation [2], [3]. Also, this system model includes noise in several blocks and demonstrates its effect on the noise performance system.

In this paper we present the simulation and the conception of a radio frequency transmitter operating in the commercial S-band (2,2-2,29 GHz) with a data rate of 8Mbps. The system model architecture is based on the principle of the RF transmitter module integrated on the nanosatellite SNAP-1 launched in 1999 [4], [5]. In the simulation, we consider the characteristics of commercially available components.

2. Conception and discussion

Figure 1 shows a simplified block diagram of S-Band transmitter designed for a variety of low-cost nanosatellite, microsatellite and enhanced microsatellite applications. This transmitter module is also suitable for all classes of satellite missions. It provides a low power output, can be configured for a wide range of data rates and supports BPSK and QPSK modulation schemes. The transmitter is comprised of a data processing unit, a Controller Area Network (CAN) for TT&C, a frequency synthesizer, an I/Q modulator and power amplifiers. As shown in Figure 1, this transmitter generates a very high

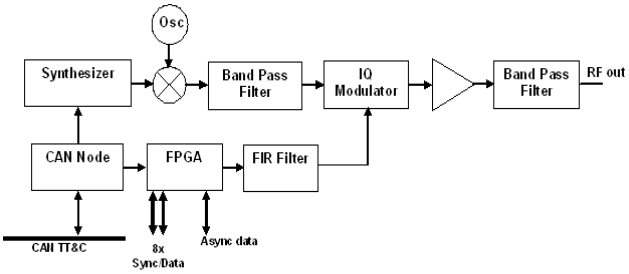

Figure 1. S-band transmitter module block diagram.

stable S-band signal with a frequency synthesizer. It then translates the signal to the up-conversion by mixing it with a temperature compensated crystal oscillator. The resulting RF signal is directly converted to baseband and amplified with a power amplifier.

2.1. Frequency Synthesizer

Figure 2 shows the PLL's linear model with feedback. This PLL is called an integer-N system. This means the Voltage Controlled Oscillator (VCO) frequency and the crystal reference are some integer multiple of the reference frequency. The PLL consists of a high stability crystal reference oscillator, a frequency synthesizer, a voltage controlled oscillator, and a passive loop filter. The frequency synthesizer includes a phase detector, a current mode charge pump, and programmable frequency dividers. The passive filter is desirable for its simplicity, low cost and low phase noise.

To achieve optimal circuit performance, the phase noise should be evaluated for proper loop design and it will impact many critical operating characteristics of the synthesized oscillator including adjacent channel power [6]. The simple approximations for different noise sources (crystal reference noise, phase detector noise and VCO phase noise) were used in the simulation [7]. Also, reference spurs can occur at the multiples of the comparison frequency, and can be translated by the mixer to the desired signal frequency and cause an AC modulation on the tuning line of the VCO, which can be viewed as FM modulation.

In the simulation, we use the characteristics of a National Semiconductor model LMX2326 programmable frequency synthesizer capable of phase locking a VCO between 500 MHz and 3 GHz. The VCO used is from Mini-Circuits (JTOS-2700V), which utilizes a high performance transistor operating in the fundamental, rather than the doubling push-push mode and capable to generate a power of +8 dBm over a load of 50Ω. Its linearity is relatively good (46 – 56 MHz/V). This data is very important in the loop filter calculation. Also, This

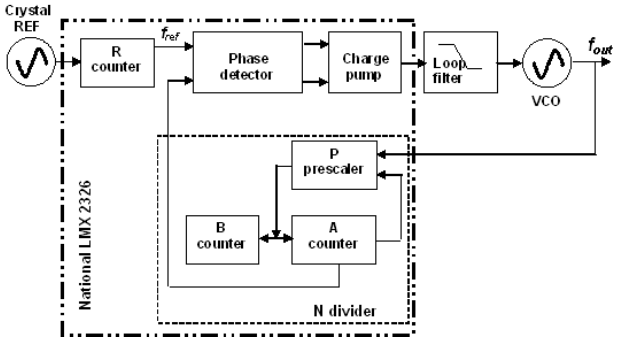

Figure 2. Block diagram of the designed frequency synthesizer.

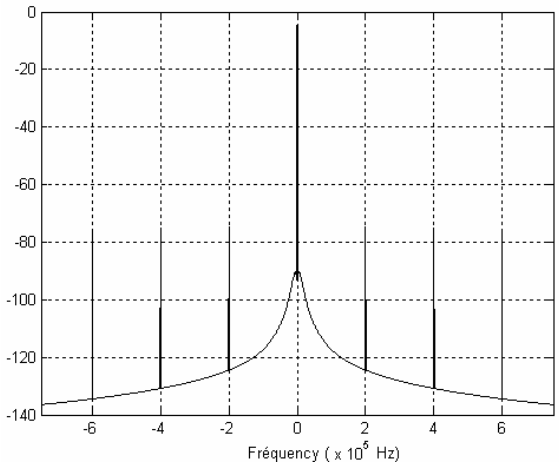

Figure 3. PLL output spectrum.

VCO presents a pulling of 5 MHz, a pushing of 1 MHz and a phase noise of -114 dBc/Hz at an offset frequency of 100KHz. In practice, the PLL can be programmed via a laptop computer and parallel port cable. The frequency changes were done using software provided by National Semiconductor, of which the PLL serial-control data are controlled by three inputs (data, LE and clock).

The 21-bit data register programmed with the data stream is shifted into 14-bit R Counter, 18-bit N Counter, and 18-bit Function Latch according to control bits. In this work, the output frequency range of the synthesizer is (2,2 - 2,29 GHz) (FVCO) with a spacing channel of 1MHz (Fcomparison). The reference frequency of the oscillator is 10 MHz (Fosc). To begin with, we choose a frequency within the operating range and we determine the values of the N and R counters. In this case, the reference divider (R counter) equal to 10 and the N counter equal to 2005 (A counter=21 and B counter = 62), the output frequency resulting ((32xB+A)xreference frequency) is equal to 2005 MHz.

In this work, the loop filter design is a very critical part of the PLL synthesizer. In general, a low loop filter cutoff makes the PLL response slower and the setting time of frequency switching (PLL lockup time) longer and the PLL spurious suppressed. Conversely, increasing cutoff frequency provides faster PLL response, shorter PLL lockup time. Also as results, the PLL output signal is frequency-modulated and contains high level spurs. The output spectrum plot is displayed in Figure 3 for a performed loop filter design. The results show a noise density of -93 dBc/Hz at 10 kHz and -118 dBc/Hz at 100 kHz offset frequencies. The results indicate that the PLL gives an rms of 0.008 radian and a signal-to-noise ratio of 35.74 dB. The output power level of the synthesizer is about 6,4 mW (+8dBm) which is sufficient to feed the balanced mixer of (level 10 or level 13) series, generally used in transmit/receive applications.

2.2. Mixer and BP filter

In such systems, it was found to be optimal to offset the synthesizer to prevent the modulated BPSK signal form pre-modulating VCO output, only to be remodulated again [5]. Generally, RF circuits are designed to be as linear as possible from input to output to prevent distorsion of the information signal. Mixers are designed to translate signals from one frequency to another by an additional crystal oscillator. For best performance, mixers are designed to respond in a strongly nonlinear fashion to the local oscillator. As shown in Fig. 4, the two input signals of the mixer the S-band signal form frequency synthesizer and the 240 MHz offset frequency are generated by a Temperature Compensated Crystal Oscillator. This signal was missed with the S-band signal through a passive mixer and passed through a block filter to remove all but the desired channel. In system simulation, the mixer can be incorporated by a macromodel that consists of several transfer functions. These transfer functions are found by reducing the large systems of equations that describe this circuit. The noise is characterized by using the noise figure of the block because it is relatively simple to combine it of cascaded blocks to determine the noise figure of the entire

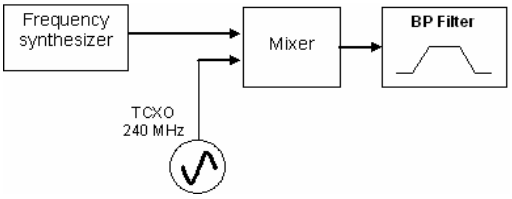

Figure 4. Simplified diagram of the mixer with the band-pass filter.

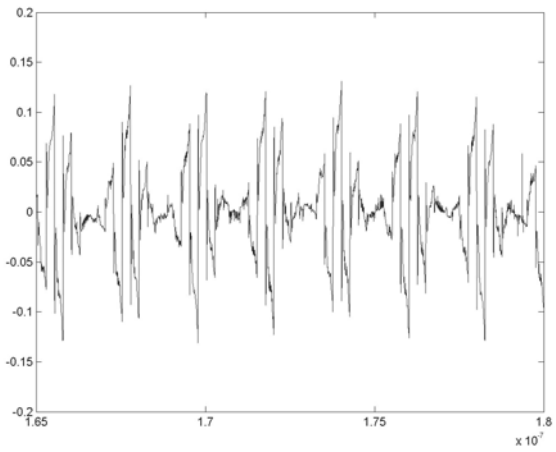

Figure 5. Output signal of the mixer.

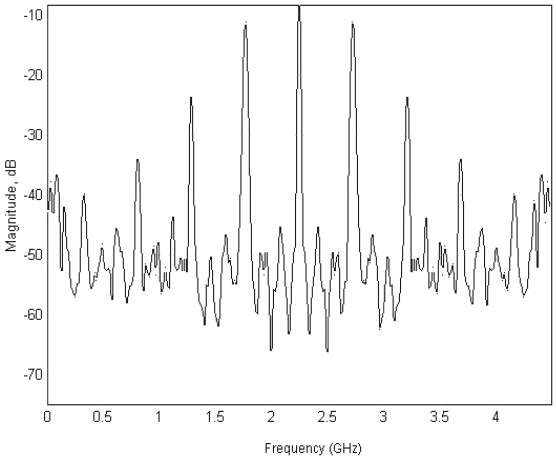

Figure 6. Mixer output spectrum.

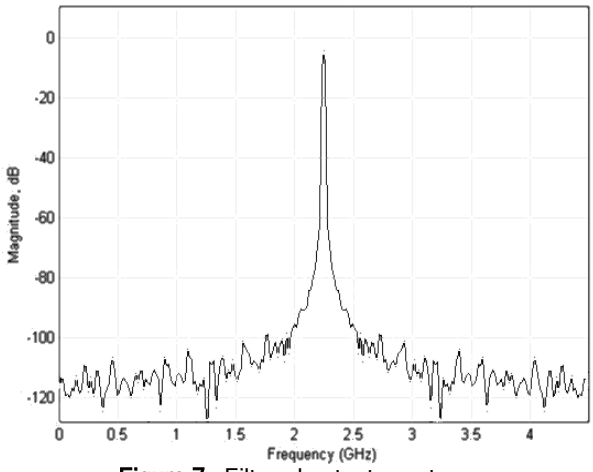

Figure 7. Filtered output spectrum.

transmitter.

While consulting companies catalogues, notably Mini Circuits, we find many models perfectly adapted. The mixer selected is TUF-2500 MHSM specified up to 2.5 GHz with isolation more than 24 dB between RF and IF ports and a conversion loss lower than 8.5 dB. The output spectrum and the form of signal plots of the mixer are displayed in fig. 5 and fig. 6, respectively. The filtered signal spectrum plot is illustrated in fig. 7.

2.3. I/Q modulator

In addition to the S-band signal, I and Q channels from FPGA are fed through the I/Q modulator for direct up-conversion to S-Band. Today's QPSK modulators as those of Analog Devices, Sirenza Microdeviceses or those of Mini- Circuits are designed to take RF inputs from S-band frequencies and convert directly down to baseband I and Q signals, thus providing cost savings over multiple-stage devices. Regarding the baseband I

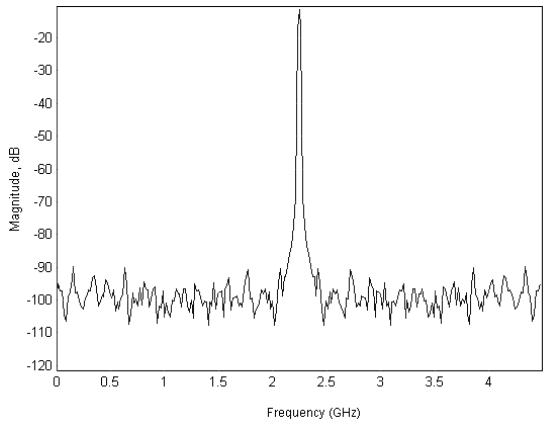

Figure 8. QPSK modulated output spectrum.

and Q outcoming from FPGA, we use only a short sequence of 29-1 bits. For optimal noise performance, the I and Q binary data streams are shaped into Nyquist baseband pulses with root-raised-cosine spectral distributions [5]. The QPSK modulated signal spectrum plot is illustrated in fig. 8. The results show unwanted out-of-band spurs of -90dB/Hz at an offset frequency of 100 KHz, which present a very important performance level for such application.

2.4. Power amplifier

The modulated signal is then fed through the band pass filter and the power amplifier (PA). In this design, a simple RF amplifier based on a GaAs-MESFET transistor from NEC Company has been used. This device presents a power gain of 51 dB at operating frequencies. In practice, the output spectrum must not contain unwanted spurs or distortion products and must not contain appreciable noise at the corresponding S-Band frequency. As we work at 50Ω, we must add the matching networks in both input and output ports of the PA.

In this system simulation, the power amplifier is incorporated as a simple RF circuit macromodel that provides accurate abstractions for time-varying circuits over S-band frequencies. This macromodel form corresponds to block diagram structures that are easily incorporated into the system simulation based on

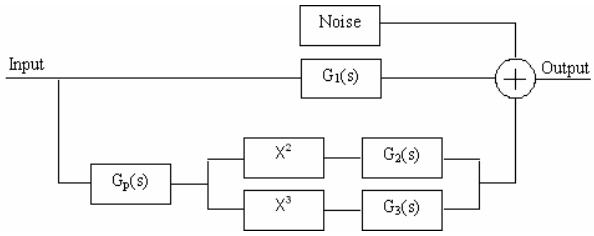

Figure 9. Macromodel circuit for PA.

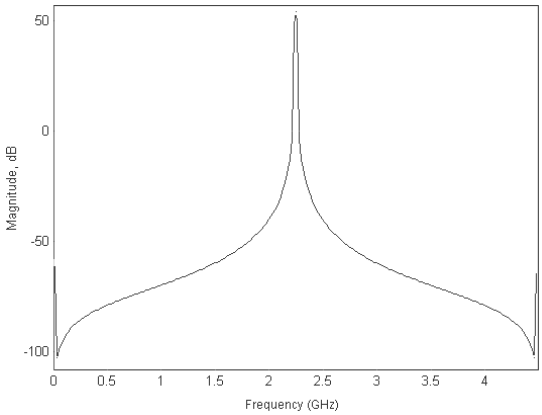

Figure 10. Final signal spectrum delivered to transmission antenna.

Simulink. For the reason of simplicity, we assume that the circuit macromodel used is weakly nonlinear and its maximum order of nonlinearities is equal to 3.

For the macromodel in Fig. 9, the PA is presented by its first transfer function G1(s) which represents the linear component of the power amplifier. So, the output signal of the PA varies linearly with the incoming signal in order to achieve the appropriated specifications of the gain and to avoid any distortion of the output signal.

Also, the second and third-order components (second and third transfer functions, respectively) are taken into account in order to represent the non-linear components introduced in the simulation. Higher order components are ignored because their contribution to the nonlinearities is negligible. We note that Gp(s) represents the transfer function of the input impedance match network employed in the circuit. In addition to the input signal, the noise source is also incorporated in this design. It is composed of a white noise generator joined to a transfer function with which we can calculate the spectral noise power density [8]. The amplified signal spectrum contains in addition to the useful stripe of 2245 MHz the parasitic spurs around the central frequency, which requires to be eliminated by a pass-band filter before routing the output signal toward the antenna for transmission. Figure 10 represents the spectrum plot of the signal delivered to the transmission antenna. This signal has been filtered by a 90 MHz pass-band filter centred on the frequency 2245 MHz.

3. Conclusion

A simple conception of a small satellites RF transmitter operating in the commercial S-band (2.2 - 2.29 GHz) with a data rate of 8Mbps is presented. The system model is performed to incorporate simple macro models for weakly nonlinear mixer and power amplifier and the

noise in different blocks. The results indicate a very important performance level and demonstrate the efficiency of this procedure for analyzing and designing RF systems.

4. References

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