

Monolithic Microwave Integrated Circuits for 5G and Satellite Communication

by Quoc Toan Chau

Thesis submitted in fulfilment of the requirements for
the degree of

Philosophy of Doctor

under the supervision of Dr. Forest Zhu

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CERTIFICATE OF ORIGINAL AUTHORSHIP

I, Quoc Toan Chau declare that this thesis, is submitted in fulfilment of the requirements for the award of Doctor of Philosophy, in the School of Electrical and Data Engineering/Faculty of Engineering and Information Technology at the University of Technology Sydney.

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Declaration by Author

This thesis presents original work carried out by me – Quoc Toan Chau, and has not been submitted previously, in whole or in part, for the award of any degree or qualification at any university or tertiary institution. Artificial intelligence tools were used only to assist with language clarity, structural refinement, and editorial improvements. All technical content, research methodology, experimental work, data analysis, interpretation of results, and conclusions are my own.

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List of publications for this thesis

First GaAs W-band amplifier design, submitted to APMC 2023, accepted.

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List of Abbreviations

5G	Fifth Generation (Mobile Communications)
6G	Sixth Generation (Mobile Communications)
RF1	Radio Frequency Path 1
RF2	Radio Frequency Path 2
GEO	Geostationary Earth Orbit
LEO	Low Earth Orbit
RF	Radio Frequency
RX	Receiver
TX	Transmitter
LNA	Low Noise Amplifier
PA	Power Amplifier
BA	Buffer Amplifier
SATCOM	Satellite Communications
MMIC	Monolithic Microwave Integrated Circuit
pHEMT	Pseudomorphic High Electron Mobility Transistor
FET	Field-Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
QAM	Quadrature Amplitude Modulation
GaAs	Gallium Arsenide
GaN	Gallium Nitride
SiGe	Silicon-Germanium
SiC	Silicon Carbide
InP	Indium Phosphide
PDK	Process Design Kit
S-Parameter	Scattering Parameter
NF	Noise Figure
P_{out}	Output Power
PAE	Power Added Efficiency
IMD3	Third-Order Intermodulation Distortion
OIP3	Output Third-Order Intercept Point
EM	Electromagnetic

Abstract

Designing high-frequency microwave amplifiers remains challenging as modern 5G networks and satellite communication (SATCOM) systems demand higher data rates, broader bandwidths, and robust performance. This thesis investigates three monolithic microwave integrated circuit (MMIC) amplifier designs: two GaAs-based and one GaN-based. These designs address two critical frequency bands: the millimetre-wave W-band (75 – 110 GHz) for high-capacity links and the K-band (18 – 27 GHz) for next-generation 5G fronthaul and SATCOM payloads. The results confirm GaAs's suitability for low-noise front-ends and GaN's superiority for high-power amplification.

The first design is a 75 – 85 GHz GaAs amplifier targeting high-throughput systems. By employing broadband matching and parasitic control, the design achieves unconditional stability and competitive noise performance, proving GaAs's viability for high-frequency receiver stages despite increasing passive losses at W-band.

The second design is a 17 – 22 GHz GaAs low-noise amplifier (LNA). Achieving a noise figure below 1.3 dB required rigorous optimisation of transistor sizing and electromagnetic simulation, reinforcing GaAs as the leading technology for high-gain K-band front-ends.

The third design is a 17 – 22 GHz GaN power amplifier. Leveraging GaN's wide bandgap, the design utilizes load-pull optimisation and harmonic tuning to deliver high output power while meeting strict efficiency and spectral requirements for 5G and SATCOM transmitters.

Initially focusing on the extreme electrical density of the W-band, this research establishes robust EM-based modeling and design methods. These methodologies are then transferred and refined for K-band applications where increased device flexibility enables high linearity and low noise. Demonstrating successful MMICs in both bands validates the methodology's reliability while responding to the multi-band demands of future space and terrestrial systems. These practical contributions highlight the complementary roles of GaAs and GaN in modern telecommunications.

The main original contributions of this thesis include the practical demonstration of a 75-85 GHz GaAs driver amplifier achieving unconditional stability with competitive flat gain, a 17-22 GHz GaAs single-supply LNA achieving a noise figure below 1.3 dB through optimized inductive source degeneration and EM-aware packaging co-design, and a 17-22 GHz GaN power amplifier delivering over 30 dBm saturated output power with >30% PAE. These designs validate a comprehensive methodology integrating full-wave EM simulation, rigorous stability analysis, and tailored biasing strategies for next-generation space and terrestrial mm-wave front-ends.

Chapter 1: Introduction

In the recent era of technological development, the demand for faster, more efficient and higher capacity wireless communication has been getting increasingly popular. As a result, microwave monolithic integrated circuits (MMIC) with robust data rate, high linear power, low noise, wide bandwidth and sustainable stability are required, especially at higher frequency. While lower frequencies are occupied by majority of wireless networks such as household appliances, Bluetooth and Wi-Fi connected devices, higher frequencies like millimeter-wave such as K-band and W-band still have a lot of potential for development, which can be dominantly used for 5G/6G, satellite and space applications. On the other hand, MMIC designs face major challenges like atmosphere interference, heat, coupling effect among the elements of the design, sustainable penetration and path loss in the environment. Therefore, MMIC design engineers need to come up with sufficient solutions to overcome these challenges.

1.1 Background and Motivation

Over the last three decades, the center of focus in radio-frequency and microwave engineering has drifted steadily toward the millimeter-wave spectrum. Several forces drive this trend such as the relentless growth of global data traffic; the proliferation of low-Earth-orbit (LEO) satellite constellations providing broadband access; the need for higher-resolution radar, imaging, and sensing; and the availability of semiconductor processes capable of useful gain beyond tens of gigahertz. In this landscape, the front-end amplifier takes on enormous importance. On the receive path, the low-noise amplifier (LNA) largely fixes the receiver noise temperature and therefore the achievable link margin and data rate. On the transmit path, the power amplifier (PA) sets the effective isotropic radiated power (EIRP) and the energy efficiency with which that power is delivered. When an amplifier underperforms, systems compensate by increasing antenna aperture, raising platform power budgets, or adding satellites, each of which increases cost and mass, complicates operations.

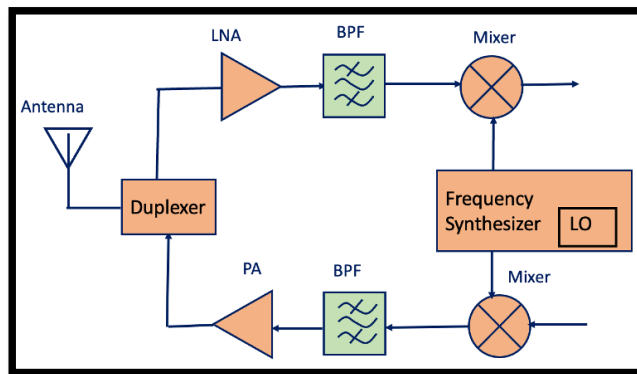


Figure 1.1: A simple RF transceiver system.

The consequences are particularly pronounced in small-satellite applications. CubeSats and microsatellites are constrained by limited power generation and thermal rejection, strict mass budgets, and modest form factors for antennas and feed networks. Within these constraints, even fractional improvements in noise figure (NF) or power-added efficiency (PAE) can tip a link from marginal to robust. The Australian context amplifies this observation. The SmartSat Cooperative Research Centre (CRC) was established to accelerate sovereign capability in space communications, Earth observation, and defence technologies; compact and reliable RF front-ends have been identified as a priority because they amplify the effectiveness of every downstream subsystem [1], [2]. Australia's strength in design, test, and systems integration can be translated into flight-ready hardware by focusing on amplifier modules that exploit commercial foundry processes while meeting space reliability demands.

Although the thesis spans both W-band and K-band circuit design, the progression between these frequency regimes is intentional rather than incidental. The work begins at W-band, where the extreme electrical compactness demands full-wave-driven design, enabling the development of high-fidelity modelling, interconnect optimisation and layout methodologies. These techniques form the foundation for the subsequent K-band projects, where greater device flexibility allows their refinement toward high-linearity and low-noise objectives relevant to 5G system and SATCOM terminals. By demonstrating successful MMIC realisations across two distinct mm-wave regions, the thesis validates the robustness and generality of its design methodology while simultaneously addressing system-level needs for emerging multi-band space and terrestrial communication platforms.

This thesis is motivated by that practical intersection. It pursues amplifier designs that are not only high-performing in laboratory conditions but are also stable across process spread, tolerant of packaging and layout parasitics, and resilient under the environmental stresses of orbit. Rather than treating the technology choice as a binary contest, the work adopts a complementary view: GaAs pHEMTs are pursued for ultra-low-noise receive chains, while GaN HEMTs are developed for high-power transmit chains. Electromagnetic (EM) co-design, bias stabilization, and radiation-aware margins are treated as first-class elements of the design, not afterthoughts. The goal is to deliver reproducible performance in the bands of greatest interest to near-term missions while articulating a framework for technology selection that outlives the specific prototypes reported here.

1.2 Research Objectives

The research objectives of this thesis are defined through several coordinated directions of investigation addressing both millimetre-wave and microwave bands for advanced 5G transport networks and SATCOM systems. At W-band frequencies, the primary objective is to realise high-performance MMIC building blocks with competitive gain, low noise, and adequate output power under the severe constraints imposed by device scaling, passive losses, parasitic effects, and thermal limitations, while ensuring stable, repeatable, and packaging-compatible operation suitable for system-level integration. At lower microwave frequencies, the work aims to demonstrate the effective use of GaAs technology to realise low-noise, high-gain amplification across the targeted bands with strong post-packaging robustness and manufacturing viability. In parallel, the work establishes the capability of GaN power amplifiers operating in the K-band range (17 - 22 GHz) to simultaneously achieve saturated output power exceeding 30 dBm and power-added efficiency above 30% under strict power consumption and thermal constraints. Finally, the research systematically identifies and validates stability design methodologies that ensure unconditional stability without degrading critical performance requirements, including the normalized determinant function, return-ratio analysis, dual RC bias trapping, deliberate gain tapering, layout-based damping, and WS-probe analysis.

Accordingly, this research is structured around five interrelated technical objectives:

- Objective 1: To develop and assess W-band GaAs driver amplifiers operating between 75 and 85 GHz, targeting competitive flat gain, low noise, and sufficient output power under conditions of unconditional stability, utilizing full-wave EM-simulation for passive component integration.
- Objective 2: To design K-band GaAs LNAs (17 - 22 GHz) achieving a noise figure below 1.3 dB and flat gain exceeding 20 dB, addressing packaged performance through co-design of RF launches.
- Objective 3: To design K-band GaN power amplifiers (17 - 22 GHz) that deliver flat gain, saturated output power above 30 dBm, and PAE exceeding 30% using load-pull simulation and RC stabilised networks.
- Objective 4: To establish a structured comparative framework for GaAs and GaN technologies in the targeted bands, accounting for noise, power, efficiency, and packaging losses.
- Objective 5: To address qualification-oriented refinements ensuring stability and resilience under thermal cycling and process variations.

What is novel in this work is the comprehensive co-design methodology that explicitly integrates full-wave EM simulations of packaging transitions and bias network parasitics into the core stability and performance optimizations, directly bridging the gap between bare-die potential and module-level reality. Furthermore, this work uniquely demonstrates the practical implementation of true single-supply, enhancement-mode GaAs LNAs at K-band to eliminate negative bias sequencers. These methodologies and designs were rigorously verified through on-wafer and packaged measurements, validating the simulated small-signal, noise, and large-signal power responses under realistic operating constraints.

1.3 Frequency bands of interest and challenges

The K-band (17 - 22 GHz range) overlaps well-established allocations used for satellite downlinks and uplinks. In this band, signal transmitted propagation is dominated by rain attenuation rather than oxygen absorption. As a result, receiver NF and antenna gain dominate the system temperature and link margin. A front-end NF improvement of a few tenths of a decibel can translate into several decibels of end-to-end margin after cascaded losses and modem implementation penalties are accounted for. The component ecosystem is comparatively mature, where GaAs LNAs with around 1.6 - 1.9 dB NF and 20 - 25 dB gain are main concentrations, and GaN HPAs in the 10 W-class are widely reported. This development lowers integration risk for near-term Small-Sat missions [11] - [16].

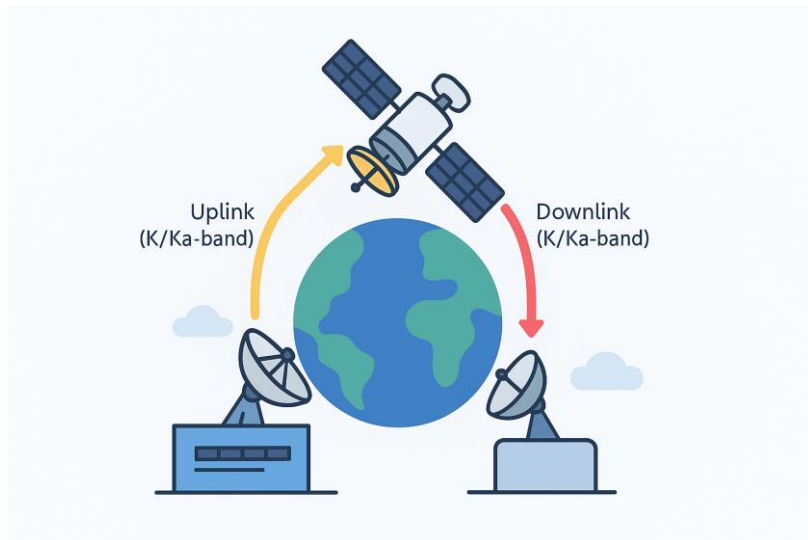


Figure 1.2: SATCOM link architecture.

By contrast, 75 - 85 GHz sits within W-band, where gaseous attenuation grows but a practical window remains among strong oxygen lines. The payoff is substantial contiguous bandwidth, enabling wide instantaneous data rates and high radar resolution [3], [4]. The design regime changes qualitatively,

where passive structures behave as transmission lines, via inductance and pad capacitance become resonant, and EM modelling/simulation shifts from helpful to mandatory. Packaging transitions like coax-to-waveguide or waveguide-to-microstrip launches can consume tenths of a decibel of NF or PAE if not carefully considered, and small misalignments can move matches appreciably. For these reasons, W-band is treated as an EM-dominated domain in which layout and packaging are inseparable from circuit design.

Neighbouring bands place this choice in context. X-band (from 8 to 12 GHz) has deep heritage and favourable propagation, but it cannot deliver comparable throughput without very large antennas. Q/V-band (between 40 and 75 GHz) offers more spectrum yet suffers greater atmospheric loss and a younger supply chain. Optical cross-links promise extreme data rates but impose pointing precision, weather constraints and qualification complexity. This dual focus supports the requirements of next-generation wireless systems while preserving spectral headroom, and the selected frequency bands represent a realistic compromise between performance potential and the increasing risks associated with propagation and implementation losses.

1.4 Amplifier technologies at millimeter-wave

Two compound semiconductor families dominate practical millimeter-wave amplifiers, which are Gallium Arsenide (GaAs) and Gallium Nitride (GaN). Each process relates naturally to a role in the RF front end because their physical properties offer different operating points. Two compound semiconductor families dominate practical millimetre-wave amplifier technology, which are Gallium Arsenide (GaAs) and Gallium Nitride (GaN). Each technology aligns naturally with specific roles in the RF front end because their intrinsic material properties support different operating frequencies.

GaAs pHEMT designs continue to serve as the workhorse for low-noise reception. In the K-band range, such as 17 - 22 GHz, commercial designs routinely demonstrate noise figures in the vicinity of 1.6 to 1.9 dB together with approximately 20 dB of gain across substantial bandwidths. Carefully optimised custom designs can further improve these parameters within more restricted bands [11] - [13]. At W-band, state-of-the-art GaAs low-noise amplifiers achieve noise figures of approximately 5 to 6 dB with more than 20 dB of gain from 75 to 85 GHz, and specialised coplanar implementations near 94 GHz have reported noise figures close to 3.6 dB [7]. The continuing appeal of GaAs stems not only from its competitive noise performance but also from the maturity of its device uniformity, its well-developed process design kits, and its packaging options with substantial flight heritage.

These characteristics contribute to reproducible performance and enable predictable degradation when devices transition from wafer-probe measurements to module-level integration and environmental qualification.

On the other hand, GaN HEMT technologies outweigh in applications where breakdown voltage and power density are the principal constraints. Within the K-band, single-die power amplifiers delivering more than 30 dBm of saturated output power and power-added efficiencies exceeding 30 percent are now widely reported in both academic and commercial developments [14] - [16]. These performance levels are particularly valuable in SmallSat platforms because they support compact transmit modules that require only modest corporate combining to reach the necessary EIRP targets without imposing excessive thermal loads. The principal limitation is the comparatively higher noise figure, which prevents GaN from serving as the first-stage LNA, together with sensitivity in some process nodes to charge trapping and dynamic on-resistance effects under radiation exposure and temperature cycling. Although these behaviours can be mitigated through conservative biasing, ballast structures, and appropriate device screening, they must be accounted for explicitly in both the design methodology and the qualification plan.

Other technologies play narrower roles. Indium phosphide (InP) still sets the absolute NF record at W-band, but its cost, supply chain, and mechanical fragility limit its practicality for small programs. Silicon-germanium (SiGe) BiCMOS offers excellent integration for mixed-signal arrays and 77 GHz automotive radar, but beyond 90 GHz where its gain and thermal headroom decrease. In space payloads where reproducibility and qualification heritage weigh heavily, GaAs for LNAs and GaN for HPAs remain the pragmatic baseline [5] - [7], [14] - [16].

1.5 Stability considerations

As amplifier designs extend toward the device oscillation frequency $f_{\max}$ and passive structures assume increasingly distributed behaviour, stability must be treated as a primary design objective on par with noise performance or efficiency. Classical small-signal indicators such as Rollet's K -factor and the associated μ -parameters remain useful screening tools, yet they can become unreliable in multi-stage networks or in situations where device bias conditions interact with passive resonances. To address these limitations, Ohtomo's stability analysis provides a more precise foundation by examining the characteristic determinant of the active network and identifying the operating conditions under which its roots shift into the right half of the complex plane. When evaluated across frequency, bias, and temperature, this determinant offers a direct and compact criterion for

unconditional stability and serves as a robust sign-off mechanism for millimetre-wave designs. In practical design flows, Ohtomo’s method is supplemented with focused return-ratio inspections at internal loops to capture localised feedback paths, together with large-signal stability evaluations to confirm that the circuit remains well behaved under the full range of anticipated drive levels and operating environments. This combined approach ensures that stability margins are preserved not only in nominal operation but also in the presence of packaging transitions, thermal excursions, and process variation.

Effective stabilisation relies on a combination of schematic-level circuit techniques and layout practices informed by full EM simulation. Series gate resistors provide reliable damping of finger-level resonances, while lossy shunt loading at high-impedance inter-stage nodes suppresses excessive peaking. Dual RC networks incorporated into bias tees are used to attenuate low-frequency loop gain that can otherwise re-emerge under thermal drift. Stage-by-stage gain is deliberately moderated to maintain a uniform stability margin across the broader system. The physical layout plays an equally important role, where dense via fencing around high-impedance nodes reduces unintended inductance, symmetric routing mitigates odd-mode coupling, and geometries that facilitate broadside interaction, such as extended meanders, are avoided. Pad and transformer structures are typically validated through back-to-back test coupons to ensure predictable behaviour once integrated. At frequencies above 75 GHz, full EM simulation of transformers, bends, routing discontinuities, and pad structures becomes essential rather than discretionary. Packaging is treated as an intrinsic part of the circuit, with launches, bond-wire arrangements, and waveguide transitions incorporated directly into the electromagnetic model and reflected explicitly in the stability assessment and in the overall noise and efficiency budgets [3], [4].

1.6 Summary and thesis outline

This chapter presents the motivation and technical challenges associated with MMIC design at microwave and millimetre-wave frequencies. The shift toward millimetre-wave operation is shaped by escalating global data requirements, the emergence of large LEO constellations, and the demand for finer resolution in sensing and imaging systems. In that context, the front-end amplifier remains a dominant contributor to overall system performance whereas the LNA establishes the receiver noise figure, while the PA determines the achievable EIRP and strongly influences efficiency and thermal loading. These considerations become even more critical in small satellite platforms, where mass, volume, and available power impose strict limits on architectural choices. The selected frequency ranges of K-band for near-term communications and W-band for wide instantaneous bandwidth and high-resolution radar, which represent a balance between attainable performance and the integration

risks inherent at higher frequencies. Correspondingly, the choice of semiconductor technologies reflects complementary strengths, with GaAs well suited to ultra-low-noise receive chains, GaN enabling high-power transmit functions, and InP or SiGe employed only in specialised scenarios.

The remainder of the thesis is organised as follows. Chapter 2 develops a literature review including GaAs W-band amplifiers, GaAs LNAs in the K-band and GaN PAs in the same band. Chapter 3 presents the process technologies, small and large-signal design methodology, stability analysis, biasing strategies and emphasising EM-aware simulation. Chapter 4, 5 and 6 reports the designs, simulated/measured results of GaAs W-band (75 - 85 GHz) driver amplifiers, a packaged GaAs K-band (17 - 22 GHz) single positive bias supply LNA and GaN K-band (17 – 22 GHz) PAs. Chapter 7 concludes with a summary of all the designs, outcomes and a roadmap for future work.

Chapter 2: Literature Review

A comprehensive literature review is presented in this chapter. It serves as a map of related works, a critical evaluation of its strengths and limitations and a review for targeting new contributions. In the context of microwave and millimeter-wave amplifiers, the literature review is also an opportunity to trace the rapid evolution of semiconductor devices, circuit topologies, and design strategies over the decades.

2.1 Overview

The primary goal of this chapter is to review the state-of-the-art in K-band and W-band MMIC amplifiers, with a specific focus on GaAs LNAs and GaN PAs relevant to 5G and SATCOM architectures. Rather than an exhaustive catalogue, this review critically analyses the achievements, limitations, and design trade-offs of directly related prior works to establish a baseline for the contributions of this thesis.

In the early 1980s and 1990s, using GaAs MESFETs established the feasibility of LNAs and PAs in the tens of gigahertz of range, although performance was limited by device gain and stability margins. The introduction of pseudomorphic high electron mobility transistors (pHEMTs) in GaAs technology and later the maturation of GaN HEMTs dramatically extended the achievable power gain and breakdown voltages, enabling practical designs at frequencies once considered infeasible for compact designs [21], [22].

The purpose of this literature review is to establish a clear and coherent understanding of the state of the art in millimetre-wave amplifier design, with particular focus on the K-band (specifically 17 - 22 GHz) and the W-band (75 - 85 GHz), identified in Chapter 1 as central to emerging 5G/6G and satellite communication systems. Although radio-frequency and microwave engineering encompass a broad spectrum of topics, the scope of this chapter is intentionally focused on the frequency ranges, semiconductor processes, design methodologies, and published works directly relevant to front-end low-noise amplifiers and power amplifiers operating within these bands. Amplifiers at these frequencies play a decisive role in determining link margin and energy efficiency in modern communication architectures. The existing literature exhibits distinct technological trajectories that invite systematic comparison and benchmarking. Furthermore, persistent challenges in packaging, stability, and long-term reliability remain unresolved and provide a direct rationale for the research advanced in this thesis.

Another important purpose of this literature review is to highlight the interconnection between academic research and commercial practice. Academic studies frequently push the boundaries of performance in highly optimized laboratory configurations, producing narrowband amplifiers with record noise figures or experimental PAs with unprecedented efficiency. Commercial offerings, by contrast, emphasize reproducibility, manufacturability and qualification under real mission constraints. By comparing these two domains, the literature review identifies where experimental insights have translated into robust commercial products and where gaps remain between laboratory promise and deployable systems. For example, while numerous academic reports describe GaAs LNAs at W-band with noise figures near 3.6 dB, commercial works still offer LNAs closer to 5–6 dB at similar frequencies. Understanding this divergence is essential when positioning the contribution of this thesis.

On the other hand, the scope of this chapter also includes methodological evolution. Amplifier design is not only about device choice but also about analytical and simulation frameworks. Classical small-signal stability analysis using Rollet’s K-factor and the μ -metric remains a foundation, but the literature increasingly demonstrates the necessity of normalized determinant function (NDF) analysis, return-ratio methods and full-wave EM simulation of components, especially above 60 GHz. Likewise, bias network design, which is long considered a peripheral detail, is now recognized as a determinant of both stability and radiation resilience. By reviewing methodological advances alongside performance benchmarks, this chapter provides a holistic view of what constitutes State of the Art.

2.2 Frequency bands of interest

Millimetre-wave communication and wireless systems have transitioned from conceptual demonstrations to operational payloads, driven by the demand for higher data transfer and efficiency. Within this evolution, the K-band and W-band represent two pivotal frequency bands for 5G transport networks and SATCOM applications, offering complementary trade-offs in propagation, bandwidth, and component maturity. K-band supports robust downlinks and uplinks with proven GaAs/GaN front-ends, while W-band extends spectral capacity for emerging inter-satellite links, synthetic-aperture radar (SAR) and atmospheric sensing. Together, they form the architectural span for the high-frequency subsystem strategy supporting this thesis [1], [2].

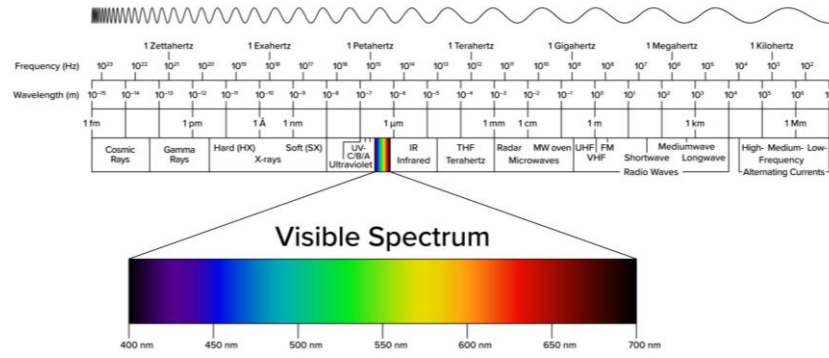


Figure 2.1: Electromagnetic spectrum.

Table 2.1 states the goal of the chapter: reviewing the state-of-the-art in K-band and W-band MMIC amplifiers, focusing on GaAs LNAs and GaN PAs relevant to 5G and SATCOM.

Table 2.1: Typical Specifications and Applications of K- and W-Bands.

Band	Frequency range	Typical applications	Typical require bandwidth	Target noise figure (LNA)
K-band	18 – 27 GHz	SATCOM downlinks, 5G backhaul, radar	~ 1 – 3 GHz	1.2 – 2.0 dB
W-band	75 – 110 GHz	Space-to-space cross-links, automotive radar, high-res imaging	~ 10 GHz	3.5 – 6.0 dB

2.2.1 Regulatory allocations and missions

The K-band allocations between 18 - 27 GHz are well established under ITU coordination for fixed satellite and mobile services. Their moderate attenuation and mature component ecosystem make them the feasible choice for high reliability SATCOM payloads supporting broadband downlink and uplink. Adaptive coding and modulation (ACM) combined with uplink power control provides resilience against rain-fade events typical of mid-latitude ground terminals [3]. Conversely, W-band (75 - 110 GHz) allocations remain under active standardisation for next-generation cross-links and high-resolution imaging radar. The 10 GHz usable window provides up to 5 times the contiguous spectrum of K-band but demands precise EM modelling and packaging co-design due to the short wavelengths involved [4], [5]. Despite the immaturity of packaging and test infrastructure, the W-band's spectral density and compact aperture size make it attractive for inter-satellite networking and fine-resolution radar imaging in future SATCOM missions [6].

2.2.2 Propagation and atmospheric effects

K-band lies between major oxygen and water-vapour absorption lines, which results in manageable gaseous attenuation. For Earth-space paths, the dominant impairment remains rain attenuation, which can exceed 10 dB/km in tropical climates. Mitigation involves diversity reception, adaptive modulation and fade margin budgeting. In contrast, W-band propagation is strongly affected by molecular absorption near 60 GHz and 118 GHz, with partial transparency between 75 - 85 GHz. For space-to-space and short-range terrestrial links, this sub-band remains practical. However, atmospheric path loss increases rapidly beyond 85 GHz [3], [4]. System link budgets must therefore incorporate gaseous absorption, surface scattering, and transition losses from on-chip to waveguide interfaces [5], [7].

Figure 2.2 introduces the comparative attenuation and system margin characteristics for K-band and W-band frequencies, which illustrates the relative advantages of each frequency domain.

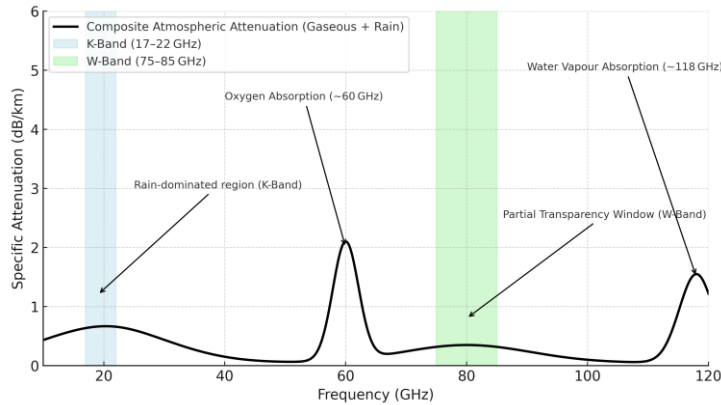


Figure 2.2: Composite Attenuation for K-band and W-Band.

2.2.3 Device technologies

The K-band benefits from decades of refinement in GaAs pHEMT and GaN HEMT MMIC processes. Recent GaAs pHEMT LNAs using 0.15 - 0.1 μm gates have achieved noise figures below 1.2 dB and gain of 20 - 25 dB at 17 - 22 GHz [9] - [12]. GaN HPAs in the same band routinely deliver 8 - 12 W saturated output power with 25 - 35% power-added efficiency (PAE) per die, extending to wideband 18 - 24.5 GHz operation with minimal gain ripple [48]. These devices exhibit excellent linearity and radiation tolerance, making them strong candidates for flight qualification. From a design perspective, stability conditioning through dual RC traps and resistive loading has proven essential to suppress low-frequency oscillations. At the module level, co-simulation of bias networks, microstrip transitions, and thermal vias ensures predictable gain and phase margin [46].

In the W-band, GaAs pHEMT technology remains the workhorse for low-noise amplification, with typical noise figures of 4.5 - 5 dB and gain above 20 dB from lower W-band [6], [7]. Recent work

from [6] demonstrated stabilised pHEMT amplifiers using network determinant functions and dual RC traps, which achieves reproducible small-signal stability without bandwidth sacrifice. Power amplification remains more challenging as GaAs PAs exhibit saturated output (P_{sat}) around 23 - 25 dBm with 20 - 25% of PAE, while emerging GaAs W-band PA [8] are approaching multi-watt outputs with enhanced thermal robustness. At these frequencies, EM-aware packaging becomes mandatory. Co-design of waveguide transitions, flip-chip interconnects and bias decoupling reduces parasitic coupling that can otherwise shift impedance trajectories by greater than 15%. Thus, W-band designs serve as both a performance frontier and a proving ground for co-integration and EM stability methods.

A quantitative comparison of GaAs, GaN, and InP technologies has been included in Table 2.2, detailing NF capabilities, power, and typical applications.

Table 2.2: Quantitative Comparison of mm-Wave Semiconductor Technologies.

Technology	NF capability (mm-wave)	Power density	Application
GaAs pHEMT	Excellent (~ 1.2 dB at K-band)	Moderate (~ 0.5 W/mm)	LNAs, driver amplifiers
GaN-on-SiC	Fair (~ 2.0 dB at K-band)	Superior ($\sim 3 - 5+$ W/mm)	High power amplifiers (HPAs)
InP HEMT	Superior (< 1 dB at K-band)	Low (< 0.3 W/mm)	Ultra-Low Noise Rx, Sub-THz

2.2.4 System-level technology considerations for 5G system and SATCOM payload architecture

At the system level, K-band provides a mature and procurement-ready foundation for both emerging 5G backhaul links and contemporary SATCOM payloads, offering a steady balance between link performance, manufacturability, and qualification cost. Its established process design kits, reliable component supply chain, and extensive flight heritage make it the practical baseline for missions that require stable downlink throughput and predictable behaviour under environmental stress. W-band, although still developing industrial maturity, aligns closely with the long-term ambitions of 5G evolution and 6G research, where enormous spectral bandwidths and finer spatial resolution are essential for ultra-high-capacity feeder links, inter-satellite connectivity, and high-resolution sensing.

Progress at these frequencies is limited primarily by the difficulty of realising robust packaging transitions at electrically minute dimensions, the requirement for high-fidelity full EM simulation to capture distributed passive result, and the incomplete radiation characterisation of GaAs and GaN devices operating deep into the millimetre-wave region. These considerations naturally motivate a staged development trajectory in which near-term implementations exploit K-band architectures built around GaAs low-noise amplifiers and GaN high-power amplifiers using qualified foundry processes and heritage module technologies; intermediate phases concentrate on advancing W-band hardware through improvements in EM-aware packaging, stability-centred LNA design, and enhanced thermal management; and longer-term visions converge toward unified front-end solutions that leverage GaN's scalability to support concurrent K-band and W-band operation with consistent calibration across both satellite and terrestrial 5G/6G infrastructures. This integrated pathway enables immediate mission readiness while steadily developing the capabilities required for future high-rate communication networks and high-resolution millimetre-wave payloads.

2.3 GaAs amplifiers

Gallium arsenide (GaAs) pseudomorphic high-electron-mobility transistor (pHEMT) technology has remained a cornerstone of millimetre-wave front-end design for more than three decades. While gallium nitride (GaN) has increasingly displaced GaAs in high-power transmit functions, GaAs continues to define the state of the art in low-noise amplification at millimetre-wave frequencies. Its sustained relevance stems from a favourite combination of high electron mobility, excellent device modelling, and a level of process maturity and reliability characterisation that remains unmatched at K-band and W-band. In these frequency ranges, GaAs processes consistently offer superior noise performance and predictable gain, making them the preferred choice for receiver front ends in communication, sensing and space systems. GaAs power amplifiers, although limited in output power density relative to GaN, still play supporting roles with moderate power, linearity and integration density are prioritised. This section reviews representative GaAs amplifier implementations across K-band and W-band, with primary emphasis on low-noise amplifiers, and examines the recurring design trade-offs that shape contemporary performance.

2.3.1 GaAs LNAs in the K-band

The K-band represents one of the most strategically important windows in satellite communications and radar front-end design. This range 17 - 22 GHz covers K-band downlink and uplink channels for broadband satellite networks, as well as portions of the spectrum allocated for defence and Earth observation radar payloads. Low noise amplifiers (LNAs) at these frequencies directly define the link margin of space systems, which makes their optimization a common goal of both academic research

and industrial product development.

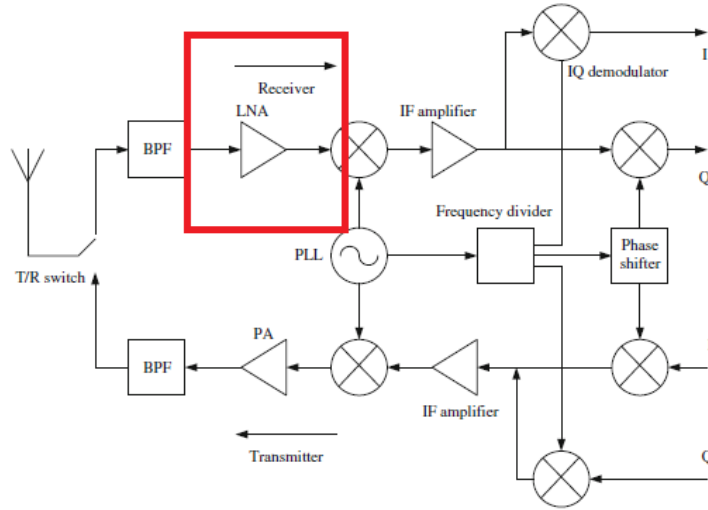


Figure 2.3: Block diagram of a transceiver system with LNA at receiver path.

The literature over the past three decades reflects a steady tightening of performance requirements in GaAs LNAs at these frequencies, with reported noise figures (NFs) declining from 3 dB in the early 1990s to around 1.2 dB in the best narrowband academic demonstrations of the 2010s. Alongside these improvements, design practices have matured to balance noise performance with gain, input/output matching, and above all, stability under process variation and packaging parasitics.

In the early 2000s, the authors in [28] presents several K-band receiver front-end circuits implemented in a 0.18- μm GaAs metamorphic HEMT (MHEMT) process incorporating a 60% indium-content InGaAs channel, demonstrating that metamorphic growth on GaAs can deliver InP-like noise and frequency performance while retaining the cost and scalability advantages of GaAs substrates. The authors report three key MMICs including a subharmonic mixer, a subharmonic down-converter and a three-stage low-noise amplifier (LNA). The integrated mixer shows a conversion loss of 14 dB with LO–IF isolation of 65 dB, and the down-converter improves this to a 3 dB conversion loss and an overall noise figure of 5 dB across 26 - 30 GHz. The LNA achieves 23 dB of gain and a noise figure below 1.57 dB at 30 GHz while consuming only 15 mW of dc power. Its measured broadband gain and noise characteristics are summarised in Figure 2.4, which illustrates the consistency of the device performance across multiple bias points. A large-sample statistical evaluation of 310 fabricated LNA dies further demonstrates an average gain of 23.45 dB, an average noise figure of 1.56 dB, and an RF yield of 84%, representing the first published statistical yield analysis of an MHEMT integrated circuit. These results position GaAs-based MHEMT technology as a strong candidate for high-performance, low-power K-band receiver front-ends.

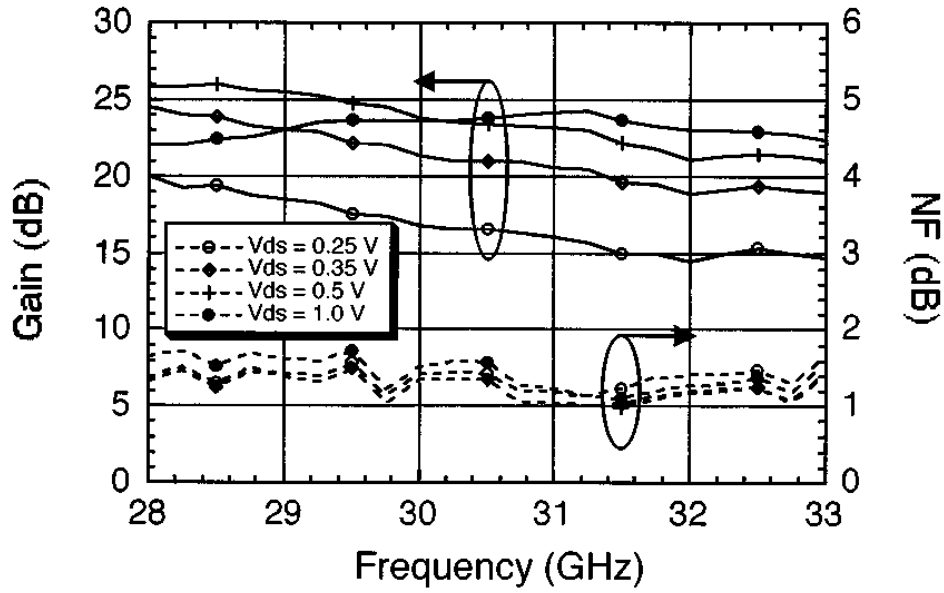


Figure 2.4: Measured gain and NF of the LNA for various dc bias points [28].

The paper [29] presents the development of a complete 24-GHz MMIC chipset that comprises a low-noise amplifier, power amplifier, and single-balanced diode mixer. The design was implemented in a 0.15- μm GaAs pHEMT process for automotive radar applications. The LNA employs two common-source stages with source-degenerative inductors to achieve simultaneous gain and noise optimisation, delivering more than 20 dB of gain from 19 - 32 GHz and an average noise figure of 3.5 dB between 20 and 26 GHz, with a minimum of 3 dB at 24.5 GHz. Its result is summarised in Figure 2.5, which shows the measured gain and noise figure across the operating band. The power amplifier, based on a two-stage topology with a 400- μm output device, provides over 20 dB of gain, output 1-dB compression levels above 20 dBm, saturated output power exceeding 23 dBm, and peak PAE beyond 32%. The mixer achieves a conversion loss better than 9 dB from 20 to 32 GHz, together with LO-to-RF and LO-to-IF isolations of more than 24 dB and 35 dB, respectively, and an IF bandwidth extending to 5 GHz.

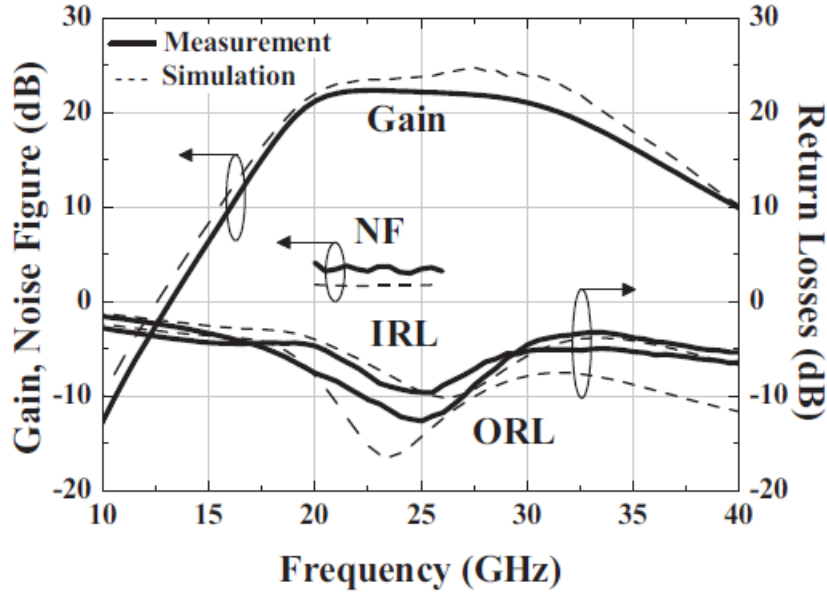


Figure 2.5: The simulated and measured small signal gain, return losses and noise figure [29].

The study in [30] reports the design and measurement of a high-gain K-band monolithic low-noise amplifier using a 0.1- μm GaAs pseudomorphic HEMT process developed for radio astronomy applications. The three-stage common-source topology employs source degeneration in the first two stages to optimise noise performance, while a shunt resistor is introduced in later stages to ensure stability despite the reduced device size. Measured results show a small-signal gain of approximately 29 dB from 18.5 to 30 GHz with a 3-dB bandwidth of 47%, achieved under a total DC power consumption of 27 mW. The LNA also demonstrates an average noise figure of 2.1 dB from 20 to 33 GHz, remaining below 3 dB from 18 to 35 GHz. The key gain and noise characteristics are summarised in Figure 2.6, which displays both the measured and simulated S-parameters and the corresponding noise figure across the operating band. A figure-of-merit of 544 GHz/mW, derived from the gain-bandwidth product, noise figure, and dc power consumption, is reported. This represents one of the highest FOM values published for K-band LNAs in GaAs technology at that time. These results confirm that a 0.1- μm GaAs pHEMT process can deliver wideband, low-noise performance suitable for highly sensitive radio astronomy receivers under stringent power constraints.

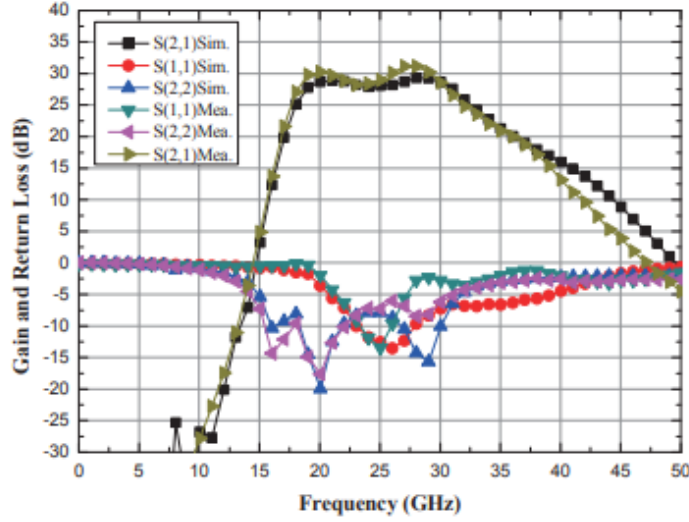


Figure 2.6: Simulate and measured S -Parameter of the K-band LNA [30].

In [31], the authors describe the development of a broadband low-noise amplifier covering 1 - 40 GHz, realised in a 0.15- μm GaAs E-mode pHEMT process and designed using multiple bandwidth-extension techniques. The work combines resistive-capacitive feedback, shunt peaking, and double series peaking within a cascode LNA cell to mitigate Miller effects and reshape the amplifier's high-frequency response, enabling wideband operation without resorting to distributed-amplifier topologies. A three-stage MMIC is fabricated with a total die area of 1.06 mm², demonstrating an average gain of 26.5 dB, input and output return loss better than 9 dB, and a noise figure between 2.8 and 3.8 dB across the entire 1 - 40 GHz band. The essential broadband gain and matching result are captured in Figure 2.7, which shows the measured and simulated S -parameters across the operating range. Linearity testing further reports OP1dB values of 4.9 - 12.7 dBm and OIP3 between 15 and 22.5 dBm, confirming robust performance under wideband excitation. A comparison with previously reported GaAs broadband LNAs indicates that this design achieves one of the widest operational bandwidths and highest gain levels in its process class, while also maintaining a compact footprint relative to distributed-amplifier implementations.

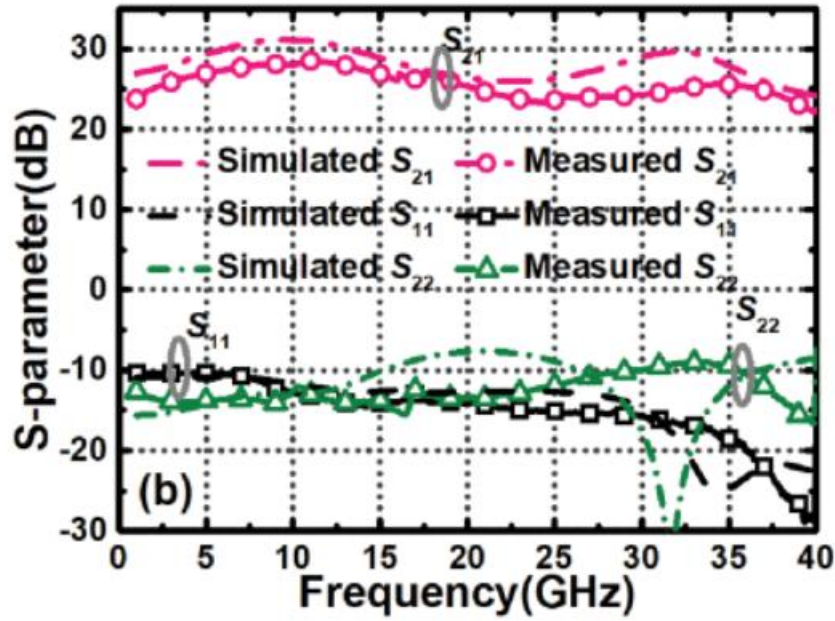


Figure 2.7: simulated and measured S -parameters of the proposed broadband LNA [31].

Table 2.3 summarises the key performance of the GaAs-based LNAs discussed above.

Table 2.3: Comparison of presented LNAs.

Ref	Technology	Frequency (GHz)	Gain (dB)	NF (dB)	Power consumption (mW)
[28]	0.18- μm GaAs MHEMT	26 - 30	23	1.57	15
[29]	0.15- μm GaAs pHEMT	20 - 32	20	3 - 3.5	N/A
[30]	0.1- μm GaAs pHEMT	18 - 35	29	2.1	27
[31]	0.15- μm GaAs E-mode pHEMT	1 - 40	26.5	2.8 - 3.8	N/A

The literature identifies several recurring design trade-offs in low-noise amplifier development. Foremost among them is the tension between achieving the minimum possible noise figure and maintaining a well-controlled input match. Noise-optimal matching typically places the source impedance away from $50\ \Omega$, which improves noise performance but compromises return loss. Paper [28] explicitly discusses this trade-off, noting that the first stage of the LNA is matched for noise rather than input reflection and that source degeneration is introduced to shift the noise-optimal impedance closer to $50\ \Omega$. This adjustment improves the practical input match while preserving most of the noise benefit, illustrating the general principle that any movement toward noise-optimal matching inevitably reduces input return loss, whereas improving return loss requires sacrificing some noise performance. This performance, observed across many GaAs and GaN designs, forms a foundational constraint that must be accounted for when targeting low-noise operation in K-band and W-band MMIC front ends.

2.3.2 GaAs LNAs in the W-band

The W-band (75 - 110 GHz) has been a proving ground for high-frequency MMIC design. Within this range, the 75 - 85 GHz sub-band is especially relevant for atmospheric sensing, security imaging radars, automotive collision-avoidance sensors, and emerging satellite cross-links. GaAs pHEMTs have consistently provided a practical balance between reproducible performance, manufacturability, and reliability. Although InP HEMTs occasionally surpass GaAs in record low noise figures, and SiGe BiCMOS demonstrates strong integration potential, GaAs remains the mainstream technology for commercial W-band LNAs because of its maturity and relatively low cost per mm² of die area.

Paper [34] reports one of the earliest high-performance demonstrations of W-band monolithic low-noise amplifiers based on pseudomorphic InGaAs/GaAs HEMT technology and establishes a design and analysis methodology that strongly influenced subsequent millimetre-wave MMIC practice. The first W-band GaAs LNAs in the early 1990s reported noise figures on the order of 5–6 dB with limited gain, reflecting both device limitations and the immaturity of distributed passive modelling at the time. Building on these early results, the authors present one- and two-stage monolithic LNAs operating near 94 GHz, achieving measured noise figures of approximately 5.1 dB for the single-stage design and 5.5 dB for the two-stage design, with corresponding gains of about 7 dB and up to 13.3 dB, respectively. These measured noise and gain characteristics are shown in Figure 2.8, which captures the core performance improvement enabled by refined device models and accurate passive representation. The paper further demonstrates the scalability of the approach by cascading four two-stage MMICs to realise an eight-stage amplifier with 49 dB of gain and a noise figure of 6.5 dB at 94 GHz. A central contribution of the work is the explicit requirement for accurate modelling and full EM simulation of passive structures at W-band, which is shown to be essential for achieving first-pass success and predictable stability. As such, the paper represents both a performance benchmark and a methodological reference for GaAs-based W-band LNA design.

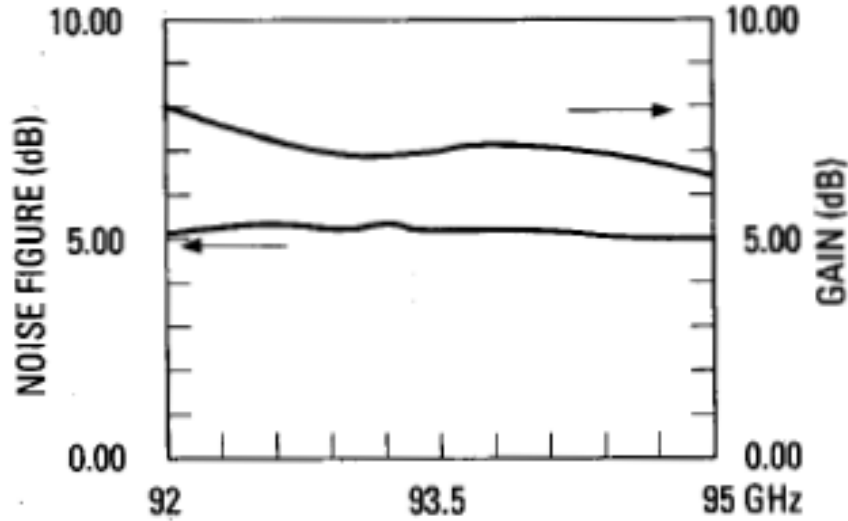


Figure 2.8: Measured noise figure and gain versus frequency of the W-band LNA around 94 GHz [34].

Developed in the mid-1990s, when W-band radiometric payloads were beginning to transition from discrete assemblies to monolithic solutions, the work in [35] addresses the implementation of GaAs-based low-noise amplifiers for spaceborne microwave remote-sensing applications. The authors describe W-band monolithic LNAs fabricated using a 0.15- μm AlGaAs/InGaAs/GaAs pseudomorphic HEMT process with passivation, targeting the Advanced Microwave Scanning Radiometer (AMSR). Emphasis is placed on achieving low noise and stable gain using reactive matching techniques informed by on-wafer S-parameter measurements up to 50 GHz and noise-parameter characterisation at 60 and 90 GHz. A two-stage MMIC demonstrates a measured noise figure of 3.4 dB and a small-signal gain of 8.7 dB at 91 GHz, results that were competitive with the best GaAs-based W-band LNAs reported at the time. These measured noise and gain characteristics are shown in Figure 2.9, where close agreement between simulation and measurement highlights the effectiveness of the adopted noise-matching methodology. To extend gain for system-level use, three two-stage chips are cascaded to form a six-stage amplifier, achieving 29.7 dB of gain with a noise figure of 4.2 dB at 91 GHz, proving the scalability of the monolithic approach.

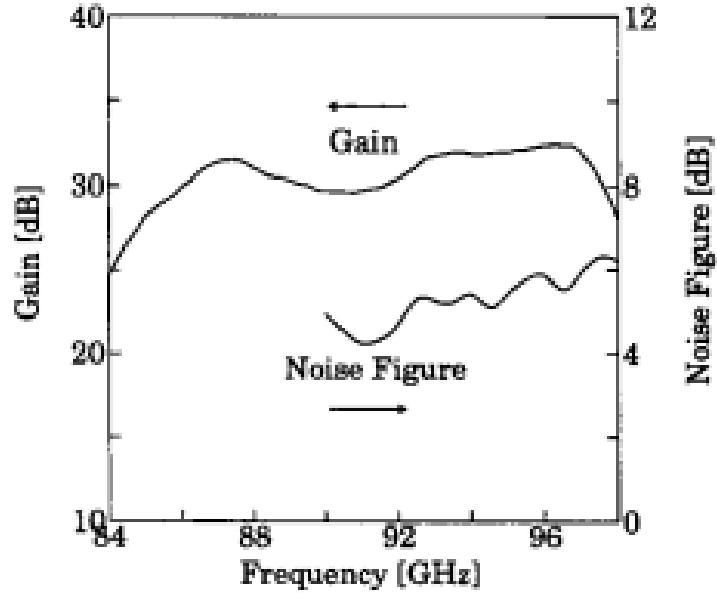


Figure 2.9: Measured noise figure and gain of the six-stage amplifier [35].

In the early 2000s, growing demand for low-noise W-band radiometer front ends stimulated interest in GaAs-based technologies capable of approaching InP-level performance while keeping higher manufacturability. The work in [36] investigates this opportunity through the design of W-band low-noise amplifiers implemented in a 70 nm metamorphic HEMT technology grown on GaAs substrates, targeting operation near 94 GHz. Two-stage and three-stage monolithic amplifiers are realised using coplanar waveguide layouts and are optimised for low-noise bias conditions suitable for passive sensing applications. On-wafer measurements demonstrate that the three-stage design achieves greater than 15 dB of gain with a minimum noise figure approaching 2.5 - 3 dB at W-band, confirming the viability of metamorphic GaAs processes for high-frequency, low-noise receivers. The primary noise and gain performance of the amplifier is shown in Figure 2.10, which captures the key outcome of the design. In summary, the study highlights the importance of accurate device modelling, bias optimisation, and distributed passive design in achieving stable and repeatable W-band performance, positioning GaAs-based MHEMT LNAs as a credible solution for large-format radiometer and sensing payloads of that era.

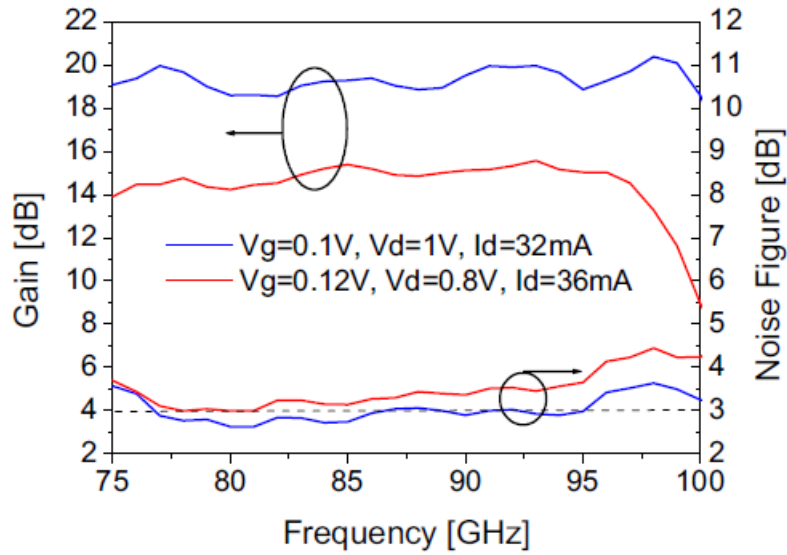


Figure 2.10: Noise-figure and gain measurement for the three-stage LNA at two different bias conditions [36].

The work in [37] investigates the use of coplanar-waveguide W-band low-noise amplifiers implemented in a 100-nm GaAs-based metamorphic HEMT technology, targeting 94 GHz cloud-profiling radar applications. Four monolithic LNAs with different bandwidth and gain–noise trade-offs are designed and fabricated, including narrowband, wideband, and noise-optimised three- and four-stage configurations. The designs employ inductive source feedback, resistive bias stabilisation, and distributed matching networks to ensure stable operation across W-band while maintaining low noise. On-wafer measurements show that the amplifiers achieve 17 - 23 dB of gain at 94 GHz with measured noise figures between 3.0 and 3.3 dB, under low supply voltage and modest bias current, demonstrating robust low-noise performance suitable for radiometric front ends. The measured noise figure and gain characteristics of the representative designs are shown in Figure 2.11, which captures the primary performance outcome of the study.

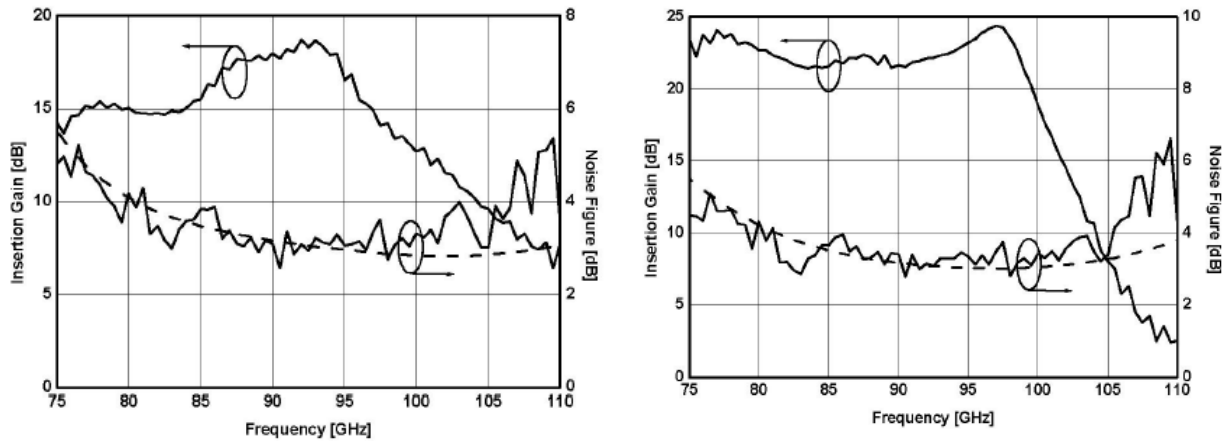


Figure 2.11: Measured noise figure and insertion gain of the narrowband LNA1 and wideband LNA2 [37].

W-band amplifier design imposes stringent constraints. At these frequencies, every discontinuity in the layout like pads, bends, vias, can behave as a resonant structure. The literature consistently emphasizes the importance of full-wave EM co-simulation of interconnects, passive structures, and packaging transitions. Without full EM simulation, measured S-parameters often deviate significantly from simulations. Input matching is especially critical. Achieving $NF < 6$ dB at this high frequency requires precise noise matching at the input transistor, which may conflict with input return loss requirements. Designers frequently employ inductive source degeneration combined with series capacitors to balance NF and input VSWR. Multi-stage cascades of 3 - 4 stages are typical, with careful distribution of gain to avoid overloading later stages. Stability is an importantly critical concern. The literature describes instances of oscillations at half-band (40 - 50 GHz) and at out-of-band resonances in the 120 - 150 GHz range. To counter this, designers introduce resistive loading at high-impedance nodes, RC traps in bias networks, and strategic gate resistors. These stability measures typically add 0.1 - 0.2 dB to NF per stage but are indispensable for reliable operation.

Academic prototypes often achieve best-in-class noise figures under controlled conditions. However, commercial catalogues remain more conservative. The gap between academic NF records (around 3 dB) and commercial products (around 5.5 - 6 dB) reflects multiple factors, which are packaging compensation, variability across wafer lots, and qualification under radiation and thermal stress.

Packaging is a decisive factor at W-band. Bond wires act as inductors with self-resonances in the 80–100 GHz range. Launch transitions from waveguide or coax to microstrip can introduce 0.5–1 dB of additional NF if not carefully designed. The literature increasingly reports co-simulation of these transitions alongside active devices. For example, Lee et al. [36] demonstrated a W-band LNA where inclusion of bond-wire and coaxial launch in the EM simulation reduced prediction error from ~ 1 dB to < 0.2 dB across the band. Radiation testing at W-band is less frequently reported, but limited data suggest that GaAs devices exhibit moderate TID resilience. NF increases of 0.3 - 0.5 dB after 100 krad exposure have been received [37]. Commercial parts are seen to mitigate these effects, while academic reports seldom address them.

Table 2.4 illustrates the representative GaAs W-band low noise amplifiers.

Table 2.4: Comparison of the discussed GaAs W-band LNAs.

Ref	Technology	Frequency (GHz)	Gain (dB)	NF (dB)
[34]	InGaAs pHEMT on InP	95	20	2.5 - 3
[35]	0.15 μm AlGaAs/InGaAs/GaAs pHEMT	91	8.7/29.7	3.4/4.2
[36]	70 nm metamorphic HEMT on GaAs	94	13	3
[37]	100 nm metamorphic HEMT on GaAs	94	17 – 23	3 – 3.3

The overall trajectory of GaAs LNAs in the W-band can be summarized as a steady reduction of NF from 5 to 6 dB in the early 1990s to 2 to 3 dB in modern designs, with academic records pushing down to around 2 dB in narrowband cases. Gain has increased from 5 dB to over 20 dB, with bandwidths of 8 to 10 GHz becoming more frequent.

2.3.3 GaAs PAs in K-band

Power amplifiers (PAs) play a critical role in determining the output capability, efficiency, and linearity of RF and millimeter-wave systems. While LNAs define system sensitivity, PAs determine the ability of the transmitter to deliver high-power signals with acceptable spectral purity and efficiency. The main performance requirements of interest are output power (P_{out}), power-added efficiency (PAE), linearity (measured through adjacent channel power ratio, ACPR, or error vector magnitude, EVM), and reliability under mismatch and thermal stress.

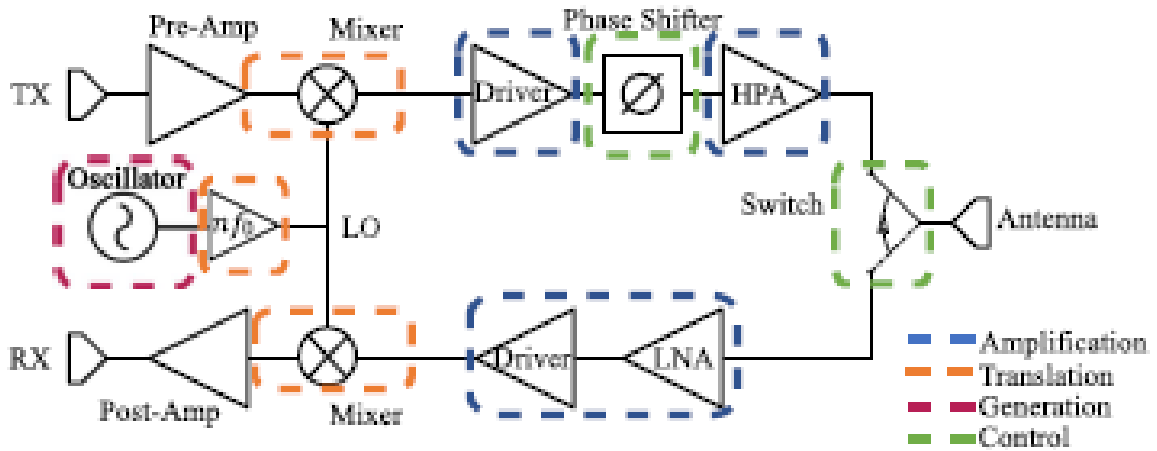


Figure 2.12: Block diagram of a transceiver system with highlighted PA.

Historically, GaAs MESFETs and HEMTs dominated PA design for satellite communications, wireless infrastructure, and radar, offering reproducibility and excellent linearity. In the past two decades, GaN HEMTs have revolutionized PA design by enabling high power density, ruggedness under high voltage standing-wave ratio (VSWR) and operation at mm-Wave frequencies. Today, GaAs and GaN define the state of the art in PAs, with complementary strengths where GaAs offers superior linearity and reproducibility, while GaN offers unparalleled power handling and efficiency. GaAs PAs remain relevant in satellite ground terminals and wireless infrastructure, where high linearity and reproducibility are valued more than ultimate output power density.

In [58], a K-band Doherty power amplifier was presented in which the conventional fixed load-modulation conditions were replaced by a load-pull-based selection of the optimum main-device back-off impedance, from which the required main-to-peaking current ratio and impedance-inverter parameters were consistently derived. It was demonstrated that, due to millimeter-wave device nonidealities, the efficiency-optimum back-off load deviates from $2R_{opt}$, and that enforcing this empirically extracted impedance enables alignment of main-device compression with peaking-device turn-on at the desired back-off level [58]. Figure 2.13 presents the measured PAE versus output power back-off, showing a peak PAE of 38% and a maintained PAE of 32% at 6-dB back-off, thereby confirming the effectiveness of the proposed modified load-modulation scheme.

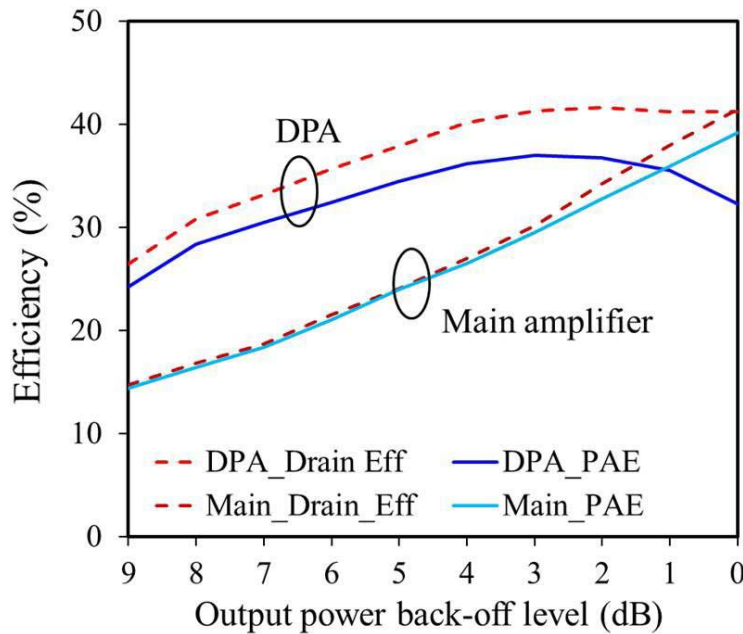


Figure 2.13: Comparison of measured drain efficiency and PAE of the DPA and single main amplifier at 29.5 GHz [58].

Rather than changing the conventional load-modulation mechanism, the contribution of [59] lay in a systematic architectural and matching network co-design that enhanced overall gain while preserving Doherty back-off efficiency, enabling operation over a 10% fractional bandwidth around 24 GHz. The fabricated amplifier delivered 30.9 dBm output power with 38% peak PAE and 20% PAE at 6-dB output power back-off under continuous-wave operation, showing the viability of GaAs-based Doherty solutions at K-band for microwave backhaul systems. Figure 2.14 presents the measured PAE versus output power at 24 GHz, showing the achieved peak efficiency and sustained back-off efficiency that constitute the principal experimental result of the paper.

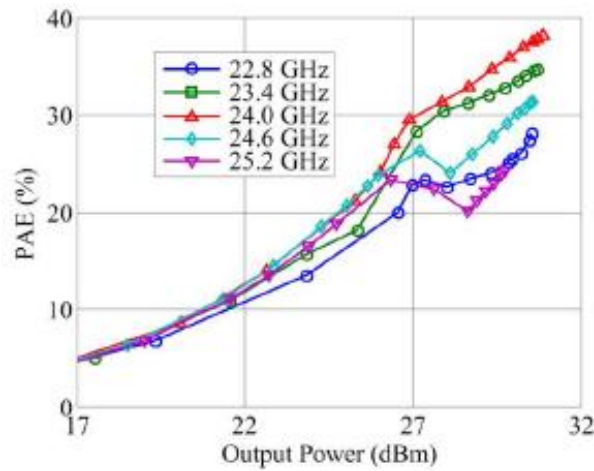


Figure 2.14: Gain and PAE versus output power at BIAS#1 in the 22.8–25.2-GHz band [59].

Similarly, in [60], a compact 20 - 30 GHz GaAs pHEMT differential power amplifier was presented in which broadband operation was enabled by a coupled-line-based magnetically and capacitively coupled resonator (MCCR) matching network that integrates impedance transformation, power combining, and DC biasing within a fourth-order structure. It was shown that, by avoiding conventional feedback or distributed architectures, wideband gain could be maintained while significantly reducing chip area, thereby addressing a key limitation of broadband millimeter-wave GaAs power amplifiers. The fabricated MMIC achieved a measured saturated output power of 23 dBm with a peak PAE of 19.4% at 26 GHz, while sustaining more than 19 dB gain across the entire 20–30 GHz frequency range. Figure 2.15 presents the measured power gain, output power and PAE versus input power at 26 GHz, demonstrating the large-signal performance and efficiency that confirm the proposed MCCR-based matching technique.

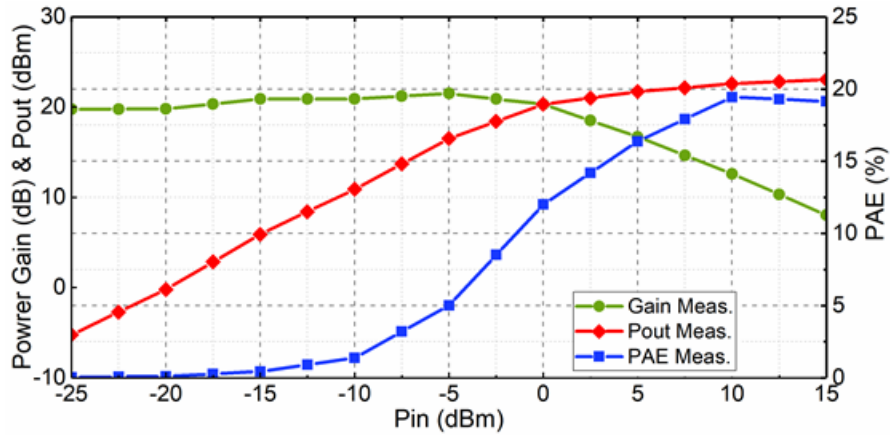


Figure 2.15: Measured power gain, P_{out} and PAE vs. P_{in} at 26 GHz [60].

The work in [71] proposed an 18 - 23 GHz GaAs pHEMT MMIC power amplifier for satellite downlink applications in which the matching networks were synthesized using an approximate optimal impedance region (AOIR) framework rather than conventional point-target impedance matching. Through the formulation of multiple mathematical constraints on the reflection-coefficient trajectories, the AOIR method enabled automated topology selection in CAD while simultaneously accounting for efficiency, output power, mismatch, and insertion loss, thereby allowing a more balanced utilization of device capabilities. When applied to a three-stage architecture, the resulting MMIC achieved an average P_{1dB} of 27 dBm and an average PAE of 38% across 18 - 23 GHz, with a peak efficiency approaching 40% and a gain exceeding 27 dB over the band. In Figure 2.16, the measured P_{1dB} and PAE versus frequency are reported.

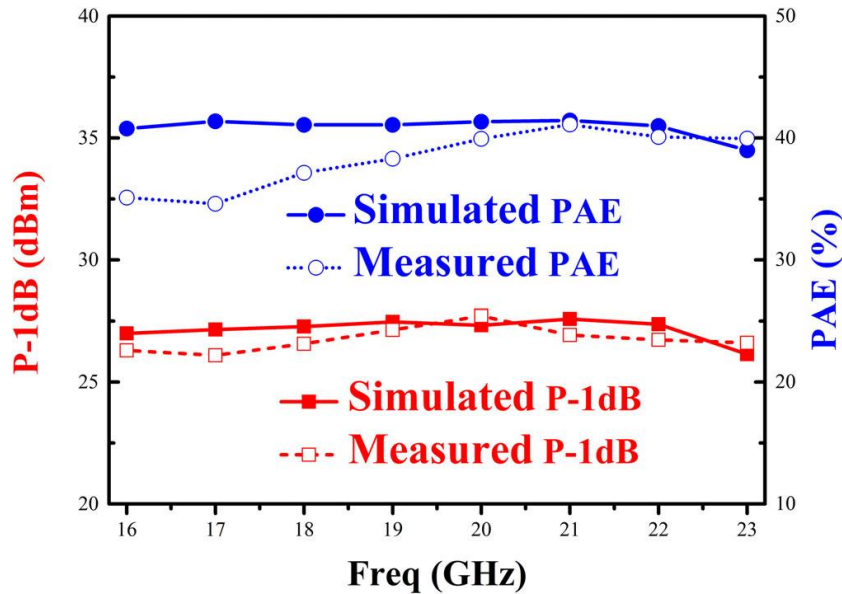


Figure 2.16: Measured P_{1dB} and PAE vs frequency [71].

A watt-level K-band Doherty power amplifier was demonstrated in the work reported in [72], where broadband operation was enabled by an integrated output combiner that explicitly embeds the intrinsic drain capacitances of the GaAs pHEMT devices rather than resonating them out. By adopting a semi-lumped wideband Doherty combiner and symmetric driver architectures for the main and auxiliary paths, a 6-dB back-off DPA was realized that simultaneously addresses the conflicting requirements of bandwidth, efficiency and output power in GaAs technology. The fabricated MMIC achieved measured saturated output power between 29.5 and 30.2 dBm across the 21 - 25 GHz band, with a corresponding PAE exceeding 30%, while keeping more than 19% PAE and over 10 dB gain at 6-dB output power back-off. The measured continuous-wave output power and PAE versus frequency are reported in Figure 2.17, by which the record 4-GHz bandwidth and sustained back-off efficiency of the proposed integrated Doherty architecture are experimentally validated.

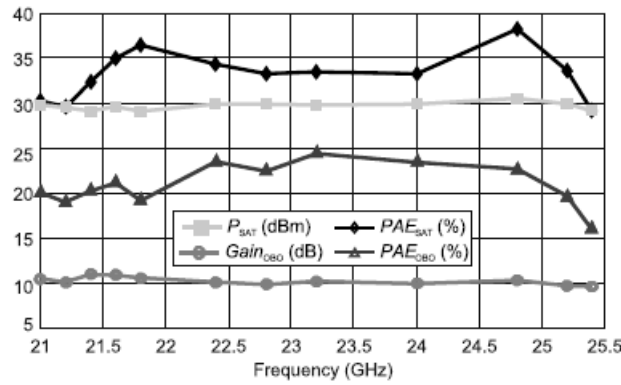


Figure 2.17: Measured CW performance versus frequency [72].

Recent works have also highlighted the linearization potential of GaAs. A high efficiency K-band MMIC linear power amplifier was reported in the authors' work [61], in which linearity enhancement was achieved through an internal diode compensation technique rather than through architectural solutions such as Doherty or feedback-based linearization. By introducing a parallel Schottky diode at the gate-drain node of the output-stage pHEMT, the nonlinear variation of the effective input capacitance with drive level was compensated, thereby mitigating AM/AM and AM/PM distortion while incurring negligible additional power loss. Implemented in a 0.15- μm GaAs pHEMT process, the three-stage amplifier achieved more than 30 dBm output power with 33 - 35% PAE at the 1-dB compression point over 20 - 22 GHz, while maintaining an IMD3 better than -20 dBc at 27 dBm per carrier. Figure 2.18 shows the measured output power and PAE at the 1-dB compression point are reported.

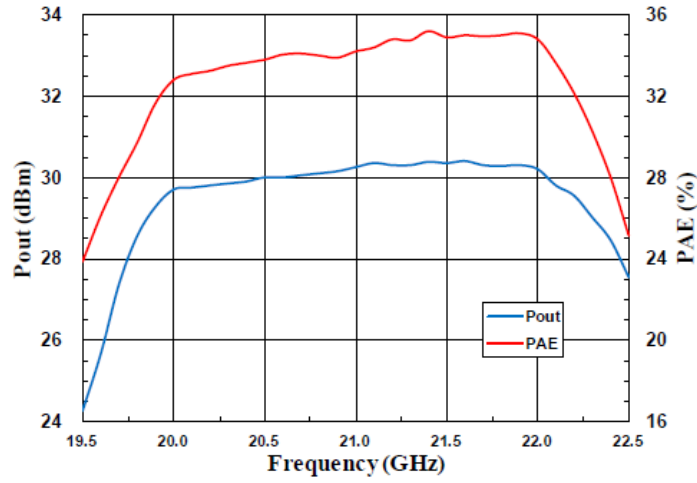


Figure 2.18: Measured output power and PAE at 1 dB compression [61].

Moreover, A symmetrical 28-GHz Doherty power amplifier based on stacked-FET unit cells was investigated in [62], where the limitations imposed by low breakdown voltage in GaAs technology were alleviated through vertical transistor stacking rather than device scaling or architectural asymmetry. Proper Doherty load modulation in the stacked-FET configuration was enabled by the joint optimization of the common-gate transistor capacitance and stack gate bias voltage, by which the voltage swings of both upper and lower devices were restored over the 6-dB power back-off range while preserving gain flatness. In addition, a dual-driver topology and a dedicated gate-bias circuit were employed to enhance overall gain and mitigate gate-leakage-induced efficiency degradation in an enhancement-mode process. The fabricated MMIC achieved a measured output power of 28.7 dBm with a peak PAE of 37% and 27% PAE at 6-dB back-off at 28 GHz. In Figure 2.19, the measured PAE and gain versus output power are reported.

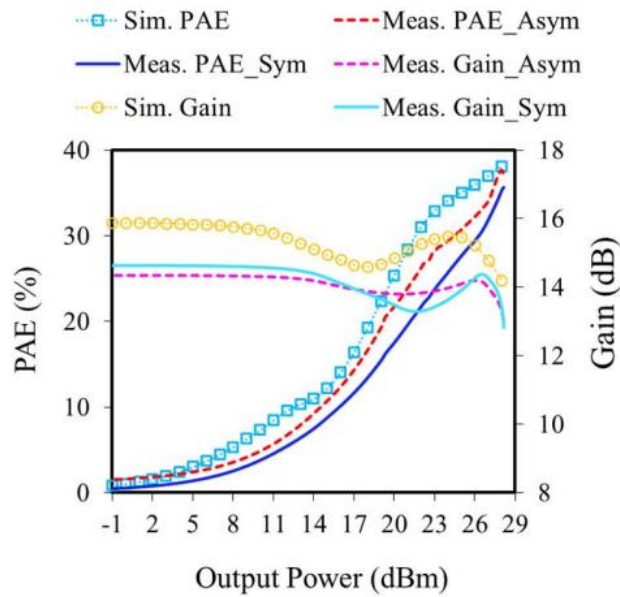


Figure 2.19: Measured at two different bias conditions and simulated PAE and gain at 28 GHz [62].

Table 2.5 presents the comparison of the explored GaAs K-band power amplifiers.

Table 2.5: Comparison of the GaAs K-band PAs.

Ref	Architecture	Frequency (GHz)	P _{out} (dBm)	PAE (%)	Back-off/Linearity
[58]	Doherty PA with load-pull-based modified load modulation	30	26 – 27	38	32% PAE @ 6-dB PBO
[59]	Doherty PA with optimized dual drivers	24	30.9	38	20% PAE @ 6-dB PBO
[60]	Differential PA with coupled-line MCCR broadband matching	20 – 30	23	19.4	Broadband CW operation
[71]	Single-ended PA using AOIR matching methodology	18 – 23	27	40	Broadband efficiency
[72]	Integrated Doherty PA with wideband combiner	21 – 25	29.5 – 30.2	30	>19% PAE @ 6-dB PBO
[61]	Linear PA with diode compensation	20 – 22	30	33 – 35	Improved IMD3
[62]	Symmetrical stacked-FET Doherty PA with dual drivers	28	28.7	37	27% PAE @ 6-dB PBO

Overall, the results show that the design of K-band GaAs power amplifiers has evolved along several complementary paths, each responding to practical limitations met at millimeter-wave frequencies. Doherty architectures continue to play a significant role when high efficiency at power back-off is required, with recent designs carefully refining load modulation, driver configuration, output combining, and device stacking to balance efficiency, gain, bandwidth, and achievable output power. At the same time, broadband single-ended amplifiers prove that, through more sophisticated matching strategies, wideband and efficient K-band operation can be realized without the additional complexity of Doherty operation, albeit without inherent back-off efficiency benefits. Approaches that prioritize linearity further illustrate that efficiency can also be supported through device-level compensation techniques, offering an alternative when stringent spectral requirements dominate. Overall, these works make it clear that there is no single dominant solution for K-band GaAs power amplifiers; instead, the most suitable architecture depends strongly on system-level priorities, motivating continued exploration of tailored and hybrid design strategies.

2.3.4 GaAs PAs in W-band

Gallium arsenide (GaAs) power amplifiers continue to be an important enabling technology for W-band (75 - 110 GHz) systems, where a combination of high-frequency performance, process maturity and predictable large-signal performance is needed. GaAs pHEMT-based MMIC power amplifiers have proved sufficient output power, gain, and efficiency to support demanding millimeter-wave applications, including high-resolution automotive and imaging radar, passive and active radiometers, point-to-point wireless backhaul, and emerging space and remote-sensing payloads. In these systems, W-band operation offers wide available bandwidth and improved spatial resolution, while GaAs technology provides a practical trade-off between performance, reliability, and development risk compared with more aggressive compound semiconductor alternatives. As a result, GaAs remains a relevant and widely used platform for W-band power amplifier implementations.

The first reported monolithic GaAs power amplifier operating in the W-band was presented in [121], establishing an early reference point for millimeter-wave PA integration. In this work, a three-stage MMIC power amplifier was implemented using a 0.1- μm AlGaAs/InGaAs/GaAs pseudomorphic HEMT process on a 50- μm GaAs substrate, with the design targeting broadband medium-power operation rather than narrowband peak output. Progressive scaling of transistor periphery across the amplifier stages was adopted to manage compression behaviour, while grounded coplanar waveguide interconnects and distributed power-combining networks were employed to enhance stability and simplify biasing, as shown in Figure 2.20. Experimental results demonstrated output power exceeding 100 mW over the 75 - 93 GHz frequency range with approximately 11 dB of large-signal gain, confirming the feasibility of GaAs technology for W-band MMIC power amplification. Although the reported efficiency was limited, the design emphasized robustness, broadband coverage, and unconditional stability, reflecting the primary challenges at the time. As the earliest GaAs-based W-band MMIC power amplifier reported in the open literature, this work provided a foundational benchmark that guided subsequent developments in GaAs W-band PA design.

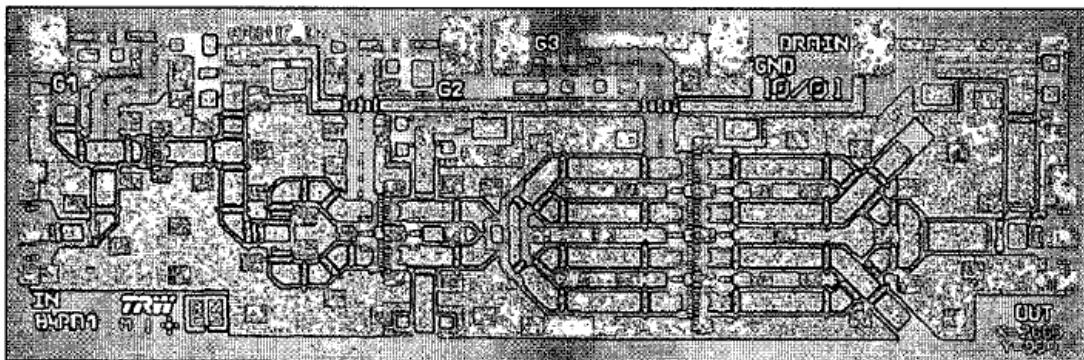


Figure 2.20: Photograph of the MMIC PA. Circuit dimensions are 2.6 x 0.84 mm. GaAs substrate is 50 μm thick [121].

Following the initial demonstrations of GaAs-based W-band power amplifier, a significant advance in achievable output power was reported in [122], where a monolithic GaAs MMIC power amplifier showed half-watt-class performance above 90 GHz. The design targeted high-gain, high-power operation and employed a multi-stage architecture consisting of dedicated driver stages followed by three successive power stages, implemented in a 0.1- μm GaAs pHEMT process. To ensure reliable operation at W-band frequencies, an unconditionally stable unit-cell concept was adopted and combined with compact matching networks, enabling aggressive power scaling without compromising stability. An efficient eight-way output power combiner was realized to present each device with an impedance close to the optimal load condition. Figure 2.21 illustrates the measured results showed saturated output power exceeding 26 dBm across 93 - 102 GHz, with a peak output power of 27.3 dBm and approximately 12% power-added efficiency, confirming the effectiveness of the proposed topology. This work established a new performance reference for GaAs W-band MMIC power amplifiers and demonstrated that GaAs technology could deliver watt-level output power at millimeter-wave frequencies while maintaining high gain and broadband operation.

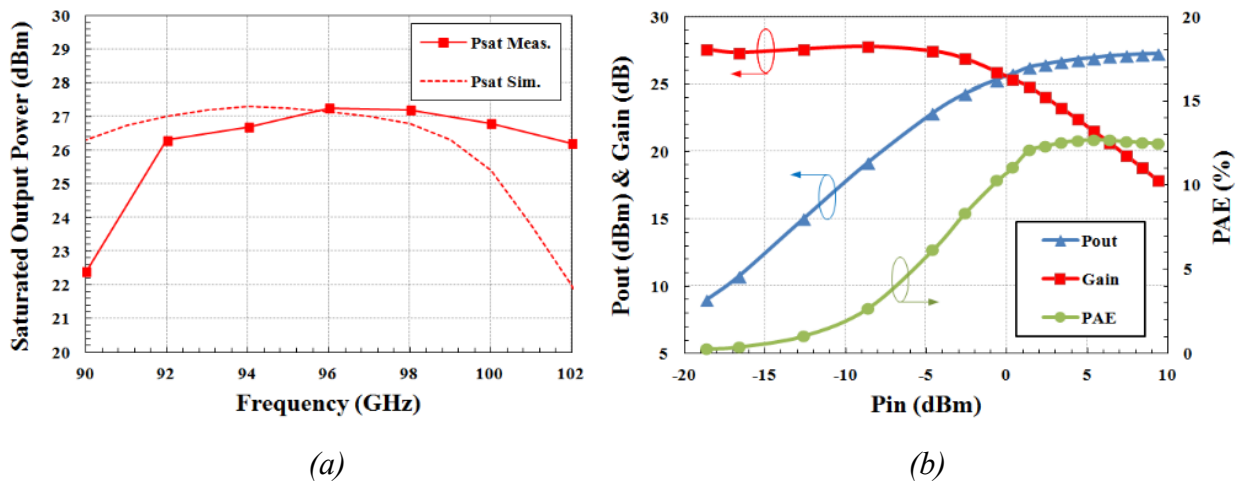


Figure 2.21: (a): Saturated power measured vs. simulated results across the band, (b) Measured PAE, Psat and gain at 96 GHz [122].

A further step toward practical and scalable GaAs W-band power amplification was reported in [123], where a family of compact MMIC power amplifiers was demonstrated using a commercially available 0.1- μm GaAs pHEMT process. Rather than pursuing maximum output power alone, this work emphasized die-size reduction, manufacturability, and modularity, addressing key constraints for cost-sensitive millimeter-wave systems. Multiple amplifier variants were realized, including driver, medium-power, and higher-power designs, all derived from a common compact building block and optimized for broadband operation across the 80 - 100 GHz range. Efficient matching networks and careful layout optimization enabled saturated output power up to 24.5 dBm with more than 12 dB gain, while maintaining relatively small chip areas suitable for integration and parallelization. The

compact MMICs, shown in Figure 2.22, highlighted how GaAs technology could simultaneously achieve competitive W-band performance and reduced footprint using a mature commercial process. This work demonstrated that GaAs W-band power amplifiers could be optimized not only for performance but also for cost, scalability, and practical deployment.

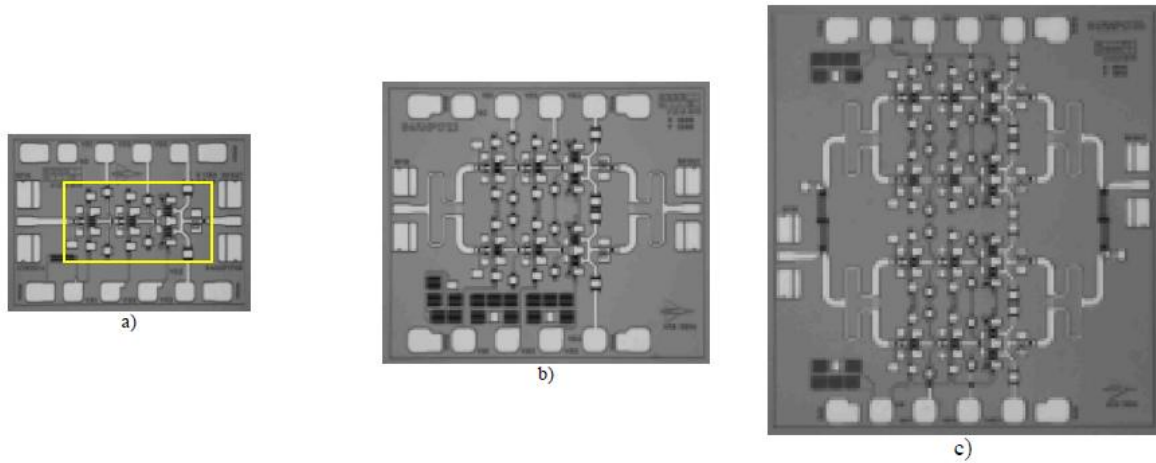


Figure 2.22: Microphotographs of the driver amplifier (a) with core amplifier (inset), (b) medium power amplifier, and (c) higher power amplifier MMICs [123].

The authors in [124] introduced a balanced GaAs W-band power amplifier architecture, addressing the need for improved impedance matching, bandwidth, and stability in millimeter-wave MMIC power amplifiers. The design employed a four-stage topology implemented in a commercially available 0.1- μm GaAs pHEMT process, where on-chip Lange couplers were used at both the input and output to realize a fully balanced configuration. This approach enabled simultaneous power combining and enhancement of input and output return losses, while also mitigating odd-mode oscillations commonly encountered at W-band frequencies. Measured results demonstrated an average saturated output power of approximately 21.5 dBm across 84 - 100 GHz with a peak value of 22.3 dBm, accompanied by an average small-signal gain of 15 dB and return losses better than 10 dB over the full operating band. Figure 2.23 shows the measured saturated output power, highlights the broadband and stable result enabled by the balanced topology.

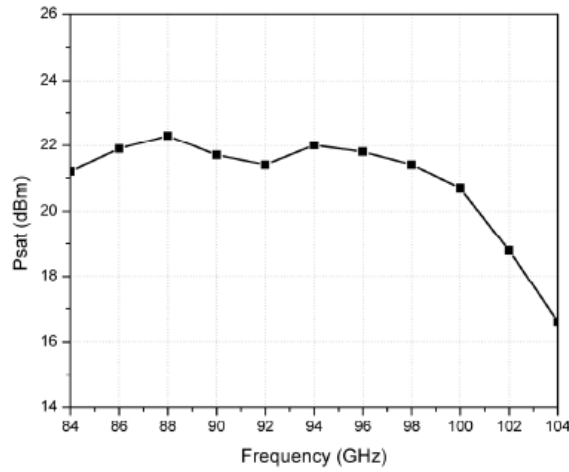


Figure 2.23: Measured saturated output power versus frequency for the power amplifier MMIC [124].

Another balanced GaAs MMIC power amplifier targeting the upper part of the W-band was presented in [125], addressing the growing demand for high-gain millimeter-wave backhaul transmitters operating above 100 GHz. The design employed a three-stage balanced architecture implemented in a commercial 0.1- μm GaAs pHEMT process, where Lange couplers were used for both input power splitting and output power combining to achieve wideband impedance matching and robust stability. By carefully optimizing low-loss matching networks and exploiting high per-stage gain, the amplifier achieved saturated output power between 20.3 and 24.1 dBm across the 100–114 GHz band, together with peak power-added efficiency approaching 12%. In addition to competitive output power, the amplifier showed an unusually high overall gain of up to 18.2 dB with only three amplification stages, highlighting the effectiveness of the balanced topology and matching strategy. The measured broadband power performance, shown in Figure 2.24, confirms that GaAs technology remains a viable and efficient solution for high-frequency W-band power amplification in practical communication systems.

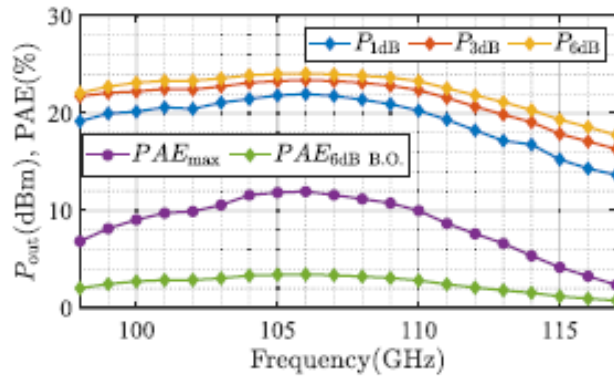


Figure 2.24: Output compression points and PAE versus operating frequency [125].

Table 2.6 presents the comparison of the discussed 0.1- μm GaAs W-band pHEMT PA designs.

Table 2.6: Comparison of Representative GaAs W-Band Power Amplifiers.

Ref	Architecture	Frequency (GHz)	P _{out} (dBm)	Gain (dB)	PAE (%)	Chip area (mm ²)
[121]	Single-ended, 3-stage	75 – 93	26 – 27	11	N/A	2
[122]	Multi-stage with 8-way combiner	93 – 102	30.9	27	12	5.5
[123]	Modular single-ended (driver/MPA/PA)	80 – 100	23	12	N/A	3.5
[124]	Fully balanced with Lange couplers	84 – 100	27	15	N/A	4
[125]	3-stage fully balanced	100 – 114	29.5 – 30.2	15.2 – 18.2	5.3 – 11.9	8.2

The progression of GaAs W-band power amplifiers from the earliest monolithic demonstrations to recent high-gain and broadband implementations highlights the continued relevance of GaAs technology at millimeter-wave frequencies. Early work established the feasibility of W-band MMIC power amplification, while next designs introduced effective power-combining, balanced architectures, and compact layouts that significantly improved output power, bandwidth, and robustness. More recent efforts have demonstrated that, even beyond 100 GHz, GaAs pHEMT processes can deliver competitive gain, efficiency, and stable operation using commercially available technologies. Collectively, these developments show that GaAs remains a practical and mature platform for W-band power amplifiers, particularly in applications requiring a balance between performance, cost, and design reliability.

2.4 GaN amplifiers

Gallium nitride (GaN) has emerged over the past three decades as the premier semiconductor technology for high-power and high-frequency electronics. Unlike Gallium Arsenide (GaAs), which has matured primarily as a low-noise technology for LNAs, GaN is most strongly associated with high power density, high breakdown voltage, and thermal resilience. The road map of GaN's development has been shaped by improvements in epitaxial growth, substrate technology and device fabrication, each of which has incrementally addressed the early barriers to performance and reliability.

2.4.1 GaN LNAs in K-band

GaN low noise amplifiers (LNAs) have emerged as a robust alternative for K-band receiver front ends, where a combination of low noise figure, high gain and strong input power handling is required. Although GaAs technologies traditionally offer superior noise performance, GaN LNAs offer their high breakdown voltage and excellent thermal conductivity to achieve enhanced linearity, large-signal tolerance and improved survivability under high-power or interference-rich operating conditions. In K-band applications such as satellite communications, radar receivers, and sensing systems, these characteristics allow GaN LNAs to operate reliably without external limiters or complex protection circuitry, while still providing competitive gain and acceptable noise performance. As device scaling and modelling accuracy continue to advance, GaN LNAs are increasingly considered as a promising solution for K-band systems that prioritize robustness and long-term reliability alongside low-noise operation.

For early GaN LNA in K-band, a highly rugged GaN low-noise amplifier operating in the upper K-band was reported in [126], representing one of the earliest demonstrations of GaN LNAs at millimeter-wave frequencies. The work targeted receiver front ends required to withstand extreme input power levels, such as satellite communication and radar systems, where survivability is as critical as noise performance. Monolithically integrated three- and four-stage LNAs were implemented using an AlGaIn/GaN HEMT process on SiC substrates, achieving measured noise figures between 3.7 and 3.9 dB across the 27 - 31 GHz band without active cooling. A distinguishing feature of this study was the rigorous robustness evaluation, in which the LNA input was stressed with continuous-wave power levels up to 33 dBm for extended durations, followed by post-stress noise measurements to verify the absence of performance degradation. The measured noise figure before and after high-power stressing, shown in Figure 2.25, shows the exceptional survivability of the GaN technology while keeping stable low-noise operation. This work set up a critical benchmark for GaN-based K-band LNAs and motivated later research into robust receiver front ends capable of operating in high-interference or transmit–receive environments.

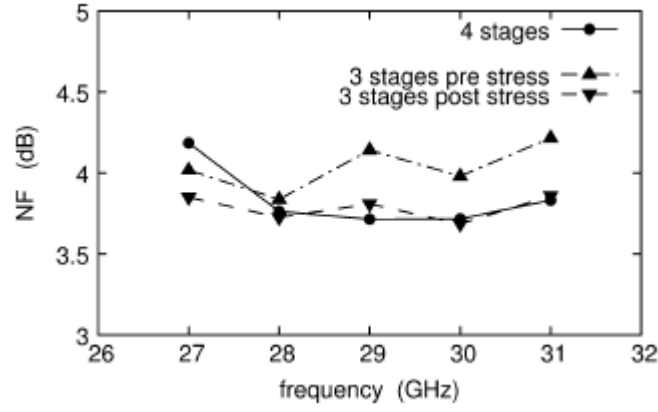


Figure 2.25: Measured noise figure (NF) of four-stage LNA [126].

Exceptionally low noise performance in a GaN-based K-band LNA was demonstrated in [127], challenging the conventional view that GaN technology is inherently noise-limited at millimeter-wave frequencies. The reported three-stage MMIC, fabricated using a 0.1- μm GaN-on-silicon HEMT process, achieved a measured noise figure between 0.4 and 1.1 dB over the 22 - 30 GHz band while maintaining small-signal gain in excess of 19 dB. Rather than relying solely on device scaling, the design emphasized accurate noise modelling, optimized input matching, and controlled source degeneration to simultaneously approach minimum noise and conjugate matching conditions. In addition to its low-noise characteristics, the amplifier exhibited strong linearity and robustness, with an output-referred 1-dB compression point above 20 dBm and verified survivability under a 30-dBm continuous-wave input stress. The measured noise figure before and after high-power stressing, shown in Figure 2.26, provides clear evidence that ultra-low noise operation and high input power tolerance can be achieved concurrently in GaN LNAs.

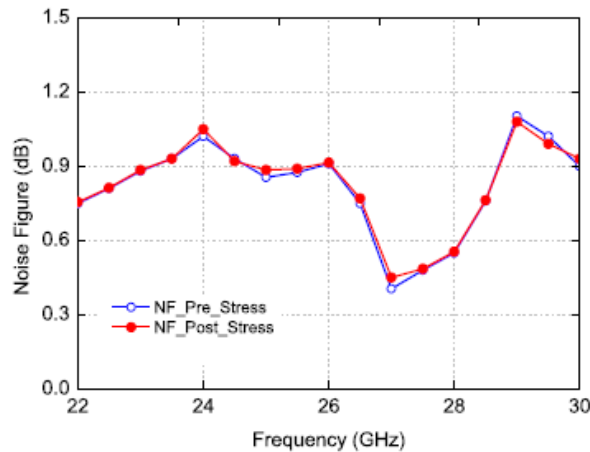


Figure 2.26: Measured NF before and after stress [127].

The work reported in [128] addressed the combined challenges of wideband operation, gain flatness, and long-term survivability in GaN K-band low-noise amplifiers. The presented MMIC LNA was implemented in a 100-nm GaN-on-silicon HEMT process and achieved a flat small-signal gain of 21 ± 0.5 dB across the 18 - 31 GHz frequency range, accompanied by a minimum measured noise figure of 0.8 dB. A simplified input matching strategy was adopted, in which an RC network placed in the drain path was used to improve return loss and bandwidth while minimizing additional noise contribution. Robustness was treated as a primary design objective, with the LNA demonstrating continuous survivability under 28–30 dBm input power stress for up to 60 minutes without significant degradation in gain or noise figure. The post-stress RF performance, shown in Figure 2.27, highlights the ability of the GaN LNA to maintain stable low-noise operation under prolonged high-power excitation.

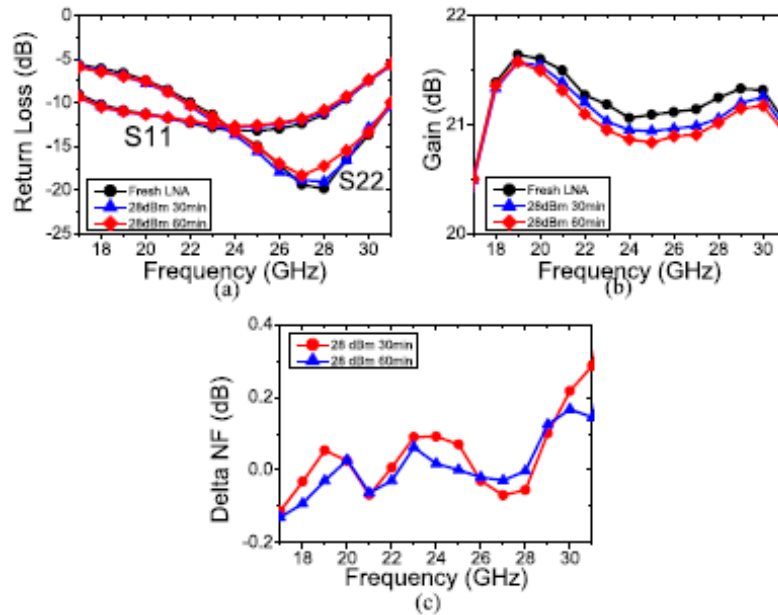


Figure 2.27: Performance of the LNA after the stress, (a) return loss, (b) gain, and (c) changes in the NF [128].

System-level integration considerations were placed at the center of the GaN LNA reported in [129], which targeted K-band receiver front ends for frequency-modulated continuous-wave (FMCW) MIMO radar applications. The two-stage MMIC was fabricated using a 100-nm GaN-on-silicon HEMT process and refined for low and flat noise performance rather than extreme robustness or record-low minimum noise figure. Across the 18 - 22.5 GHz band, the amplifier achieved a measured noise figure between 2.0 and 2.3 dB together with an average small-signal gain of 17.2 dB, providing sufficient sensitivity for multi-antenna radar receivers. Design emphasis was placed on practical noise matching and stability control, including the use of a π -type interstage matching network and an RC-based damping filter to suppress potential oscillations. The measured noise figure, shown in Figure 2.28, confirm stable and repeatable low-noise operation over the targeted K-band range.

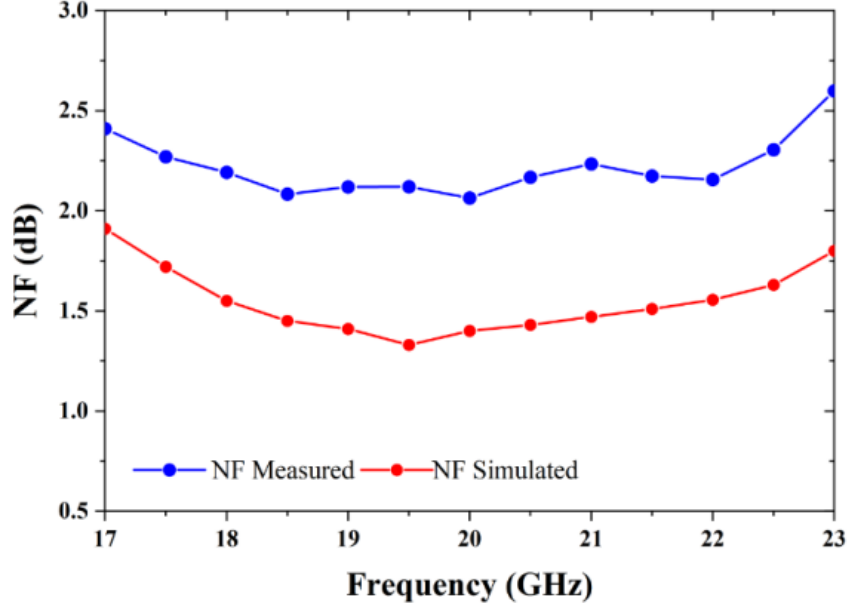


Figure 2.28: Simulated and measured NF [129].

To overcome the gain - stability trade-off that becomes pronounced near the transistor cutoff frequency, the GaN LNA reported in [130] introduced a drain-to-source coupling feedback technique tailored for broadband K-band operation. Implemented in a 0.15- μm GaN-on-SiC process, the four-stage common-source MMIC employed electromagnetically coupled transmission lines between the drain and source paths to partially neutralize the gate-drain capacitance and suppress reverse signal coupling. This feedback mechanism enhanced forward gain while maintaining unconditional stability without incurring a significant noise penalty. In addition, a wideband interstage matching strategy based on a TL-C-TL π -type network was adopted to extend the usable bandwidth without the excessive loss associated with higher-order matching networks. Measured results showed a 3-dB bandwidth from 23.6 to 29.8 GHz, a peak small-signal gain of 23.7 dB, and a minimum noise figure of 2.2 dB, together with an output-referred 1-dB compression point of 13 dBm. The measured noise figure and gain responses, shown in Figure 2.29, confirm that controlled electromagnetic feedback can effectively enhance gain and stability in GaN LNAs while preserving competitive noise performance across the K-band.

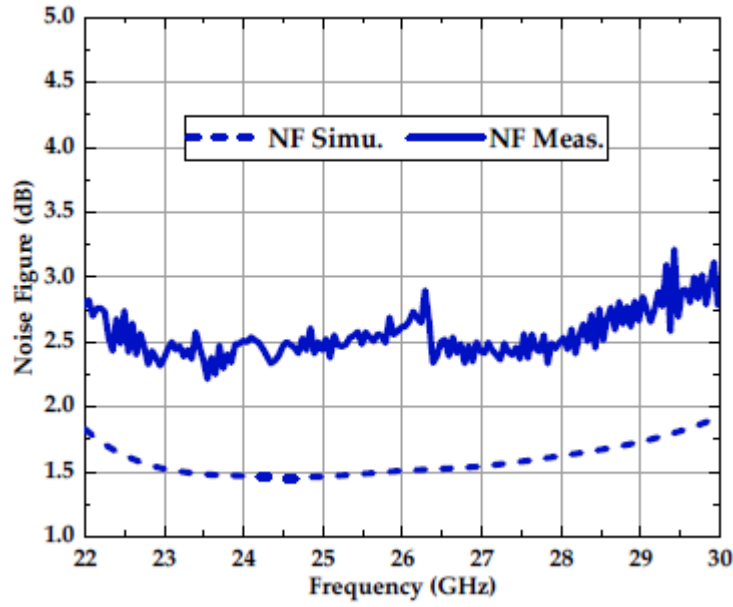


Figure 2.29: Simulated and measured NF of the LNA [130].

Table 2.7 illustrates the performance of the explored GaN K-band LNAs.

Table 2.7: Comparison of Representative GaN K-Band Low-Noise Amplifiers.

Ref	Architecture	Frequency (GHz)	Gain (dB)	NF (dB)	P_{1dB} (dBm)
[126]	3 & 4-stage CS	27 – 31	12 – 19.6	3.7 – 3.9	N/A
[127]	3-stage CS	22 – 30	19	0.4 – 1.1	20
[128]	2-stage CS	18 – 31	21 ± 0.5	0.8	N/A
[129]	2-stage CS	18 – 22.5	17.2	2 – 2.3	10.5
[130]	4-stage CS with DS feedback	23 – 29	23.7	2.2	13

The evolution of GaN K-band low-noise amplifiers reflects a clear shift in design priorities over time. Early implementations focused primarily on ruggedness and survivability under high input power stress, while later works progressively closed the noise-figure gap with GaAs technologies through improved device modelling and matching strategies. More recent designs emphasize application-driven optimization and circuit-level innovation, enabling wideband operation, higher gain, and stable performance tailored to specific receiver architectures. Together, these results demonstrate that GaN technology has matured into a versatile platform for K-band LNAs, capable of simultaneously addressing noise performance, robustness, and system-level requirements.

2.4.2 GaN LNAs in W-band

At W-band frequencies (75 - 110 GHz), low-noise amplifier design becomes increasingly constrained by device parasitics, stability margins and reliability under high-power illumination. Gallium Nitride (GaN) technology has appeared as a compelling choice for W-band LNAs, not primarily for achieving the lowest possible noise figure, but for enabling robust receiver front ends with high linearity, wide dynamic range and improved survivability. Compared with GaAs- and InP-based LNAs, GaN W-band LNAs offer higher breakdown voltage and superior thermal handling, allowing operation in environments where strong interferers, leakage from co-located transmitters, or harsh operating conditions are present. As GaN device scaling and millimeter-wave modelling have matured, a growing body of work has demonstrated that GaN LNAs can achieve competitive noise performance at W-band while providing unique advantages in robustness and long-term reliability.

Linearity is treated as the primary design goal in [131], and the reported W-band LNA is optimised to provide predictable large-signal performance rather than minimum noise alone. The four-stage MMIC, implemented in AlGaIn/GaN HEMT technology, is centered at 84 GHz, where it achieves approximately 25 dB small-signal gain with a 3-dB bandwidth of about 4 GHz. When biased for noise performance, the amplifier exhibits a minimum measured noise figure of 5.6 dB at 84 GHz, indicating a deliberate trade-off between noise and linearity suitable for robust W-band receiver front ends. The combined measured gain and noise characteristics, shown in Figure 2.30, clearly illustrate the narrowband optimization around the target frequency and the resulting noise performance achieved under the reported operating conditions.

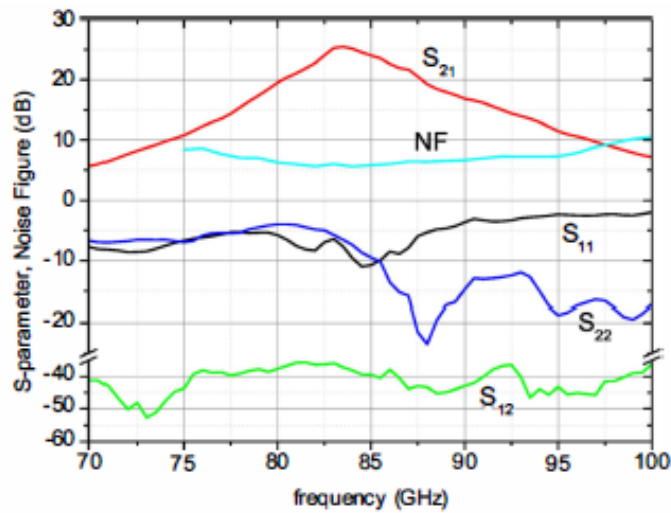


Figure 2.30: S-Parameters and noise figure [131].

A unique design approach is adopted in [132], where the primary objective is to reduce the achievable noise figure of GaN LNAs at W-band through device-level and matching optimization rather than through architectural complexity. A four-stage MMIC LNA is implemented using two GaN HEMT epitaxial variants within an otherwise identical circuit topology, enabling a direct experimental comparison of noise performance without confounding layout effects. Measured results show that the baseline implementation achieves a minimum noise figure of approximately 4.5 dB at 95 GHz with around 18 dB gain, while the advanced HEMT version improves the minimum noise figure to about 3.25 dB at the same frequency and provides more than 20 dB gain across the operating band. Under optimized bias conditions, a further reduction toward 3 dB minimum noise figure is reported, showing the impact of material and device optimization on W-band GaN LNA performance. The measured gain and noise figure comparison between the two implementations, presented in Figure 2.31, clearly highlights the performance improvement enabled by the advanced GaN technology and supports the claim of state-of-the-art noise performance at W-band.

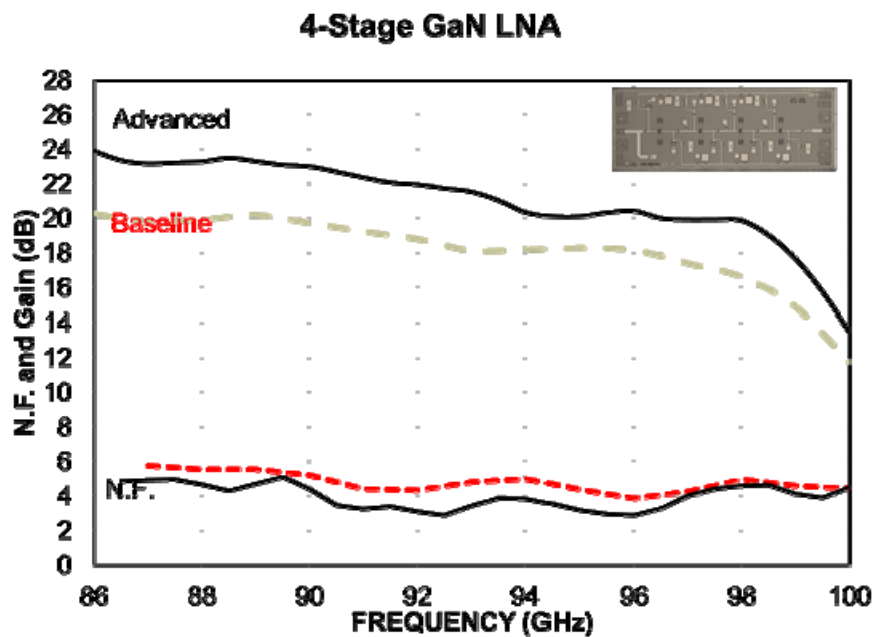


Figure 2.31: Comparison of measured on-wafer LNA noise figure and gain [132].

Integration potential rather than record noise performance is the central theme of [133], which explores the feasibility of implementing W-band LNAs in a 100-nm GaN-on-silicon process. Two MMIC LNAs with different bandwidth targets are presented, illustrating how circuit trade-offs can be adjusted within the same technology to address distinct receiver requirements. For the narrower-band design, measurements indicate a small-signal gain of approximately 17.5 - 20.5 dB over 77.5 - 84 GHz, while the reported noise figure remains around 4 dB under the specified bias conditions. Although the achieved noise performance is higher than that of GaN-on-SiC implementations, the

results demonstrate stable operation and repeatable gain across the intended W-band range, highlighting the practicality of GaN-on-Si for cost-sensitive or highly integrated front-end solutions. The measured NF of 2 designed LNAs shown in Figure 2.32 confirm the targeted W-band operation and provide direct evidence of the achievable performance using this commercially scalable process.

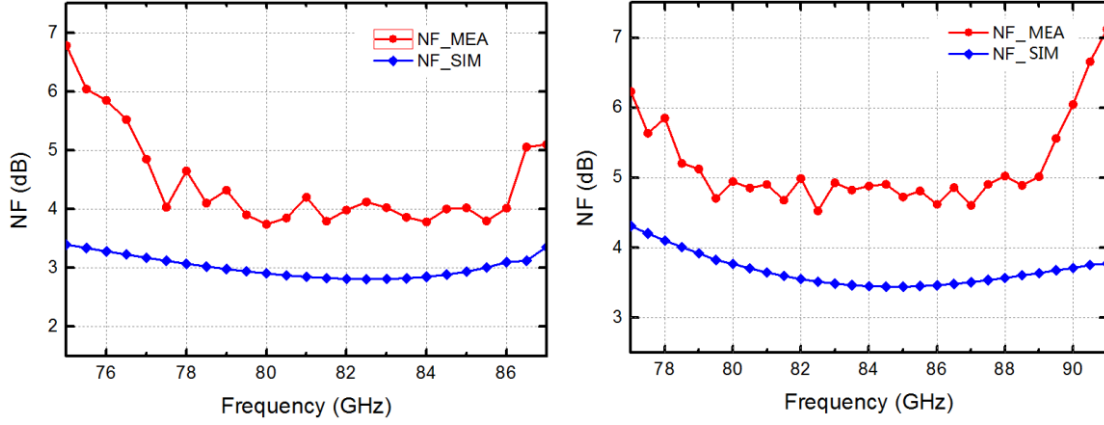


Figure 2.32: Measured and simulated NF of the two LNAs [133].

Bandwidth expansion is the defining contribution of [134], where a W-band GaN LNA is designed to maintain competitive noise performance over an unusually wide frequency range. The reported MMIC is implemented using a 70-nm gate-length GaN HEMT technology and adopts a multi-stage topology combined with broadband matching networks to avoid the narrowband result typical of earlier W-band GaN LNAs. Measured results show a small-signal gain exceeding 21 dB from 63 to 101 GHz, with a peak gain of approximately 24 dB near 67 GHz, showing continuous coverage well beyond the conventional W-band limits. When biased for noise optimization, the amplifier achieves an average noise figure of about 3 dB between 75 and 101 GHz, with a minimum value around 2.8 dB near 84 GHz, while staying below 3.8 dB up to 110 GHz. The measured gain and noise figure characteristics presented in Figure 2.33 clearly illustrate the simultaneous achievement of wide bandwidth and low noise, establishing this work as a key reference for broadband GaN W-band LNA design.

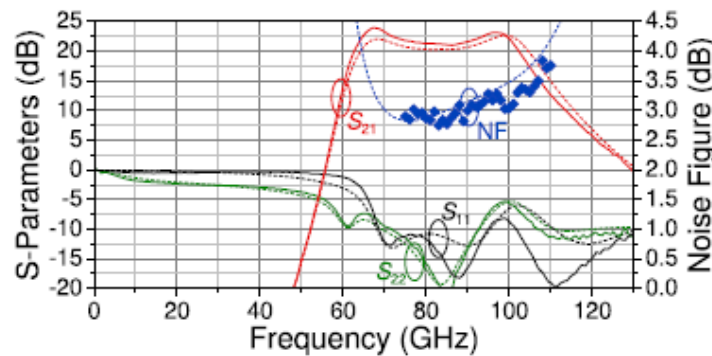
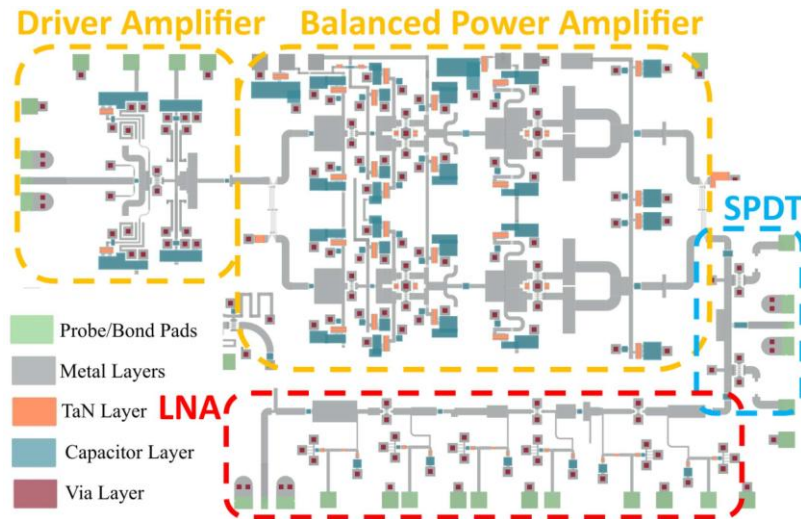
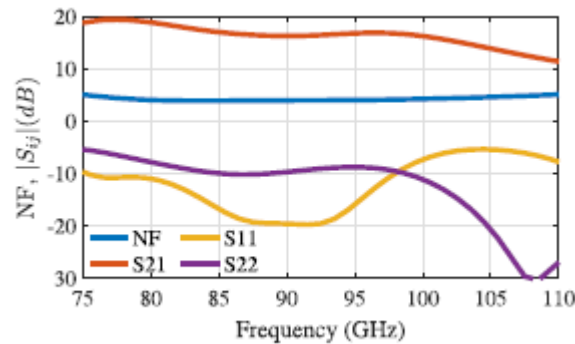


Figure 2.33: Measured (solid lines) and simulated (dashed lines) S-parameters of the presented LNA. The measured NF is shown by blue symbols [134].

The work in [135] offers a consolidated view of GaN MMIC development at V- and W-band, placing low-noise amplifiers in the broader context of millimeter-wave front-end integration. The paper surveys multiple GaN MMIC building blocks, including LNAs, power amplifiers, switches, and phase shifters, and highlights how advances in GaN device scaling and modelling have enabled operation well above 60 GHz with increasing performance maturity. Within the LNA discussion, GaN-based designs are positioned as robust alternatives to GaAs and InP solutions, offering competitive noise figures at W-band while providing superior linearity, power handling, and environmental tolerance. Reported W-band GaN LNAs in the survey demonstrate noise figures approaching the lower end of the 3 - 5 dB range with useful gain and bandwidth, supporting their suitability for demanding applications such as high-resolution radar and sensing systems. The front-end architectures and representative GaN MMIC implementations summarized in Figure 2.34 clearly illustrate the role of LNAs within complete V-/W-band GaN-based receiver and transceiver solutions, reinforcing the system-level relevance of GaN LNA research at these frequencies.



(a)



(b)

Figure 2.34: (a) Layout of W-band front end integrated MMIC, (b) noise factor and S parameters in RX mode [135].

Table 2.8 shows the performance comparison of the discussed GaN W-band LNA designs.

Table 2.8: Comparison of GaN W-Band Low-Noise Amplifiers.

Ref	Technology	Frequency (GHz)	Gain (dB)	NF (dB)
[131]	AlGaIn/GaN HEMT	84	25	5.6
[132]	GaN HEMT	90 – 100	18 – 22	3 – 4.5
[133]	100-nm GaN-on-Si	77 – 84	17.5 – 20.5	4
[134]	70-nm GaN HEMT	63 – 101	21	2.8 – 3.8
[135]	40-nm GaN on 50- μ m SiC	V/W-band	11 - 19	3 – 5

GaN W-band LNA development has progressed from early narrowband, high-linearity demonstrations toward broadband, low-noise implementations enabled by improved device scaling and matching strategies. While initial designs prioritized robustness and predictable behaviour at a single frequency, later work significantly reduced the noise figure and expanded the usable bandwidth, culminating in E/W-band LNAs with competitive noise performance over tens of gigahertz. Survey-level studies further highlight the growing role of GaN LNAs as integral components of complete millimeter-wave front ends, where robustness, linearity, and integration increasingly complement noise performance as key design drivers.

2.4.3 GaN PAs in K-band

Gallium Nitride (GaN) power amplifiers operating in the K-band have emerged as a key enabling technology for modern millimeter-wave transmitters, driven by the stringent requirements on output power, efficiency and reliability at high frequencies. The intrinsic material advantages of GaN, including its wide bandgap and high breakdown voltage, allow power amplifiers to sustain large voltage swings and high-power densities that are difficult to achieve with silicon-based technologies in this frequency range. These characteristics make GaN PAs particularly attractive for K-band systems such as satellite communications, radar sensors, and high-capacity wireless backhaul links. As K-band frequencies push device dimensions and passive networks into increasingly parasitic-sensitive regimes, careful circuit and layout optimization becomes essential to fully exploit the performance potential of GaN-based power amplification.

Building on early exploratory work in GaN material growth and heterostructure physics that laid the groundwork for high-field nitride devices, the study in [38] systematically demonstrates the performance potential of AlN/GaN HEMTs through careful strain and barrier-thickness optimization. The authors show that maintaining the AlN barrier below the critical thickness for relaxation is

essential to preserving high two-dimensional electron gas quality, which directly translates into superior device characteristics. With an optimized structure consisting of a 4.5 nm AlN barrier and a thin GaN cap, the fabricated transistors achieve a high sheet charge density and low sheet resistance, enabling exceptionally strong DC performance. As shown in Figure 2.35, HEMTs with a 1 μm gate length deliver drain current densities approaching 1.8 A/mm along with a peak transconductance of 400 mS/mm, highlighting the suitability of strained AlN/GaN heterostructures for high-current operation.

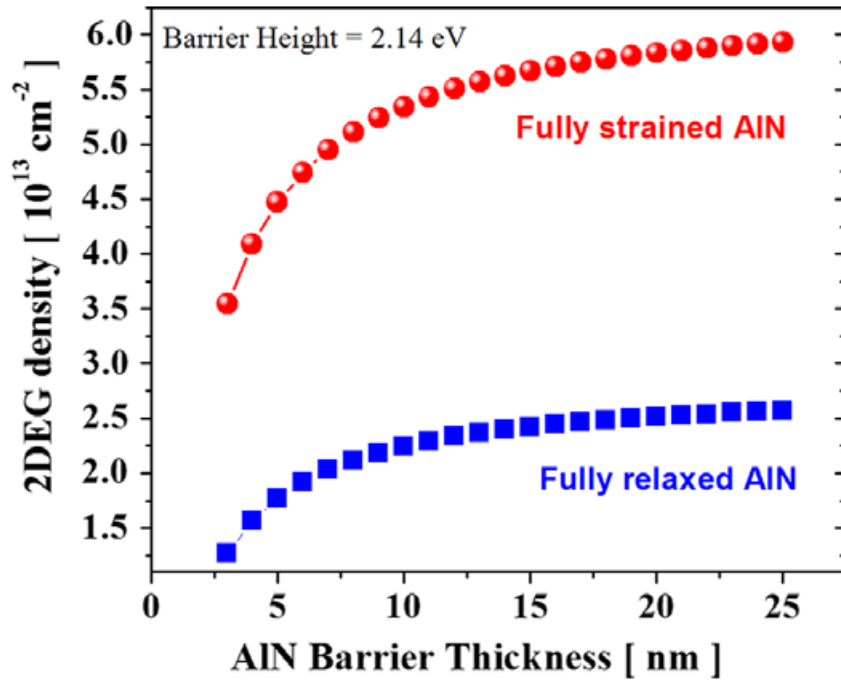


Figure 2.35: I – V characteristics of HEMT devices, with 1 μm gate length, fabricated from a 1 nm GaN/4.5 nm AlN/GaN heterostructure [38].

Building upon earlier advances in GaN heterostructure devices, the work reported in [39] demonstrates a major leap in microwave power performance by addressing the long-standing challenge of translating high DC current capability into usable RF output power. The study shows that careful suppression of trapping effects and current collapse is critical for achieving high large-signal efficiency, particularly under high drain bias operation. Figure 2.36 illustrates the optimized AlGaIn/GaN HEMTs fabricated on SiC substrates achieve a record continuous-wave power density of approximately 9.8 W/mm at 8 GHz, together with nearly 10 dB of power gain and close to 50% power-added efficiency. Furthermore, the results highlight the strong influence of substrate thermal conductivity, as devices realized on sapphire exhibit earlier power compression despite similar intrinsic device characteristics. These findings establish a clear device- and thermal-level benchmark that underpins subsequent development of high-power GaN amplifiers at higher millimeter-wave frequencies, including K-band operation.

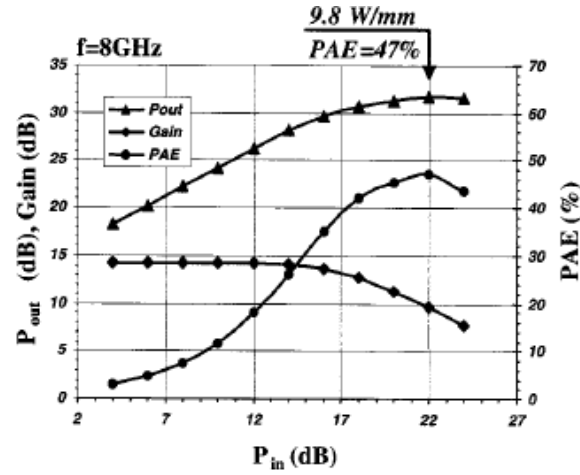


Figure 2.36: Power performance of the AlGaIn/GaN HEMTs [39].

Positioned at a stage where GaN technology had transitioned from laboratory demonstrations to volume MMIC production, the work in [40] provides a comprehensive perspective on the factors that established GaN as the leading solution for high-power RF and millimeter-wave amplifiers. The paper synthesizes device- and circuit-level results demonstrating that high breakdown voltage, large current density, and the superior thermal conductivity of SiC substrates collectively enable output power and efficiency levels unattainable with GaAs-based technologies over a wide frequency range. Practical validation of these advantages is provided through Ka-band PA MMIC implementations, where balanced and multi-stage architectures are employed to maintain gain and efficiency under elevated thermal stress. The measured Ka-band power and efficiency characteristics reported in Figure 2.37 confirm watt-level output power with power-added efficiency exceeding 20% across much of the 25 - 30 GHz band, illustrating that GaN retains strong large-signal performance deep into the millimeter-wave regime.

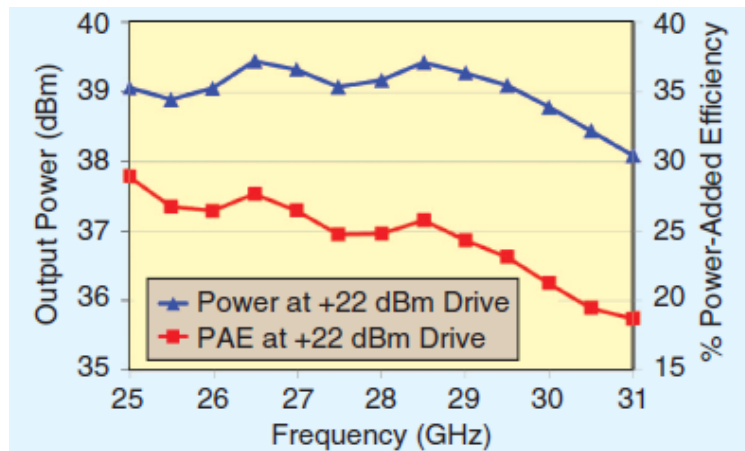


Figure 2.37: Measured CW output power and PAE for a GaN Ka-band PA MMIC [40].

Tracing the maturation of GaN technology from early material and device breakthroughs into a commercially robust platform, the review in [41] synthesizes how GaN-on-SiC HEMTs enabled a step change in RF and millimeter-wave power amplifier performance. The paper highlights that the combination of high breakdown voltage, large current density, and superior thermal conductivity of SiC substrates allows GaN devices to support aggressive voltage and current swings while maintaining manageable channel temperatures. Beyond discrete transistor capability, substantial emphasis is placed on the co-evolution of accurate large-signal models and MMIC processes, which made it possible to reliably translate device potential into broadband and high-efficiency amplifier realizations. The close agreement between measured and modelled large-signal result illustrated in Figure 2.38 demonstrates that GaN HEMTs can be predicted accurately under realistic load–pull conditions, a prerequisite for high-power and high-efficiency PA design.

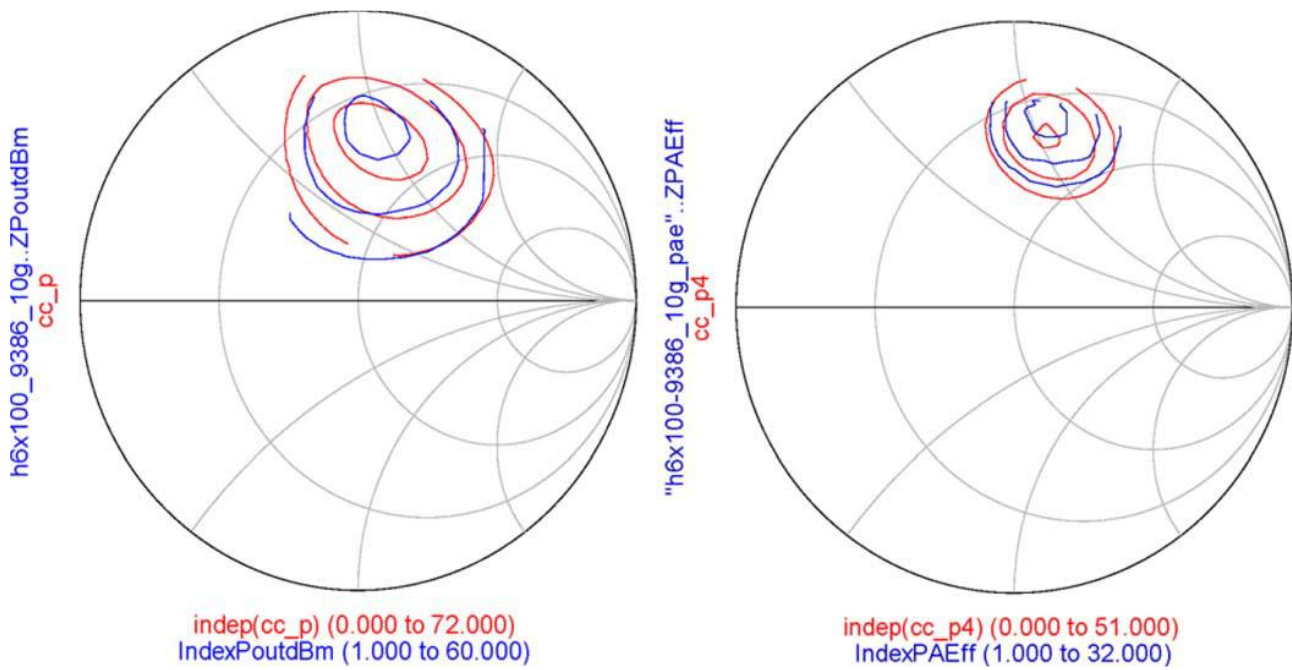


Figure 2.38: Measured versus modelled load–pull contours (output power: left, PAE: right) [41].

One of the most important inflection points in GaN’s history was the resolution of reliability concerns. Addressing reliability as a key requirement for satellite-oriented millimeter-wave transmitters, the work reported in [44] presents one of the earliest K-band GaN MMIC power amplifiers in which environmental lifetime considerations are evaluated alongside RF performance. Beyond demonstrating high output power and efficiency at 20.2 - 21.2 GHz, the study explicitly investigates the robustness of the AlGaIn/GaN-on-SiC technology under accelerated radiation and thermal stress conditions relevant to space operation. The authors subject multiple amplifier samples from the same fabrication lot to cumulative total ionizing dose exposure followed by prolonged high-temperature biasing, enabling separation of radiation-induced and thermally driven degradation mechanisms. This

performance is evident from the large-signal power characteristics introduced in Figure 2.39, where negligible change in output power is seen after 100 krad radiation exposure, while a modest about 0.5 dB reduction emerges after extended high-temperature oven testing.

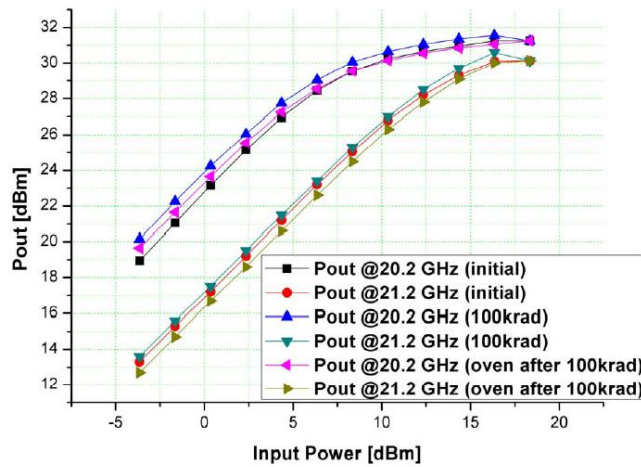


Figure 2.39: Large signal measurement results of one of the 100 krad radiation applied amplifier (before radiation, after radiation and after 1 week oven tests) [44].

Focusing on long-term robustness under realistic operating conditions, the study in [45] presents one of the most comprehensive DC- and RF-based reliability assessments reported for a millimeter-wave-capable GaN HEMT technology. The paper evaluates a 28 V, 150-nm GaN-on-SiC process using a combination of DC-HTOL, HTRB, RF-accelerated life testing, and RF high-temperature operating life stress, thereby addressing both intrinsic wear-out mechanisms and application-relevant degradation modes. Importantly, reliability is verified not only at low microwave frequencies but also under millimeter-wave excitation, where Ka-band operation near 30 GHz is explicitly assessed using pre-matched single-stage and multi-stage MMICs. The sustained output power during extended RF-HTOL stress at 31.5 GHz reported in Figure 2.40 demonstrates that no measurable degradation exceeding 1 dB occurs even after thousands of hours at elevated junction temperatures, confirming the suitability of the technology for continuous high-frequency operation. Together with the projected mean time to failure exceeding 10^6 hours at a junction temperature of 225 °C, these results establish that temperature-driven mechanisms such as field-plate voiding and ohmic contact degradation, rather than frequency-dependent effects, dominate lifetime limitations, providing strong evidence of the maturity of GaN MMIC technology for reliable K-band and adjacent millimeter-wave power amplifier applications.

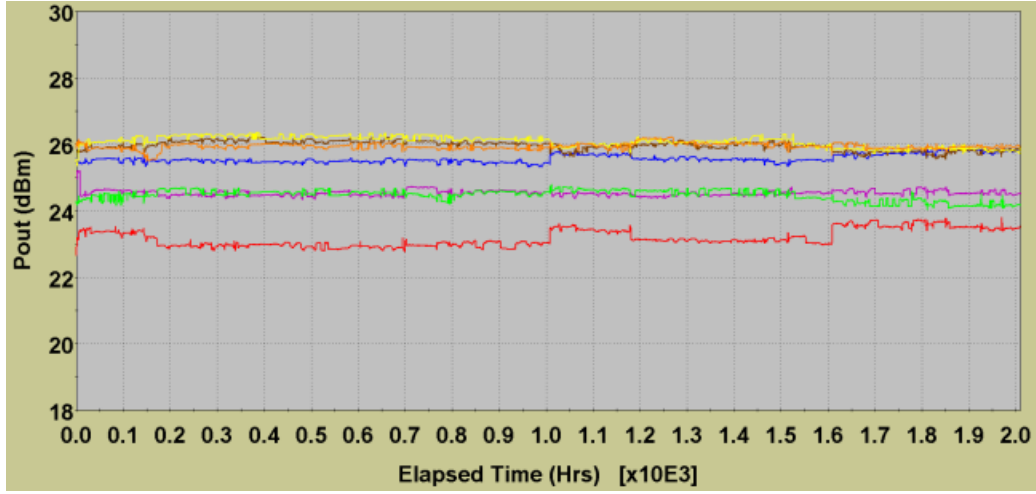


Figure 2.40: In-situ P_{out} plots during RF-HTOL stress at 31.5 GHz, $P_{in} = 20$ dBm, and $T_j = 225^\circ\text{C}$ [45].

At the same time, GaN-on-Si technology matured as a cost-effective alternative to GaN-on-SiC. Although Si has lower thermal conductivity than SiC, its low cost and large wafer sizes (up to 200 mm) enabled lower-cost manufacturing and compatibility with CMOS processes. GaN-on-Si is now widely used for commercial RF and power electronics, though high-end defense and satellite systems continue to prefer GaN-on-SiC for its superior thermal performance.

The K-band occupies a strategically critical region of the spectrum for modern satellite communications, radar systems and deep-space links. While GaAs has historically dominated this band for low-noise amplification, GaN has emerged as the technology of choice for high-power amplification. Its combination of high breakdown voltage, high electron saturation velocity, and superior power density has allowed GaN-based power amplifiers (PAs) to achieve unprecedented output powers, efficiencies, and bandwidths in the K-band. The following subsection surveys the evolution of GaN K-band amplifiers, with attention to academic demonstrations and the trade-offs between GaN and GaAs in this frequency window.

Situated in the early-to-mid 2010s, when sub-100-nm GaN HEMT technologies were beginning to be explored for millimeter-wave solid-state transmitters, the work reported in [47] evaluates the feasibility of a 100-nm AlGaIn/GaN MMIC process for K-band power amplifier. Rather than pursuing broadband operation, the study adopts narrowband, single-stage architectures to benchmark the intrinsic efficiency and power capability of the emerging microstrip-based process around 19 GHz. Two amplifier realizations are investigated, one using a single 8×75 μm device and the other employing on-chip power combining, thereby enabling a direct comparison of scalability within the same technology. The large-signal measurement results presented in Figure 2.41 highlight that the

single-cell design delivers close to 1 W output power with peak power-added efficiency exceeding 35%, while the power-combined MMIC achieves higher output power approaching 1.5 W with comparable efficiency. Reproducibility across multiple wafer runs further confirms that the perceived performance is not an isolated result but reflects a stable and manufacturable process. Collectively, these results demonstrate that, at this stage of GaN technology development, 100-nm HEMTs could already support efficient and scalable K-band PA implementations, thereby forming a technological bridge between earlier 250-nm designs and later high-frequency GaN MMICs targeting Ka-band and beyond.

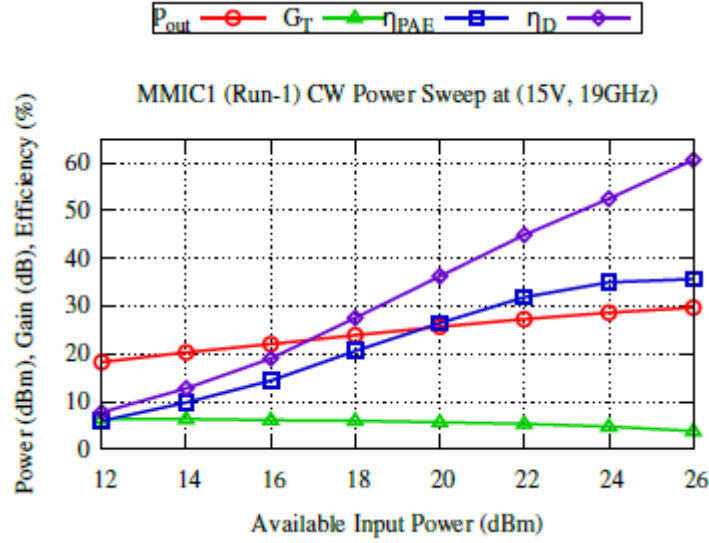


Figure 2.41: CW power sweep of MMIC1 at 15V supply voltage and at a frequency of 19 GHz [47].

Adopting a system-level perspective on K-band power generation, the work presented in [48] demonstrates how careful multi-stage architecture and reactive matching can be leveraged to simultaneously achieve high output power, high efficiency, and broadband operation in a GaN MMIC. The amplifier employs a three-stage topology implemented in a 150-nm GaN-on-SiC process, with transistor sizing and staging ratios selected to minimize driver losses while maximizing overall power-added efficiency. Rather than prioritizing peak gain alone, the design flow emphasizes efficiency-oriented load and source impedance synthesis across the entire signal chain, supported by stability analysis tailored for power-combining stages. The measured results summarized in Figure 2.42 indicate that the MMIC delivers peak output power exceeding 4 W with power-added efficiency above 40%, while maintaining more than 3.2 W output and over 20 dB saturated gain across a wide 18.5 - 24 GHz bandwidth.

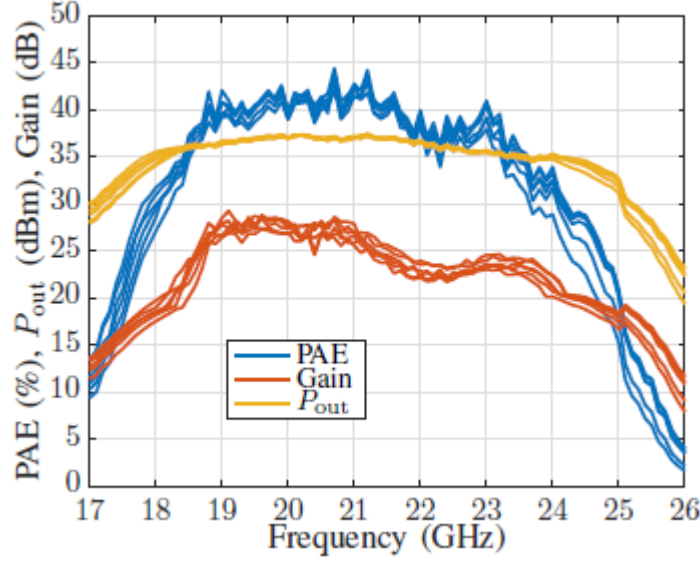


Figure 2.42: Measured large signal amplifier performance at maximum PAE point [48].

The authors in [49] introduces a nonlinear input-capacitance compensation concept aimed at improving linearity in broadband GaN power amplifiers targeting Ku- and K-band operation. The proposed approach intentionally combines multiple transistors of different sizes and bias conditions so that their individual nonlinear input capacitance trends counteract each other, effectively flattening the overall capacitance variation seen at the PA input. This device-level compensation is shown to be particularly effective under large-signal excitation and elevated temperature, conditions that typically exacerbate AM–PM distortion in GaN PAs. The measured AM–PM and intermodulation performance summarized in Figure 2.43 demonstrate that the resulting MMIC maintains AM–PM distortion below 0.07° and achieves IMD3 improvements exceeding 18 dB compared with a conventional class-AB design, without relying on digital predistortion.

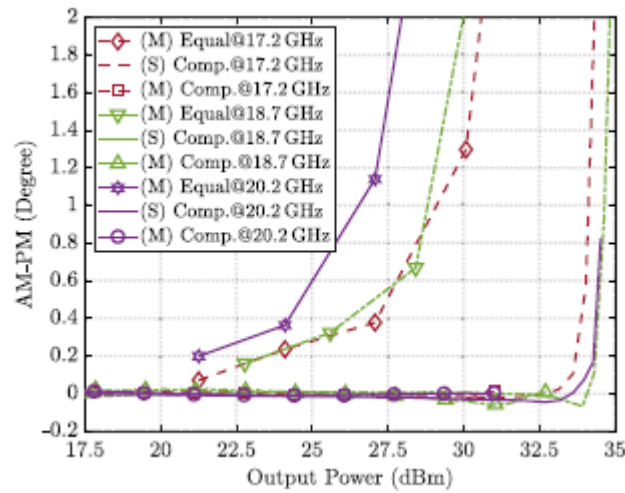


Figure 2.43: Simulated (S) (no markers) and measured (M) (with markers) AM–PM conversion versus output power of the proposed PA in comparison to an EB PA for selected frequencies [49].

Rather than optimising a fixed operating band, the work in [51] explores architectural flexibility in K-band GaN power amplifiers through the introduction of a frequency-reconfigurable MMIC enabled by a switch-loaded coupled-line interstage matching network. The design strategically confines reconfigurability to the interstage network, while retaining a broadband output matching network to avoid excessive loss from switch on-resistance, thereby preserving efficiency at high output power. By toggling the embedded switch states, the amplifier can be reconfigured between two distinct K-band sub-bands without altering the active device biasing or topology. The measured large-signal performance presented in Figure 2.44 confirms that the PA maintains saturated output power above 30 dBm in both the 19.5 - 21.5 GHz and 23.5 - 25.5 GHz bands, with peak power-added efficiency reaching 26.5% in the lower band and exceeding 20% in the upper band. In addition to continuous-wave characterization, modulated-signal measurements demonstrate acceptable linearity without digital predistortion, underscoring the practicality of the proposed approach for adaptive K-band transmitters.

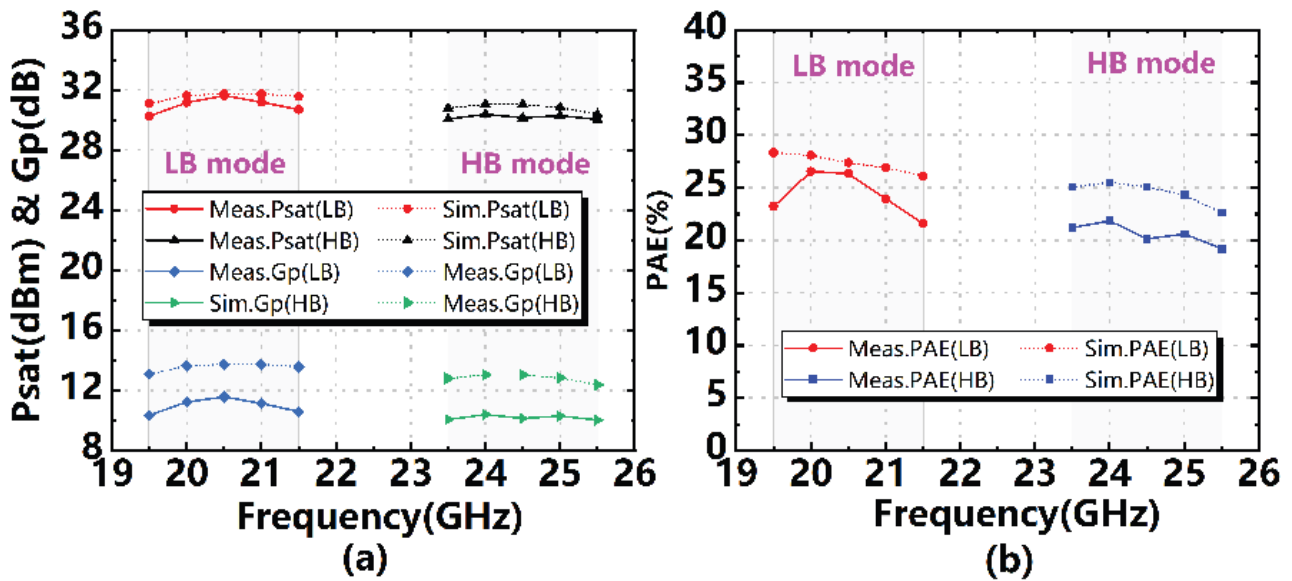


Figure 2.44: Measured and simulation. (a) P_{out} and power gain. (b) PAE in the LB/HB mode [51].

GaN PAs dominate applications requiring high output power, linearity and stability, particularly in defence and high-capacity satellite communications. Their wide bandgap and high breakdown voltage enable power densities exceeding 5 W/mm, compared to ~ 1 W/mm for GaAs.

The study in [64] demonstrates that deliberately exploiting input nonlinearity can be an effective means of enhancing efficiency in high-power K-band GaN amplifiers. The proposed three-stage MMIC adopts a driver stage configured to generate a half-sinusoidal voltage waveform, which is

subsequently delivered to the power-stage gate and interacts constructively with the intrinsic nonlinear capacitances of the device. By aligning the harmonic impedance requirements of both the driver and power stages through a compact interstage matching network, the design relaxes conventional input harmonic tuning constraints while maintaining high gain. The measured large-signal results reported in Figure 2.45 show that the amplifier achieves an average output power of approximately 42 dBm with peak power-added efficiency near 41% under pulsed operation across 17–20.5 GHz, while continuous-wave measurements still sustain more than 40 dBm output power with PAE exceeding 33%. These results indicate that input waveform manipulation provides a practical circuit-level approach for realizing watt-level K-band GaN PAs with high efficiency, even when implemented on thermally challenging substrates, thereby expanding the design space for satellite downlink applications.

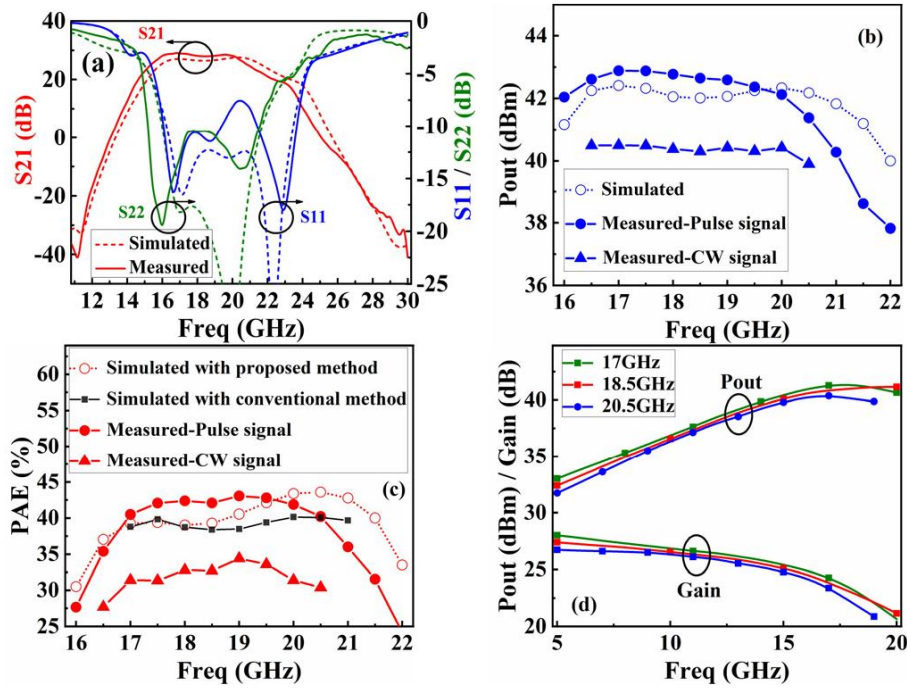


Figure 2.45: (a) Measured small signal. Both pulse and CW signal results for (b) Pout and (c) PAE. ($P_{in} = 18$ dBm.) (d) Measured CW power sweeps [64].

Pursuing broadband performance rather than narrowband optimization, the work reported in [65] presents a K-band GaN MMIC power amplifier designed to sustain high output power and efficiency over an exceptionally wide frequency range. The amplifier employs a three-stage architecture implemented in a 0.15- μm GaN HEMT process, where transistor sizing and driving ratios are carefully selected to balance gain flatness against efficiency across the entire 17 - 26.5 GHz band. Instead of relying on distributed techniques, the design adopts a broadband low-loss reactive matching topology combined with integrated harmonic control in the driver-stage matching network, allowing second-harmonic terminations to be managed without excessive insertion loss. The

measured continuous-wave large-signal performance summarized in Figure 2.46 confirms that the MMIC delivers saturated output power exceeding 42.5 dBm with an average power-added efficiency of approximately 30%, while maintaining output power flatness within 1 dB over the full K-band.

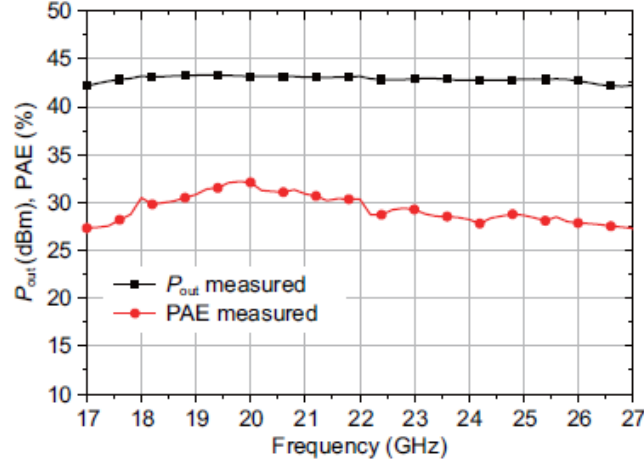


Figure 2.46: The measurement results of large signal characteristics [65].

The study presented in [66] demonstrates a K-band GaN MMIC power amplifier that prioritizes gain enhancement without resorting to excessive stage count. The design leverages a 0.15- μm GaN HEMT process incorporating a source field plate (SFP) structure to suppress gate-drain capacitance, thereby mitigating high-frequency negative feedback and improving transistor gain. Instead of increasing the number of amplifier stages, gain is recovered at the device level, allowing the three-stage architecture to maintain competitive efficiency and compact chip size. The effectiveness of this approach is substantiated by the measured continuous-wave results summarized in Figure 2.47, where the amplifier achieves output power up to 44.2 dBm with power gain exceeding 25 dB across 17 - 21.4 GHz, while the estimated junction temperature remains near 160 °C under saturated operation. By combining device-level gain engineering with careful output matching and thermal co-design, this work establishes a practical pathway toward realizing >20 W K-band GaN power amplifiers suitable for phased-array satellite communication systems.

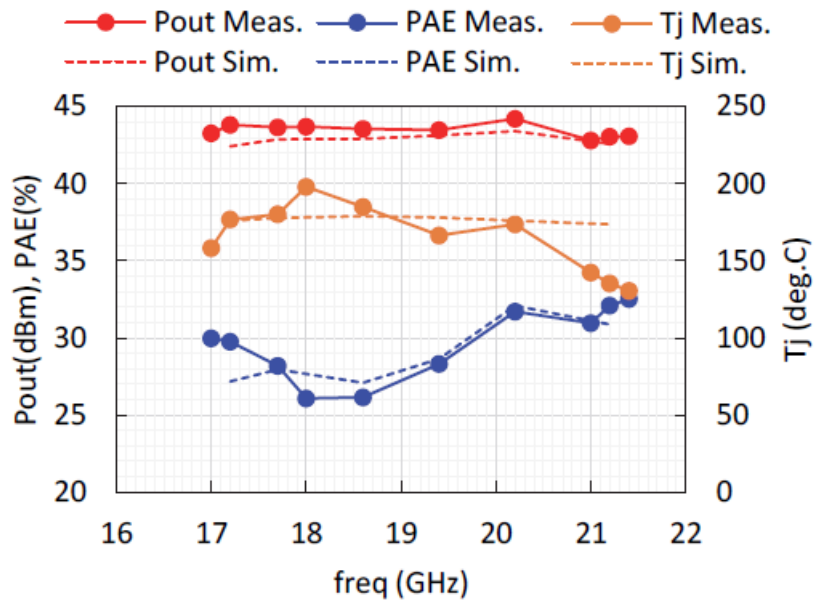


Figure 2.47: Frequency response of output power, PAE and junction temperature [66].

Table 2.9 shows the comparison of discussed K-band GaN PA.

Table 2.9: Comparison of Representative K-Band GaN MMIC Power Amplifiers.

Ref	Topology	Process	Frequency (GHz)	Power (dBm)	PAE (%)	Gain (dB)	Advantages	Disadvantages
[47]	Single-stage & power-combined MMIC	100 nm AlGaIn/GaN HEMT on s.i. SiC	19	31 – 32	35	N/A	Early microstrip library evaluation, good power densities and potential for wideband match.	Primarily narrowband matching techniques were employed.
[48]	Three-stage broadband MMIC	150 nm GaN on SiC (Qorvo)	18.5 – 24	36	40	20	High efficiency (>40% PAE) and high saturated gain (>20 dB) over broad bandwidth.	Requires careful multi-stage stability analysis beyond standard K-factor.
[51]	Reconfigurable PA using switch-loaded coupled lines	0.15 μ m GaN-on-SiC	19.5 – 21.5	30	20 – 26.5	N/A	Frequency agility, switchless broadband OMN reduces insertion loss and enhances efficiency.	Reconfigurability in output matching is avoided due to switch ON-state resistance.

[64]	Input nonlinearity & half-sinusoidal waveform shaping	0.1 μm GaN-on-Si	17 – 20.5	42	33	22	High efficiency achieved through input nonlinearity and gate voltage waveform shaping.	Si substrate exhibits poorer thermal dissipation compared to SiC.
[65]	Three-stage broadband low-loss matching	0.15 μm GaN HEMT	17 – 26.5	42.5	30	17.5	Wide bandwidth (17–26.5 GHz) with high output power flatness (<1 dB).	Large chip size compared to some other designs.
[66]	High-gain three-stage PA with thermal co-design	0.15 μm GaN-HEMT on SiC (MELCO)	17 – 21.4	44 – 44.2	26 – 32	25	High gain (over 25 dB) and significant output power (over 20 W).	SFP increases parasitic capacitances C_{gs} and C_{ds} , requiring careful optimization.

The rapid evolution of K-band GaN MMIC power amplifiers from early efficiency-oriented demonstrations toward highly integrated, high-power, and functionally versatile solutions. Initial efforts focused on validating device scalability and efficiency at K-band frequencies, while later works increasingly emphasize broadband coverage, gain enhancement, linearity improvement, and architectural flexibility through waveform engineering and reconfigurable matching networks. Recent designs further demonstrate that watt-level and multi-tens-of-watt output power can be achieved without excessive stage count by combining device-level innovations with careful thermal and matching co-design. Collectively, these achievements confirm that GaN technology has matured into a robust platform capable of meeting the stringent power, efficiency, and functionality requirements of modern K-band satellite and high-throughput communication systems.

2.4.4 GaN PAs in W-band

GaN power amplifiers operating in the W-band have emerged as a critical enabling technology for next-generation millimeter-wave systems that demand simultaneously high output power, wide bandwidth and robust operation at extreme frequencies. Compared with silicon-based technologies, GaN offers superior breakdown voltage and power density, which become increasingly important as device parasitics and loss mechanisms intensify above 75 GHz. These material advantages make GaN

particularly attractive for W-band applications such as high-resolution radar, high-capacity point-to-point links, and emerging sub-terahertz communication front ends. Nevertheless, achieving efficient and stable power amplification at W-band remains challenging due to aggressive device scaling, limited gain per stage, and stringent thermal constraints, motivating continued research into advanced device structures, power-combining techniques, and millimeter-wave circuit architectures tailored to GaN technology.

Representing a milestone in the early development of W-band GaN power amplifier, the work reported in [42] demonstrates that GaN MMIC technology can deliver output power levels previously unattainable with conventional millimeter-wave semiconductor platforms. The authors implement a three-stage W-band PA using 0.15- μm GaN DHFET devices on SiC, where corporate on-chip power combining is employed to efficiently scale output power while preserving phase and amplitude balance across the output stage. Rather than relying on narrowband resonant techniques, the amplifier adopts distributed microstrip matching networks optimized through extensive electromagnetic simulation to mitigate parasitic effects at frequencies approaching 100 GHz. The measured continuous-wave module performance presented in Figure 2.48 shows that the single-chip GaN MMIC achieves a peak output power of 842 mW at 88 GHz with an associated power-added efficiency of approximately 14.7% and power gain of 9.3 dB. These results exceed the output power of contemporaneous InP HEMT amplifiers by nearly a factor of two, despite using substantially smaller total gate periphery. By conclusively demonstrating both power scalability and practical module integration at W-band, this work established GaN as a viable and ultimately superior technology for high-power millimeter-wave solid-state transmitters.

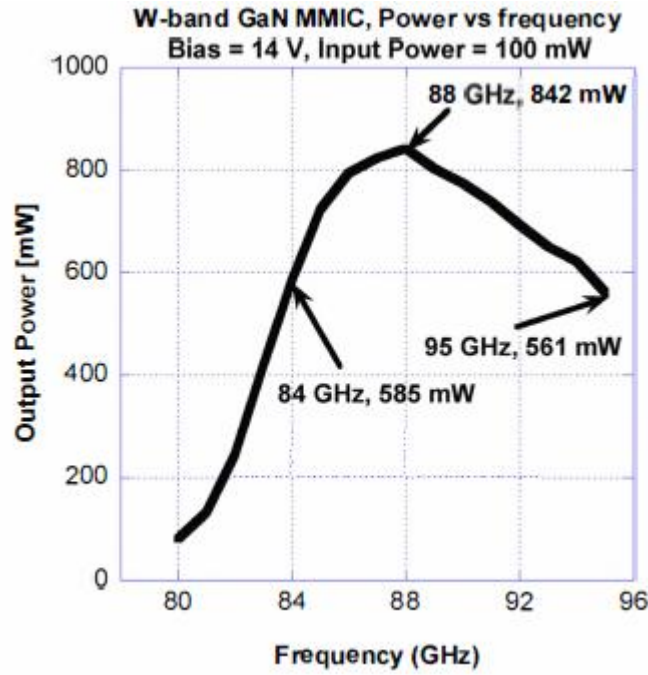


Figure 2.48: Output power versus frequency of a WR-IO power module that contains a single W-band GaN MMIC measured in CW mode at a drain bias of 14 V and input RF power of 100 mW [42].

Shifting the focus from single-chip capability to system-level power scaling, the work presented in [43] demonstrates that W-band GaN technology can be extended to multi-tens-of-watt output power through efficient broadband power combining. The amplifier employs a radial waveguide divider/combiner architecture to coherently combine 24 GaN MMIC chips, each based on a broadband 0.15- μm GaN-on-SiC process, thereby overcoming the limited output power of individual W-band devices. Careful attention is given to amplitude and phase uniformity across the constituent modules, as well as to minimizing dissipative losses in the waveguide combiner, which is essential for maintaining high overall efficiency. The broadband output power achieved by the assembled solid-state power amplifier, summarized in Figure 2.49, shows an average continuous-wave output power of approximately 37 W across the entire 75 - 100 GHz band, with peak output exceeding 50 W at the lower end of the band under controlled thermal conditions. By validating high combining efficiency together with forced-air and liquid-cooling operation, this work establishes a practical and scalable pathway for realizing high-power W-band GaN SSPAs suitable for demanding communication and electronic warfare applications.

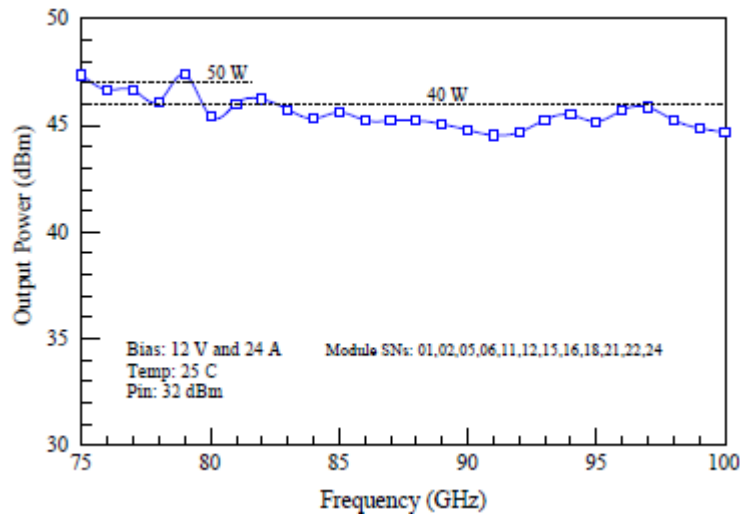


Figure 2.49: Using water cooling ($T = 25^{\circ}\text{C}$), the SSPA produces an average output power of 37 W across the 75 to 100 GHz band. Quiescent bias: 12 V and 24 A [43].

Pushing beyond the narrowband limitations that had characterized most early W-band GaN amplifiers, the work presented in [50] demonstrates the first GaN MMIC power amplifiers covering the entire W-band through deliberate broadband circuit innovation rather than aggressive power scaling. The authors implement three-stage and four-stage PA architectures using a 100-nm GaN-on-SiC HEMT technology, with wide microstrip matching networks chosen to minimize dissipative loss and preserve gain at extreme frequencies. A key contribution of this work lies in the introduction of a novel broadband radial stub topology within the bias network, which significantly extends the achievable fractional bandwidth without incurring substantial area or loss penalties. The measured large-signal performance shown in Figure 2.50 confirms that the three-stage amplifier delivers an average output power of approximately 26 dBm with peak power density reaching 2.55 W/mm across 70–110 GHz, while the four-stage variant provides higher gain exceeding 11 dB over the same frequency span. Although the absolute efficiency remains modest due to the extreme bandwidth and frequency of operation, the demonstrated 61.5% fractional bandwidth represents a major advance for W-band GaN PAs.

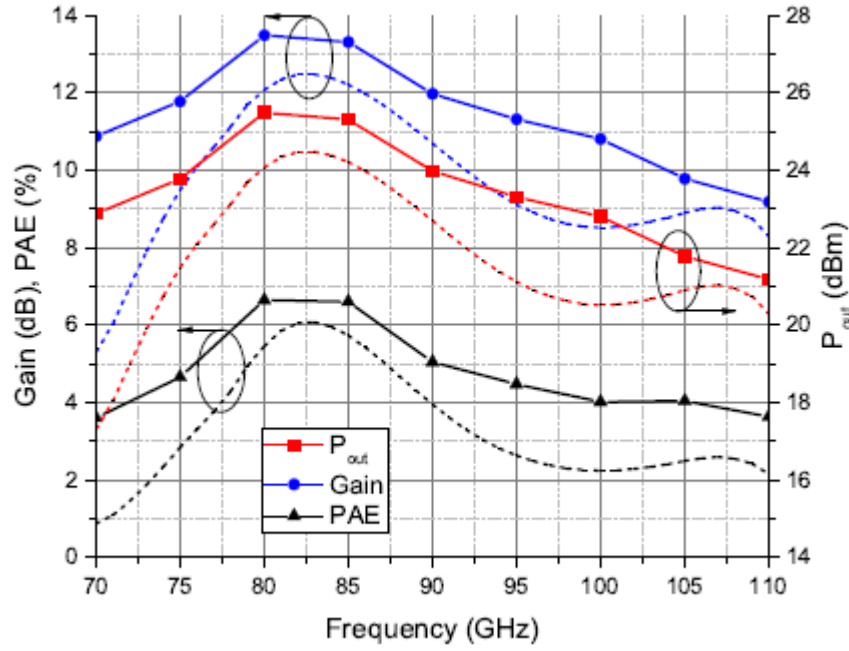


Figure 2.50: Measured (symbols) and simulated (dashed lines) large-signal response of the 3-stage power amplifier versus the frequency at $P_{in} = 12$ dBm ($V_{DS} = 15$ V, $I_D = 400$ mA/mm) [50].

Addressing the limited output power of single-chip W-band GaN amplifiers, the work in [57] focuses on on-chip power combining as a scalable solution for broadband 75 - 110 GHz operation. The authors design a three-stage GaN MMIC power amplifier using a 40-nm GaN-on-SiC process, where low per-device gain at W-band necessitates both multistage amplification and reactive combining at the circuit level. Rather than relying on narrowband resonant networks, broadband reactive matching and combining structures are employed to maintain stability and gain across the full W-band. Two identical three-stage PAs are further combined using a balanced architecture based on Lange couplers, enabling additional power scaling while preserving amplitude and phase balance. The measured large-signal results of the balanced amplifier presented in Figure 2.51 show output power exceeding 26 dBm with peak power-added efficiency of approximately 14.8% and large-signal gain above 10 dB across a 37.8% fractional bandwidth.

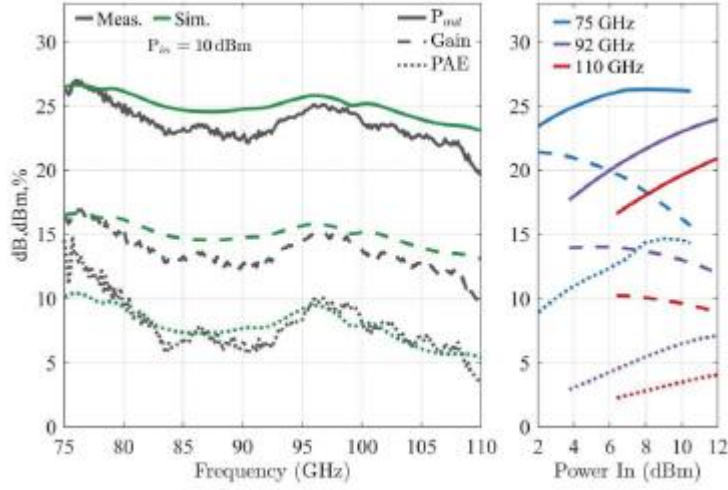


Figure 2.51: Large-signal measured characteristics of the balanced PA at $V_{DD} = +12V$, over frequency (left) and as a function of input power at the lower, center and upper parts of W-band (right) [57].

The work reported in [63] establishes a new benchmark for W-band solid-state transmitters by realizing a fully integrated 100-W GaN solid-state power amplifier (SSPA). Rather than relying on extreme scaling of a single chip, the design adopts a highly modular architecture in which 128 W-band GaN MMIC PAs are hierarchically combined using low-loss split-waveguide networks and balanced magic-tee combiners. Each MMIC, fabricated in a W-band GaN-on-SiC process, delivers approximately 1.2 W with 15% power-added efficiency, forming compact submodules that can be thermally coupled efficiently to a cold plate. The system-level large-signal measurements summarized in Figure 2.52 show that the assembled SSPA achieves saturated output power of approximately 100 W at 93 GHz under pulsed operation, with stable compression behavior and more than 30 dB of overall gain. Importantly, the reported wall-plug efficiency, which accounts for dc–dc conversion, bias control, and pulse modulation circuitry, exceeds 5% across the 92 - 96 GHz band, underscoring the practicality of the approach. These results demonstrate that GaN technology, when combined with scalable waveguide power-combining architectures, can effectively displace traveling-wave tubes for high-power W-band radar and communication systems.

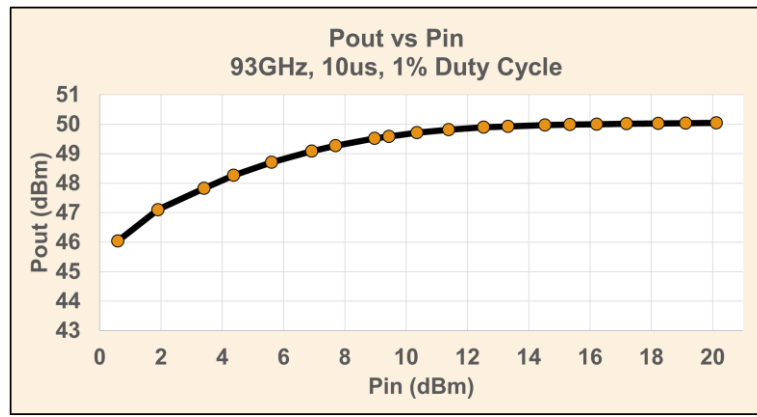


Figure 2.52: Full SSPA power sweep at 93 GHz [63].

Table 2.10 shows the comparison of the discussed W-band GaN PAs.

Table 2.10: Comparison of Representative W-Band GaN Power Amplifiers.

Ref	Topology	Process Technology	Frequency (GHz)	Power (dBm)	PAE (%)	Gain (dB)	Advantages	Disadvantages
[42]	3-stage MMIC with on-chip power combining	250 nm GaN on SiC	88	29.3	14.7	9.3	High output power (>12 W), CPW eliminates need for backside processing/vias.	Higher thermal resistance compared to microstrip designs.
[44]	Waveguide-combined SSPA (24 MMICs)	100 nm AlGaIn/GaN on SiC	75 – 100	45.6	N/A	N/A	Record output power for its time at 88 GHz, successful multi-cell combining.	High power density leads to significant thermal management requirements.
[50]	3- & 4-stage MMIC with broadband radial stubs	100 nm GaN-on-SiC	70 – 110	26	N/A	11	Exceptional bandwidth (50 GHz), first GaN PA to cover full W-band.	Complex matching networks required for multi-octave bandwidth.
[57]	On-chip + balanced (Lange coupler) combining	100 nm AlGaIn/GaN on SiC	75 – 110	26	14.8	10	Compact design with high gain (>20 dB), flat power response across full W-	Efficiency (PAE) is relatively low (peak 8.2%).

							band.	
[63]	Modular waveguide SSPA (128 MMICs)	100 nm AlGaIn/GaN on SiC	92 - 96	50	5	30	Extremely high power (100 W), potential to replace TWTAs.	Large system size/complexity, requires complex liquid cooling.

Overall, the reviewed W-band GaN power amplifier implementations prove a clear technological evolution from early single-chip MMIC realizations toward highly scalable, system-level solid-state transmitters. Initial efforts confirm the feasibility of GaN devices at frequencies approaching 100 GHz, while later work addresses the inherent limitations in gain, bandwidth, and output power through broadband circuit techniques, on-chip power combining, and low-loss waveguide architectures. The successful transition to modular and hierarchical combining schemes enables multi-tens-of-watt and ultimately 100-W-class output power, proving solid-state GaN solutions as credible alternatives to traditional vacuum electronic devices. As a result, these developments highlight the maturity of GaN technology for high-power W-band radar and communication systems and underscore its leading role in future millimeter-wave transmitter architectures.

2.5 Further explore the spectrum

The telecommunications landscape is currently undergoing a paradigm shift of historical magnitude, driven by the insatiable global demand for data bandwidth and ubiquitous connectivity. As the deployment of Fifth Generation (5G) networks reaches maturity and the research community pivots toward the definition of Sixth Generation (6G) standards, the electromagnetic spectrum has emerged as the primary constraint and enabler of future systems.

The conventional sub-6 GHz spectrum, although well suited for wide-area coverage, is increasingly constrained by its limited available bandwidth as multi-gigabit data rates become a fundamental requirement. To address this limitation, modern wireless systems are migrating toward higher operating frequencies where much wider contiguous spectrum is accessible. In this context, the Ka-band, broadly spanning 18 - 40 GHz, and the D-band, extending approximately from 110 to 170 GHz, have emerged as two critical frequency regions for next-generation communication infrastructure. Ka-band represents a pragmatic compromise between increased bandwidth and technological maturity, whereas D-band unlocks exceptionally large spectral resources capable of supporting ultra-high-throughput links. Together, these bands are poised to play a central role in future high-capacity wireless and satellite communication systems [80].

This section provides an exhaustive, comparative analysis of Monolithic Microwave Integrated Circuits (MMICs) designed for these frequency domains. It explores the intricate interplay between semiconductor device process, circuit topology, and system-level architectural constraints, with a specific focus on the trade-offs between Gallium Arsenide (GaAs), Gallium Nitride (GaN), Indium Phosphide (InP), and Silicon Germanium (SiGe) technologies.

The operational context for these bands is distinct yet interconnected. The K-band represents the current frontier of commercial mass deployment, serving as the backbone for High-Throughput Satellite (HTS) constellations like Starlink and Kuiper, as well as the 5G Frequency Range 2 (FR2) networks providing widely deployed fixed wireless access. In contrast, the W-band represents the future frontier, enabling 6G wireless backhaul (X-haul), inter-satellite cross-links, and high-resolution automotive radar sensing. The transition from K-band to W-band design is not merely a scaling exercise; it represents a fundamental discontinuity in engineering challenges, where the physical limitations of gain, noise, and power generation necessitate novel device architectures and heterogeneous integration strategies.

2.5.1 Spectrum allocation and challenges

Understanding the utility of K-band and W-band requires an attentive examination of the atmospheric physics that dictate their propagation characteristics. The selection of these bands is not arbitrary but is governed by the interaction of electromagnetic waves with atmospheric gases, primarily oxygen (O_2) and water vapor (H_2O).

The K-band is formally defined by the IEEE as the 18 - 27 GHz range, but in the context of satellite and 5G communications, it is inextricably linked with the Ka-band (26.5 - 40 GHz). The combined spectrum is bisected by a water vapor resonance absorption peak at 22.24 GHz. This absorption feature renders the center of the band unsuitable for long-range terrestrial communications but creates a natural isolation barrier that can be exploited for frequency reuse in short-range applications.

Consequently, the International Telecommunication Union (ITU) has allocated the windows flanking this peak, which is 17.7 - 21.2 GHz for satellite downlinks and 27.5 - 31 GHz for satellite uplinks, as the primary conduits for global broadband [81]. These windows offer a good point where atmospheric attenuation is manageable (typically < 0.2 dB/km in clear air), yet the frequency is high enough to allow for high-gain, compact antenna arrays.

Moving higher in frequency, the V-band (40 - 75 GHz) is dominated by a severe oxygen absorption

complex centered around 60 GHz, where attenuation spikes to > 15 dB/km. This creates a wall that naturally limits interference, making V-band ideal for secure, short-range inter-device communication but challenging for long-range backhaul.

Beyond this oxygen wall lies the W-band (75 - 110 GHz), a spectral window of immense strategic importance for 6G. Attenuation drops significantly in the 75 - 100 GHz range, creating a second sweet spot for long-range transmission. This window creates an opportunity for terrestrial backhaul links to operate over distances of several kilometers with available bandwidths exceeding 10 GHz, which is sufficient to support the terabit-per-second (Tbps) data rates envisioned for 6G [82]. Furthermore, the W-band serves as a bridge to the D-band (110 - 170 GHz), which is currently the subject of intense research for sub-THz wireless cognition and sensing applications.

At the heart of every radio transceiver operating in these bands lies the Front-End Module (FEM), a subsystem responsible for the analogue processing of signals. The performance of the FEM is dictated by two critical components: the Low Noise Amplifier (LNA) on the receive side and the Power Amplifier (PA) on the transmit side.

In the context of 5G and LEO satellite constellations, the demands on these components are contradictory. Receivers require ultra-low Noise Figures (NF) to maximize link budgets and data rates, yet they must also possess high linearity to handle complex modulation schemes like 64-QAM and 256-QAM without distortion. Transmitters must generate high output power to overcome path loss ($L_{\text{path}} \propto f^2$), yet they must do so with high Power Added Efficiency (PAE) to minimize the thermal load and energy consumption of the satellite or base station.

These conflicting requirements drive the selection of semiconductor technologies. While Silicon (CMOS and SiGe) offers unparalleled integration density for digital processing and beamforming control, it struggles to generate sufficient RF power or provide the lowest noise figures at mm-Wave frequencies due to the low breakdown voltage and conductive substrate losses [83]. This physical reality preserves the dominance of III-V compound semiconductors, which are GaAs, GaN, and InP in the high-performance RF front end.

2.5.2 Technology processes at Ka-band and D-band

To truly understand the trade-offs in MMIC design, designer must descend to the level of crystal lattices and electron transport properties. The performance of a transistor is fundamentally limited by

the material from which it is constructed. The key figures of merit include the bandgap energy (E_g), electron mobility (μ_n), saturation velocity (v_{sat}), and thermal conductivity (κ).

GaAs has long served as the foundation of the microwave integrated circuit industry, with the pseudomorphic high electron mobility transistor (pHEMT) emerging as its dominant device implementation in modern MMICs. In GaAs pHEMTs, a thin InGaAs channel is embedded between AlGaAs layers, where intentional lattice mismatch introduces pseudomorphic strain that significantly enhances electron mobility, typically reaching 6,000–8,500 $\text{cm}^2/\text{V}\cdot\text{s}$ [84]. This high carrier mobility results in low parasitic resistances and high transconductance, enabling excellent low-noise performance and establishing GaAs as the benchmark technology for low-noise applications, with noise figures routinely below 1.5 dB at K-band. However, the relatively small bandgap of GaAs (1.42 eV) imposes a low critical electric field for breakdown of approximately 0.4 MV/cm, constraining practical drain bias voltages to about 5–8 V. As a result, achieving high output power necessitates increased current and larger device peripheries, which in turn require extensive and lossy power-combining networks. This challenge is further compounded by the poor thermal conductivity of GaAs substrates, approximately 55 $\text{W}/\text{m}\cdot\text{K}$, which limits heat dissipation and restricts the scalability of GaAs technology for high-power microwave and millimeter-wave applications [85].

On the other hand, GaN has fundamentally transformed RF and millimeter-wave power generation by overcoming the intrinsic voltage and power density limitations of GaAs-based technologies. From a device-physics perspective, GaN is a wide-bandgap semiconductor with a bandgap of approximately 3.4 eV, resulting in a critical electric field on the order of 3.3 MV/cm, nearly an order of magnitude higher than that of GaAs. This property enables GaN HEMTs to sustain drain bias voltages typically ranging from 28 V to 50 V, and potentially higher, which directly translates into substantially increased power density through large voltage swings [86]. Consequently, GaN devices routinely achieve power densities of 4–12 W/mm of gate periphery at Ka-band, far exceeding the ~ 1 W/mm characteristic of GaAs technologies. Since native GaN substrates remain prohibitively expensive and limited in size, GaN devices are typically realized through hetero-epitaxial growth on alternative substrates. Silicon carbide has become the substrate of choice for high-power applications due to its exceptional thermal conductivity, approximately 350–450 $\text{W}/\text{m}\cdot\text{K}$, which enables efficient heat extraction from the active channel and supports reliable high-power operation, making GaN-on-SiC the standard for satellite and defense MMICs [87]. In contrast, GaN-on-Si leverages large-diameter silicon wafers, up to 200 mm, to achieve significant cost reductions, albeit at the expense of reduced thermal conductivity (~ 130 $\text{W}/\text{m}\cdot\text{K}$) and increased RF loss. Although traditionally viewed as less suitable for continuous-wave high-power operation, GaN-on-Si is increasingly recognized as

a disruptive platform for cost-sensitive applications such as 5G massive MIMO and, potentially, future W-band systems [88].

As operating frequencies extend into D-band, the limiting factor in transistor performance increasingly becomes carrier transport speed, particularly the electron transit time across the active region of the device. Indium phosphide-based technologies, including both HBTs and HEMTs, employ InGaAs channels with high indium content, which results in the highest electron saturation velocities among commonly used semiconductor materials, exceeding 2.5×10^7 cm/s. Such high carrier velocities enable extremely short transit times, pushing the current-gain cutoff frequency f_T and the maximum oscillation frequency $f_{\max}$ well beyond 500 GHz and, in advanced research demonstrations, even beyond 1 THz [89]. These characteristics establish InP as the leading technology for ultra-low-noise operation at millimeter-wave frequencies, with noise figures below 3–4 dB at D-band, and as the only practical platform capable of maintaining reasonable power amplifier efficiency above 150 GHz. Nevertheless, the adoption of InP is limited by several practical constraints, including the mechanical brittleness of InP substrates, relatively small wafer diameters typically restricted to 3–4 inches, and the lack of large-scale, high-volume commercial foundries compared with the more mature GaAs and GaN ecosystems [89].

2.5.3 Ka-band MMICs

The Ka-band represents the current commercial battleground. Along with the deployment of 5G FR2 and LEO satellite constellations, the focus of MMIC design has shifted from pure performance demonstrations to optimizing Size, Weight, Power, and Cost (SWaP-C). The primary challenge in this band is handling high-order modulation schemes (like 64-QAM and 256-QAM) which require high linearity, while simultaneously maximizing efficiency to reduce the energy footprint of the network.

Traditionally, GaAs pHEMTs have been the default choice for K-band LNAs due to their superior noise performance. The study presented in [90] reports a compact GaAs-based Ka-band low-noise amplifier MMIC that explicitly targets gain flatness across a wide operating bandwidth. The design employs a three-stage common-source cascade implemented in a 0.15- μ m GaAs pHEMT process, where inductive source degeneration is used in the first stage to achieve simultaneous noise and input matching, while stagger tuning is deliberately introduced across the three stages to equalize gain over frequency. Instead of distributing gain peaks uniformly, the authors strategically place the peak responses of the first and third stages near the lower end of the band and the second stage near the upper end, producing an overall flattened response. The noise performance illustrated in Figure 2.53

confirms a noise figure below 2.2 dB across the same range. Achieved with a modest DC power consumption of 56 mW and a compact chip area of $1.5 \times 0.9 \text{ mm}^2$, these results highlight GaAs pHEMT technology as a highly competitive solution for Ka-band low-noise receiver applications where uniform gain and low noise are critical system-level requirements.

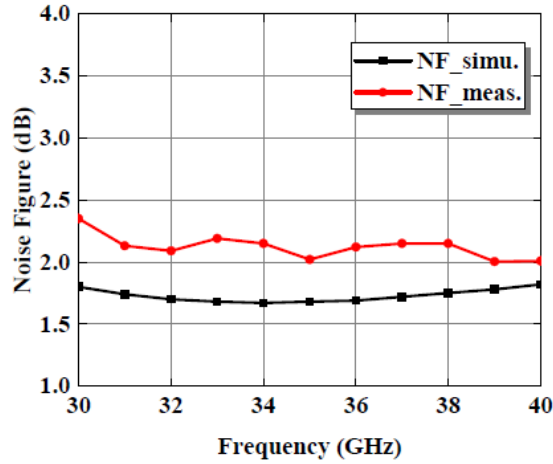


Figure 2.53: Simulated and measured noise figure [90].

A growing system-level consideration in modern RF receivers is survivability under high-signal stress conditions. In dense electromagnetic environments, receiver front ends are frequently exposed to strong jamming signals or leakage from nearby transmitters, which can pose a serious reliability risk. GaAs-based devices are particularly susceptible to such events, as input power levels on the order of +10 dBm are sufficient to cause irreversible gate damage. To mitigate this vulnerability, GaAs LNAs are typically preceded by input limiter circuits, most commonly implemented using PIN diodes, to protect the active device from excessive signal levels. While effective for protection, these limiters introduce additional insertion loss ahead of the amplifier, which directly degrades noise performance. As a result, a GaAs LNA exhibiting an intrinsic noise figure of 1.5 dB can experience an effective system noise figure of approximately 2.3 dB once a 0.8 dB limiter loss is included.

This is where GaN technology disrupts the paradigm. Addressing the increasing need for robust receiver front ends in high-interference environments, the work presented in [88] reports a Ka-band MMIC low-noise amplifier implemented in a 100-nm GaN-on-Si technology, explicitly targeting high dynamic range radar applications. The amplifier is conceived as the first stage of an FMCW radar receiver for small-drone detection, where extremely weak echo signals must be amplified in the presence of strong blockers arising from clutter and transmitter leakage. To meet these conflicting requirements, a three-stage single-ended topology is adopted, with progressively larger device peripheries and conservative biasing chosen to balance noise performance, gain, and linearity. The design strategy emphasizes source impedance synthesis close to the optimum noise condition in the

first two stages, while the final stage is intentionally optimized for distortion reduction rather than maximum gain. The measured performance summarized in Figure 2.54 demonstrates a linear gain of approximately 26 dB and a noise figure close to 2 dB over the 33 - 38 GHz band, while large-signal characterization confirms an output 1-dB compression point of 20 dBm and an output third-order intercept point of 28.4 dBm. This combination of low noise, high gain, and exceptional linearity establishes GaN-on-Si technology as a compelling solution for Ka-band receivers requiring enhanced survivability and dynamic range, extending GaN's relevance beyond transmitters into demanding low-noise front-end applications.

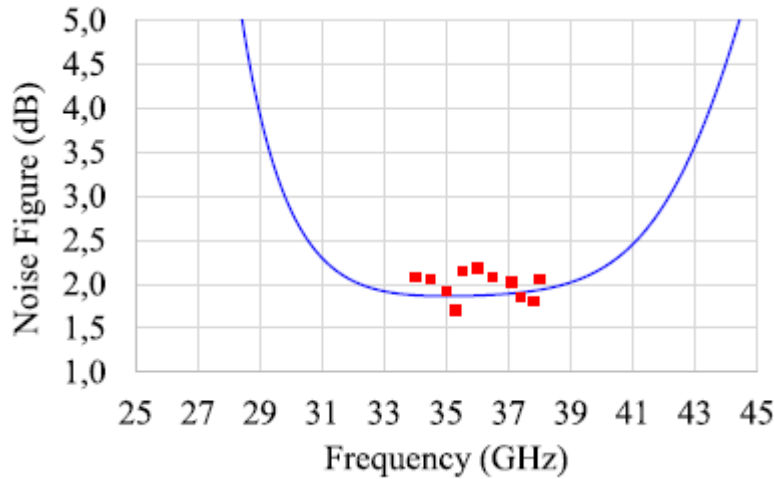


Figure 2.54: Measured NF and comparison with simulations [88].

The Power Amplifier is the single largest consumer of DC power in a transceiver. In the Ka-band, the transition from GaAs to GaN for high-power applications is trendy, driven by the physics of power density. At Ka-band frequencies, generating high power (e.g., >10 Watts) with GaAs is architecturally inefficient. Since GaAs power density is low (~ 0.5 W/mm), achieving 10W would require combining the output of 16 to 32 parallel transistor cells. The combining network required to sum these outputs becomes large and physically lossy. If the combiner has 1 dB of loss, 20% of the generated RF power is wasted as heat before it even leaves the chip.

Paper [92] provides an application-oriented investigation into linearity characterization methods for a GaN-based Ka-band satellite communication power amplifier, emphasizing the limitations of conventional RF requirements when applied to modern modulated signals. The study evaluates a commercial GaN solid-state power amplifier operating over 27.5–31 GHz with a saturated output power of approximately 46 dBm and compares traditional indicators such as P_{1dB} , P_{sat} , and IMD3 against modulation-dependent adjacent channel power ratio (ACPR) measurements using BPSK and QPSK waveforms. While small-signal and two-tone tests suggest early onset of nonlinearity due to the large separation between P_{1dB} and P_{sat} , the results demonstrate that these requirements alone

significantly underestimate usable output power in realistic operating conditions. This contrast is clearly illustrated in Figure 2.55, where ACPR remains above 30 dBc at substantially lower back-off levels than those implied by IMD3-based criteria. The analysis further shows that QPSK modulation consistently achieves approximately 3 dB better ACPR than BPSK at equivalent output power, underscoring the strong dependence of linearity on modulation format. By correlating ACPR, IMD3, and output power as a function of back-off, the work highlights ACPR as the most relevant figure of merit for defining the optimal operating point of Ka-band GaN PAs in satellite systems.

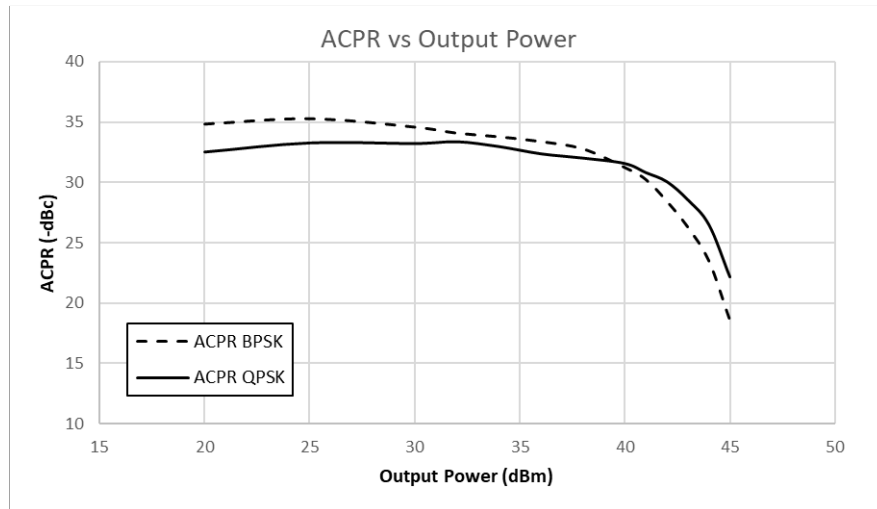


Figure 2.55: ACPR for BPSK and QPSK versus output power [92].

GaN's high voltage operation (28V+) allows for power densities of 4 - 10 W/mm. A 10W amplifier can be constructed with a simple 2-way or 4-way combination of large GaN cells. This drastically simplifies the matching network and reduces passive losses. The higher operating voltage also implies a higher optimum load impedance ($Z_{\text{opt}} \approx V_{\text{dd}}^2 / 2P_{\text{out}}$), which is closer to the standard 50 Ω system impedance. This reduces the impedance transformation ratio (Q factor) required of the matching network, inherently enabling wider bandwidths.

2.5.4 D-band MMICs

As the industry looks toward 6G backhaul and cross-link satellite communication, the focus shifts to W-band (75 - 110 GHz) and D-band (110 - 170 GHz). In this regime, the design challenges are dominated by the Terahertz Gap, where the frequency range where electronic devices struggle to provide gain and optical devices struggle to generate power.

The fundamental limit at these frequencies is the transistor's cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). A general rule of thumb is that for a robust circuit design, the

technology's $f_{\max}$ should be at least 3-4 times the operating frequency. For a 150 GHz D-band amplifier, this necessitates a technology with $f_{\max} > 450 - 600$ GHz.

Operation in the D-band imposes stringent requirements on transistor speed, making semiconductor scaling a decisive factor in determining which technologies remain practical. Indium phosphide devices, particularly HBTs, comfortably satisfy these demands, with reported maximum oscillation frequencies extending from roughly 600 GHz to beyond 1 THz, which provides ample margin for D-band operation [93]. Gallium nitride, by contrast, faces more severe scaling challenges, as conventional Ka-band GaN technologies with gate lengths around 0.25 μm are fundamentally too slow for D-band frequencies. To enable operation in this regime, GaN HEMTs must undergo aggressive gate-length reduction to 100 nm, 70 nm, or even 40 nm T-gate structures in order to suppress electron transit time and minimize parasitic capacitances. Silicon-germanium technologies occupy an intermediate position, where advanced BiCMOS nodes, such as 0.13 μm platforms, have pushed the maximum oscillation frequency to approximately 500 GHz, allowing competitive D-band performance despite inherently lower breakdown voltages compared with III-V compound semiconductors [93].

On one hand, for LNA designs at over 110 GHz, the noise figure becomes the primary limiter of link distance. Path loss is severe, and every decibel of receiver sensitivity is precious. InP HEMTs remain the undisputed champions of noise performance in the W/D-bands. Their ultra-high electron mobility InGaAs channels allow for high transconductance at very low noise temperatures. Reported InP LNAs at D-band (110 - 170 GHz) achieve noise figures in average 5 dB [89]. For scientific radiometry and deep-space communication, where link budgets are measured in fractions of a dB, InP is often the only practical choice.

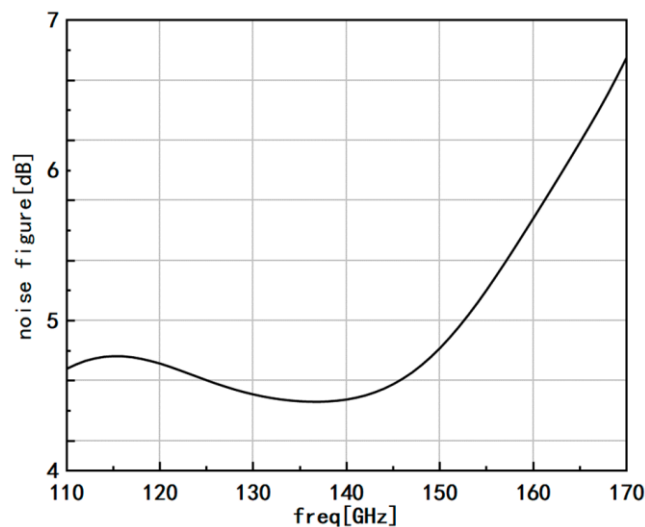


Figure 2.56: Noise performance of amplifier [89].

Conventionally, GaN is viewed as a power only technology. However, the same robustness that makes it attractive at K-band applies at W-band. GaN technology is pushing into the D-band, typically reserved for Indium Phosphide. While it may have a slightly higher noise figure, it offers massive survivability advantages. A W-band radar front-end using GaN can survive direct illumination from a nearby transmitter, whereas an InP LNA would require a bulky waveguide limiter that adds loss and weight. Recent breakthroughs have demonstrated GaN-on-Si transistors operating in D-band (110-170 GHz) [96]. While currently less performant than SiC-based devices, this proves the feasibility of low-cost, wafer-scale manufacturing for future 6G consumer devices.

SiGe and CMOS LNAs at D-band typically exhibit noise figures of 6 - 9 dB [94]. While inferior to III-V technologies, they enable the construction of Digital Radar chips where the LNA, mixer, and ADC are all on the same die. In massive phased-arrays (e.g., 1024 elements), the array gain ($10 \log N$) can compensate for the higher element noise figure, making Silicon the preferred choice for short-range automotive and consumer sensing applications.

On the other hand, for PA, generating RF power at 150 GHz is arguably the hardest challenge in mmWave electronics. As frequency increases, the gain per stage drops, needing multi-stage designs that degrade PAE. At D-band, passive component losses (transmission lines and matching networks) become severe. Skin effect losses increase with $\sqrt{f}$, and substrate coupling losses increase. Consequently, a sizeable portion of the power generated by the transistor is lost before it reaches the output pad.

At D-band frequencies, clear distinction performance between indium phosphide, gallium nitride, and silicon–germanium technologies in terms of achievable power, efficiency, and circuit complexity. Indium phosphide HBTs currently represent the state of the art in efficiency, offering high gain density that enables power amplifiers with relatively few stages, and recent demonstrations report saturated output powers in the range of 20 - 27 dBm with power-added efficiencies of 12 – 16 % at D-band [95].

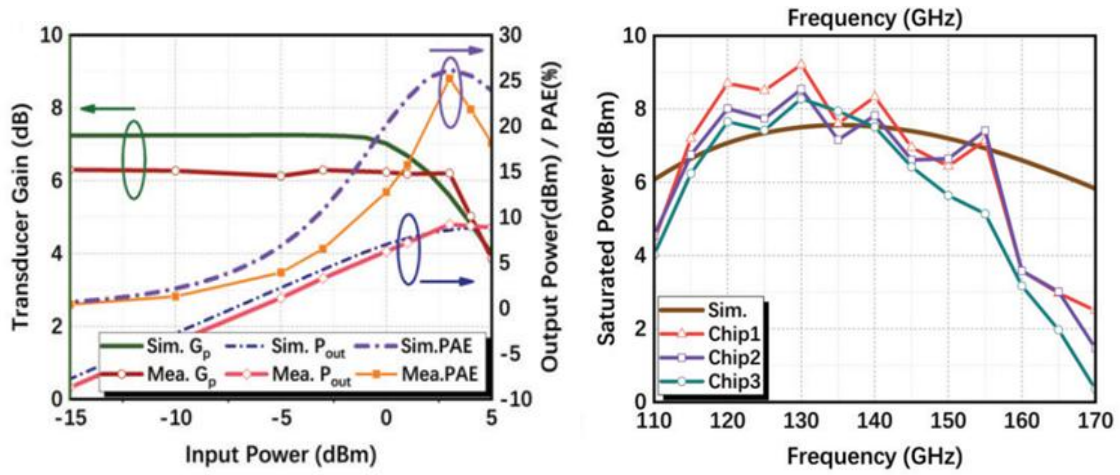


Figure 2.57: On-wafer measurements of the PA [95].

Gallium nitride HEMTs retain their intrinsic voltage handling advantage even as frequency increases toward W-band, delivering higher raw power density than InP, on the order of 1.5–2 W/mm, and enabling W-band power amplifiers with output power exceeding 30 dBm. However, the lower gain of GaN devices necessitates additional stages, and at D-band frequencies efficiency typically decreases from 5 to 10% because devices must be driven deeply into saturation to compensate for limited gain. Silicon–germanium HBTs, in contrast, are constrained by both breakdown voltage and device speed at D-band, resulting in relatively low output power levels of approximately 10 - 18 dBm and efficiencies in the 2 - 5% range, which confines their use to short-range links or to driver stages in heterogeneous systems that combine SiGe with higher-power III–V technologies [95].

2.5.5 System-level applications for satellite and 6G architecture

The selection of Ka-band and D-band technologies is ultimately a system-level optimization problem involving link budgets, atmospheric conditions, and process constraints.

One of the most promising application domains for D-band systems is inter-satellite links, where the vacuum of space eliminates atmospheric absorption effects that severely limit terrestrial millimeter-wave propagation. Shifting inter-satellite communications from K-band to D-band enables a dramatic reduction in antenna size for a given gain, since antenna gain scales with the square of the ratio between aperture diameter and wavelength. Consequently, a 30-cm antenna operating at D-band can provide comparable gain to a meter-class antenna at K-band, offering substantial benefits for size-, weight-, and power-constrained satellite platforms such as CubeSats [97]. From a technology perspective, indium phosphide power amplifiers are particularly attractive for D-band inter-satellite links due to their superior efficiency at low-to-moderate output power levels, where minimizing DC power consumption is critical in spaceborne systems. Gallium nitride devices, while dominant for

high-power terrestrial and downlink transmitters, are generally less competitive in this regime due to efficiency limitations at the extreme frequencies associated with D-band operation [97].

Another widely recognized application for D-band technology is terrestrial 6G backhaul, where the X-Haul paradigm envisions dense meshes of ultra-high-capacity wireless links interconnecting small cells and access points. At ground level, however, D-band propagation is strongly affected by atmospheric moisture absorption, which imposes severe path loss and requires very high transmitter effective isotropic radiated power to close links over practical distances on the order of a kilometer [98]. Because no single power amplifier can deliver the required radiated power at these frequencies, system architectures necessarily rely on large active electronically scanned arrays, in which output power is achieved through coherent spatial combining rather than device-level scaling. Technology selection in this context is driven by a trade-off between cost and per-element performance: although indium phosphide devices provide the highest performance at the element level, their cost and limited manufacturability make them unsuitable for large-scale deployment in street-level infrastructure. As a result, current trends favour silicon–germanium and gallium nitride on silicon beamforming solutions, where weaker individual amplifiers are compensated by high levels of integration and digital beamforming. In this spectrum of options, GaN-on-Si occupies a middle ground by offering higher per-element output power than SiGe, thereby reducing array size, while remaining substantially more cost-effective than InP or GaN-on-SiC technologies for massive D-band X-Haul deployments [98].

2.6 Summary

This chapter has presented a comprehensive literature review of Low-Noise Amplifiers (LNAs) and Power Amplifiers (PAs) across the K-band and W-band frequency ranges, alongside with an extended exploration of Ka-band and D-band, drawing upon a wide body of state-of-the-art research and industrial developments. The discussion has highlighted the vital role of these components in emerging millimeter-wave applications, including satellite communications, automotive radar and future 5G/6G infrastructures.

A comparative analysis of the surveyed literature reveals a bifurcated landscape defined by technological maturity and physical constraints. In the K-band and Ka-band (18 - 40 GHz), the industry has reached a prominent level of maturity. GaN-on-SiC has firmly set up itself as the dominant technology for power amplification in 5G infrastructure and satellite payloads, offering an order-of-magnitude advantage in power density over legacy GaAs. Consequently, the primary engineering challenge in this band has shifted from pure power generation to linearity enhancement,

using techniques such as deep Class-AB biasing and digital pre-distortion to accommodate spectrally efficient waveforms. On the other hand, GaAs is rapidly displacing SiGe and CMOS in robust LNA applications, offering limiter-less survivability that significantly helps the system-level noise figure.

Conversely, at the W-band (75 - 110 GHz) and D-band (110 - 170 GHz) frontier, design is defined by the struggle against gain roll-off and efficiency degradation. Indium Phosphide (InP) remains the unparalleled leader for ultra-low noise and high-efficiency amplification at these frequencies, making it indispensable for high-performance scientific and space applications. However, its cost structure challenges widespread commercial adoption. As a result, the 6G ecosystem is driving the development of GaN-on-Si for a balance of power and cost, and SiGe BiCMOS for high-integration phased arrays. Ultimately, the future of high-frequency communications lies not in the dominance of one material over another, but in the intelligent synthesis of their unique properties through heterogeneous integration, enabling systems that are simultaneously powerful, sensitive, and spectrally efficient.

These findings reveal persistent gaps in the current body of knowledge. There are few design frameworks that simultaneously optimise for ultra-low noise, high OP_{1dB} and high stable linearity within a single MMIC. Additionally, reliable co-design methods linking device-level models, biasing schemes and EM layout parasitics remain underrepresented, particularly regarding systematic reliability studies at high frequency bands. The insights gained from this literature review provide the motivation for the design methodology proposed in Chapter 3.

Chapter 3: Methodology

This chapter presents the comprehensive design methodology, process technology selection criteria, and simulation frameworks developed and employed in this thesis. Unlike lower-frequency RF design, where discrete component approximations and idealized transmission line models often suffice, the design of mm-wave MMICs demands a robust, full EM-simulated approach. This methodology must tightly integrate semiconductor device processes, nonlinear circuit theory, and full-wave electromagnetic (EM) analysis to predict and mitigate the parasitic effects that dominate circuit performance above 20 GHz.

The research methodology presented in this chapter relies on the strategic deployment of three complementary III-V compound semiconductor foundry processes, which are the 0.1- μm Gallium Arsenide (GaAs) pseudomorphic High Electron Mobility Transistor (pHEMT) process (WIN PP10-20), the 0.15- μm GaAs Enhancement/Depletion-mode pHEMT process (WIN PQG3-0C) and the 0.15- μm Gallium Nitride (GaN) on Silicon Carbide (SiC) HEMT process (UMS GH15-11). This heterogeneous technological approach leverages the intrinsic physical advantages of GaAs, which offers high electron mobility and low noise temperature for sensitive receiver and driver functions, while exploiting the wide bandgap and superior thermal conductivity of GaN-on-SiC for high-power amplification stages.

The following sections systematically detail the process characteristics, device modelling strategies (including the Angelov nonlinear formulation), small-signal and large-signal design flows, advanced stability analysis techniques (specifically the Ohtomo method), and the parasitic-aware layout optimization protocols that constitute the unified design framework of this thesis.

3.1 Process technologies

The selection of semiconductor process technology is the most critical decision in mm-wave MMIC design, establishing the fundamental boundaries for achievable gain, noise and power performance. At mm-wave frequencies, the designer must negotiate stringent trade-offs between transistor cutoff frequency (f_T) breakdown voltage (BV_{GD}) and thermal dissipation. This research adopts a best-in-class material strategy, assigning specific circuit functions to the semiconductor process best suited to their physical requirements.

Table 3.1 compares the technologies in terms of f_T/f_{max} , breakdown voltage, and applications to

clarify their selection.

Table 3.1: Technology comparison.

Technology	$f_T/f_{\max}$	Breakdown voltage (BV_{gd})	Application
GaAs pHEMT	100/150 GHz	$\sim 10 - 15$ V	LNAs, driver amplifiers
GaN-on-SiC	80/100 GHz	$\sim 40 - 100$ V	High power amplifiers (HPAs)
InP HEMT	200 / 300+ GHz	$\sim 4 - 6$ V	Ultra-Low Noise Rx, Sub-THz

3.1.1 WIN Semiconductors PP10-20 (0.1- μm GaAs pHEMT)

The WIN Semiconductors PP10-20 process represents a second-generation 0.1- μm gate length GaAs pHEMT technology optimized for high-frequency performance extending through the W-band and into the D-band [99]. It is an evolution of the mature PP10-10 process, incorporating advanced epitaxial growth techniques and device scaling to enhance frequency response without compromising reliability.

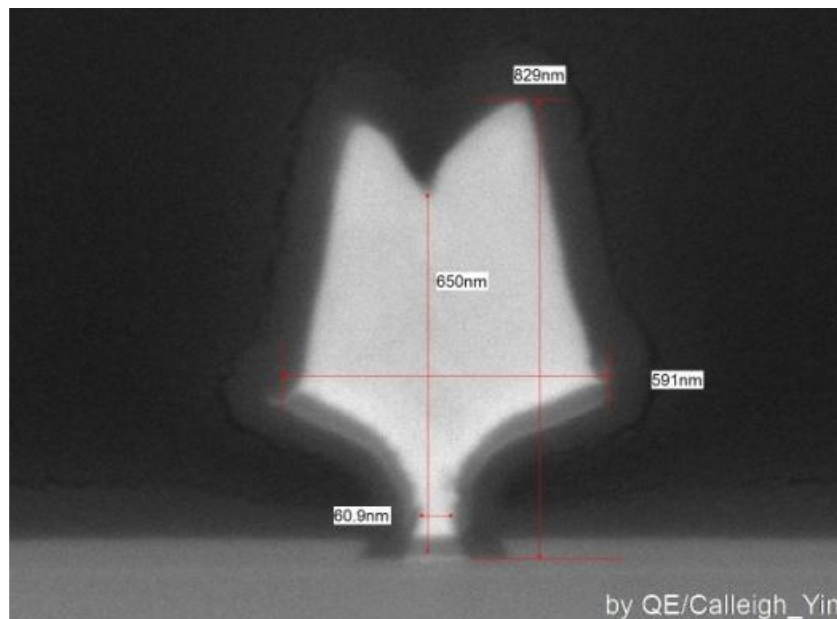


Figure 3.1: Cross-sectional SEM image of the high-stem 0.1 μm T-gate [99].

The core active device is a depletion-mode (D-mode) double-heterojunction pHEMT. The channel is formed by a strained InGaAs layer sandwiched between AlGaAs spacer layers, which confine the two-dimensional electron gas (2DEG). The high indium content in the channel enhances electron mobility (μ_n), which is critical for lowering the noise figure and increasing transconductance (g_m). The gate structure is defined using electron-beam lithography to achieve a T-shape cross-section, minimizing the gate resistance (R_g) while maintaining a short channel length of 100 nm. This reduction in R_g is vital for improving the maximum oscillation frequency (f_{max}) and minimizing thermal noise contribution from the gate metallization [100].

According to foundry specifications and independent verifications in the literature, the PP10-20 transistors typically achieve a unity current gain cutoff frequency (f_T) of approximately 160 GHz and an f_{max} of roughly 240 GHz [99], [100]. These requirements provide sufficient Maximum Available Gain (MAG) to support amplifier design well into the E-band (71 - 86 GHz). The process supports a drain bias of 4 V, balancing speed with a breakdown voltage sufficient for driver amplifier applications [99].

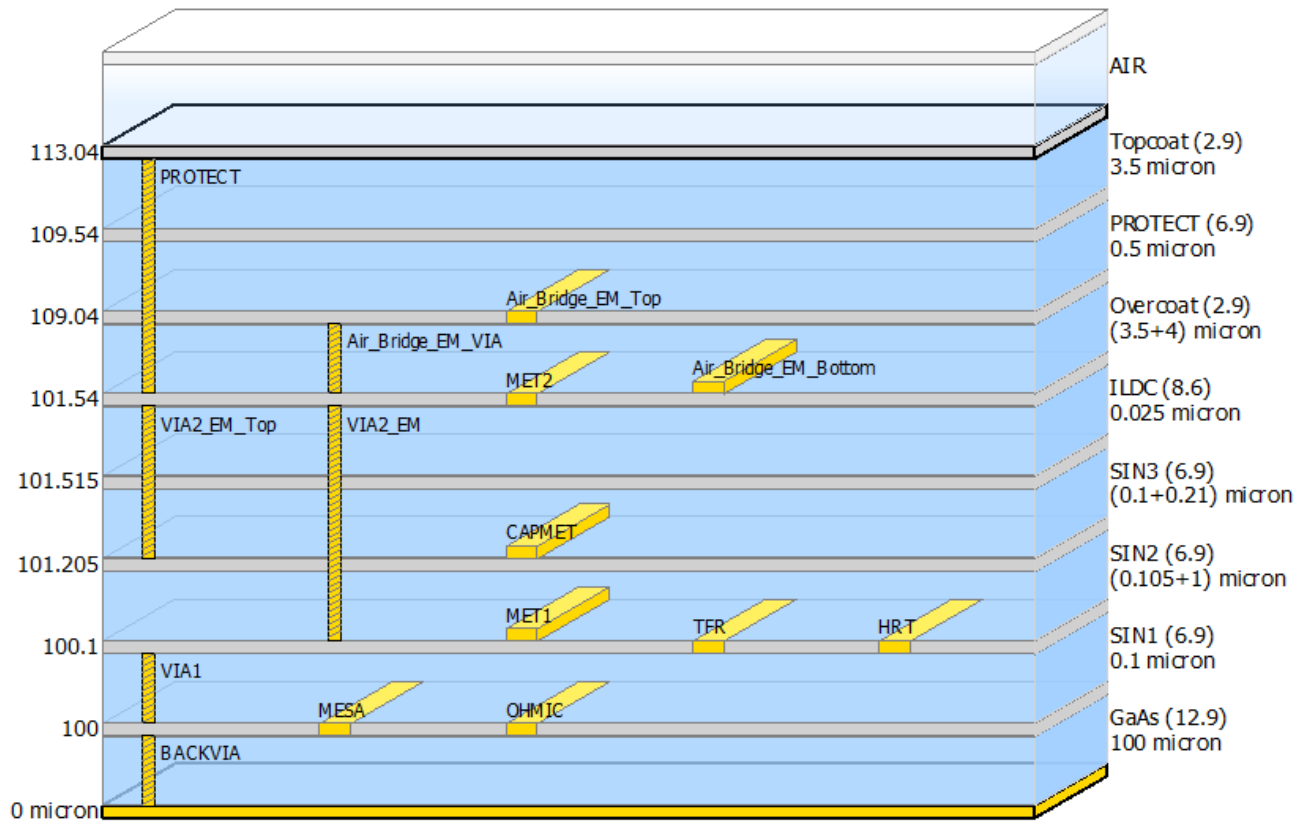


Figure 3.2: Process stack-up.

This process includes a robust backend-of-line (BEOL) process featuring two thick gold global

interconnect layers with air-bridge crossovers. Air bridges effectively reduce the parasitic capacitance between crossing lines, improving isolation and transmission line Q-factors at mm-wave frequencies. The process also offers high-density Metal-Insulator-Metal (MIM) capacitors ($\sim 565 \text{ pF/mm}^2$) [100], enabling compact inter-stage matching and effective supply decoupling networks essential for stabilizing high-gain multi-stage amplifiers. Crucially, the substrate is thinned to $50 \text{ }\mu\text{m}$ and features through-wafer vias (TWV) for low-inductance grounding. In mm-wave common-source amplifiers, source inductance acts as a negative feedback element that degrades gain; the TWV technology minimizes this degeneration, maximizing the usable gain at E-band frequencies.

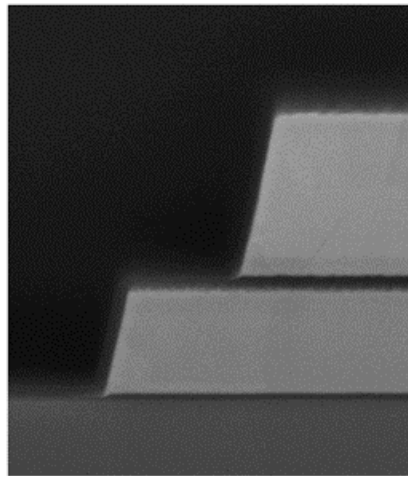


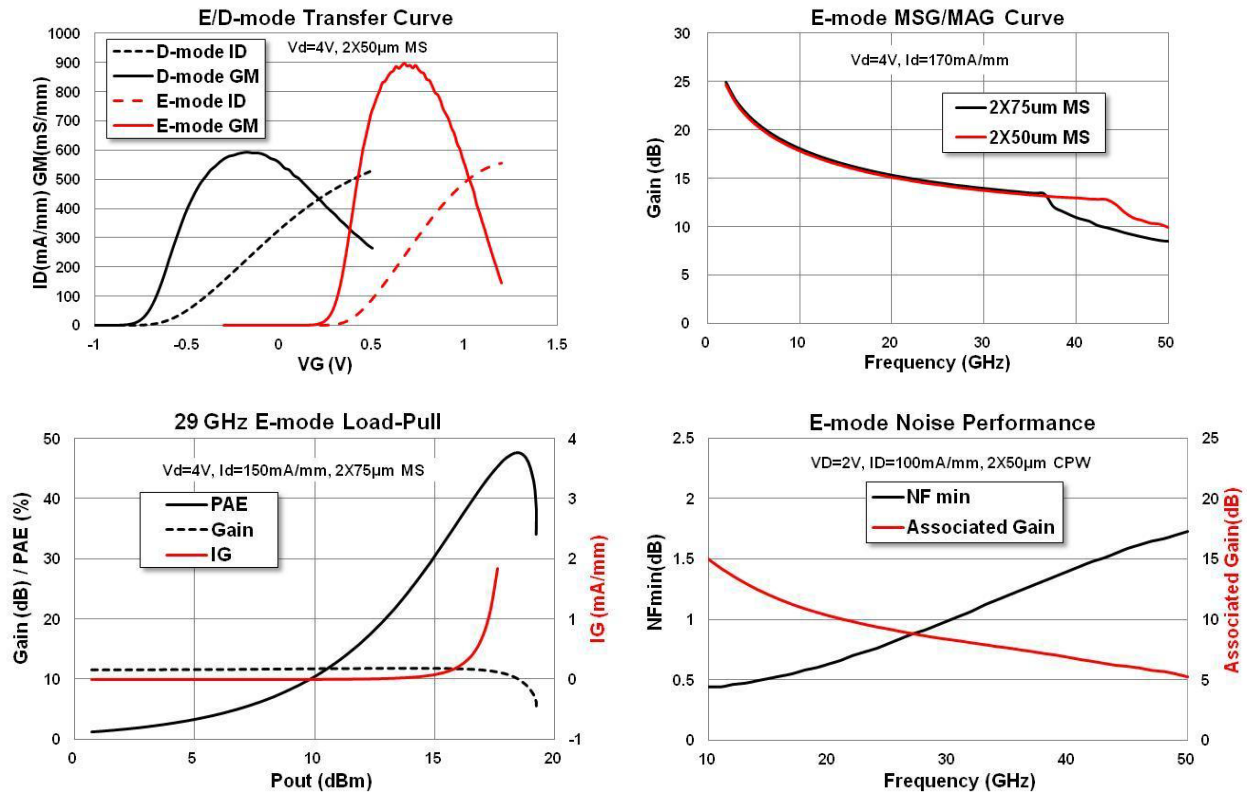
Figure 3.3: Standard MIM structure in PP10-20 technology [99].

The PP10-20 process is designated in this work for the design of high-frequency driver amplifiers in the lower W-band. Literature validates this choice, where AltumRF has reported an E-band LNA (71 - 86 GHz) achieving a noise figure of approximately 4 dB with 22 dB gain using this process [101]. Additionally, a 37 - 59 GHz LNA design demonstrated a noise figure of 2.5 dB, highlighting the process' suitability for wideband, low-noise applications [101]. These benchmarks inform the performance targets for the 75 - 85 GHz driver amplifiers developed in this thesis, where maximizing linearity and output power while maintaining low noise is the primary design objective.

3.1.2 WIN Semiconductors PQG3-0C (0.15- μm GaAs E/D-mode pHEMT)

For receiver front-ends operating in the K- and Ka-band, integration density and biasing simplicity become significantly important. The WIN PQG3-0C process offers a unique advantage by integrating both Enhancement-mode (E-mode) and Depletion-mode (D-mode) 0.15- μm pHEMTs on a single GaAs substrate [102]. This integration capability allows for sophisticated circuit topologies, such as single-supply LNAs and compact logic-control interfaces, directly on the RF die.

The fundamental difference between depletion-mode and enhancement-mode devices arises from the sign and magnitude of the threshold voltage V_{th} , which directly impacts biasing complexity and circuit integration. Depletion-mode devices are normally on and exhibit a negative V_{th} , requiring a negative gate-source voltage to pinch off the channel; although they typically offer higher drain current density, their use necessitates dual-polarity power supplies or active self-biasing circuits that reduce available voltage headroom, with the D-mode devices in the PQG3 process exhibiting a cutoff frequency of approximately 90 GHz [102]. Enhancement-mode devices, in contrast, are normally off and feature a positive V_{th} , conducting only when a positive gate-source voltage is applied, which significantly simplifies biasing by enabling the use of a single positive supply and a passive resistive divider while eliminating the need for negative voltage generation and its associated switching noise. This characteristic is particularly advantageous for low-noise amplifier design, and the E-mode pHEMTs in the PQG3 platform are specifically optimized for low-noise operation, achieving an f_T of roughly 110 GHz and minimum noise figures below 0.7 dB at 30 GHz [102].



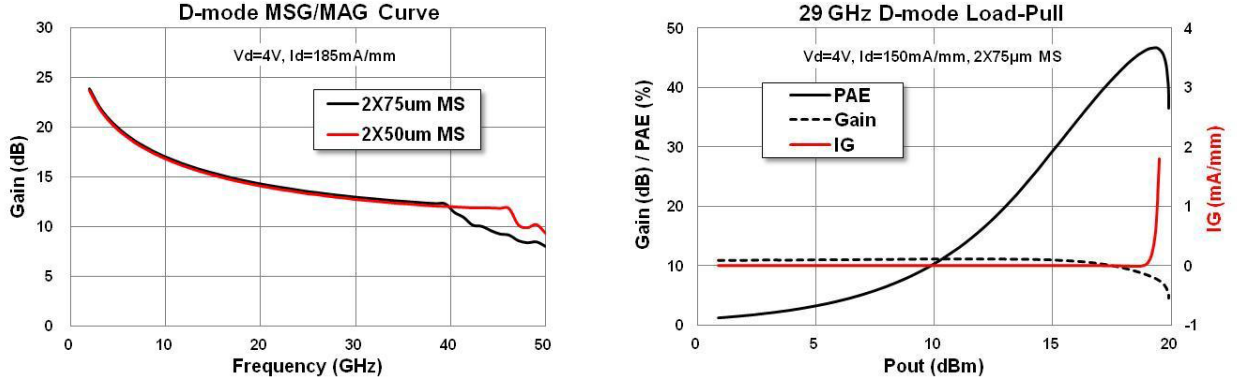


Figure 3.4: DC and RF characteristics of FET in PQG3-0C technology [102].

In this thesis, the PQG3-0C process is used to design a packaged positive single-supply LNA covering the 17 - 22 GHz band for space applications. The use of E-mode transistors in the primary gain stages simplifies the system-level power management architecture, a critical benefit for SATCOM phased arrays where thousands of elements are deployed. By removing the negative supply requirement, the routing complexity on the bias network is reduced, and the risk of device damage due to power sequencing errors (applying drain voltage before gate voltage) is eliminated. The design uses the superior transconductance efficiency g_m/I_D of the E-mode devices to achieve competitive noise figures with minimal DC power consumption.

3.1.3 UMS GH15-11 (0.15- μm GaN on SiC HEMT)

While GaAs provides in low-noise performance, its relatively low breakdown voltage limits its application in high-power output stages. To address the transmit power requirements of SATCOM and 5G transport networks, this research employs the GH15-11 process from United Monolithic Semiconductors (UMS), a 0.15- μm AlGaIn/GaN HEMT technology fabricated on a Silicon Carbide (SiC) substrate [103]. Gallium Nitride (GaN) is a wide-bandgap semiconductor ($E_g \approx 3.4$ eV) exhibiting a critical electric field higher than that of GaAs ($E_g \approx 1.42$ eV). This allows GaN transistors to operate at significantly higher drain voltages (typically 20–25 V in the GH15 process [103]) without suffering avalanche breakdown. The resulting high voltage swing, combined with high current density due to the piezoelectric 2DEG density, results in a power density of roughly 4.2 W/mm at 30 GHz [103], vastly outperforming GaAs pHEMTs (typically ~ 0.6 -0.8 W/mm).

However, high power density generates significant dissipated heat. The choice of SiC as the substrate is critical here, where SiC possesses a thermal conductivity ($\kappa \approx 350 - 490$ W/m·K) that is nearly

an order of magnitude higher than GaAs ($\kappa \approx 55 \text{ W/m}\cdot\text{K}$). This superior thermal path ensures that the junction temperature (T_j) remains within reliable limits even under continuous-wave (CW) operation, mitigating self-heating effects that would otherwise degrade mobility and reliability [104].

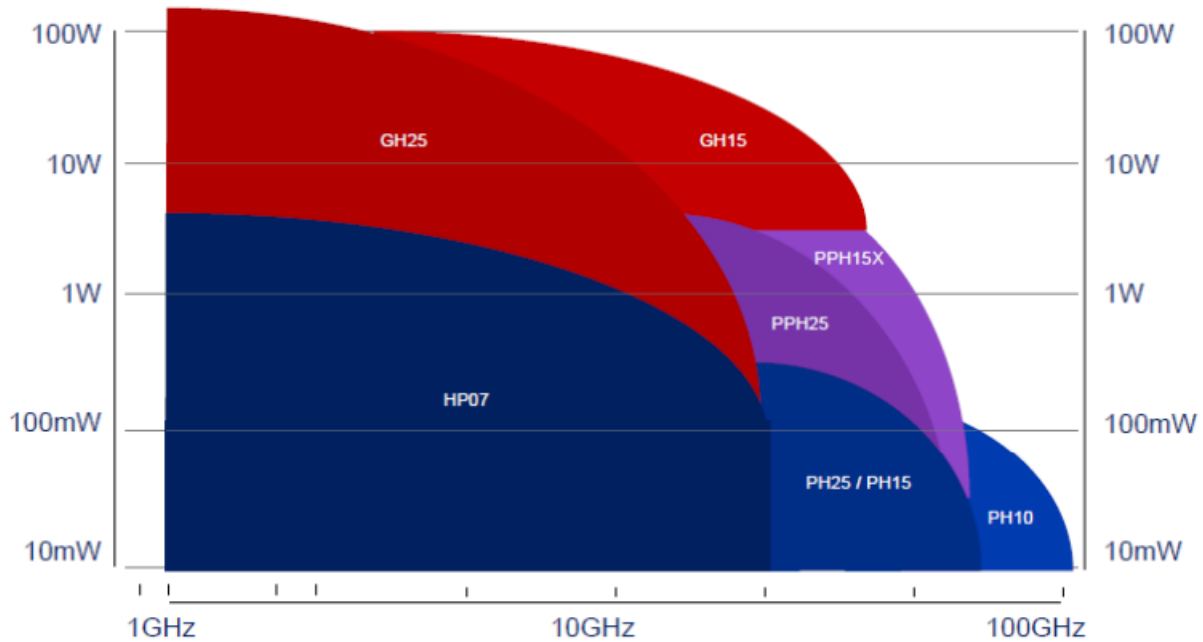


Figure 3.5: Achievable power and frequency range with UMS Foundry GaAs & GaN processes [103].

The GH15-11 process is qualified for operation up to 40 GHz [103]. It features a source-terminated field plate structure to reshape the electric field profile at the gate edge, reducing peak field intensity and minimizing trapping effects (current collapse) that can degrade dynamic linearity. The process includes precision Tantalum Nitride (TaN) resistors and high-density MIM capacitors (175 pF/mm^2) [103]. Its pedigree is derived from space-qualified processes, making it suitable for high-reliability applications where long operational lifetimes are required [103].

Table 3.2 illustrates the characteristics comparison among the processes.

Table 3.2: Comparative Analysis of Selected Foundry Processes.

Feature	WIN PP10-20	WIN PQG3-0C	UMS GH15-11
Material	GaAs pHEMT	GaAs E/D-pHEMT	GaN-on-SiC HEMT
Gate length (L_g)	$0.1 \mu\text{m}$	$0.15 \mu\text{m}$	$0.15 \mu\text{m}$
Transit Freq (f_T)	$\sim 160 \text{ GHz}$	$\sim 110 \text{ GHz}$ (E-mode)	$\sim 35 \text{ GHz}$
Max Ocs.Freq (f_{max})	$\sim 240 \text{ GHz}$	$\sim 90 \text{ GHz}$ (D-mode)	$\sim 100 \text{ GHz}$

Typical bias (V_{DD})	4 V	4 V	20 – 25 V
Power density	$\sim 0.6\text{W/mm}$	$\sim 0.6\text{W/mm}$	4.2W/mm
Design in this thesis	W-band Driver Amplifier	K-band Single-Supply LNA	K-band High-Power PA

3.2 Device modelling and characterization

Accurate simulation of mm-wave circuits requires device models that remain valid well beyond the fundamental operating frequency. This research employs a comprehensive modelling strategy that integrates small-signal extraction, noise parameter characterization, and large-signal nonlinear modelling.

3.2.1 Small-signal modelling

The basis of linear RF circuit analysis is the small-signal equivalent circuit, which for both GaAs and GaN transistors is composed of extrinsic parasitic elements and intrinsic device elements. The extrinsic network accounts for gate, drain, and source inductances, contact resistances, and pad capacitances, typically denoted by L_g , L_d , L_s , R_g , R_d , R_s , and C_{pg} , C_{pd} , which are usually extracted from cold-FET measurements with $V_{DS} = 0$ and are treated as largely bias independent [100]. At millimeter-wave frequencies, accurate de-embedding of these parasitics is essential because their reactances become comparable to the intrinsic device impedances, strongly influencing gain and stability. The intrinsic elements describe the active behavior of the transistor and include the transconductance g_m , output conductance g_{ds} , and junction capacitances C_{gs} , C_{gd} , and C_{ds} , all of which vary with bias and are extracted from hot-FET S-parameter measurements over the intended operating range. For GaN technologies in particular, careful modeling of the substrate network is required, as the conductive SiC substrate and buffer interfaces introduce frequency-dependent loss and capacitance that significantly affect output matching and large-signal behavior, especially the accurate prediction of S_{22} and output power at high frequencies [107].

The performance of the active device at high frequencies is governed by these small-signal parameters. The intrinsic transconductance (g_m) and output conductance (g_{ds}) are defined mathematically as the partial derivatives of the drain current with respect to the control voltages:

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}=\text{constant}}$$

$$g_{ds} = \left. \frac{\partial I_{ds}}{\partial V_{ds}} \right|_{V_{gs}=\text{constant}} = \frac{1}{R_{ds}}$$

Two critical figures of merit derived from the small-signal equivalent circuit define the device's high-frequency capabilities: the unity-current-gain cutoff frequency (f_T) and the maximum oscillation frequency ($f_{\max}$).

The cutoff frequency, representing the intrinsic transit time limitation, is approximated by the transconductance and the total gate capacitance:

$$f_T \approx \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

The maximum oscillation frequency, which is the frequency at which the Maximum Available Gain (MAG) drops to unity (0 dB), provides a more comprehensive metric for MMIC design as it includes parasitic resistive losses and feedback. It is approximated by:

$$f_{\max} \approx \frac{f_T}{2\sqrt{g_{ds}(R_g + R_i + R_s) + 2\pi f_T R_g C_{gd}}}$$

During the design process, these equations emphasize the necessity of minimizing gate resistance (R_g) and feedback capacitance (C_{gd}) through proper layout and device sizing to ensure sufficient gain at K-band and W-band frequencies.

3.2.2 Noise modelling

Accurate noise simulation is a central requirement in low-noise amplifier design, particularly at millimeter-wave frequencies where device noise mechanisms strongly influence overall receiver performance. Two principal noise modelling approaches are commonly employed for FET-based technologies. The Pospieszalski noise model represents device noise by assigning equivalent noise temperatures to the intrinsic gate resistance and the drain conductance, denoted by T_g and T_d , respectively, and has proven to be robust and widely applicable across a range of FET processes. In this formulation, the drain noise temperature exhibits a strong dependence on drain current and is typically extracted from measured noise parameters such as the minimum noise figure, noise resistance, and optimum source reflection coefficient [111]. In contrast, the Pucel–Haus–Statz, or PRC, model is frequently provided by foundries for GaAs processes, including those from WIN, and explicitly accounts for the correlation between gate and drain noise current sources through a correlation coefficient. This correlation becomes increasingly important in short-channel devices

operating at millimeter-wave frequencies, where neglecting it can lead to significant errors in predicted noise performance [110].

The minimum Noise Figure ($NF_{\min}$) is fundamentally governed by the device parasitics and can be approximated as:

$$NF_{\min} \approx 1 + 2\pi f K_f C_{gs} \sqrt{\frac{R_g + R_s}{g_m}}$$

where K_f is a technology-dependent fitting factor, C_{gs} is the gate-source capacitance, R_g and R_s are the gate and source resistances, and g_m is the transconductance.

3.2.3 Large-signal nonlinear modelling

For large-signal PA design, where the transistor swings across cutoff, linear, and saturation regions, a robust nonlinear model is required. This thesis employs the Angelov (Chalmers) model [106], which is widely regarded as the industry standard for modelling HEMTs.

The Angelov model's strength lies in its use of continuous, infinitely differentiable functions (primarily hyperbolic tangents) to describe the drain current (I_{ds}) and its derivatives (g_m, g_{ds}). The core current equation is formulated as [106]:

$$I_{ds} = I_{pk}(1 + \tanh(\psi)) \tanh(\alpha V_{ds}) (1 + \lambda V_{ds})$$

where ψ is a power series function of the gate voltage (V_{gs}) and drain voltage (V_{ds}), I_{pk} is the current at maximum transconductance, and α determines the saturation knee voltage.

The differentiability of the tanh function is critical for the convergence of Harmonic Balance (HB) simulators, which rely on Newton-Raphson iteration involving the Jacobian matrix of the circuit. Furthermore, accurate modelling of the higher-order derivatives of I_{ds} (specifically g_m'') is essential for predicting intermodulation distortion (IMD3) and spectral regrowth in 5G signals [106]. The model also captures the nonlinear behaviour of the intrinsic capacitances (C_{gs} and C_{gd}) using similar empirical functions. In GaN devices, the C_{gd} nonlinearity is a significant contributor to AM-PM conversion, and its accurate representation is validated against large-signal measurements [108].

3.2.4 Thermal and trapping effects in GaN

Gallium nitride HEMTs exhibit two key physical effects that must be captured accurately to ensure reliable circuit-level prediction, particularly under large-signal and high-power operation. Owing to their high power density, significant self-heating occurs during operation, causing the channel temperature to rise and consequently reducing electron mobility and drain current; to address this, the GH15-11 model incorporates a dedicated thermal subcircuit consisting of a thermal resistance and capacitance, which computes the instantaneous channel temperature from the dissipated power $P_{\text{diss}} = V_{ds} \cdot I_{ds}$ and dynamically updates the electrical parameters accordingly [104], [107]. In addition to thermal effects, GaN devices are susceptible to charge trapping phenomena, where carriers become trapped in surface states or buffer-layer defects, giving rise to gate lag and drain lag that manifest as current collapse and DC–RF dispersion. This dynamic behavior is modeled through effective gate and drain voltages that are altered by bias-dependent RC time constants representing the capture and emission processes of the traps, enabling the model to reproduce transient and frequency-dependent degradation detected in practical GaN circuits [107].

In GaN HEMTs, charge trapping at the surface and buffer interfaces leads to gate and drain lag effects, where the drain current responds slowly to pulsed RF excitations. This trapping temporarily restricts the available 2-dimensional electron gas (2DEG) density, leading to dynamic $R_{ds(\text{on})}$ degradation (an increase in the device's on-resistance under large RF voltage swings). This dynamic phenomenon reduces the achievable output power and PAE compared to static DC predictions, making conservative biasing and thermal-aware EM layout essential.

3.3 Low-Noise Amplifier (LNA) design method

The design of the LNA sets the sensitivity limit for the entire receiver chain. The methodology employs a structured approach starting with bias selection, followed by simultaneous noise and input matching (SNIM), and culminating in linearity optimization.

3.3.1 Biasing strategies: single supply and multiple supply

The biasing network establishes the DC operating point (V_{GS} , V_{DS} , I_D) and must isolate the RF signal path from the power supply.

Standard D-mode designs typically use a negative gate voltage (V_{GG}) and positive drain voltage (V_{DD}). While offering independent control, this requires negative voltage generators (e.g., charge pumps) which introduce switching noise and increase board area. Furthermore, punctilious power sequencing

circuits are needed to ensure V_{GG} is applied before V_{DD} to prevent the normally-on device from drawing excessive current and burning out [102].

Standard depletion-mode (D-mode) LNAs require a negative gate voltage and a positive drain voltage, necessitating complex power sequencing circuits (to ensure gate bias is applied before drain bias) and negative voltage generators that introduce switching noise. By contrast, the use of enhancement-mode (E-mode) devices allows for a true single-supply topology. The gate can be biased directly from the positive supply rail using a simple resistive divider, eliminating the need for negative bias generation, saving board area, and eliminating the risk of sequence-related burn-out.

To address biasing complexity and survivability concerns, the K-band LNA designs in this thesis adopt enhancement-mode devices from the WIN PQG3 process, which feature a positive threshold voltage and therefore allow the gate to be biased directly from the positive supply rail using a simple resistive divider [102]. This approach enables a true single-supply topology that is fully compatible with standard low-voltage CMOS logic levels, such as 3.3 V or 5 V, eliminating the need for negative bias generation. The gate bias voltage is nominally set by a resistor pair, while sensitivity to process-induced threshold voltage variations is mitigated through the inclusion of active stabilization mechanisms such as current mirrors or feedback-based bias networks, although their use in LNAs requires careful consideration due to potential noise injection [109]. To preserve low-noise performance, the bias network is therefore heavily filtered, with high-value resistors used in the bias tee to present a large RF impedance and minimize gain degradation, and large bypass capacitors employed to shunt bias-related noise to ground. This combination of resistive biasing, optional active stabilization, and aggressive filtering provides a practical and low-noise biasing solution for Ka- and K-band LNAs implemented in enhancement-mode GaAs pHEMT technologies [109].

3.3.2 Simultaneous noise and input matching theory

The receiver sensitivity of a satellite terminal or 5G base station is critically dependent on the first stage of the LNA. The Friis formula for noise dictates that the noise figure of the first component dominates the entire system noise. The total Noise Factor (F) of cascaded stages is:

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \dots$$

Another fundamental challenge in LNA design is that the source impedance required for minimum noise figure (Z_{opt}) is rarely the complex conjugate of the device input impedance (Z_{in}^*) required for

maximum gain and power transfer. In a generic Common Source (CS) amplifier, matching for $NF_{\min}$ typically results in poor input return loss (S_{11}).

To resolve this, the Inductive Source Degeneration technique is carefully applied. By inserting an inductor (L_s) in series with the source, a real part is synthesized in the input impedance without adding a noisy resistor [110], [111]:

$$Z_{in} \approx \frac{g_m L_s}{C_{gs}} + j \left(\omega(L_s + L_g) - \frac{1}{\omega C_{gs}} \right)$$

where L_g is the series gate inductance. The term $\frac{g_m L_s}{C_{gs}}$ represents a noiseless resistance that can be tuned to 50 Ω . Crucially, this feedback mechanism modifies Z_{opt} and moves it closer to Z_{in}^* , allowing for Simultaneous Noise and Input Matching (SNIM) [110], [113]. For the mm-wave designs, L_s is realized using short microstrip transmission lines or through-wafer vias (in the case of minimal degeneration).

The design procedure begins with selecting a proper gate width to position the optimum noise resistance close to 50 Ω , thereby simplifying source matching at the input. Once the device size is fixed, source inductance is introduced to raise the real part of the input impedance toward 50 Ω while simultaneously improving noise performance through controlled feedback. Finally, a gate inductance is added to resonate the remaining capacitive reactance of the input, completing the impedance transformation and enabling simultaneous noise and power matching at the design frequency.

3.3.3 Linearity enhancement techniques

Although minimizing noise figure remains the primary objective in LNA design, linearity is equally critical in 5G transport networks to prevent receiver desensitization caused by strong adjacent-channel interferers. One widely adopted approach to improving linearity is derivative superposition, in which an auxiliary transistor is placed in parallel with the main amplifying device and biased in weak inversion so that its third-order transconductance derivative is positive, thereby compensating for the negative third-order nonlinearity of the main device, which operates in strong inversion [109]. In addition to architectural techniques, careful bias optimization plays an important role, as load-pull and nonlinear simulations can be used to identify gate-bias operating points where the third-order transconductance derivative approaches zero or is minimized, leading to a significant improvement in output third-order intercept point without substantially degrading noise performance.

3.3.4 Broadband matching and bandwidth extension

Achieving the wide bandwidths required by 5G systems cannot be accomplished using simple narrowband LC matching techniques, prompting the use of more advanced matching strategies. In this work, the input and output networks are synthesized as multi-pole bandpass filters with responses such as Chebyshev or Butterworth, where the intrinsic device parasitics, including C_{gs} and C_{ds} , are deliberately absorbed into the filter structure to extend bandwidth without excessive loss [120]. In addition, frequency-selective feedback networks including resistive, inductive, and capacitive elements are introduced between the drain and gate to further flatten the gain response and improve bandwidth, accepting a modest degradation in noise figure as a trade-off for enhanced wideband performance [120].

3.4 Power amplifier (PA) design method

The PA methodology focuses on maximizing Power Added Efficiency (PAE) and output power (P_{sat}) while maintaining linearity for modulated signals.

3.4.1 Load-Pull simulation

For power amplifier operation, the load condition that yields maximum performance is not the small-signal conjugate match but a power-matched impedance that enables the largest possible voltage and current swing at the device terminals. To identify this operating point, harmonic-balance load-pull simulations are employed in which the load reflection coefficient is swept across the Smith chart and contours of constant output power and power-added efficiency are generated, with the design target typically chosen near the intersection of the maximum power and maximum efficiency regions [112]. Beyond the fundamental load impedance, further efficiency enhancement is achieved through deliberate harmonic termination, where the impedances presented at higher-order harmonics are controlled to shape the voltage and current waveforms. For instance, enforcing a short circuit at even harmonics and an open circuit at odd harmonics approximates a square-wave voltage characteristic of Class-F operation, which can theoretically lead to substantial improvements in efficiency [112].

3.4.2 Operational classes

The GaN power amplifiers developed in this thesis are designed to operate in class-AB and continuous class-J/F regimes in order to balance efficiency, linearity, and bandwidth. Class-AB operation, achieved by biasing the device slightly above pinch-off, provides a well-established compromise between linearity and efficiency and remains the standard choice for analogue and moderately linear RF power amplifiers. For wideband operation, however, enforcing strict harmonic terminations associated with traditional classes such as Class-F becomes impractical, prompting the

use of continuous modes. Continuous class-J and class-F concepts relax the harmonic impedance requirements by allowing a range of reactive terminations that preserve high efficiency across frequency, effectively expanding the design space from a single optimum point to a continuum of acceptable solutions suitable for broadband GaN PA implementations [113].

3.4.3 Power combining strategies

Achieving output power levels beyond the capability of a single transistor, such as exceeding 10 W at K-band, necessitates the use of power-combining techniques. In this context, corporate combining architectures based on Wilkinson dividers or Lange couplers are commonly employed to distribute drive power to multiple parallel amplifier paths and coherently recombine their outputs. A key challenge in such structures is current generated at terminals, where non-uniform current distribution can lead to localised heating and electromigration-induced failure. This issue is addressed through detailed electromagnetic simulations that visualize current density and guide the use of tapered transmission lines and optimized junction geometries to equalize current flow [114]. In addition to thermal and reliability concerns, parallel amplifier configurations are susceptible to odd-mode, or push-pull, oscillations in which branches operate out of phase, and this instability is suppressed by introducing isolation resistors between combining paths to provide damping and ensure stable operation [114].

For balanced amplifier topologies, effective power dividing and combining are essential to maximize output power while maintaining favorable input and output return losses. In this work, the Lange coupler was selected as the primary passive combining structure.

The Lange coupler is a quadrature (90-degree) directional coupler constructed from interdigitated microstrip lines. Standard two-line edge-coupled microstrip couplers cannot practically achieve the tight 3-dB coupling required for an equal power split, because the physical gap between the lines would be impractically small to manufacture on standard GaAs or GaN substrates. The Lange coupler circumvents this limitation by utilizing four or more parallel coupled lines. Alternate lines are tied together using gold bond wires or air bridges to equalize the phase velocities of the even and odd modes. This interdigitated geometry drastically increases the mutual coupling area, allowing a 3-dB power split to be realized with manufacturable line spacings.

The Lange coupler was chosen over alternative combining structures, such as Wilkinson power dividers and branch-line couplers, for several critical reasons regarding millimeter-wave MMIC design:

Interdigitated couplers natively offer an octave or more of bandwidth for both amplitude balance and phase quadrature. In contrast, standard Wilkinson dividers and branch-line couplers are generally narrow-band, resonant structures limited by quarter-wavelength ($\lambda/4$) transmission line sections.

Because the Lange coupler introduces a 90-degree phase difference between its coupled and through ports, signals reflected from the individual amplifier stages experience a 180-degree phase shift when they return to the input port. Consequently, the reflected waves cancel out at the input and are safely dissipated in the 50 Ω isolation resistor. This provides excellent broadband input and output Voltage Standing Wave Ratio (VSWR), even if the individual transistor matches are imperfect. A standard Wilkinson divider (which is an in-phase divider) does not provide this inherent VSWR absorption at the input.

At K-band and W-band frequencies, a branch-line coupler occupies a substantial footprint on the semiconductor substrate. The folded, interdigitated structure of the Lange coupler makes it highly compact, minimizing expensive MMIC die area and reducing passive insertion loss prior to the active stages.

To ensure accuracy in the balanced designs, full 2.5D/3D electromagnetic (EM) simulations of the Lange couplers were utilized. This was necessary to correctly account for the parasitic inductances of the crossover air-bridges and the fringing capacitances at the open-ended finger terminations, which standard schematic models fail to capture at millimeter-wave frequencies.

3.4.4 Linearity vs efficiency trade-off

GaN devices exhibit soft compression, where gain decreases gradually as power increases. To maintain linearity (EVM) for 64-QAM signals, the PA must typically be operated at 6 - 8 dB back-off from saturation. To improve efficiency at back-off, techniques like dynamic bias modulation or Doherty architectures are considered, although the primary focus of the MMIC design here is on improving the core amplifier's intrinsic linearity through bias and harmonic termination [112].

3.5 Stability analysis and stabilization networks

Ensuring unconditional stability is paramount, as mm-wave MMICs are prone to oscillations due to high gain and parasitic feedback paths.

3.5.1 Classical stability criteria (Rollet and μ -factor)

The initial screening uses the Rollett K-factor ($K > 1$) and the geometric stability factor μ ($\mu > 1$) [115], [116]. The μ -factor is preferred as it provides a single necessary and sufficient condition for unconditional stability [116]:

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1$$

However, these criteria assume the device itself is stable and only check for stability under passive source/load terminations. They often fail to detect internal loop oscillations in multi-stage or parallel-combined architectures.

3.5.2 Loop-gain analysis: Ohtomo method

To overcome the limitations of conventional K-factor stability analysis, the Ohtomo loop-gain method is employed as a more rigorous tool for detecting potential instabilities in complex RF circuits [117], [118]. This approach treats the circuit explicitly as a feedback system by breaking it at a critical node, such as the gate of a transistor, and evaluating the resulting closed-loop transfer function in simulation. Stability is then assessed using the Nyquist criterion, where instability is indicated if the loop-gain trajectory encircles the critical point at $1 + j0$ in the complex plane. This method is particularly effective for identifying odd-mode oscillations in power-combined stages, where conventional K-factor analysis may incorrectly predict stability while internal feedback paths between parallel devices remain unstable. In addition, the loop-gain technique enables the detection of parametric oscillations that arise only under large-signal excitation, driven by nonlinear capacitance modulation at specific input power levels, making it well suited for validating stability in high-power and broadband amplifier designs [118].

3.5.3 Bias network stability and low-frequency oscillation

A common failure case in mm-wave MMICs is low-frequency oscillation (LFO) in the MHz range. This occurs because the high-frequency transistors have massive gain at low frequencies, and the bias networks (RF chokes) can present inductive impedances that resonate with decoupling capacitors. To suppress this, de-Qing resistors are placed in series with the gate bias lines or in parallel with the drain chokes. These resistors are sized to be transparent at RF (where the choke impedance is high) but lossy at low frequencies, damping any potential resonances [119].

3.6 Electromagnetic (EM) simulation and layout optimization

At higher frequencies like K-band and W-band, the schematic simulation of passive components is not always accurate. A parasitic-aware design method is mandatory.

All circuit and electromagnetic co-simulations in this methodology were performed using Keysight Advanced Design System (ADS), utilizing Momentum for 2.5D planar EM extraction and EMPro for full 3D full-wave electromagnetic simulations of critical packaging structures and transitions.

3.6.1 Parasitic and coupling aware design flow

The overall design methodology follows a schematic–layout–EM–schematic workflow to ensure correct prediction of circuit performance at millimeter-wave frequencies. The process begins with an ideal schematic-level design using lumped or ideal transmission-line elements to set up the target gain, bandwidth, and matching conditions. These ideal components are then progressively replaced with foundry-provided PDK models that include substrate parasitics and loss mechanisms, providing a more realistic representation of circuit behaviour. Once the schematic is validated, the complete physical layout is implemented, incorporating all active devices, passive components, interconnects, tapers, and T-junctions. The passive network is later extracted and simulated using a three-dimensional planar electromagnetic solver, which captures coupling effects between adjacent structures as well as frequency-dependent substrate and conductor losses [105]. Finally, the resulting S-parameter representations of the passive structures are reintegrated into the schematic-level simulator and co-simulated with the nonlinear active device models, allowing the circuit to be re-optimized in the presence of electromagnetic effects and ensuring robust agreement between simulated and measured performance.

3.6.2 EM simulation setup and mesh density

Accurate electromagnetic simulation demands careful attention to solver setup in order to obtain reliable results at millimeter-wave frequencies. Port calibration is performed using transmission-line calibration techniques to de-embed port discontinuities and ensure that the simulated reference planes accurately represent the intended circuit interfaces. In addition, the mesh density is defined based on the highest harmonic of interest, such as the third harmonic of an 80 GHz signal at 240 GHz, to guarantee sufficient spatial resolution for precise current and field modelling. Edge meshing is explicitly enabled to capture the elevated current density that arises along microstrip conductor edges due to skin effect, which becomes increasingly significant at high frequencies and strongly influences loss and impedance accuracy [105].

3.6.3 Thermal awareness

For the GaN power amplifier, thermal management is treated as an integral part of the layout design

rather than a post-processing consideration. The spacing between gate fingers is carefully optimized to minimize thermal cross-talk and prevent localized hot spots that can degrade performance and reliability. In addition, the GH15 process enables the placement of individual source vias beneath each source finger, or as close as physically possible, creating a low-thermal-resistance path from the active region to the SiC substrate and ultimately to the package heat sink [103]. The effectiveness of these measures is verified through electro-thermal simulations using tools such as ADS Electro-Thermal or ANSYS Icepak, which confirm that the peak channel temperature remains below typical reliability limits of approximately 200 °C even under worst-case power dissipation conditions [104].

3.7 Summary

This chapter has established a detailed, multi-disciplinary design flow for 5G transport networks and SATCOM MMICs. By synergising the low-noise capabilities of GaAs (PP10-20, PQG3) with the high-power density of GaN-on-SiC (GH15-11), the inherent material limitations are overcome. The methodology moves beyond simple S-parameter design to incorporate advanced nonlinear modelling (Angelov), robust stability analysis (Ohtomo), and full-wave EM simulation. This holistic approach ensures that the theoretical performance of the semiconductor technologies is fully realized in the final MMIC implementations, minimizing the risk of design slippages and ensuring first-pass success. The specific circuit implementations resulting from this methodology are detailed in the subsequent chapters.

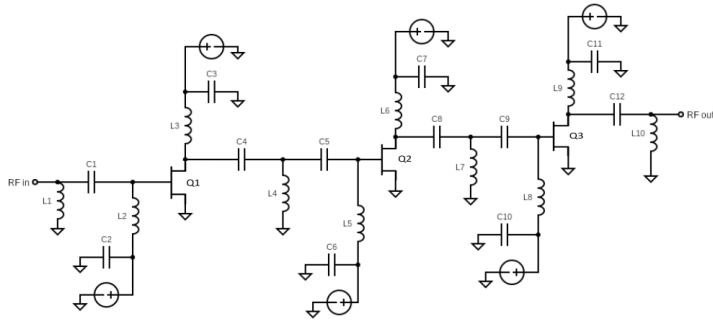
Chapter 4: W-band GaAs Driver Amplifiers

This chapter describes the first set of MMIC amplifier designs developed in this thesis using the WIN Semiconductor PP10-20 GaAs pHEMT process, targeting operation over the 75 - 85 GHz frequency range. The design work begins with a single-ended driver amplifier, which is intentionally kept simple and used to establish the overall design flow and to validate the initial device models and matching approach. Based on the experience gained from this first implementation, a revised single-ended amplifier is then developed using an updated transistor model, allowing a more reliable assessment of circuit performance across the frequency band. Finally, the revised single-ended amplifier is extended to a balanced amplifier structure in order to improve broadband behaviour and tolerance to load mismatch, which are critical requirements for practical 5G transport networks and SATCOM front-end applications. These designs make use of in-house linear FET model provided by AltumRF.

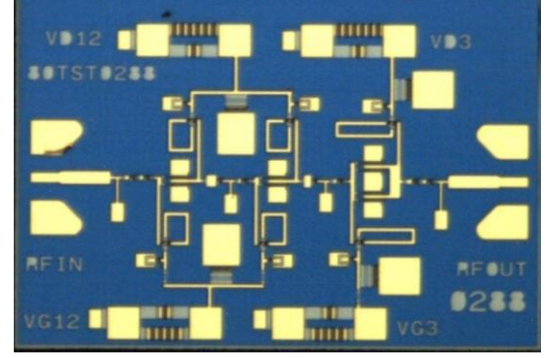
4.1 First design of the Driver Amplifier

The first driver amplifier design presented in this chapter is a three-stage depletion mode MMIC targeting operation over the 75 - 85 GHz frequency range. To balance low noise performance with sufficient output power, the selected FET device sizes for the three stages are $2 \times 50 \mu\text{m}$, $2 \times 50 \mu\text{m}$, and $4 \times 50 \mu\text{m}$, respectively. A consistent biasing strategy is employed, with all gate bias networks routed toward the south of the layout and all drain bias networks toward the north, resulting in a compact and well-organized implementation. The amplifier is unconditionally stable across the operating band and occupies a chip area of only $1.2 \times 0.76 \text{ mm}^2$, including all RF and DC pads. Under nominal bias conditions, the circuit draws 100 mA from a 4 V supply. Figure 4.1 shows the schematic of the driver amplifier together with the microscope die photograph.

The measured results demonstrate solid overall performance of the first driver amplifier. At nominal bias, a small-signal gain of 18.8 dB is achieved, with both input and output return losses (S_{11} and S_{22}) remaining below -10 dB across the operating band. The measured noise figure ranges from 4 dB to 5.2 dB. Large-signal performance at 76 GHz shows a measured output power of 17 dBm, with a maximum value of 17.7 dBm obtained at a drain current of 65 mA.



(a)

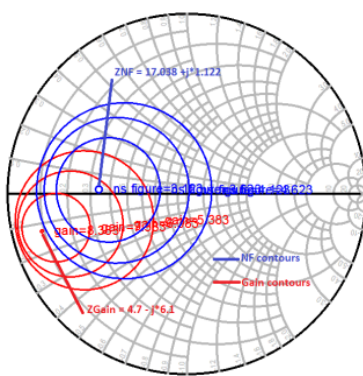


(b)

Figure 4.1: (a) Schematic diagram of the proposed driver amplifier, (b) Die-photo of the amplifier.

4.1.1 Noise figure, power and bias network analysis

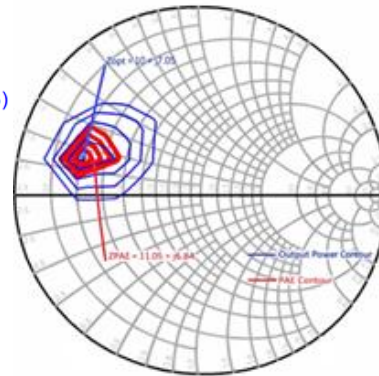
Noise and power are analysed using device sizes optimized for each requirement. After analysing several device sizes to satisfy the design requirements, a $2 \times 50 \mu\text{m}$ and a $4 \times 50 \mu\text{m}$ transistor were chosen. Noise analysis is performed on a $2 \times 50 \mu\text{m}$ transistor, where small-signal gain and noise performance use noise-source pull to identify the source impedance region that minimizes noise figure while maintaining sufficient gain. Power analysis is carried out on a $4 \times 50 \mu\text{m}$ transistor using large-signal load-pull measurements to extract output power and efficiency as a function of load impedance, establishing the optimum power-matched condition and associated trade-offs. Figure 4.2 illustrates the initial gain/NF and power analysis.



(a)

Noise Figure Contour Level (dB)
4.6
4.1
3.6
3.1

Gain Contour Level (dB)
5.3
6.3
7.3
8.3



(b)

Pout Contour Level (dBm)
19.8
20.3
20.8
21.3
21.8

PAE Contour Level (%)
14.1
16.1
18.1
20.1
22.1

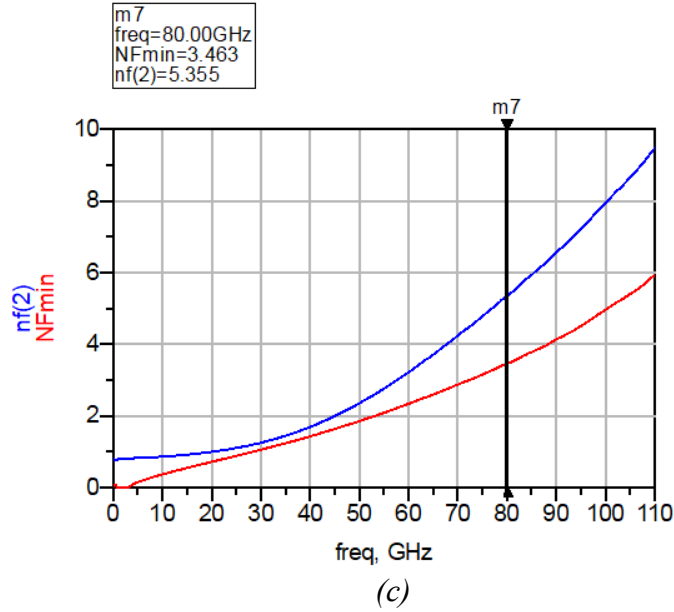


Figure 4.2: (a) Noise and gain source-pull simulation of $2 \times 50 \mu\text{m}$, (b) Load-pull simulation of $4 \times 50 \mu\text{m}$ device, (c) Minimum noise figure over frequencies of $2 \times 50 \mu\text{m}$ device.

The proposed W-band driver amplifier employs a three-stage topology requiring careful management of the DC supply routing to maintain unconditional stability. The layout is systematically arranged with the three gate bias lines routed along the bottom of the MMIC and the three drain bias lines routed along the top. This deliberate physical separation of the input (gate) and output (drain) supply rails minimizes electromagnetic cross-coupling and prevents parasitic feedback between the sensitive input loops and the higher-power output loops.

To achieve high RF isolation between the active transistor stages and the external DC voltage supplies, spiral inductors were utilized on all bias lines rather than traditional quarter-wavelength ($\lambda/4$) transmission lines. At W-band frequencies (75–85 GHz), standard $\lambda/4$ lines can consume excessive die area and are susceptible to unwanted multi-mode resonances. Instead, the spiral inductors were specifically dimensioned so that their self-inductance resonates with their inherent parasitic shunt capacitances near the center of the operating band. This creates a parallel LC resonance, presenting a very high impedance (effectively an RF open circuit) to the millimeter-wave signals.

The implementation of these spiral inductors has a profound influence on the overall stability of the amplifier. At W-band, the intrinsic high gain of the GaAs pHEMT devices makes the circuit highly sensitive to RF leakage. If RF energy from the third stage were allowed to leak into the shared DC supply rail and couple back into the first stage, it would create a positive feedback loop resulting in severe in-band or low-frequency oscillations. By acting as robust RF chokes, the spiral inductors

block this leakage path. Furthermore, terminating these inductors with series bypass capacitors provides a solid RF ground at the supply pads, suppressing low-frequency bias network resonances and ensuring the amplifier remains unconditionally stable across the entire frequency spectrum.

4.1.2 Stability analysis

Stability analysis is performed to ensure stable operation of the driver amplifier across frequencies and bias conditions. The design is unconditionally stable, as confirmed by conventional and advanced stability technique. The Rollet stability factor (K -factor) remains greater than 1 over the entire simulated frequency range, indicating unconditional stability for two-port network. However, since conventional stability factors may be insufficient for multi-stage amplifier design, Ohtomo stability analysis was additionally employed. In this analysis, the reflection coefficient remains entirely within the unit circle ($|\Gamma| < 1$) for both the loop-gain and encirclement plots, showing the absence of potential oscillation modes and confirming unconditional stability of the complete circuit. Figure 4.3 introduces the stability analysis from EDA tool – Keysight ADS.

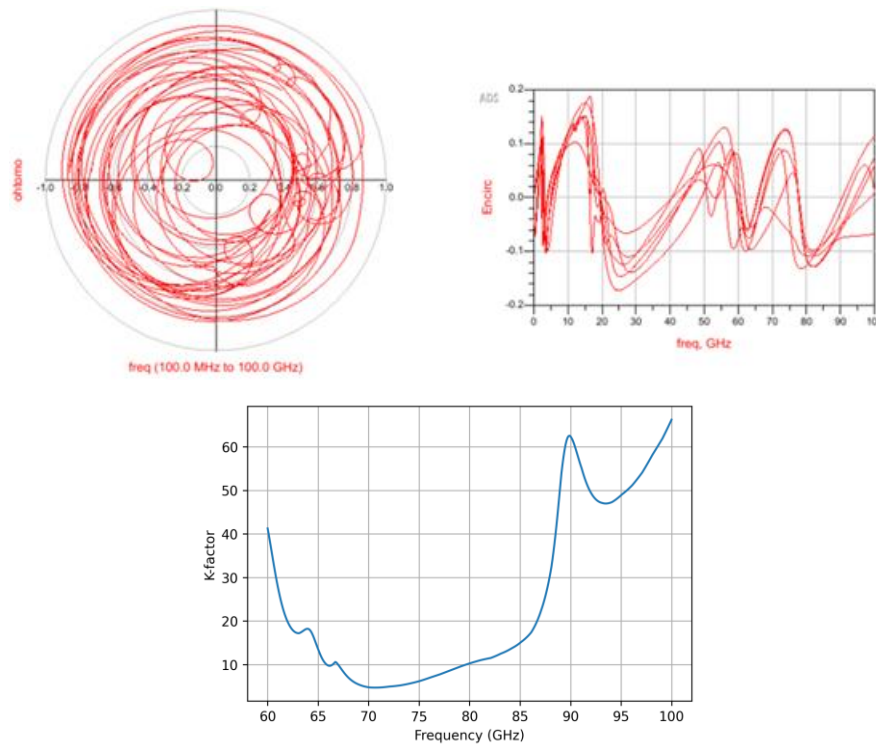


Figure 4.3: Ohtomo loop-gain and encirclement simulation and k -factor simulation.

4.1.3 S-Parameters

Small-signal S-parameter probe measurements are conducted at the nominal bias condition. The measured small-signal gain reaches 18.8 dB, while both the input and output return losses, S_{11} and S_{22} , remain below -10 dB across the operating band. A reduction in measured gain is recognised at

higher frequencies. Figure 4.4 shows the comparison of EM-simulated and measured S-parameter results as the supply voltage V_{DD} is varied from 2 V to 4 V. The S-parameter measurements use a Keysight PNA Network Analyzer (N5290A). To ensure measurement accuracy, a standard Short-Open-Load-Through (SOLT) calibration is carried out on a calibration substrate, establishing the measurement reference plane at the tips of the GSG probes.

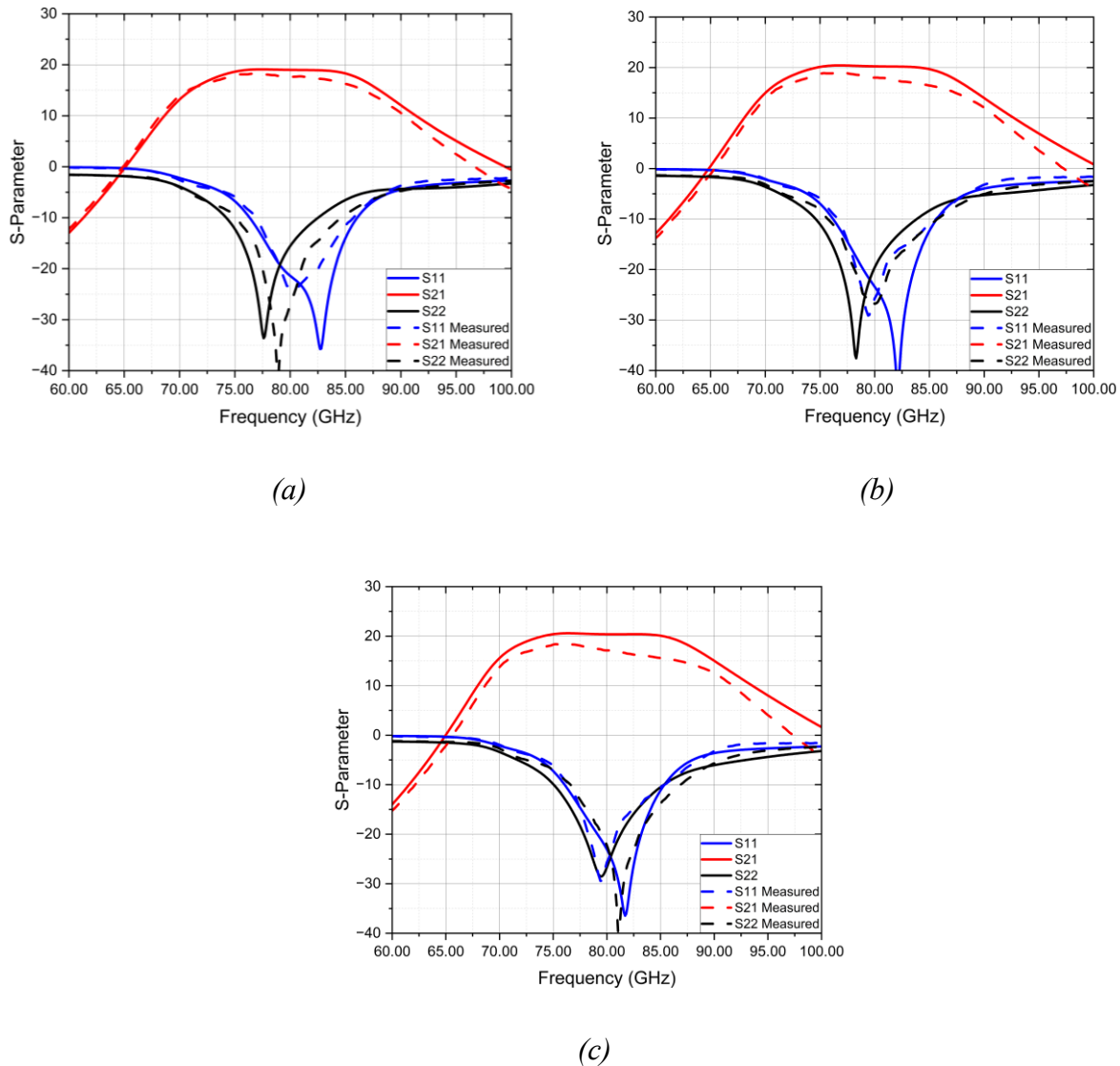


Figure 4.4: S-Parameters comparison between measured and EM-simulated results, I_d fixed at 65mA, a) $V_{dd} = 2V$, b) $V_{dd} = 3V$, c) $V_{dd} = 4V$.

4.1.4 Noise performance

For a probe noise measurement, a Keysight Signal Analyzer (N9030B) is used in conjunction with 2 noise sources connected at both the input and output ports. Prior to data acquisition, full noise figure calibration procedures are carefully completed to ensure reliable and repeatable results. As shown in

Figure 4.5, the measured noise figure varies from 4 dB to 5.2 dB across the frequency band. The close agreement between EM-simulated and measured results confirms the validity of the noise model and the accuracy of the overall design methodology.

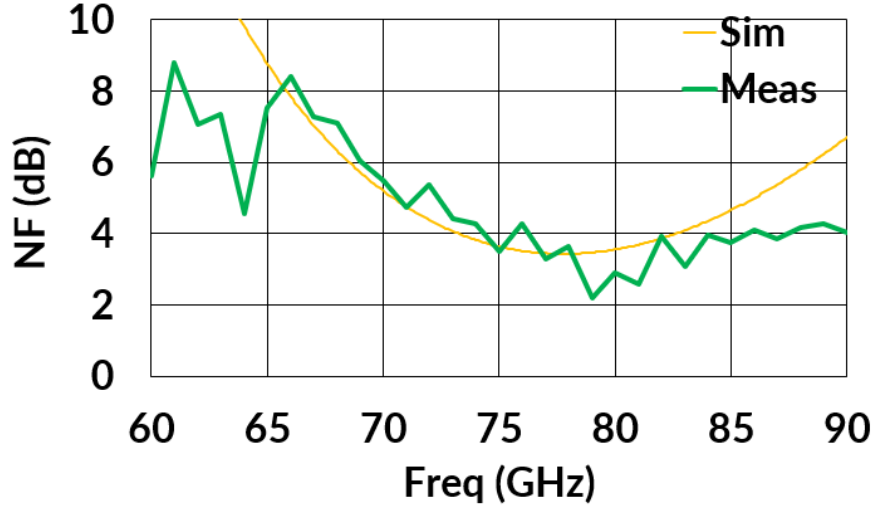


Figure 4.5: Simulated vs Measured NF at 2V 65mA.

4.1.5 Power performance

Large-signal power performance is executed through on-wafer power measurements. A Keysight signal generator (E8257D) is used to provide the RF input, while power sensors are placed at both the input and output ports to accurately monitor delivered and extracted power levels. All required calibrations are completed prior to measurement to remove systematic losses and set up the reference planes at the probe tips. At the time of measurement, power measurement is limited to operation at 76 GHz. Under these conditions, a measured output power of 17 dBm is obtained, with a maximum value of 17.7 dBm achieved at a drain current of 65 mA. The measured output power is approximately 2 dBm lower than simulation. Figure 4.6 compares the measured and simulated output power with a step of 0.1 V of V_{GS} (20mA of I_D step).

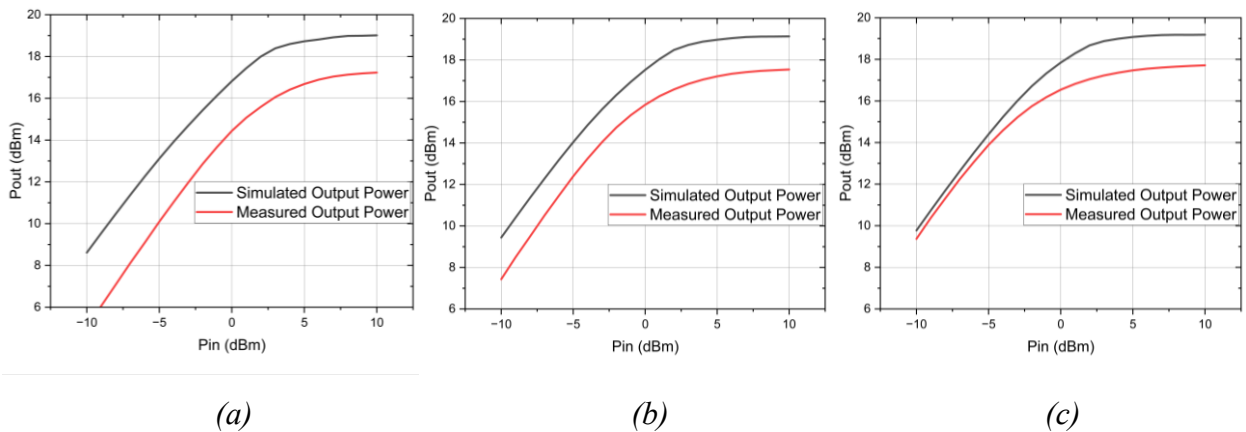


Figure 4.6: Output power comparison between measured and simulated results at $V_{DD} = 4V$,

a) $V_{GS} = -0.4V$, b) $V_{GS} = -0.3V$, c) $V_{GS} = -0.2V$.

The discrepancy between the simulation and measurement results shown in Figure 4.6 can be attributed to several practical factors inherent in high-frequency MMIC design and characterization.

At W-band frequencies (75 - 85 GHz), even minute parasitic inductances and capacitances from the Ground-Signal-Ground (GSG) probe pads and the transition between the probe tips and the chip can significantly impact the measured response. If these transition parasitics were not fully captured in the electromagnetic (EM) model, they can cause the observed shifts in gain and return loss.

Small variations in the GaAs pHEMT fabrication process, such as slight deviations in gate length, recess etch depth, or air-bridge height, can lead to shifts in the device's intrinsic transconductance (g_m) and parasitic capacitances (C_{gs} , C_{gd}). These process tolerances often result in a slight frequency shift of the matching networks compared to the nominal design.

Standard foundry models are often extrapolated for operation at the upper limits of the W-band. Discrepancies may arise if the non-linear or noise models do not perfectly account for high-frequency effects like substrate modes or complex coupling between closely spaced passive components.

The accuracy of the measurement is limited by the calibration of the Vector Network Analyzer (VNA) at the probe tips. Residual errors after calibration, or slight variations in probe placement and pressure during the characterization of the driver amplifier, can introduce small discrepancies in the measured S-parameters.

Although the driver amplifier is a relatively low-power stage, localized heating of the transistors during on-wafer CW (continuous wave) measurements can cause a slight decrease in gain and a shift in phase compared to the idealized isothermal simulations.

4.2 The revised Driver Amplifier (power cell)

This revised version of the driver amplifier (power cell) is developed following discrepancies observed between simulated and measured S-parameter and power performance in the initial design. To address these differences, an updated linear FET model is adopted and incorporated into the redesign process. The original device size selection of $2 \times 50 \mu m$, $2 \times 50 \mu m$, and $4 \times 50 \mu m$ is retained,

along with the same nominal bias conditions, in order to preserve the targeted gain and output power characteristics. In addition, the bias network layout is restructured into a symmetrical arrangement to support subsequent implementation in a balanced amplifier configuration. Power measurements cannot be performed for this revised design due to measurement limitations at the time of testing. Apart from the updated device model and revised bias routing, the overall circuit topology and design methodology remain consistent with the original driver amplifier.

Following the evaluation of the initial prototype, the design of the W-band driver amplifier was systematically revised to address performance bottlenecks. The primary objectives of the revision were to enhance gain flatness, expand the operational bandwidth across the entire 75–85 GHz target range, and guarantee unconditional stability. To achieve these improvements, several specific design strategies were implemented in the Revised Driver Amplifier:

The initial design exhibited gain peaking and a narrower-than-desired bandwidth. In the revised amplifier, the inter-stage matching networks were redesigned using higher-order, EM-optimized distributed topologies rather than simple reactive matches. This approach provided a more controlled impedance transformation over a wider frequency range, resulting in significantly improved gain flatness and extended functional bandwidth.

To mitigate out-of-band instabilities and improve isolation, the bias supply networks were heavily modified. The revised design incorporated EM-simulated spiral inductors acting as precise RF chokes, paired with strategically placed RC damping networks in the gate bias lines. This strategy successfully suppressed unwanted low-frequency loop gain without introducing excessive resistive insertion loss in the W-band RF path, thereby ensuring unconditional stability ($K > 1$) under all operating conditions.

To ensure sufficient drive capability while maintaining overall power-added efficiency, the transistor gate peripheries across the three stages were re-optimized. The output stage was deliberately scaled up to increase the 1-dB compression point (P_{1dB}) and saturated output power (P_{sat}), while the input stage was sized down to balance sufficient forward gain with an acceptable noise figure.

At W-band frequencies, even minimal parasitic source inductance can severely degrade high-frequency gain. The layout of the revised amplifier utilized rigorous 3D full-wave EM co-simulation to optimize the placement, dimensions, and proximity of the source grounding via-holes. This

minimized the parasitic source inductance to the ground plane, maximizing the available high-frequency gain of the GaAs pHEMT devices and improving the overall isolation between stages.

The revised driver amplifier (power cell) is unconditionally stable and demonstrates improved small-signal performance and consumes the same current as initial design, which is 100 mA. At the nominal bias condition, a measured small-signal gain of 20 dB is achieved at the mid-band frequency of 80 GHz, while both input and output return losses, S11 and S22, remain below -10 dB across the operating band.

4.2.1 Layout of the power cell

For the revised driver amplifier used as a power cell, the device size selection and nominal bias conditions are kept identical to the previous design in order to maintain the same gain and output power characteristics. The main modification is the implementation of a symmetrical bias network, which is intended to support subsequent integration into a balanced amplifier structure. Figure 4.7 shows the layout of the revised driver amplifier (power cell), where the die size is $1.2 \times 1.25 \text{ mm}^2$ including all RF and DC pads.

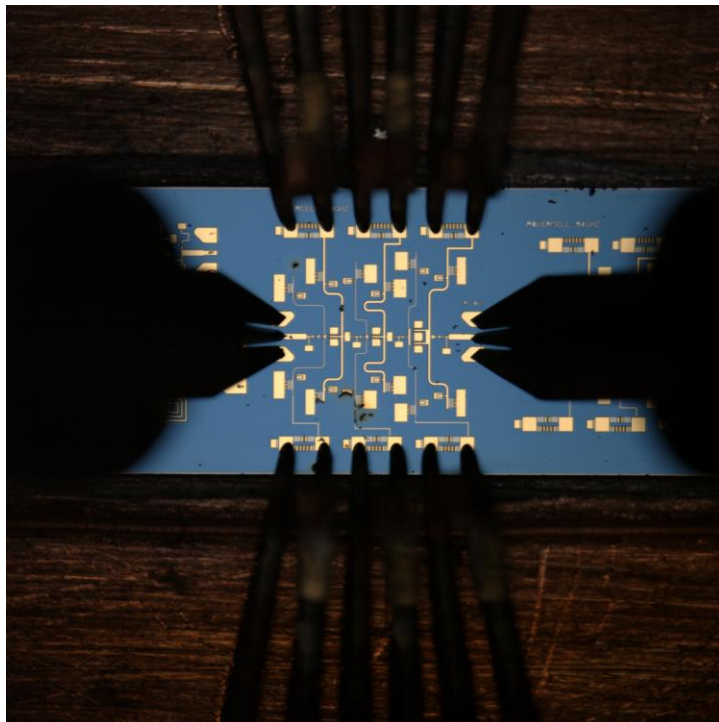


Figure 4.7: Die-photo of the revised driver amplifier.

4.2.2 S-Parameters

The S-parameter performance of the revised driver amplifier is measured through probe

measurements, with full calibration procedures completed beforehand to ensure reliable and repeatable results. Figure 4.8 presents the S-parameter comparison between EM simulation and measurement under nominal bias conditions, and the measured S-Parameter with 0.1 V step of V_{gs} . The amplifier delivers a small-signal gain of approximately 20 dB at the mid-band frequency of 80 GHz, while both S11 and S22 remain better than -10 dB over the frequency range. Although the measured S-Parameter shows the same response's shape as predicted by simulation, the gain is lower by about 2 - 3 dB, which is mainly attributed to added losses and model inaccuracies not fully captured in simulation.

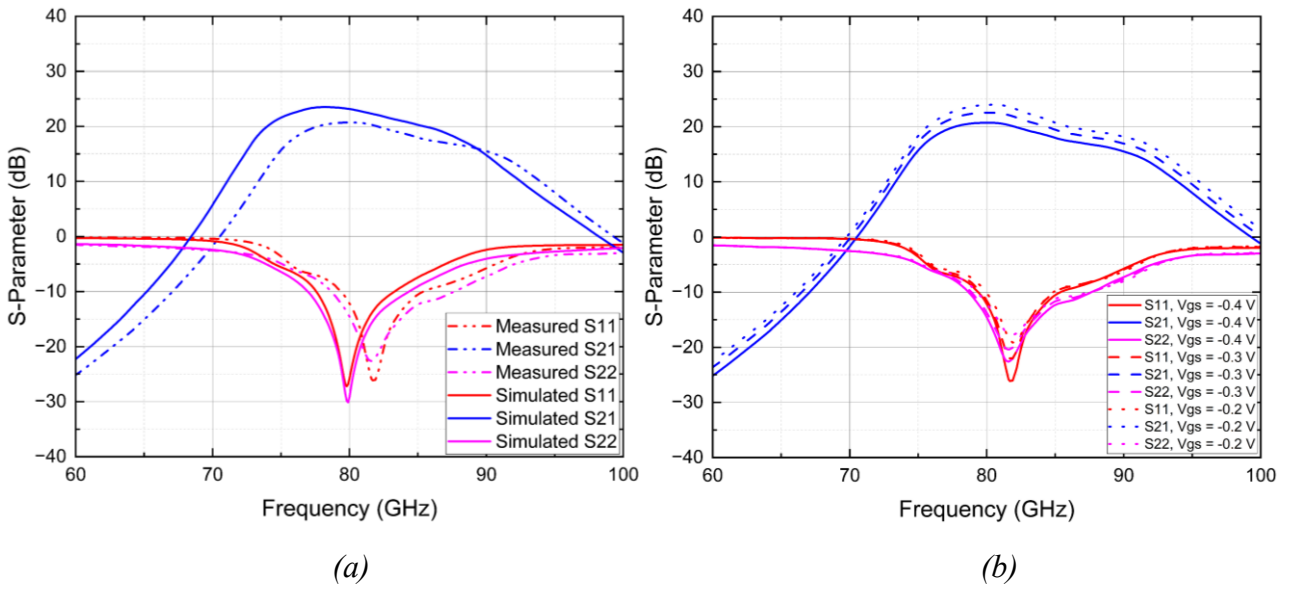


Figure 4.8: S-Parameter comparison of the revised amplifier, (a) Nominal bias, (b) measured S-Parameter with V_{GS} swept from -0.4 V to -0.2 V.

4.3 The corresponding Balanced Amplifier

The balanced amplifier is constructed by combining two identical driver amplifier power cells through a Lange coupler, forming a fully balanced architecture. This configuration improves the mismatches and widens the bandwidth. The complete balanced amplifier is unconditionally stable and occupies a total chip area of 1.77×2.2 mm², including all RF and DC pads. The total current consumption I_D is 140 mA. Figure 4.9 shows the layout of the balanced amplifier under microscope.

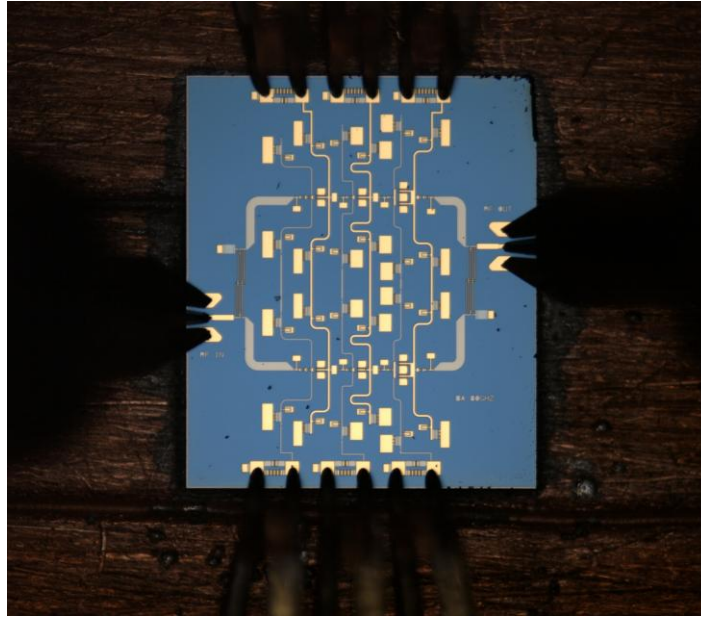


Figure 4.9: Die-photo of the proposed Balanced Amplifier.

4.3.1 Lange coupler

The Lange coupler is used in the balanced amplifier to divide and combine the RF signal with equal amplitude and a quadrature phase relationship. This enables the two identical amplifier cells to work in a balanced configuration, improving input and output matching and reducing sensitivity to load mismatch. The coupler is realized using interdigitated transmission lines with air-bridge crossovers to achieve the required strong coupling. Full EM simulation results show an approximately 3 dB power split and a 90° phase difference between the output ports, showing proper coupler operation. Figure 4.10 shows the structure of the Lange coupler and its layout as implemented in the EDA tool – Keysight ADS, followed by Figure 4.11, which presents the corresponding full EM simulation results of the coupler.

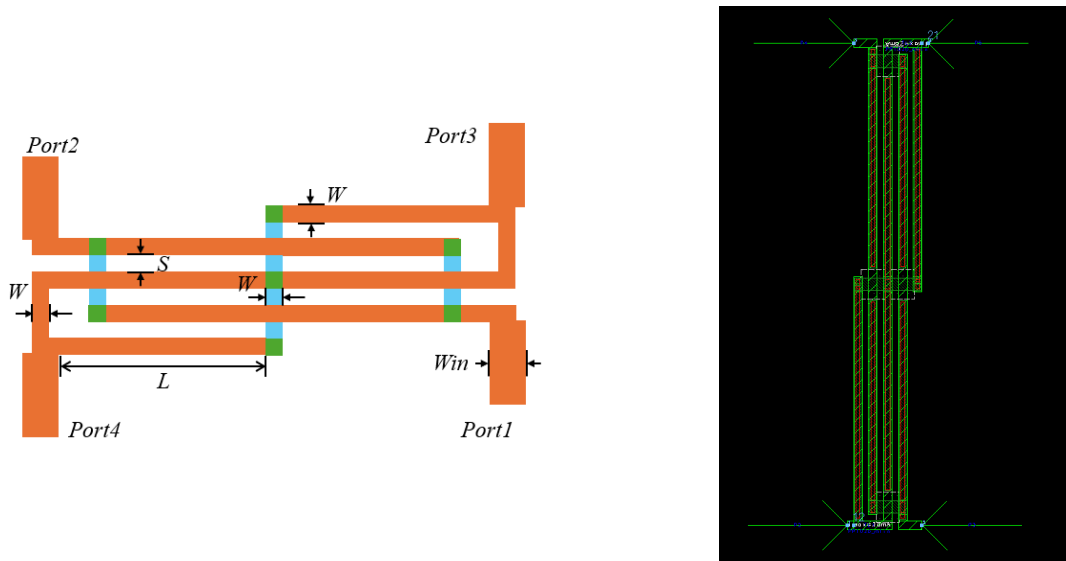


Figure 4.10: Lange coupler.

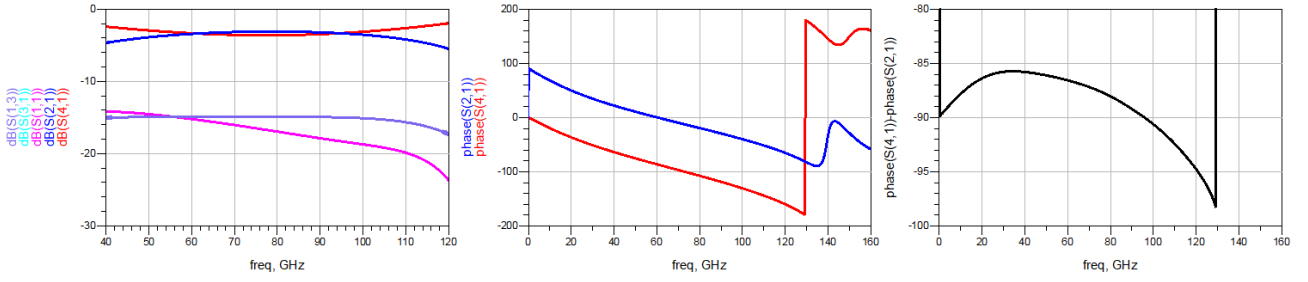


Figure 4.11: EM simulation showing S -Parameters, phase of 2 output ports and phase difference between 2 output ports of the Lange coupler.

4.3.2 S-Parameters

With the same calibrations and measurement setups, Figure 4.12 presents the comparison results between EM-simulated and measured S -Parameters of the balanced amplifier under nominal bias conditions, and the measured S -Parameters with varied step of 40mA of drain current. A small-signal gain of approximately 16 dB is achieved at the mid-band frequency of 80 GHz. Thanks to the balanced architecture, both the input and output return losses, S_{11} and S_{22} , exhibit noticeably improved bandwidth and matching performance compared to the single-ended case. The overall frequency response follows the same shape as the simulated results. However, the measured gain is lower by approximately 3 - 5 dB.

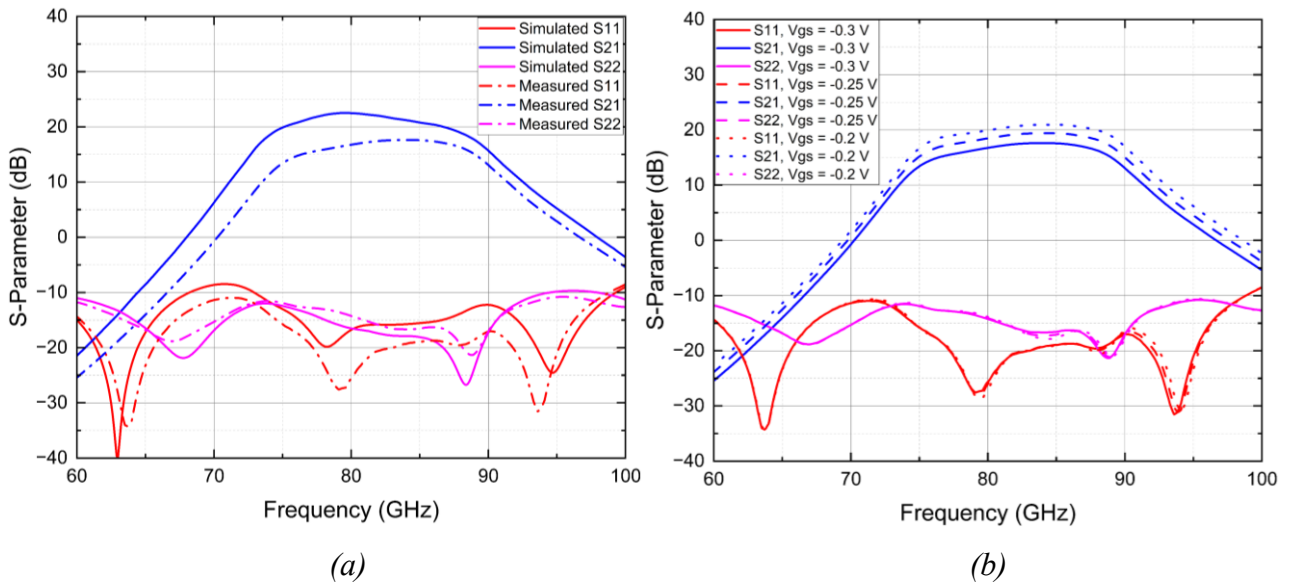


Figure 4.12: S -Parameter comparison of the balanced amplifier, (a) Nominal bias, (b) measured S -Parameter with V_{GS} swept with 0.05 V step.

4.4 Summary

This chapter presents the design, implementation, and experimental evaluation of a series of 3 driver

amplifiers developed at 75 – 85 GHz, which are built for 5G wireless back/fronthaul and 6G research applications. The work progresses from an initial single-ended driver amplifier to a revised version addressing discrepancies between simulation and measurement, and finally to a balanced amplifier configuration aimed at broader bandwidth and higher output power. Each design builds upon the previous one, allowing performance limitations to be debugged and systematically addressed.

The revised driver amplifier demonstrates a clear improvement in small-signal performance, achieving an increase of approximately 2 dB in measured gain compared to the initial design, which validates the adoption of the updated device model and the refined layout strategy. Building on this improved power cell, a balanced amplifier is designed using a Lange coupler, offering enhanced matching performance and improved robustness against load variations, as confirmed by measured S-parameter results.

Due to time constraints and measurement availability, noise figure and large-signal power measurement could not be completed for the revised driver amplifier and the balanced amplifier. Based on simulation results and observed trends, an improvement in output power of at least 2 dBm is expected for these designs. The noise and power measurements are planned as part of future work to fully validate their performance. Overall, the results presented in this chapter establish a solid foundation for the subsequent amplifier stages and demonstrate a clear and logical design evolution toward higher performance and wider bandwidth.

Table 4.1 shows the comparison result of this work and other related State-Of-The-Art.

Table 4.1: Performance comparisons between this work and other related State-Of-The-Art.

Ref	Freq (GHz)	Gain (dB)	P _{1dB} (dBm)	P _{sat} (dBm)	DC power (mW)	Tech.	Year
[52]	71 – 80	8.4	16.5	18.8	300	0.15- μ m GaAs	2011
[53]	78 – 93	11.5	18.2	19.6	660	0.1- μ m GaAs	2019
[124]	84 – 103	15	N/A	21.5	420	0.1- μ m GaAs	2020

[54]	67 – 103	17	N/A	16	300	0.1-μm GaAs	2019
This initial amplifier	75 – 85	18.8	16.3	17.7	400	0.1-μm GaAs	2023
This revised amplifier	75 – 85	20	N/A	N/A	400	0.1-μm GaAs	2024
This balanced amplifier	75 – 85	16	N/A	N/A	560	0.1-μm GaAs	2024

Chapter 5: K-band GaN Power Amplifiers

In this chapter, a second set of MMIC amplifier designs is presented, in which a power amplifier and its corresponding balanced amplifier are developed for operation from 17 to 22 GHz. These designs use the UMS GH15-11 GaN process in order to address the higher output power and robustness requirements associated with this frequency band. A single-ended power amplifier is first realised to meet the required output power and efficiency across the target band, while providing a reference for device sizing, bias conditions and output matching network topology. The power amplifier is subsequently extended to a balanced amplifier configuration, through which improves bandwidth and enhanced power performance, aligning the design with the operational requirements of SmartSAT and SATCOM satellite front-end systems.

5.1 Power amplifier cell

A three-stage power amplifier targeting operation over the 17 - 22 GHz frequency range is developed using the UMS GH15-11 GaN process. The design employs the UMS hot FET model to accurately capture large-signal behaviour under high-power operating conditions. The device sizing of $2 \times 75 \mu\text{m}$, $2 \times 75 \mu\text{m}$, and $8 \times 75 \mu\text{m}$ is selected across the three stages to provide the required output power while maintaining sufficient power consumption. Figure 5.1 shows the schematic of the proposed power amplifier. To facilitate subsequent integration into a balanced amplifier configuration, all gate and drain bias networks are routed toward one side of the die, resulting in a layout compatible with symmetric combining. The designed power amplifier is unconditionally stable across the operating band and occupies a compact chip area of $3 \times 1 \text{ mm}^2$, including all RF and DC pads, as shown in Figure 5.2.

Under nominal bias conditions suitable for space applications, the power amplifier draws a drain current of approximately 450 mA from a 20 V supply. The power amplifier cell delivers a measured saturated output power exceeding 33.4 dBm, together with a peak power-added efficiency greater than 37.7 %. The gain response is both high and broadband, remaining above 30 dB across the operating band and reaching a maximum measured value of 33.6 dB. Good impedance matching is maintained at both the input and output, with return losses consistently better than -10 dB over the 17 - 22 GHz frequency range.

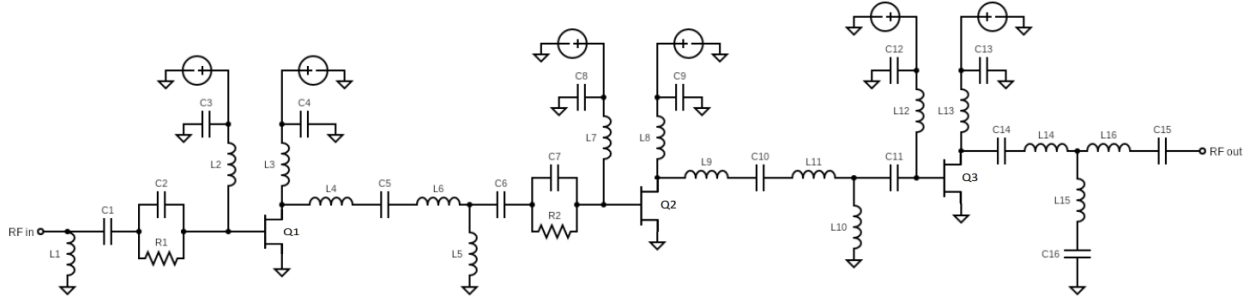


Figure 5.1: Schematic of the 3-stage power amplifier.

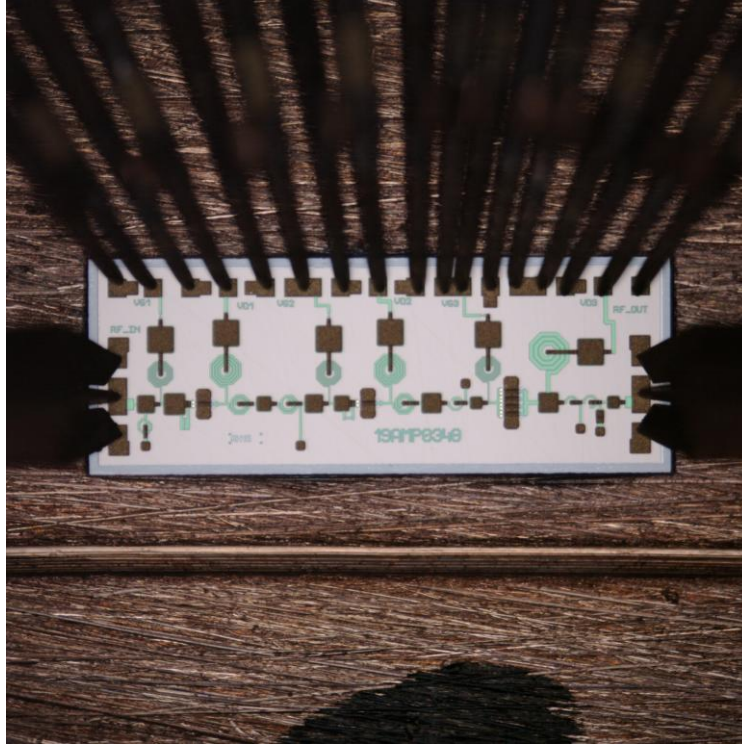


Figure 5.2: Die-photo of the 3-stage power amplifier.

5.1.1 Device selection

The selection of the optimal transistor gate periphery (total device size) is a foundational step in the design of the K-band GaN power amplifier, requiring a careful balance between targeted output power and high-frequency RF performance. In this design, the choice of device size was governed by the inherent trade-offs between maximum achievable power, parasitic component scaling, and impedance matching difficulty.

Fundamentally, the maximum saturated output power (P_{sat}) of a GaN HEMT scales linearly with the total gate periphery, assuming optimal thermal management. To achieve the target output power of >30 dBm (1 Watt) at K-band, a sufficiently large total gate width is mandatory for the final power

stage to support the required maximum drain current and voltage swings.

However, as the device size increases, its intrinsic parasitic capacitances, specifically the gate-source capacitance (C_{gs}), gate-drain feedback capacitance (C_{gd}), and drain-source capacitance (C_{ds}) increase proportionally. At K-band frequencies (17–22 GHz), these elevated parasitic reactances severely degrade the device's high-frequency metrics. Most notably, the increased C_{gd} intensifies internal feedback, reducing the maximum stable gain (MSG) and maximum oscillation frequency (f_{max}).

Furthermore, larger device peripheries result in a significantly lower optimum load impedance (R_{opt}) for maximum power transfer, as determined by load-pull simulations. At high frequencies, matching this very low R_{opt} (often just a few ohms) to the standard 50 Ω system impedance requires high impedance transformation ratios. High transformation ratios in broadband networks necessitate multiple matching sections and result in narrower bandwidths and higher passive insertion losses, which ultimately degrades the overall Power-Added Efficiency (PAE). Additionally, the large input capacitance (C_{gs}) of a highly scaled output stage creates a very low input impedance, heavily loading the preceding driver stage.

Consequently, the logic behind the chosen device sizes for this amplifier relies on a progressive scaling strategy. The final stage was sized precisely to meet the 30 dBm P_{sat} requirement under load-pull conditions without over-sizing, thereby keeping the output matching network realizable and low-loss. Conversely, the driver stages were sized progressively smaller. By using smaller gate peripheries for the driver stages, their parasitic capacitances were minimized, maximizing their available gain and presenting a higher, more manageable input impedance. This progressive sizing strategy ensures that each stage provides sufficient linear drive power to the subsequent stage while maintaining broad bandwidth and unconditionally stable operation across the 17 – 22 GHz band.

The Power-Added Efficiency (PAE) of the amplifier, which accounts for the RF input power required to drive the device, is calculated using the following equation:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \times 100\%$$

where P_{out} is the RF output power, P_{in} is the RF input power provided to the stage, and P_{DC} is the total DC power consumed by the amplifier.

After multiple careful simulation among several device sizes, for gain analysis, two transistor sizes, $2 \times 75 \mu\text{m}$ and $8 \times 75 \mu\text{m}$ FETs, are simulated through small-signal simulations to assess the achievable maximum gain and its frequency dependence across the K-band. This comparison provides insight into the trade-off between device periphery and high-frequency gain, then informing the selection of an appropriate unit cell for subsequent amplifier stages.

Power analysis is examined exclusively using the larger $8 \times 75 \mu\text{m}$ FET, for which large-signal load-pull simulations are performed to decide the delivered output power and efficiency as functions of the load impedance. The load-pull contours find the optimum power-matched region and highlight the separation between maximum output power and maximum power added efficiency. Figure 5.3 summarizes the first gain analysis for the $2 \times 75 \mu\text{m}$ and $8 \times 75 \mu\text{m}$ devices, together with the load-pull results of the $8 \times 75 \mu\text{m}$ transistor, which form the basis for the power amplifier design.

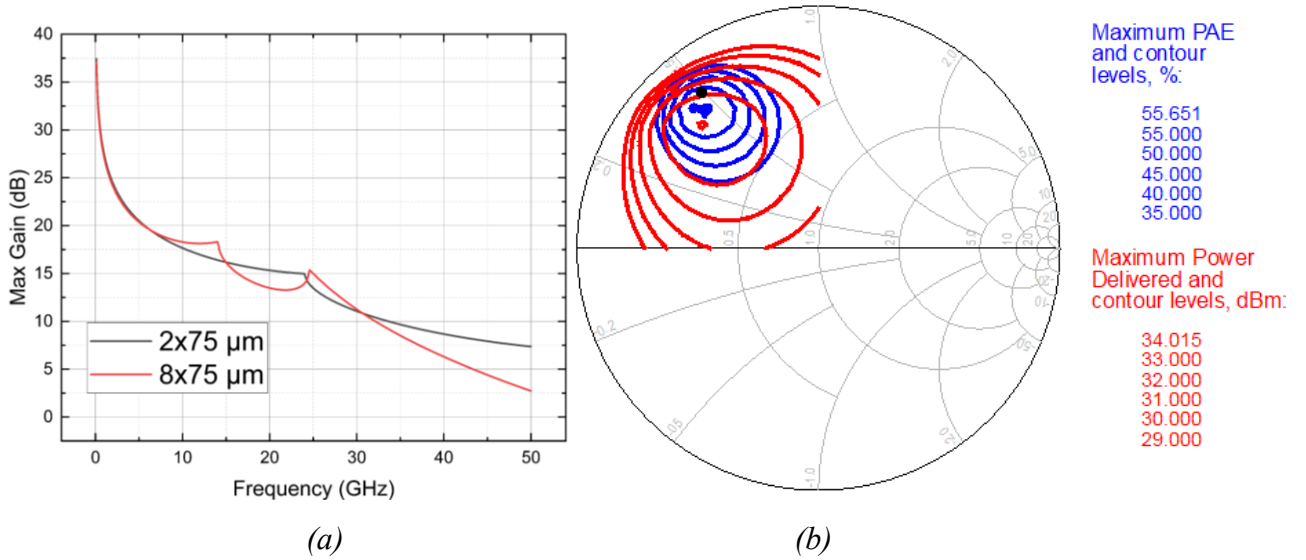


Figure 5.3: Initial analysis, (a): Max gain simulation of $2 \times 75 \mu\text{m}$ and $8 \times 75 \mu\text{m}$ FET, (b): Load-pull simulation of $8 \times 75 \mu\text{m}$ FET.

5.1.2 Stability analysis

The stability analysis is the same for all the designs, where conventional stability factors, including the Rollett stability factor K , the determinant B_1 , and the source- and load-stability measures μ_s and μ_L , are first evaluated over frequency to identify potential regions of conditional instability. While these parameters provide a convenient initial analysis, their validity becomes increasingly limited at millimetre-wave frequencies and in multi-stage amplifier, where distributed effects, internal feedback paths, and interstage coupling can invalidate the underlying two-port networks. For this reason, Ohtomo's method is additionally considered to directly examine the loop gain and the associated Nyquist encirclement behaviour, offering a more physically meaningful assessment of stability.

Design modifications are then guided by this analysis to suppress unintended feedback loops and ensure unconditional stability across the operating band and beyond.

All the stability factors are checked to ensure the unconditional stability of the complete circuit. Specifically, the determinant B_1 remains positive over the entire the frequency range, while the Rollett stability factor K and the source and load stability measures, μ_s and μ_L , are all maintained above 1, as illustrated in Figure 5.4.

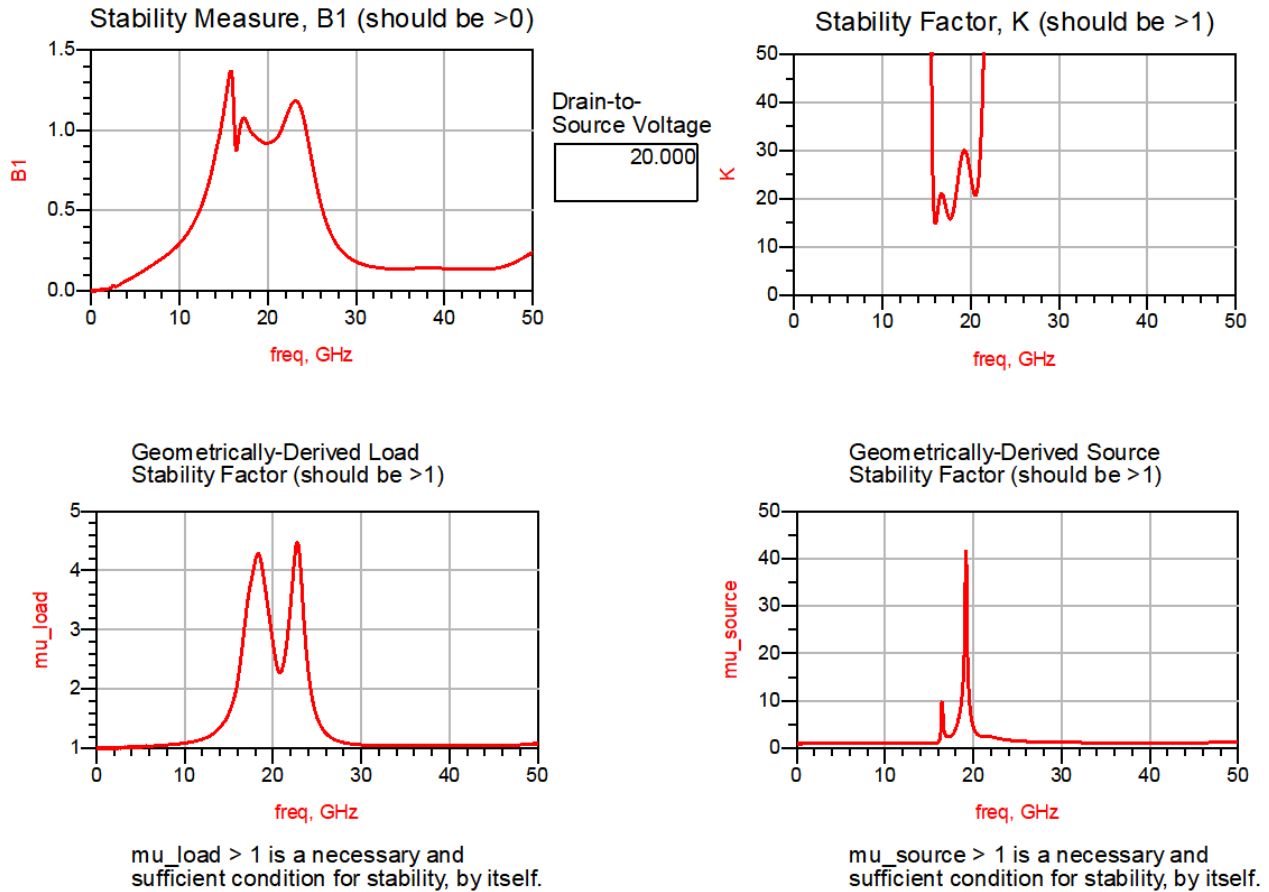


Figure 5.4: Stability factors.

Additionally, the Ohtomo analysis confirms that the computed loop gain exhibits no critical encirclement, with the corresponding trajectories lying entirely within the unit circle, as shown in Figure 5.5. The agreement between these complementary factors provides strong evidence that the power amplifier is unconditionally stable at all frequencies.

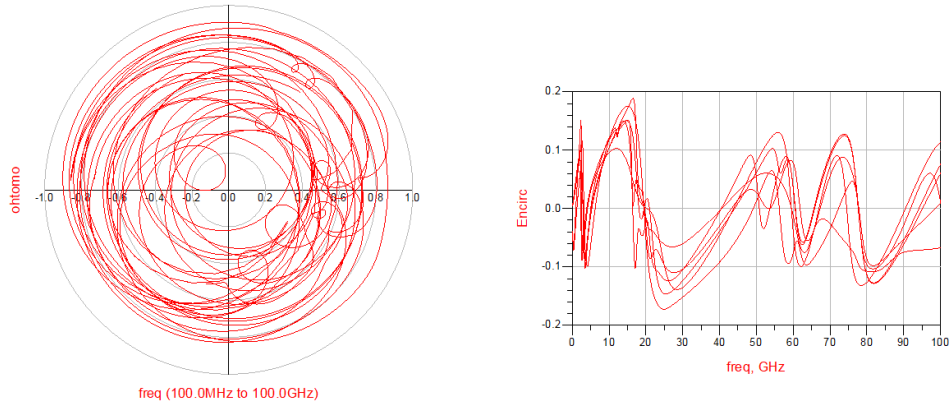


Figure 5.5: Ohtomo simulation.

To guarantee unconditional stability specifically in multi-stage topologies, an inter-stage stability analysis was performed using Ohtomo's method and return-ratio evaluations at the intermediate matching nodes. Multi-stage amplifiers are highly susceptible to internal loop oscillations where the output of a driver stage interacts resonantly with the input of the subsequent stage, which classical k-factor analysis at the external ports may fail to detect. By deliberately applying lossy shunt RC networks and series gate resistors at these inter-stage nodes, the internal loop gain was suppressed below 0 dB across all frequencies, ensuring the cascade remains unconditionally stable without severely compromising forward gain.

Moreover, an RC stabilisation network, which is shown in Figure 5.6 , is inserted at the gate terminal of the first and second transistor to further suppress low-frequency and out-of-band oscillations. This network introduces controlled damping without materially degrading the in-band gain, thereby improving robustness against process variations, bias fluctuations, and parasitic coupling. In conjunction with the verified small-signal and loop-gain stability criteria, the inclusion of this RC network ensures reliable unconditional stability of the power amplifier across all relevant operating conditions.

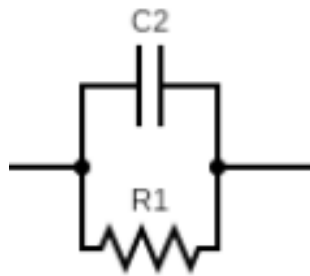


Figure 5.6: Stabilised RC network used in the circuit.

5.1.3 S-Parameter

Small-signal S-parameter measurement is carried out with all instruments' losses fully accounted by the applied calibration procedures. The measurements use a Keysight N5290A Vector Network Analyzer, ensuring accurate extraction of the amplifier's linear response over the frequency range. A comparison between simulated and measured S-parameters is presented in Figure 5.7. It is shown that the measured responses are in close agreement with the EM-simulated results. The measured small-signal flat gain remains above 30 dB across the target band, reaching a maximum value of 33.6 dB at the mid-band frequency of 20 GHz. In addition, both input and output reflection coefficients are maintained below -10 dB throughout the operating bandwidth, indicating satisfactory impedance matching at both ports.

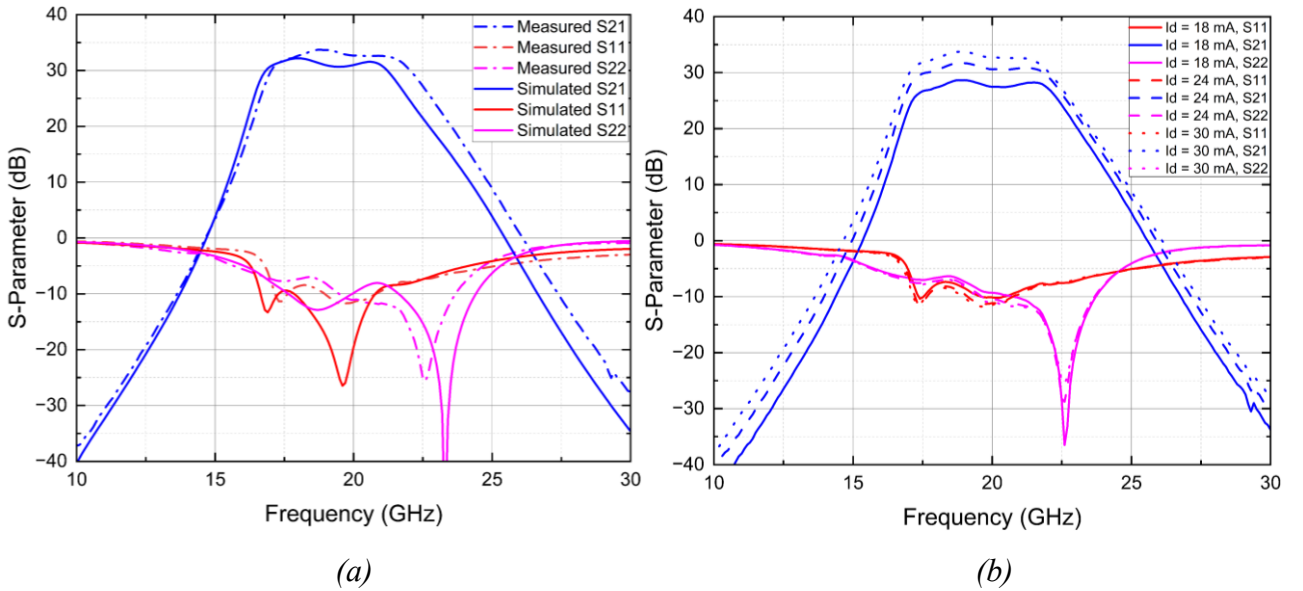


Figure 5.7: S-Parameter comparison, (a) Nominal bias, (b) Measured S-Parameter with I_{D_s} swept by a step of 6mA.

5.1.4 Power performance

Large-signal power measurements are performed after all calibration steps have been completed to ensure accurate power referencing at both the input and output planes. A continuous-wave excitation is provided by a Keysight E8257D Analog Signal Generator, delivering sufficient drive to fully explore the saturation characteristics of the power amplifier. Two calibrated power sensors, used in combination with a coaxial directional coupler and a power meter, enable precise monitoring of the power levels at the device under test.

A comparison between simulated and measured large-signal results is presented in Figure 5.8, where a reasonable agreement is achieved, which confirms the validity of the proposed power amplifier cell

design. Minor discrepancies between simulation and measurement are mainly attributed to frequency shifts arising from fabrication process tolerances. With $P_{in} = 8$ dBm, the simulations predict a power-added efficiency ranging from 36 % to 41 % and a saturated output power between 30.9 dBm and 33.4 dBm. In measurement, the power amplifier achieves a PAE from 27.8 % to 37.7 % and a saturated output power spanning 30.9 dBm to 33.4 dBm across the 17.3 - 21.2 GHz frequency range.

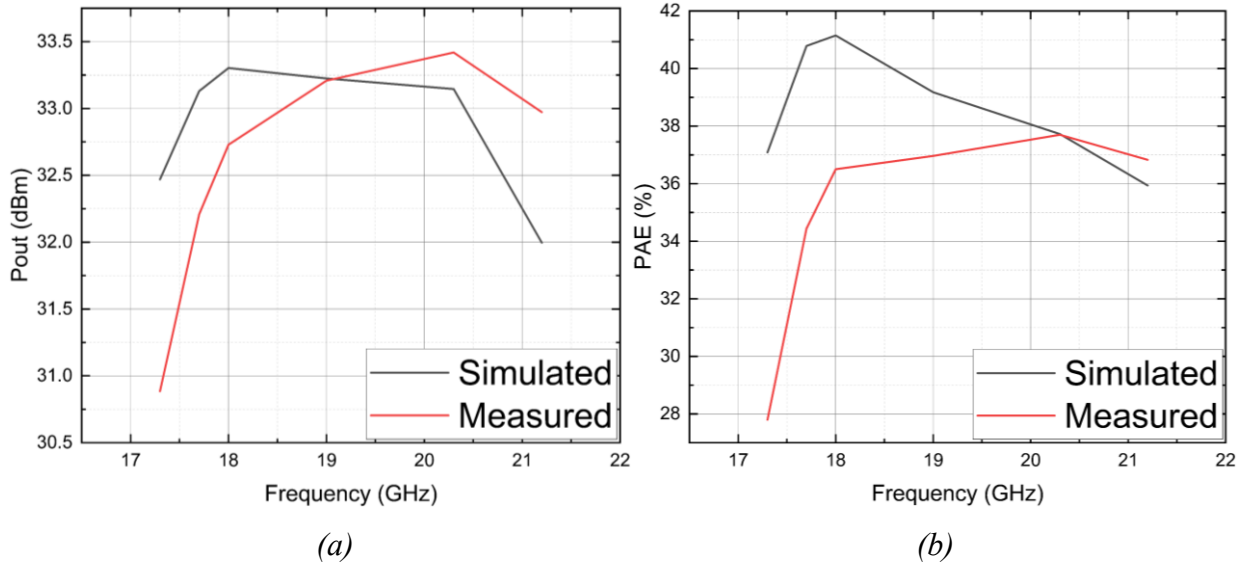


Figure 5.8: Power performance comparison of the power amplifier cell, (a) P_{out} vs Freq, (b) PAE vs Freq.

To further assess the linearity performance of the designed power amplifier cell, two-tone measurements are conducted at multiple frequencies within the operating band. As illustrated in Figure 5.9, the measured worst third-order intermodulation distortion (IMD3) and worst Output Third-Order Intercept Point (OIP3) exhibits a corresponding increase with output power, which have strong agreement with the expected nonlinear performance of GaN-based power amplifiers under large-signal condition.

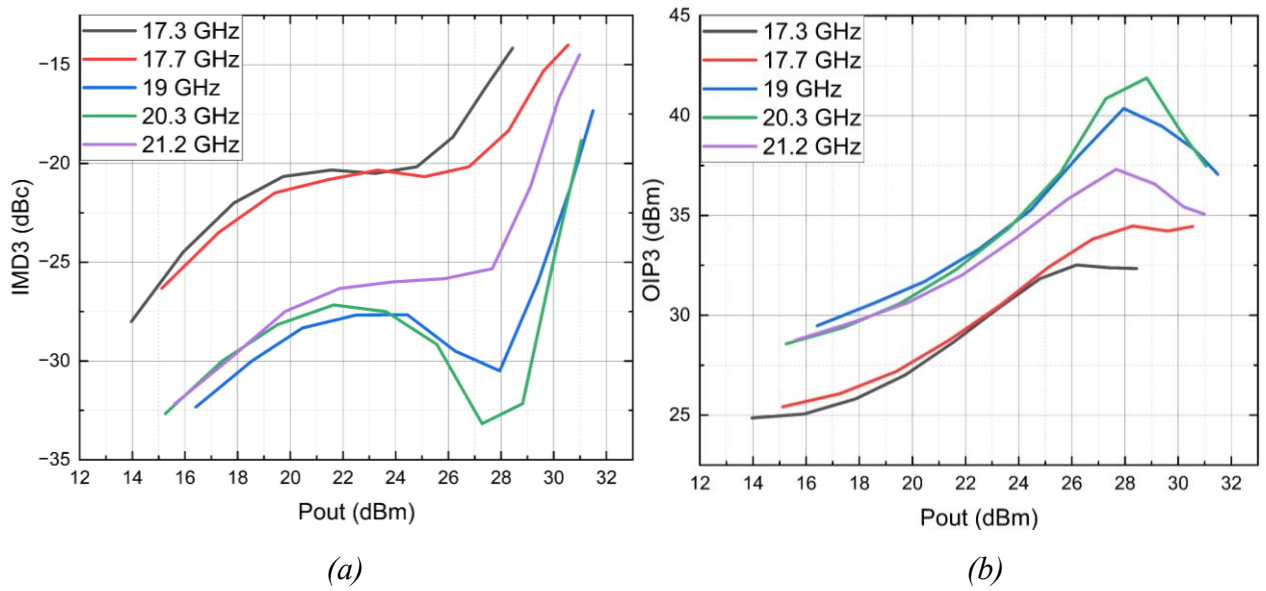


Figure 5.9: Intermodulation performance, (a) Worst IMD3 vs P_{out} , (b) Worst OIP3 vs P_{out} .

5.2 Corresponding BA

The corresponding balanced amplifier, as shown in Figure 5.10, is developed by combining two identical power cells, which are previously introduced, with Lange couplers at the input and output as power divider and power combiner, respectively. This configuration is adopted to improve bandwidth, enhance tolerance to load mismatch, and provide a more robust power amplifier solution for practical operation. The symmetrical layout of the two power cells, together with the Lange coupler network, enables balanced operation while preserving the large-signal performance of the individual amplifiers. Across the 17.3 - 21.2 GHz frequency range, the balanced amplifier (BA) shows a measured gain of 30 - 32.5 dB, a saturated output power of 35.8 dBm, and a peak power-added efficiency of 35.3%. Thanks to the balanced architecture, input and output return losses are significantly improved over the entire operating band.

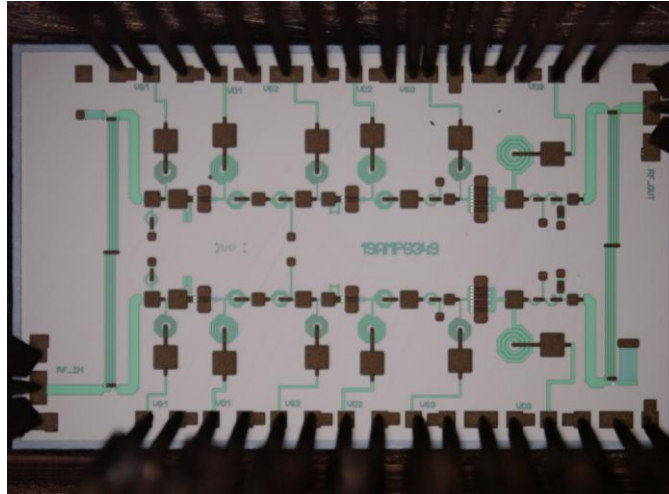


Figure 5.10: Die-photo showing the corresponding BA's layout.

5.2.1 Lange coupler

A Lange coupler is employed in the balanced amplifier to split and recombine the RF signal with equal amplitude and a 90° phase difference. This arrangement allows the two identical amplifier cells to operate in a balanced topology, which improves both input and output matching while reducing sensitivity to load impedance variations. The coupler is implemented using interdigitated transmission lines with air-bridge crossovers to realize the strong coupling required over the operating band. Full EM simulations confirm correct operation, showing an approximately 3 dB power division and a 90° phase difference between the output ports. The physical structure and layout of the Lange coupler as implemented in the EDA (ADS) simulation are shown in Figure 5.11, while the corresponding full EM simulation results are presented in Figure 5.12.

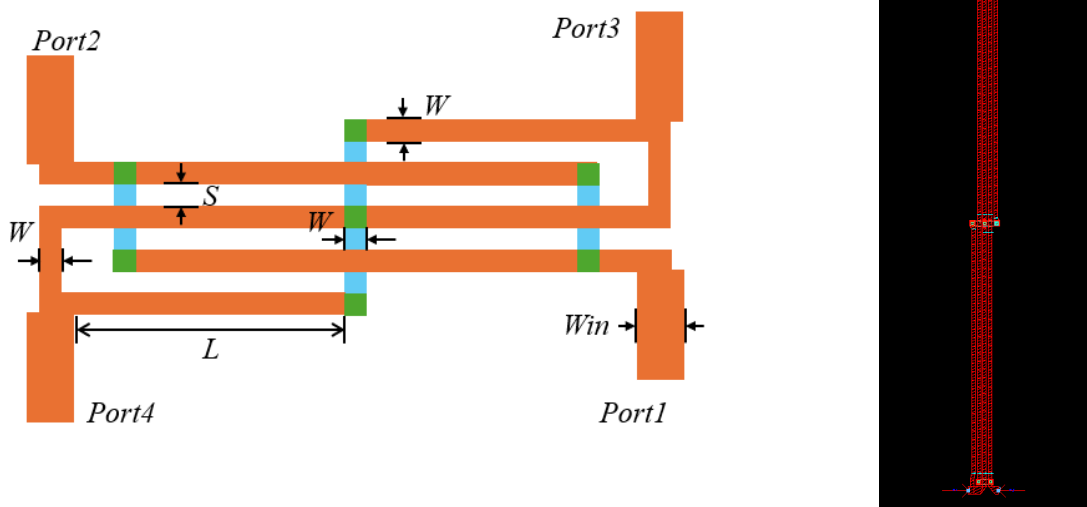


Figure 5.11: Lange coupler.

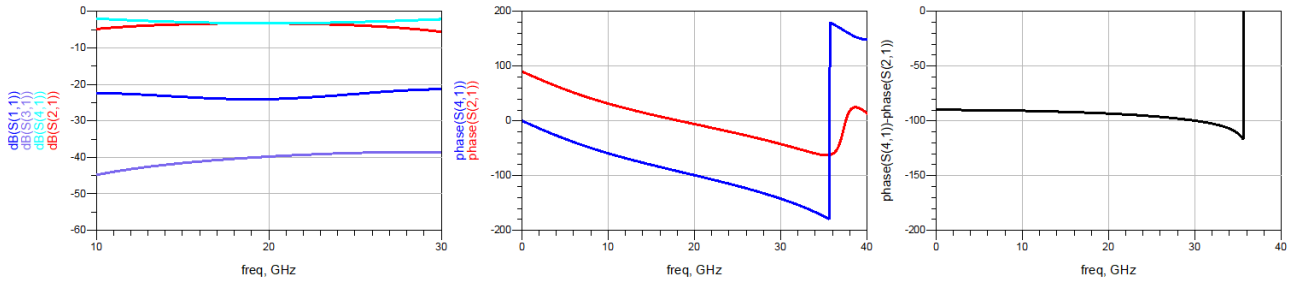


Figure 5.12: Full EM simulated results of the used Lange coupler.

5.2.2 S-Parameter

Using the same calibration procedure and measurement setup used for the amplifier cell, S-parameter measurements of the balanced amplifier are carried out under nominal bias conditions. Figure 5.13 compares the EM-simulated and measured S-parameters, together with measured results obtained for incremental drain-current variations in 12 mA step. Over the range of 17.3 - 21.2 GHz, the balanced amplifier shows a measured flat small-signal gain between 30 and 32.5 dB. It is obvious that both input and output matching are markedly improved across the entire operating band.

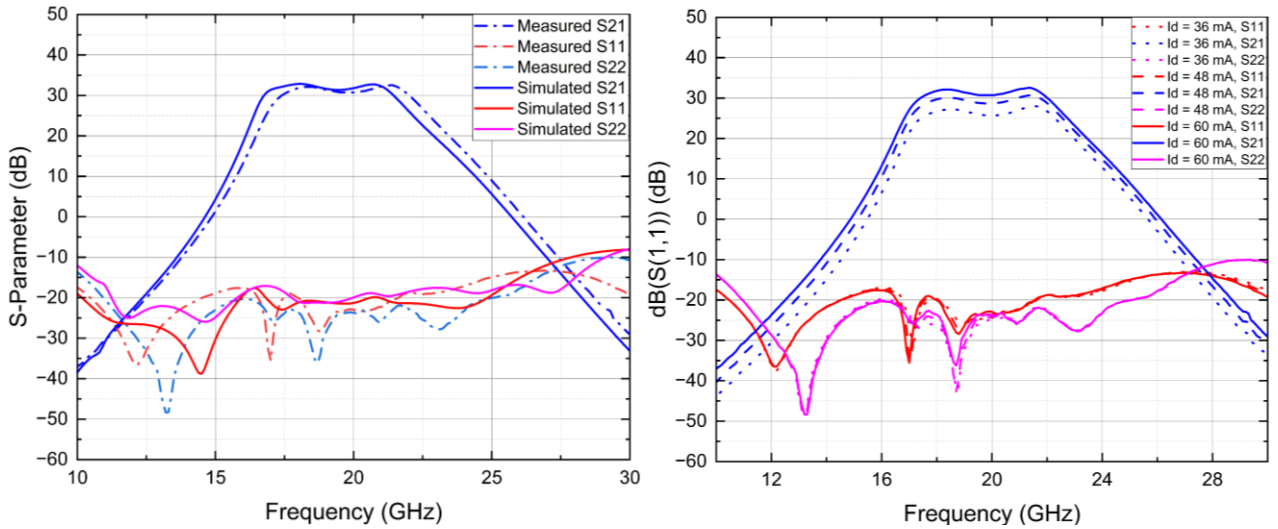


Figure 5.13: S-Parameter comparison, (a) Nominal bias, (b) Measured S-Parameter with I_{D_s} swept by a step of 12mA.

5.2.3 Power performance

Large-signal power measurements of the balanced amplifier are carried out using the same calibration procedure and measurement setup used for the power amplifier cell. With an input power P_{in} of 12 dBm, simulations show a saturated output power between 34.4 dBm and 35.8 dBm and a power-added efficiency in the range of 30 % to 36 % across the operating band. Figure 5.14 shows the measured power results, the balanced amplifier shows a measured saturated output power of up to 35.8 dBm and a peak power-added efficiency of 35.3%. Over the 17.3 - 21.2 GHz frequency range,

a saturated output power between 33.3 dBm and 35.8 dBm and the measured performance shows a PAE spanning from 24.7 % to 35.3 %, showing good agreement with simulation and confirming the effectiveness of the balanced architecture under large-signal operation.

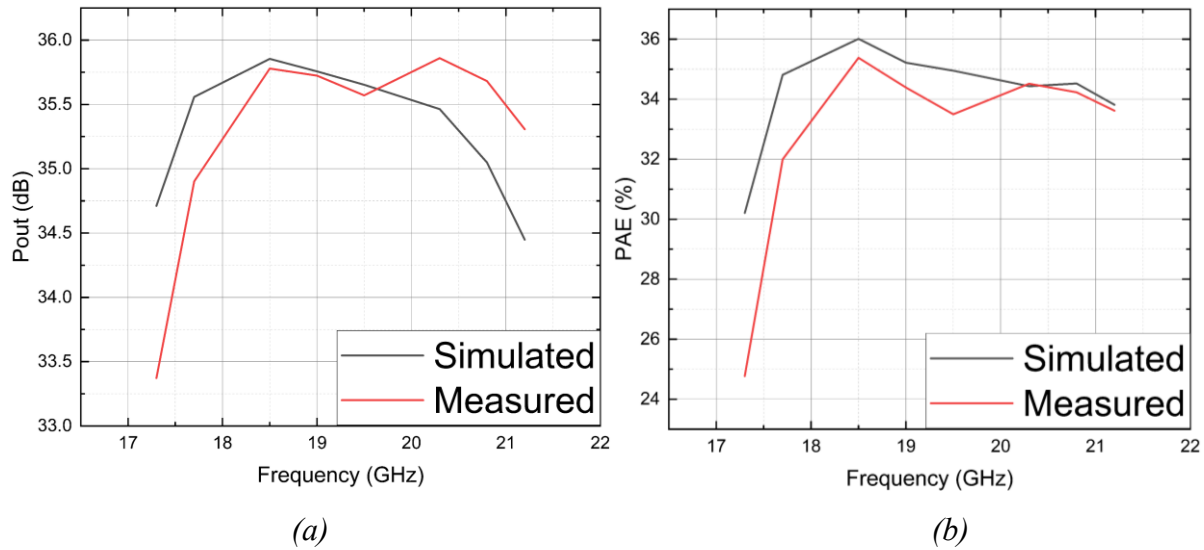


Figure 5.14: Power performance comparison of the corresponding balanced amplifier, (a) P_{out} vs Freq, (b) PAE vs Freq.

5.3 Summary

This chapter presents the design of a K-band power amplifier cell and its balanced amplifier (BA) operating over the 17 - 22 GHz frequency range using the UMS GaN technology. Through comprehensive small-signal, large-signal, stability, and linearity analyses, the proposed designs demonstrate broadband gain, high output power, and competitive efficiency, with measured results closely matching full EM simulations. The balanced architecture further enhances impedance matching and robustness while enabling higher output power levels. Overall, the measured performance confirms that the developed BA is well suited to the high demands of K-band satellite communication systems, where wide bandwidth, high efficiency and reliable operation are essential for advanced RF front-end solutions.

Table 5.1 summarizes the performance differences between this work and the latest published designs, showing that the BA inherits the advantages of its constituent PA cell.

Table 5.1: Performance comparisons between this work and other related State-Of-The-Art.

Ref	Frequency (GHz)	FBW (%)	Peak Gain (dB)	P_{sat} (dBm)	IP3 (dBc)	Peak PAE (%)	Area (mm ²)
[55]	17-2 – 20.2	16	7.5	32	N/A	22.5	4

[56]	25.5 – 27	5.7	7	32	-40	37.2	5.9
[67]	24 – 28	15.4	19	36	-25	41	6.2
[68]	24 – 28	15.4	19.7	35.4	-45.8	36.8	6
[69]	28 – 29	3.5	15	34.4	N/A	22	15.7
This PA	17.3 – 21.2	20.3	33.6	33.4	33	37.7	3
This BA	17.3 – 21.2	20.3	32.5	35.8	N/A	35.3	8.7

Chapter 6: K-band GaAs Packaged Single Positive Supply Low Noise Amplifier

In this chapter, a low-noise amplifier (LNA) design operating between 17 and 22 GHz is presented using the WIN Semiconductor PQG3-0C GaAs process with a positive single-supply bias configuration and packaged implementation. The LNA is developed using an in-house linear FET model and package provided by AltumRF. This design is intended to complement the previously presented same band GaN power amplifier, enabling a hybrid GaAs - GaN transceiver architecture suitable for SmartSAT and SATCOM front-end systems. The use of a GaAs process is selected to prioritise low noise figure and stable small-signal gain at the receiver input, while the single-supply bias and packaging are adopted to reflect practical system integration constraints. When combined with the GaN-based transmit power amplifier, the packaged LNA forms the receiver counterpart of a realistic transceiver front end, allowing the overall system to address both high transmit power and low-noise reception requirements within the same frequency band.

A key contribution of this K-band Low-Noise Amplifier (LNA) is its single-supply bias architecture, which significantly reduces system complexity, footprint, and the risk of device burnout by eliminating the need for external negative voltage generators and complex power-sequencing circuits. This single-supply operation is achieved by utilizing enhancement-mode (E-mode) GaAs pHEMT devices, which naturally require a positive gate-to-source voltage ($V_{gs} > 0$) to operate. To derive this required gate bias from the single main drain supply (V_{DD}), the design employs an on-chip resistive voltage divider network. This divider precisely steps down the positive supply voltage to the optimal gate threshold for minimum noise figure, while integrated bypass capacitors provide robust RF decoupling to prevent low-frequency loop oscillations.

6.1 The LNA

As a part of the transceiver system operating over the same frequency band and targeting the same application as the previously presented power amplifier, a three-stage packaged low-noise amplifier operating between 17 and 22 GHz is developed using a linear FET model. The amplifier draws 47 mA from a nominal 2 V supply and is unconditionally stable. In terms of small-signal results, a measured flat gain of 27 dB, peak of 28.3 dB at 21 GHz and minimum NF of 1.3 dB at 20 GHz are achieved. For large-signal performance, output power and power added efficiency exceed 10.5 dBm and 13%, respectively. To enable a simple and compact packaged implementation, a single bias line is used to supply both the gate and drain networks across all stages, with resistive voltage divider

topology for all the gates and all the bias routing directed toward the south of the die. Device sizes of $2 \times 50 \mu\text{m}$ are selected for each stage in order to minimise current consumption while achieving low-noise performance. The LNA's schematic is illustrated in Figure 6.1. The amplifier occupies a die area of $1.4 \times 1 \text{ mm}^2$ and is implemented in a $2.5 \times 2.5 \text{ mm}^2$ QFN package, which is shown in Figure 6.2.

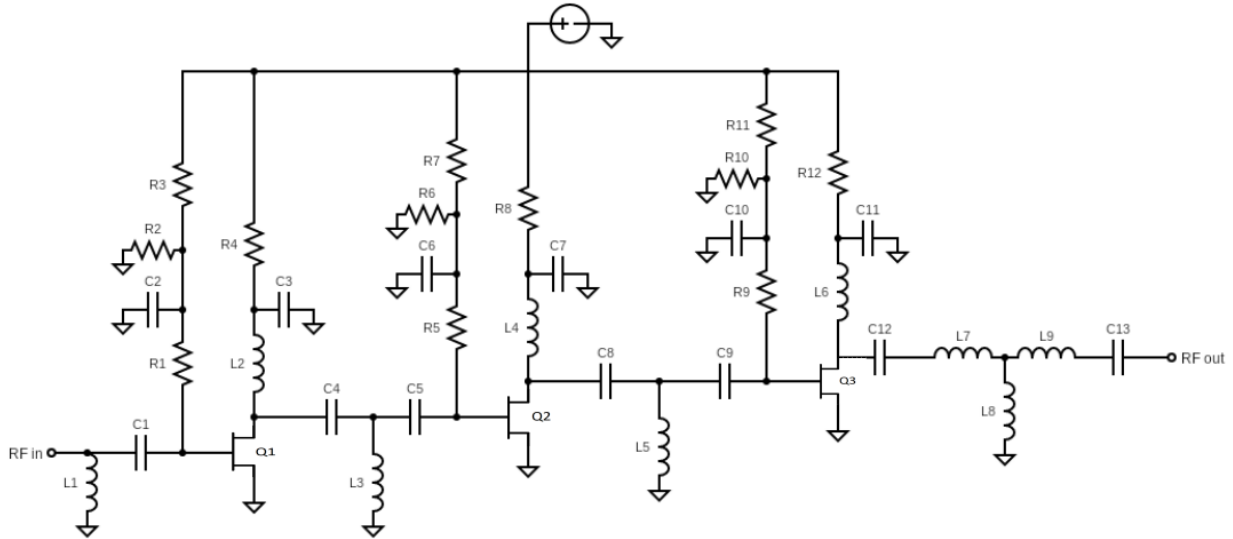


Figure 6.1: Schematic of the proposed 3-stage LNA.

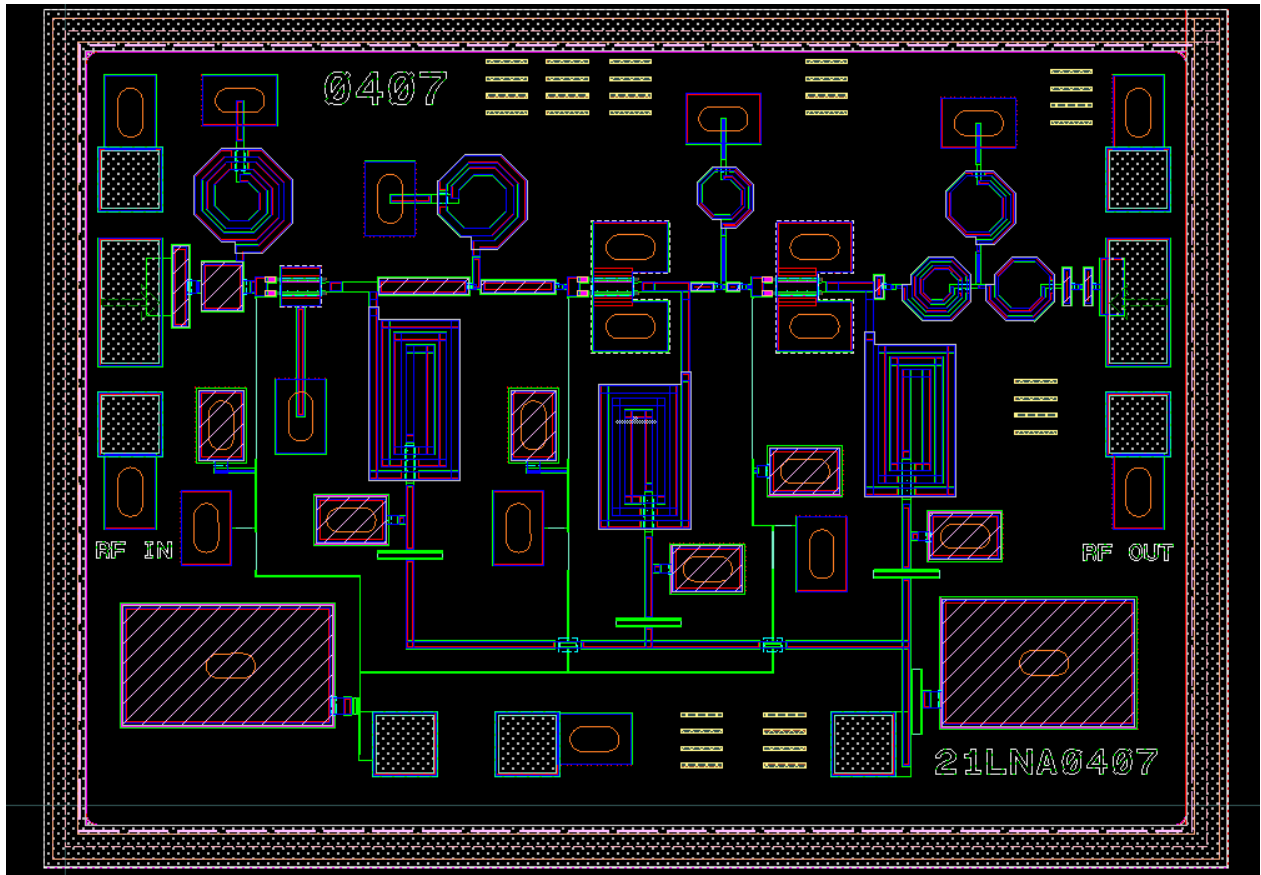


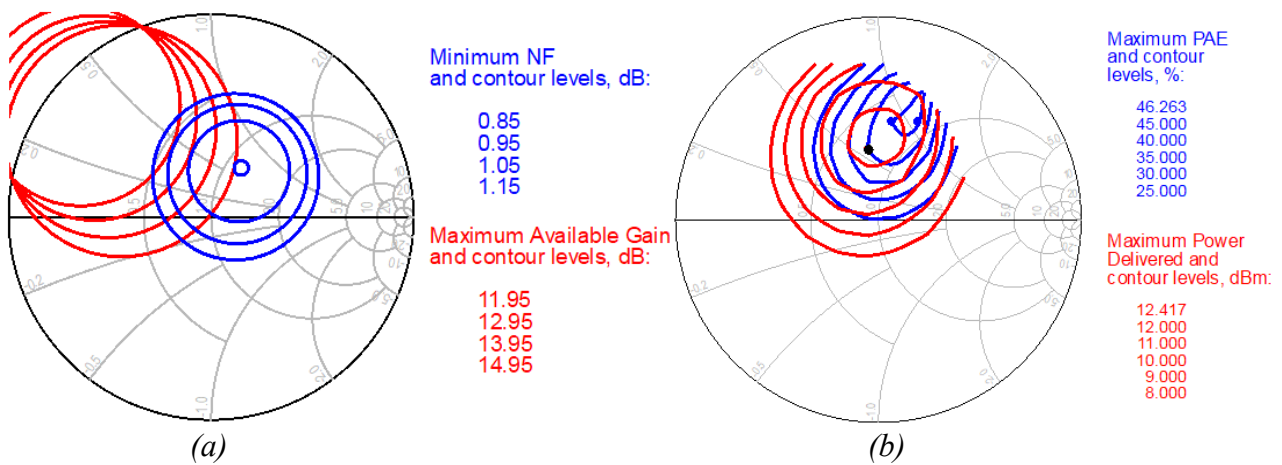
Figure 6.2: Layout of the proposed LNA.

6.2 Noise figure and power analysis

To determine the optimal transistor gate periphery for the single-supply LNA, a comprehensive parametric analysis of various device sizes was initially conducted. The Maximum Available Gain (MAG) and minimum noise figure (NF_{min}) were simulated as a function of device size and frequency across the K-band. While larger gate peripheries inherently provide higher current drive and output power, their increased parasitic capacitances (C_{gs} and C_{gd}) significantly degrade high-frequency MAG and make broadband noise matching highly challenging. Conversely, devices that are too small offer excellent NF_{min} but lack the requisite forward gain and power handling.

Based on these comparative simulations, the $2 \times 50 \mu m$ transistor was selected for the design as it provided the optimal trade-off, delivering a highly competitive NF_{min} while sustaining sufficient MAG across the target bandwidth. Consequently, the detailed noise and power are analysed using this optimized $2 \times 50 \mu m$ device size.

Noise analysis is performed on the $2 \times 50 \mu m$ transistor, where small-signal gain and noise performance use noise-source pull to identify the source impedance region that minimizes noise figure while maintaining sufficient gain. Power analysis is also simulated on the $2 \times 50 \mu m$ transistor using large-signal load-pull measurements to extract output power and efficiency as a function of load impedance, which establishes a sufficient output power while maintaining as low current consumption as possible. Figure 6.3 illustrates the initial gain/NF and power analysis for this selected device periphery.



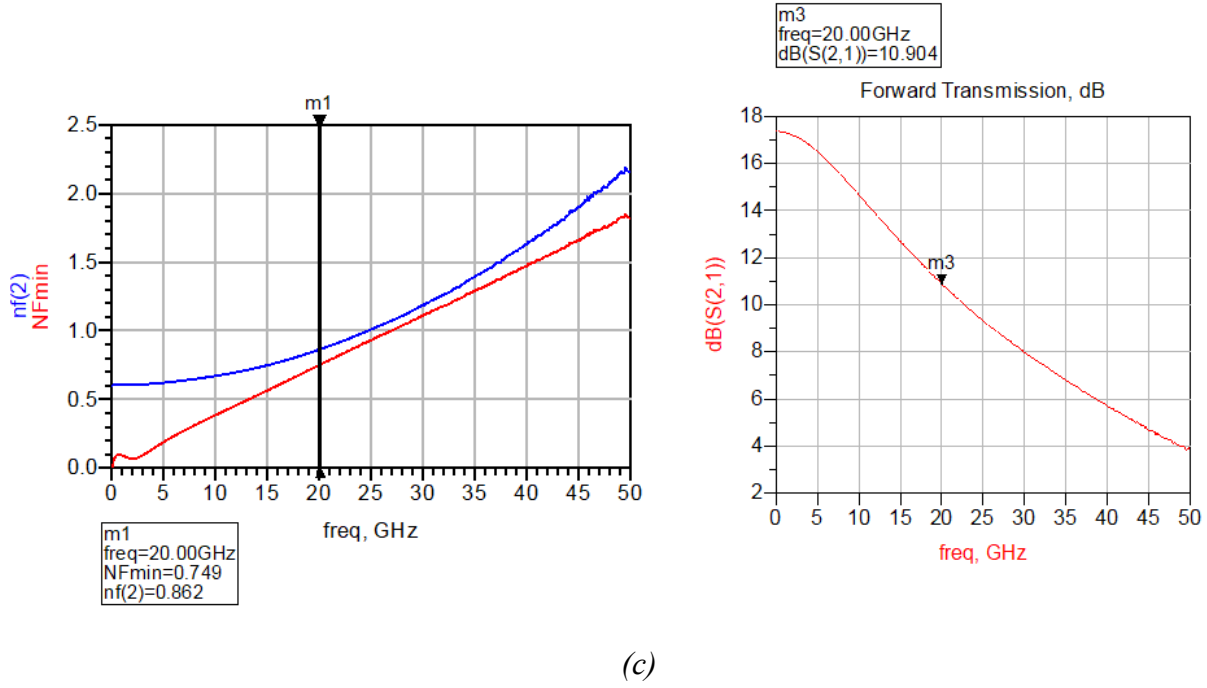


Figure 6.3: (a) and (b) Noise/Gain and Power contours analysis, (c) Simulated NF_{min} and MAG.

6.3 Stability analysis

At K-band, LNAs are particularly prone to high-frequency oscillations due to the high intrinsic f_T of the GaAs pHEMT devices, as well as low-frequency oscillations stemming from bias network resonances. Furthermore, the use of inductive source degeneration, while beneficial for noise matching, introduces positive feedback that can push the input impedance into the negative resistance region if not carefully controlled.

The stability analysis follows the same procedure for all designs. Conventional stability metrics, including the Rollett stability factor K and the source- and load-stability measures μ_s and μ_L , are first evaluated over frequency to find regions of potential conditional instability. Although these parameters provide a convenient first assessment, their validity becomes increasingly limited at millimetre-wave frequencies and in multi-stage amplifiers, where distributed effects, internal feedback paths, and interstage coupling can violate the assumptions of a two-port network. As a result, the analysis also applies Ohtomo's method, which directly evaluates the loop gain and the associated Nyquist encirclement behaviour and provides a more physically meaningful assessment of stability. The design process then incorporates modifications based on this analysis to suppress unintended feedback loops and to ensure unconditional stability across the operating band and beyond.

All the stability factors are checked to ensure the unconditional stability of the complete circuit. The Rollett stability factor K and the source/load stability measures (μ_s/μ_L) are all maintained above 1,

and all the stability factors are always lying outside the unit circle, as illustrated in Figure 6.4.

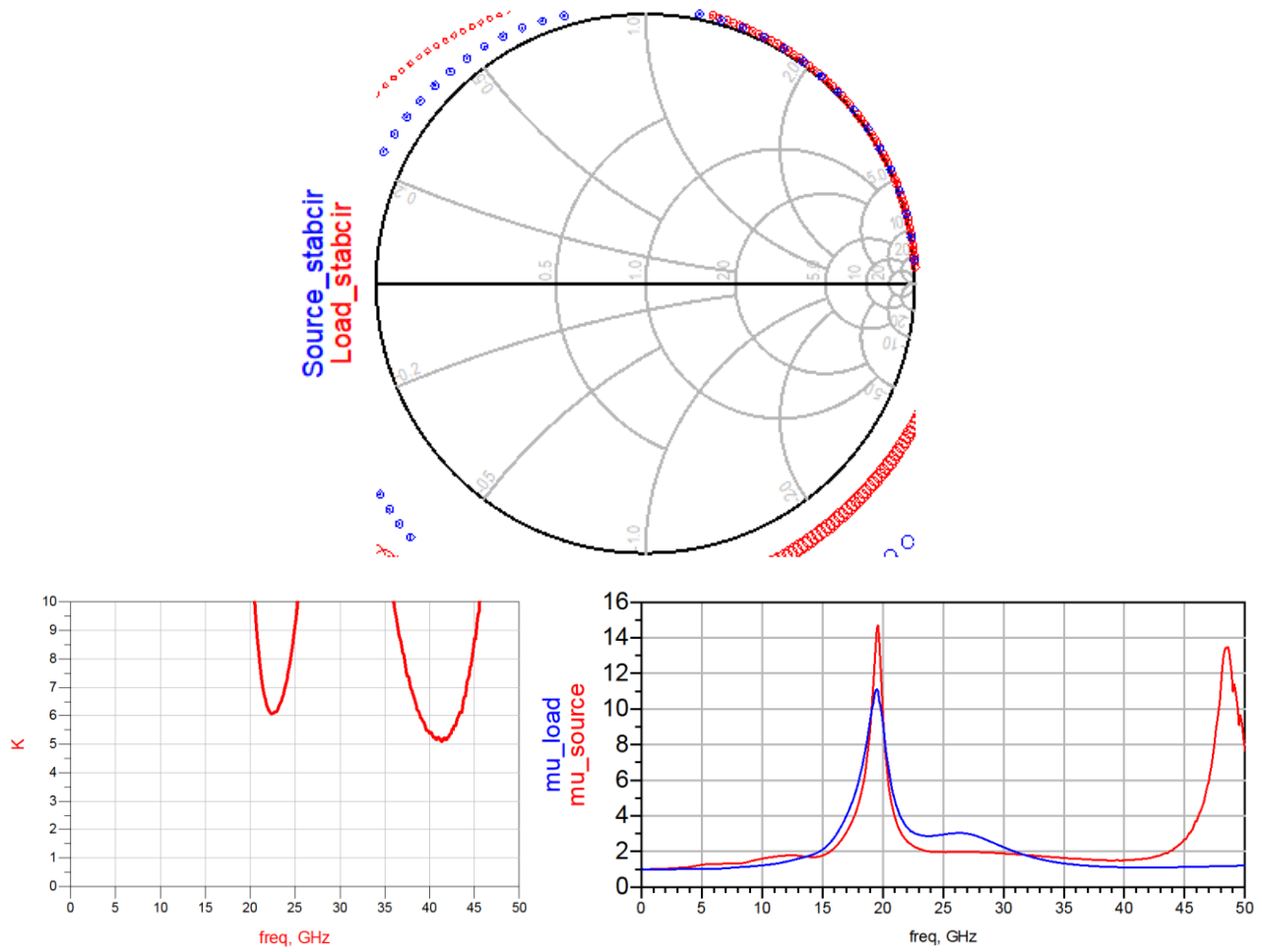


Figure 6.4: Conventional stability factors and circles.

In addition, the Ohtomo analysis confirms that the computed loop gain exhibits no critical encirclement, with the corresponding trajectories lying entirely within the unit circle, as illustrated in Figure 6.5. The agreement between these complementary factors provides convincing evidence that the power amplifier is unconditionally stable at all frequencies.

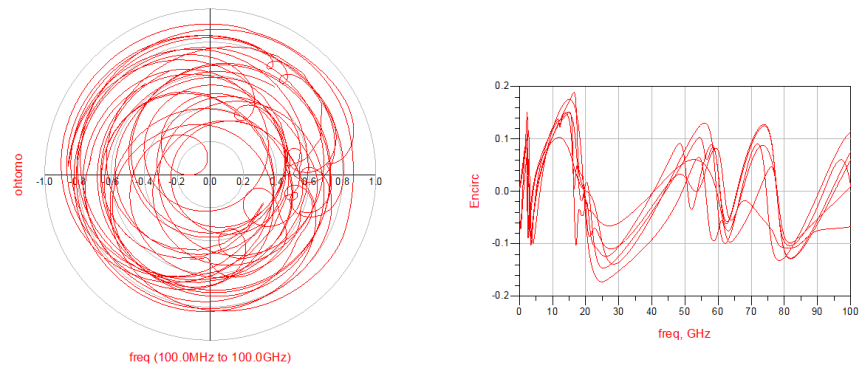


Figure 6.5: Ohtomo simulation.

6.4 Operation of the single positive supply bias network

The proposed K-band Low-Noise Amplifier (LNA) utilizes a single positive supply configuration. This topology significantly simplifies the overall system architecture by eliminating the need for external negative voltage generators and complex drain-gate bias sequencing circuits, which are typically required for standard depletion-mode (D-mode) pHEMTs to prevent accidental device burnout. This single-supply operation is made possible through the use of enhancement-mode (E-mode) GaAs pHEMT devices, which naturally require a positive gate-to-source voltage ($V_{gs} > 0$) to turn on the channel and establish the quiescent drain current.

To generate the necessary bias points from a single external power source, an on-chip resistive voltage divider network is employed. A single positive DC voltage (V_{DD}) is supplied to the chip to bias the drain terminals directly. The required gate bias voltage (V_{GG}) is concurrently derived from this same main V_{DD} rail using a precision thin-film resistor divider comprising a series resistor (R_1) and a shunt resistor to ground (R_2). The resulting gate voltage applied to the transistors is determined by the standard voltage division ratio:

$$V_{GG} = V_{DD} \left(\frac{R_2}{R_1 + R_2} \right)$$

By meticulously selecting the values of R_1 and R_2 , the voltage is stepped down to the exact optimal positive threshold required to bias the E-mode transistors for minimum noise figure and optimal forward gain.

Crucially, deriving both the gate and drain voltages from the same DC rail introduces a potential vulnerability, which is the unwanted RF feedback from the high-power drain nodes back to the highly sensitive gate nodes through the resistive network. To prevent this feedback and maintain unconditional stability, the bias network features robust RF decoupling. Large on-chip bypass capacitors are integrated at the center node of the voltage divider (the V_{GG} node) to provide a solid low-frequency AC ground. This ensures that the resistive divider strictly transfers the DC bias potential while remaining completely electrically isolated from the millimeter-wave signal path, thereby suppressing any potential low-frequency loop oscillations.

6.5 Effects of packaging of bond wires and transition losses

While the bare-die MMIC demonstrates optimal performance in a controlled on-wafer environment,

the transition to a packaged module introduces critical parasitic elements that heavily influence performance at K-band frequencies (17 – 22 GHz). The packaging process impacts the Low-Noise Amplifier (LNA) primarily through two mechanisms, which are bond wire parasitics and RF transition insertion losses.

The electrical connections between the MMIC RF pads and the external package or printed circuit board (PCB) are realized using gold bond wires. At microwave and millimeter-wave frequencies, these wires cannot be treated as ideal short circuits. They introduce significant series inductance (approximately 1 nH per millimeter of length) as well as minor skin-effect resistive losses. For an LNA, this parasitic series inductance at the RF input is particularly critical. It shifts the carefully optimized optimum noise reflection coefficient (Γ_{opt}) and the input impedance match away from the 50 Ω system reference. If uncompensated, this inductive shift leads to a degraded overall noise figure and poor input return loss (S_{11}). To minimize these effects in the final assembly, double or triple parallel bond wires are often employed to reduce the equivalent series inductance, and the physical length of the wire profile is kept as short as the package cavity allows.

Beyond the bond wires themselves, the physical transition from the die pad to the package substrate (typically a microstrip or grounded coplanar waveguide line) introduces passive insertion loss and structural impedance discontinuities. According to Friis's formula for cascaded noise figure, any passive loss preceding the first active amplifier stage adds directly, decibel-for-decibel, to the overall system noise figure. For instance, an input transition loss of 0.3 dB will directly increase the packaged LNA's noise figure by 0.3 dB compared to the on-wafer bare-die measurements. Furthermore, impedance mismatches at this boundary cause signal reflections that can create gain ripple across the operating band.

Because these packaging parasitics drastically alter the intrinsic LNA performance, true standalone die simulations are insufficient. Accurate prediction of the packaged LNA requires comprehensive 3D full-wave electromagnetic (EM) co-simulation. By modelling the exact bond wire loop profiles, the thickness of the die-attach epoxy, and the package routing lines, the MMIC's internal input and output matching networks can be intentionally offset during the design phase to absorb these packaging parasitics into the final match.

6.6 S-Parameter

The packaged LNA operates from a nominal 2 V supply and exhibits unconditional stability across

the frequency band of interest. All calibrations are completed prior to testing. The S-parameters are measured with an Anritsu 3739C Vector Network Analyzer. As shown in Figure 6.6, the amplifier achieves a measured flat gain of approximately 27 dB from 17 to 22 GHz, with a peak gain of 28.3 dB. Throughout the operating band, the input and output return losses, S_{11} and S_{22} , remain better than -10 dB.

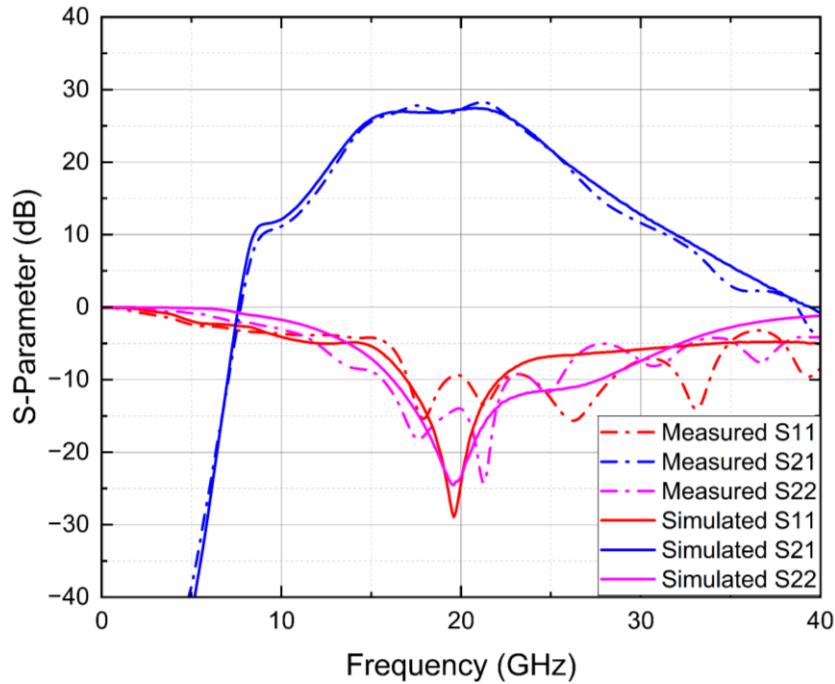


Figure 6.6: S-Parameter comparison between simulation and measurement.

6.7 Noise Performance

The noise figure performance of the packaged LNA is tested after completion of all required calibrations. The noise figure measurement uses a Keysight N9030B Signal Analyzer, with a Keysight U1832C noise source connected at the input and a Keysight U7228F pre-amplifier connected at the output. As shown in Figure 6.7, the measured noise figure varies from 1.3 dB to 1.46 dB across the frequency band. The minimum noise figure reaches 1.3 dB at 20 GHz.

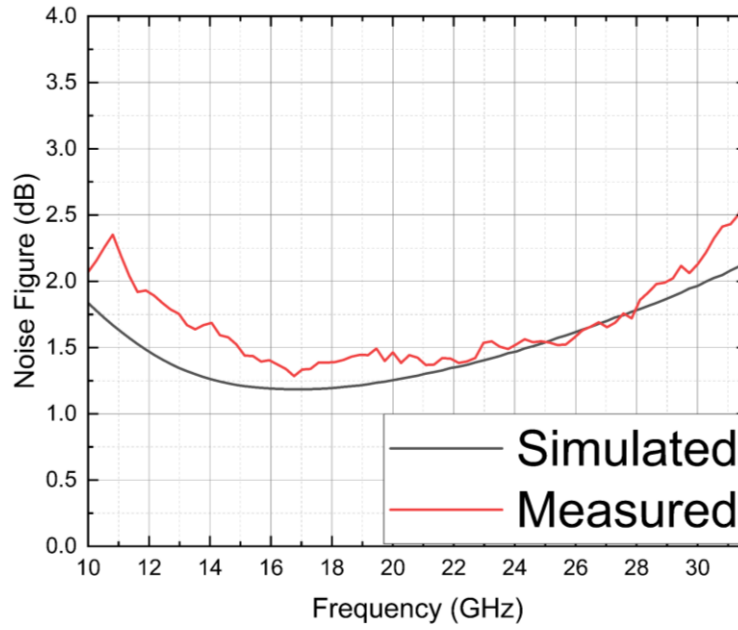


Figure 6.7: Noise Figure comparison between simulation and measurement.

6.8 Power performance

The measured power performance of the packaged LNA is evaluated after completion of all required calibrations. The power measurements use a Keysight E8267D vector signal generator as the input source. An Agilent 8487D power sensor monitors the input power, and an Agilent 8487A power sensor measures the output power. Figure 6.8 shows the measured power performance, where at $P_{in} = -10$ dBm, the output power exceeds 10.5 dBm and the power-added efficiency exceeds 13% across the frequency band, and the measured power results with swept input power at mid band 20 GHz.

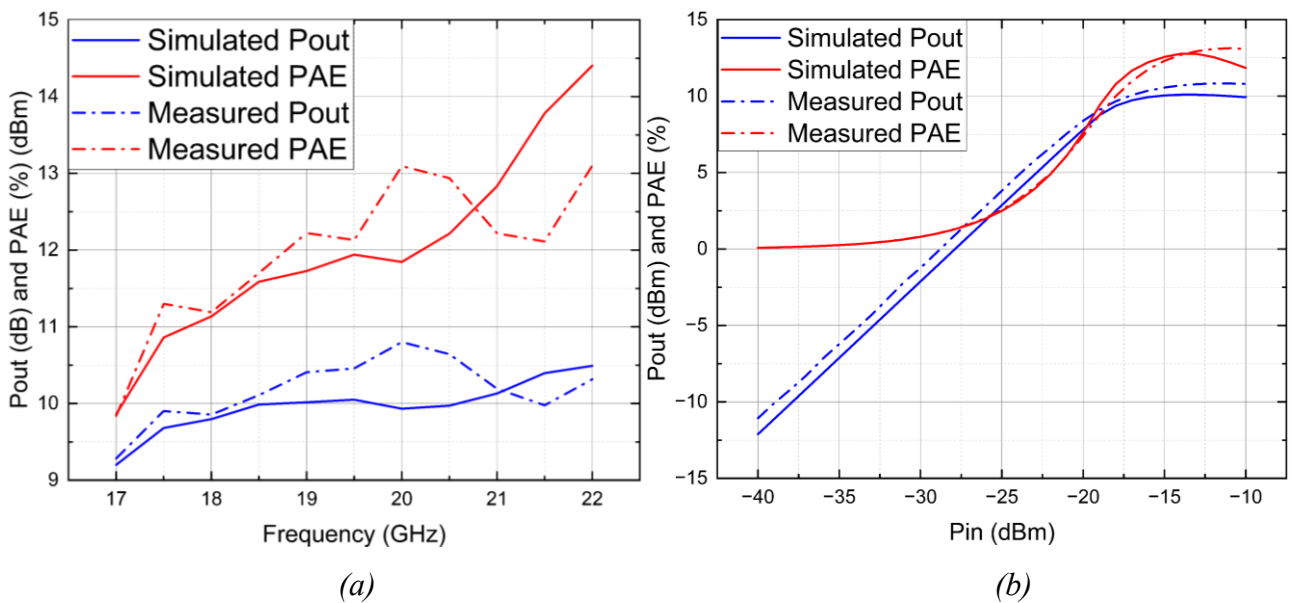


Figure 6.8: Power results, (a) P_{out} and PAE vs frequency at $P_{in} = -10$ dBm, (b) P_{out} and PAE vs P_{in} at 20 GHz.

To further assess the linearity performance of the designed amplifier, two-tone measurements are performed at multiple frequencies within the operating band. As shown in Figure 6.9, the measured worst-case third-order intermodulation distortion (IMD3) and the corresponding worst-case output third-order intercept point (OIP3) behave accordingly with output power. These results show strong agreement with the expected nonlinear behaviour of the LNA under large-signal operating conditions.

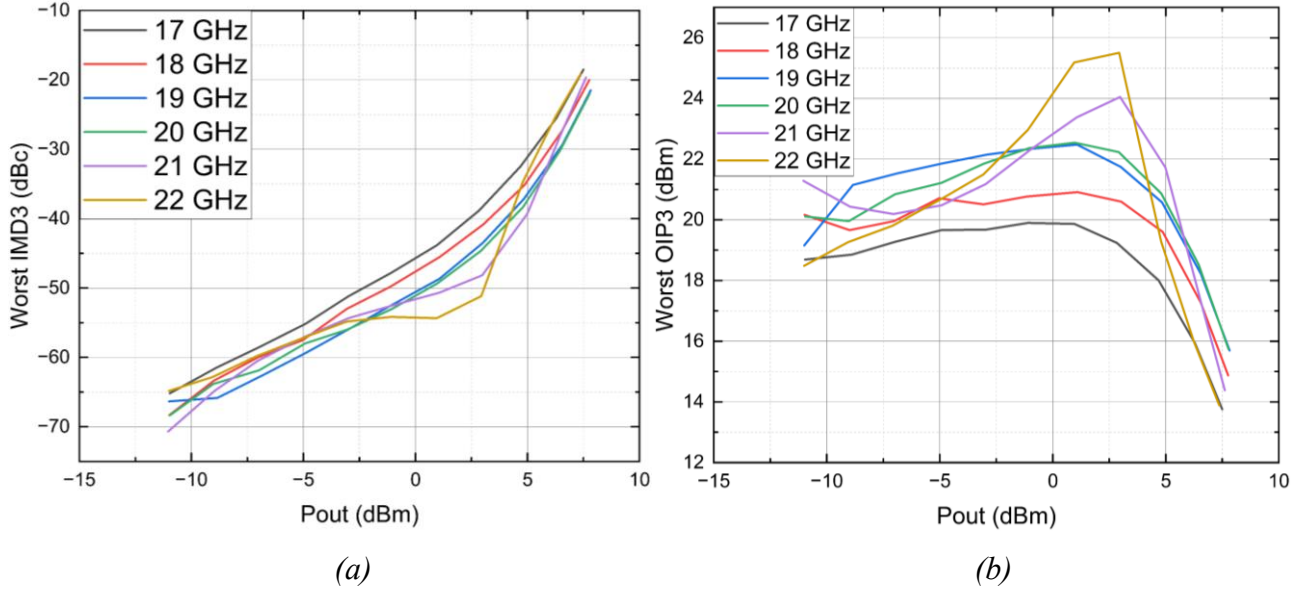


Figure 6.9: Intermodulation performance, (a) Worst IMD3 vs P_{out} , (b) Worst OIP3 vs P_{out} .

It should be noted that Figure 6.9 presents only the measured IP3 performance. Due to the limitations of the large-signal non-linear models provided in the foundry design kit, which primarily optimize for fundamental output power and do not accurately capture higher-order intermodulation products (IMD3) at K-band frequencies, the simulated IP3 deviates significantly from physical reality. Consequently, the linearity analysis relies strictly on the empirical measured data, which confirms the LNA's capability to handle complex modulation schemes.

6.9 Summary

This work presents a complete GaAs three-stage packaged positive single-supply low noise amplifier that operates from 17 to 22 GHz. The measured results show good agreement with simulations across small-signal, large-signal, and linearity performance, which validates the proposed design methodology. Together with the previously developed GaN power amplifier, the LNA forms a complete front-end transceiver solution for space applications. The use of a packaged implementation, combined with robust measured performance, supports the suitability of this LNA design for high-volume manufacturing and commercial deployment.

Table 6.1 compares the performance of this work with other state-of-the-art LNAs and demonstrates its competitive performance.

Table 6.1: Performance comparisons between this work and other related State-Of-The-Art.

Ref	Freq (GHz)	Tech	Gain (dB)	NF (dB)	Pout (dBm)	DC power (mW)	Package
[70]	17 – 25	GaAs	27	1.4	8	81	4 x 4 mm QFN
[73]	17 – 22	GaAs	25	1.3	20	315	4 x 4 mm QFN
[74]	17.7 – 21.2	SOI	22	1.2	-2	15 per channel	2.7 x 2.7 mm BGA
This work	17 – 22	GaAs	28.3	1.3	10.5	94	2.5 x 2.5 mm QFN

Chapter 7: Conclusion and Future Work

7.1 Conclusion

This thesis has examined the design, methodologies and characterisation of millimetre-wave monolithic microwave integrated circuits intended for next-generation 5G transport networks and SATCOM front-ends, with an emphasis on the K-band and W-band frequency band. Across these two spectral regions, the work has demonstrated how careful device-level modelling, topology selection, and electromagnetically informed layout strategies can meaningfully advance the state of MMIC low noise and power amplifier performance in technologies relevant to spaceborne and terrestrial systems.

At W-band, the GaAs driver amplifier designs represent an extension of the thesis into the sub-THz domain, where the electrical size of passive structures becomes comparable to the device dimensions themselves. The investigation reveals that at these frequencies, the boundary between circuit-level and field-level behaviour dissipates, demanding the use of full-wave-derived compact models, carefully shaped transmission-line transitions, and layout configurations aimed at suppressing slot-mode leakage and unintended resonances. The measured W-band results align closely with the predicted gain and bandwidth performance, illustrating that GaAs remains a practical and manufacturable process for high-frequency driver stages even in the era of advanced InP and SiGe processes.

The GaN PAs designed for the K-band further demonstrate how high-linearity, high-output-power operation may be reconciled with efficiency and thermal robustness. Through a combined exploration of harmonic terminations, bias strategy and interconnect parasitics, the amplifiers achieve competitive saturated power and third-order intercept levels suitable for multi-carrier and wideband 5G waveforms. The work highlights the critical role of electromagnetic simulation and substrate mode control, both of which remain decisive factors in ensuring predictable and repeatable PA behaviour across wide process spreads.

For the K-band GaAs LNA, the work establishes that sub-1.3 dB noise figures can be achieved within the WIN PQG3 process by judiciously balancing minimum-noise and conjugate-match conditions in the presence of non-negligible parasitics. The design methodology developed here underscores the importance of simultaneously accounting for transistor geometry optimisation, matching network topologies and layout-induced coupling, all of which become increasingly influential as operating frequencies approach the upper limits of GaAs pHEMT technology. Measurements confirm the

simulated performance, which confirm that the LNA design can serve as a practical front-end element for high-dynamic-range SATCOM receivers operating under stringent noise-temperature budgets.

As a result, the contributions of this thesis provide a coherent design framework applicable to mm-wave LNAs, driver amplifiers and power amplifiers across multiple semiconductor processes. The findings emphasise that agreeable performance gains are still attainable when classical MMIC design principles are combined with modern EM-driven optimisation techniques and a system-level perspective tailored to emerging broadband wireless standards.

7.2 Future work

The work presented in this thesis opens several opportunities for further development. For the low-noise amplifier designs, future efforts could focus on reducing DC power consumption while preserving the low noise figure achieved in this work. This could be explored through more detailed optimisation of the bias conditions and device dimensions, particularly within the constraints of single-supply operation and packaged implementation. Additional refinement of the matching networks may also allow further improvements in noise performance without increasing power dissipation.

For the power amplifier designs, higher output power levels may be obtained by extending the current single-ended and balanced architectures toward more advanced power-combining approaches. Topologies such as distributed power combining or load-modulated balanced amplifiers (LMBAs) could be investigated to increase output power and efficiency while maintaining the bandwidth and robustness required for SATCOM and SmartSAT applications. Such techniques would build naturally on the balanced amplifier work presented in this thesis.

A further interest would be the development of a fully integrated MMIC front end incorporating both the low-noise amplifier and power amplifier within the same chip. Combining the receiver and transmitter functions would enable a more compact and system-oriented solution, but would require careful consideration of isolation, stability and biasing interactions between the two paths. Addressing these challenges would represent a logical extension of the individual LNA and PA designs presented here, and would move the work closer to a practical, integrated front-end solution.

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Appendix

W-band driver amplifier measurement setups.

The S-parameter measurements use a Keysight PNA Network Analyzer (N5290A). To ensure measurement accuracy, a standard Short-Open-Load-Through (SOLT) calibration is carried out on a calibration substrate, establishing the measurement reference plane at the tips of the GSG probes.

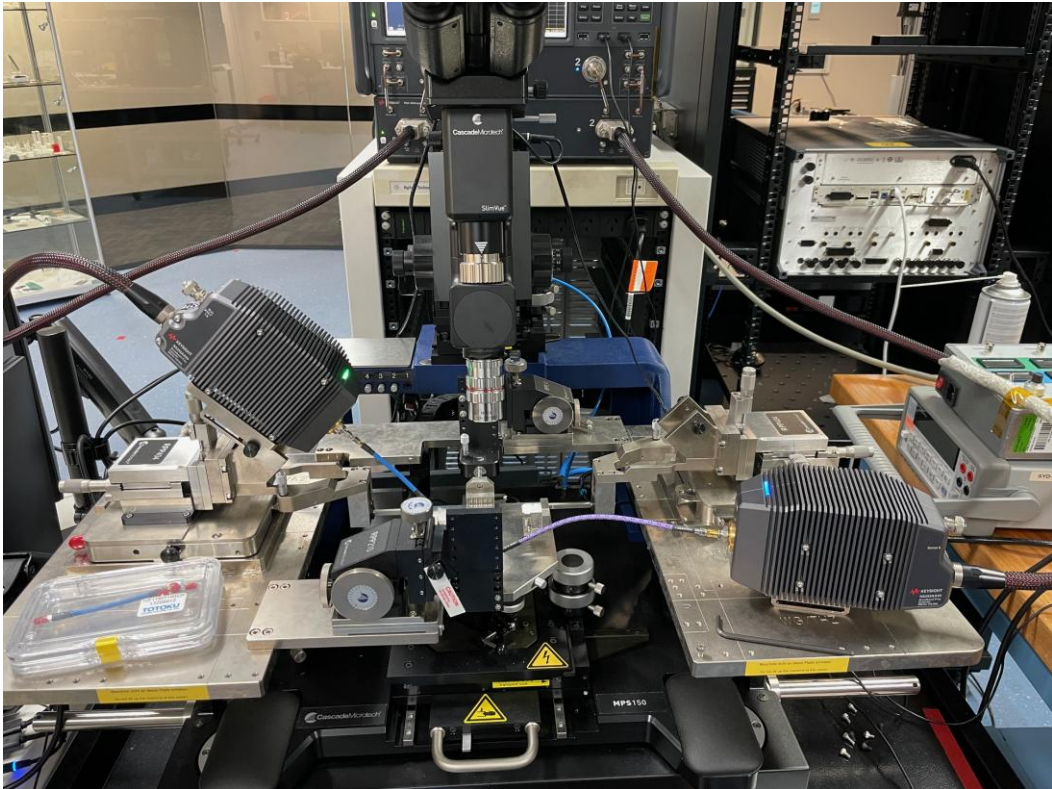


Figure 0.1: Initial probe station for the W-band S-Parameter measurement.

For a probe noise measurement, a Keysight Signal Analyzer (N9030B) is used in conjunction with 2 noise sources connected at both the input and output ports. Prior to data acquisition, full noise figure calibration procedures are carefully completed to ensure reliable and repeatable results

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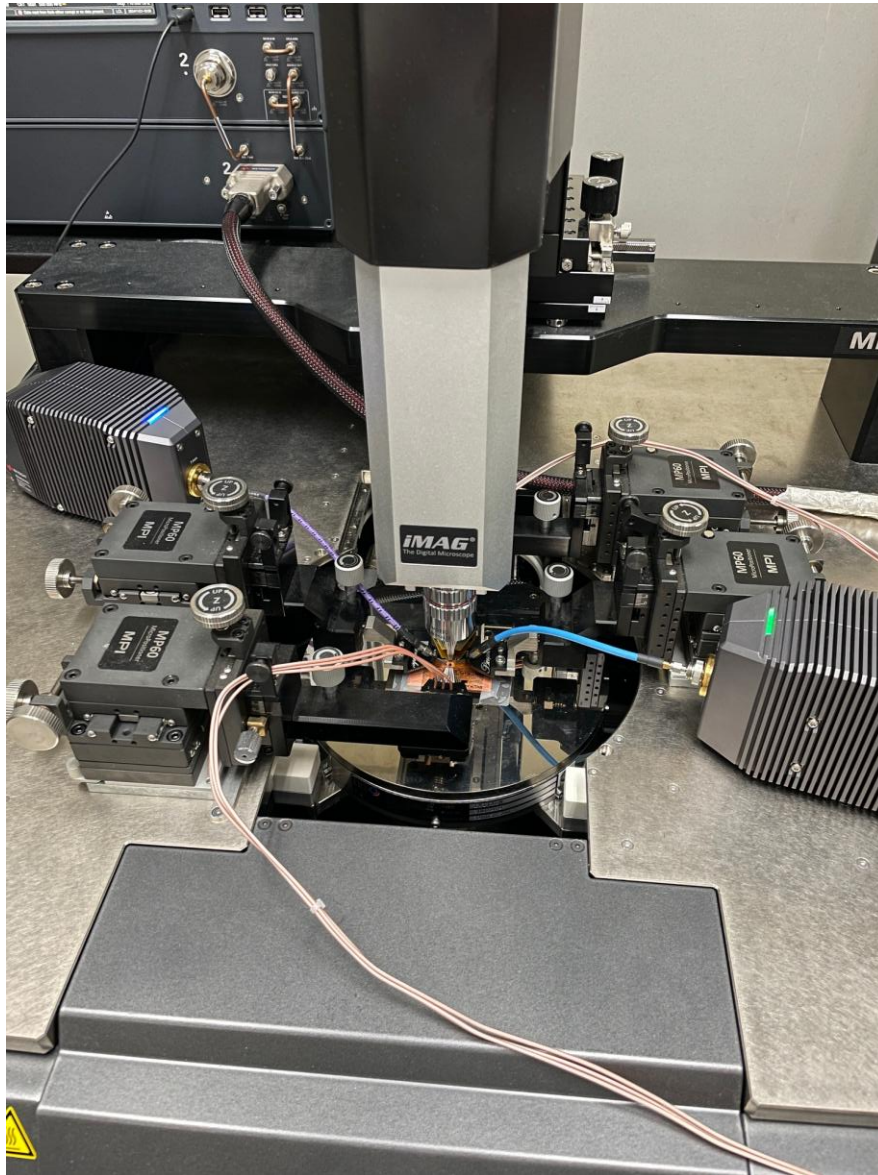


Figure 0.2: W-band driver amplifier measurement setup.

A Keysight signal generator (E8257D) is used to provide the RF input, while power sensors are placed at both the input and output ports to accurately monitor delivered and extracted power levels. All required calibrations are completed prior to measurement to remove systematic losses and set up the reference planes at the probe tips.



Figure 0.3: W-band driver amplifier power measurement setup.

K-band power amplifiers measurement setups.

The measurements use a Keysight N5290A Vector Network Analyzer, ensuring accurate extraction of the amplifier's linear response over the frequency range.

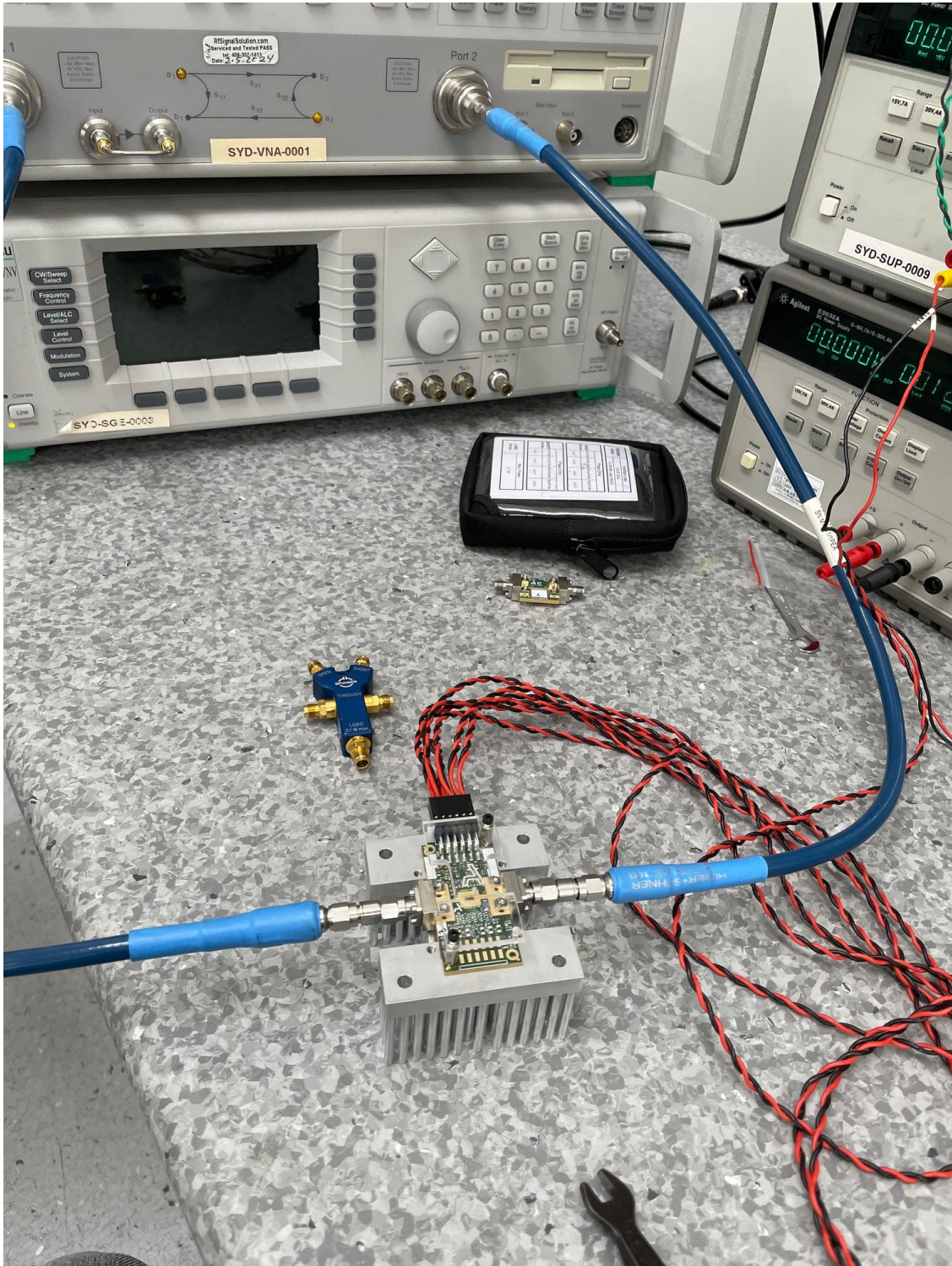


Figure 0.4: K-band power amplifiers S-Parameter measurement setup.

A continuous-wave excitation is provided by a Keysight E8257D Analog Signal Generator, delivering sufficient drive to fully explore the saturation characteristics of the power amplifier. Two calibrated power sensors, used in combination with a coaxial directional coupler and a power meter, enable precise monitoring of the power levels at the device under test.

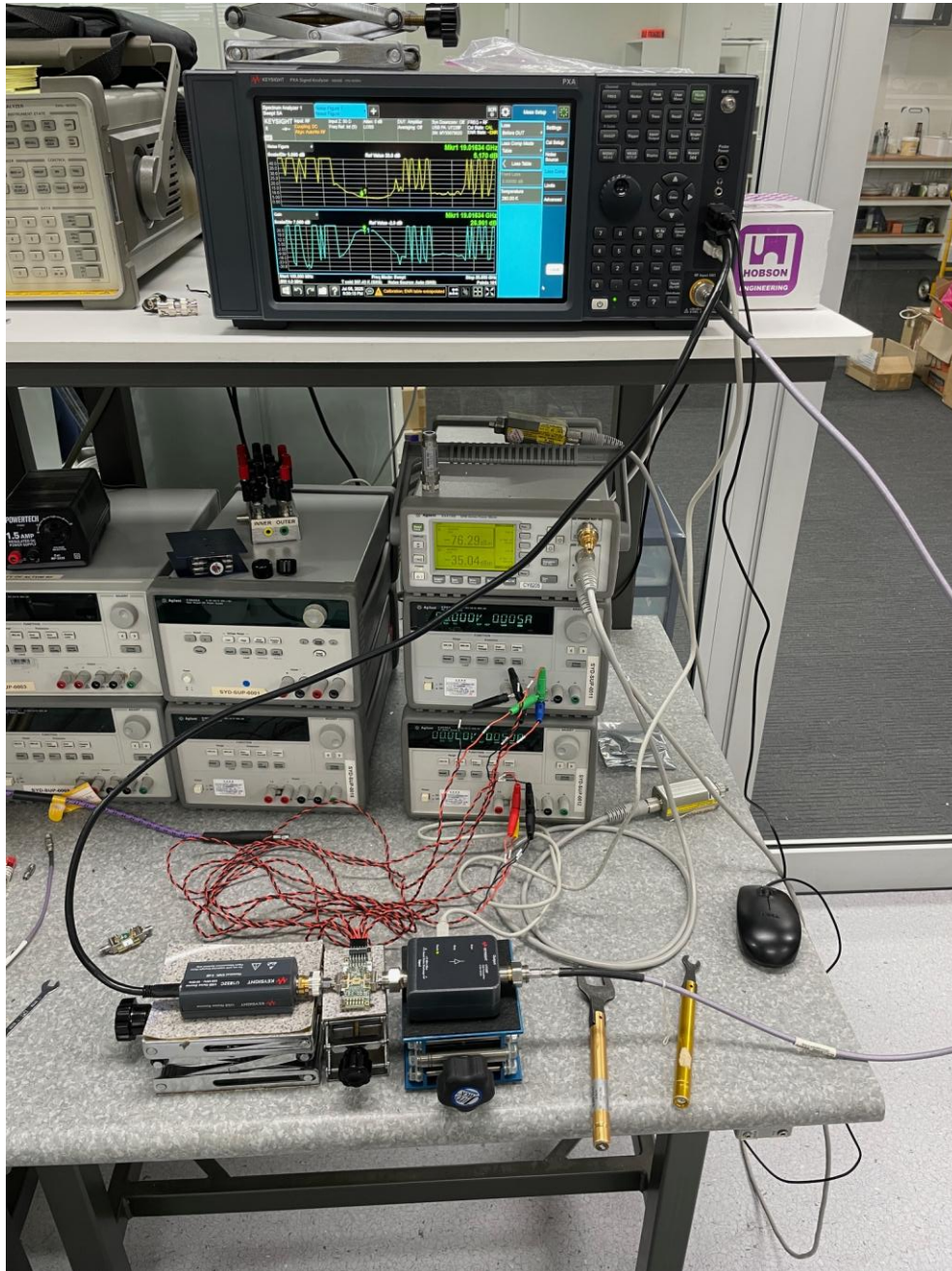


Figure 0.5: K-band power amplifiers power measurement setup.

K-band low noise amplifier measurement setups.

The S-parameters are measured with an Anritsu 3739C Vector Network Analyzer.

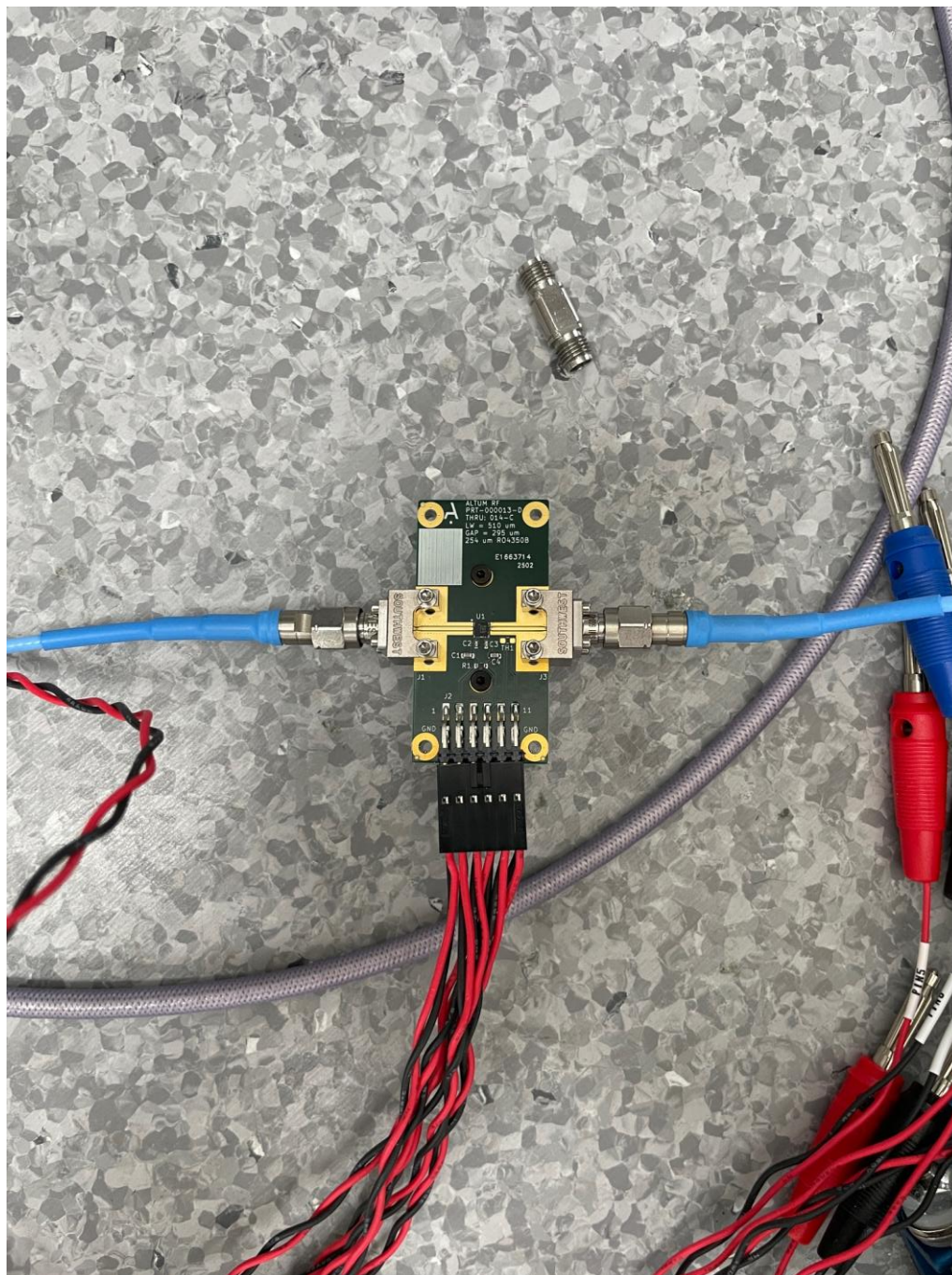


Figure 0.6: K-band low noise amplifier S-Parameter measurement setup.

The noise figure performance of the packaged LNA is tested after completion of all required calibrations. The noise figure measurement uses a Keysight N9030B Signal Analyzer, with a Keysight U1832C noise source connected at the input and a Keysight U7228F pre-amplifier connected at the output.

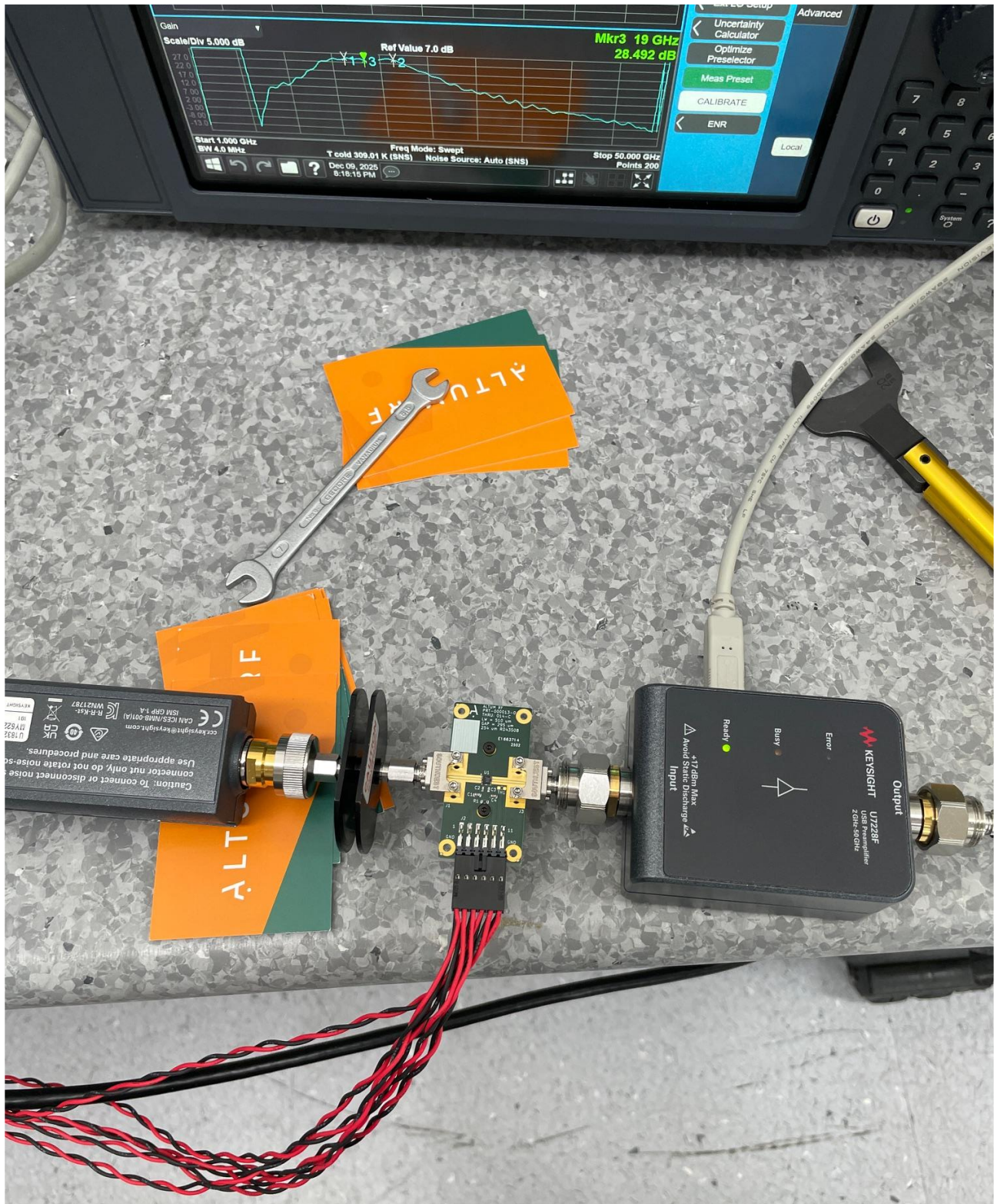


Figure 0.7: K-band low noise amplifier noise measurement setup.

The measured power performance of the packaged LNA is evaluated after completion of all required calibrations. The power measurements use a Keysight E8267D vector signal generator as the input source. An Agilent 8487D power sensor monitors the input power, and an Agilent 8487A power sensor measures the output power.

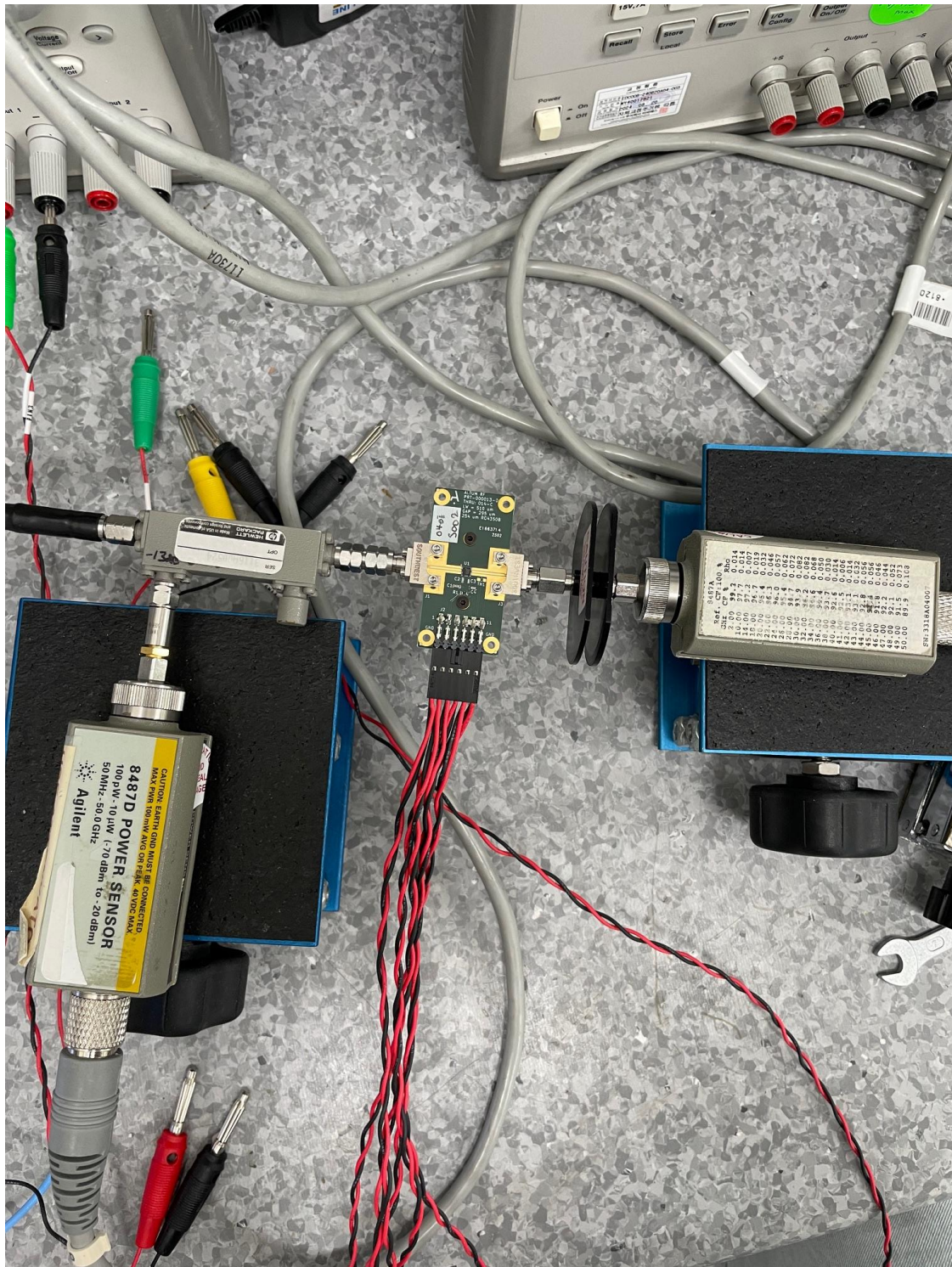


Figure 0.8: K-band low noise amplifier power measurement setup.

To further assess the linearity performance of the designed amplifier, two-tone measurements are performed at multiple frequencies within the operating band

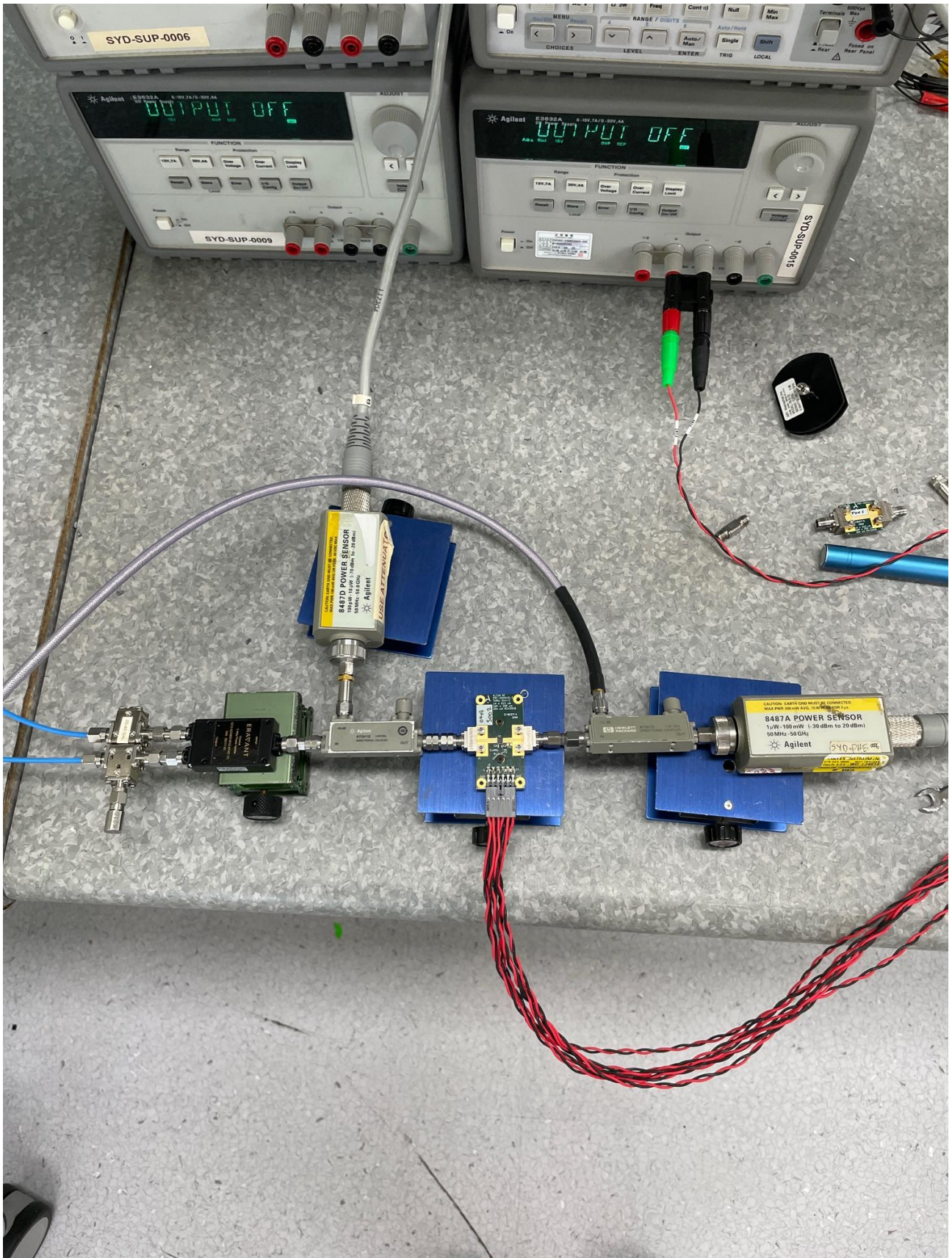


Figure 0.9: K-band low noise amplifier linearity measurement setup.