FPGA–Based Formation Control of Multiple Ubiquitous Indoor Robots

by

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A thesis submitted in fulfillment of the requirements

for the degree of Doctor of Philosophy

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May 2011

CERTIFICATE OF AUTHORSHIP/ORIGINALITY

I certify that the work in this thesis has not been previously submitted for a degree nor has it been submitted as a part of the requirements for a degree except as fully acknowledged within the text.

I also certify that this thesis has been written by me. Any help that I have received in my research and in the preparation of the thesis itself has been fully acknowledged. In addition, I certify that all information sources and literature quoted are indicated in the thesis.

Ying-Hao Yu

Abstract

This thesis explores the feasibility of using Field-Programmable Gate Array (FPGA) technology for formation control of multiple indoor robots in an ubiquitous computing environment. It is anticipated that in the future, computers will become integrated with people's daily lives. By way of a hub of surrounding sensors, computers and embedded systems, indoor robots will receive commands from users and execute tasks such as home and office chores in a cooperative manner. Important requirements for such scenarios are power efficiency and computation reliability. The focuses of this project are on exploiting the use of the System-on-Programmable Chip technology and ambient intelligence in developing suitable control strategies for the deployment of multiple indoor robots moving in desired geometric patterns.

After surveying the current problems associated with computing systems and robotics, this research was determined to design an ubiquitous robotics system using Field-Programmable Gate Array (FPGA) technology, a serial of the Register-Transfer Level (RTL) and gate level hardware for image processing, and control implementation. Work was done to develop novel, FPGA-feasible algorithms for colour identification, object detection, motion tracking, inter-robot distance estimation, trajectory generation and formation turning. These algorithms were integrated on a single FPGA chip to improve energy efficiency and real-time reliability. With the use of infrared sensors and a global high-resolution digital camera for environment sensing, all computation required for data acquisition, image processing, and closed-loop servo control was then performed on an FPGA chip as an external server. Battery-powered miniature mobile robots, Eyebots, were used as a test-bed for experiments. For realization, all the proposed algorithms were implemented and demonstrated via real-life video snapshots as shown on a PC monitor. These live images were captured from the on-board digital camera and then directly output to the monitor from a VGA interface of the FPGA platform. These together serve as the main contributions of this thesis, in both algorithm development and chip design verified by experiments.

The digital circuit designs in the chip were simulated using software specifically developed for FPGAs in order to show the timing waveforms of the chip. Experimental results demonstrated the technical feasibility of the proposed architecture for initialization and maintenance of a line formation of three robots. Effectiveness was verified through the percentage usage of the chip capacity and its power consumption. The prototype of this ubiquitous robotic system could be improved for promising applications in home robotics or for concrete finishing in construction automation.

Acknowledgements

This project has brought about some new contributions to ubiquitous computing and FPGA-based robotics. However, without the support of my principal supervisor Associate Professor Quang Ha, it would have been impossible to complete. I want to express my sincere appreciation of his kind efforts throughout my candidature. He has consistently provided me with advice, not only in reference to research but also to scholarship and other aspects. He was the person who saw the potential in this project. I also want to acknowledge his painstaking help with the writing of my research papers and of this thesis.

In addition, I want to thank Dr. Ngai Ming Kwok and my co-supervisor Dr. Sarath Kodagoda for their help with research publications in this project and suggestions for thesis from Miss. Arwen Wilson. Scholarship support from the Centre of Excellence for Autonomous Systems, funded by the ARC and the NSW Government, is also gratefully acknowledged.

Finally, I want to thank my wife and family for their encouragement, selfless love and support during my study in Australia.

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Symbols	Nomenclature	Unit
α	Ratio between perspective label width and virtual label	-
δ_h	Adjustable ratio of perspective width of leader and follower	-
δ_v	Adjustable ratio of perspective length of leader and follower	-
δ_x	Ratio of perspective width of leader and follower	-
δ_y	Ratio between perspective length of leader and follower	-
θ_0	Camera tilting angle	rad
a	Maximum number in RTL square rooting	-
b	Minimum number in RTL square rooting	-
d	Relative longitudinal distance between objects	m
d'	Relative perspective longitudinal distance between objects	m
f	Focal length of lens	m
g_n	Tolerance of green colour range in n thresholds	bit
h	Camera installation height	m
h_0	Object's height front lens	m
h_0'	Image height	m
m	Orientation of robot represented in 2D slope	-
m_2	Orientation of follower toward to point D in SBALA	-
m'	Perpendicular slope of m	-
m_R, m_G, m_B	RGB magnitude of pixel strength	-
n	Index of δ_v and δ_h	-
n_R , n_R , n_{R3}	Multiple of label width	-
p	Projected distance from image sensor to lens	m
s	Lateral relative distance between objects	m
s'	Lateral perspective relative distance between objects	m
t_n^*	Adjustable pixel strength in thresholds	bit
v_{speed}	Robots' normal speed	m/sec
x	Distance from object to lens	m
x_0	Following robot's width	m
x_1	Leading robot's width	m
x_0'	Following robot's perspective width	m
x_1'	Leading robot's perspective width	m

y	Projected distance from image sensor to lens	m
y_0	Following robot's length in longitudinal	m
y_1	Leading robot's length in longitudinal	m
y_0'	Following robot's perspective length	m
y_1'	Leading robot's perspective length	m
$D_{P(T)}$, $D_{P+1(T)}$	Recorded dynamic pixels data	bit
I(i,j)	Full colour pixel strength	bit
$M_{ln(T)}$	Moving detection marks on different image rows	-
R_h	Real lateral relative distance in ratio	-
$R_{n(i,j)}$, $G_{n(i,j)}$, $B_{n(i,j)}$	RGB pixel strength in n thresholds	bit
R_s	Real relative distance in ratio	-
R_{sat}, G_{sat}, B_{sat}	Saturated RGB pixel strength	bit
R_v	Real longitudinal distance in ratio	-
T_E	Execution time for moving detecting computing	sec
T_{OPC}	Motion detecting time of OPC	sec
T_P	Pixel data reading time	sec
$T_{reaction}$	Time of a Eyebot's reaction	sec
T_{reset}	Maximal reset interval of pursuing	sec
T_{Tr}	Motion detecting time in traditional computer	sec

Abbreviations

ADC	Analog to Digital Converter
AI	Artificial Intelligence
ALU	Arithmetic Logic Unit
AmI	Ambient Intelligence
ASICs	Application Specific Integrated Circuits
BIOS	Basic Input/ Output System
BNF	Braking Nervous Factor
CAD	Computer-Aided Design
CCDs	Charge Coupled Devices
CMOS	Complementary Metal Oxide Silicon
CPLDs	Complex Programmable Logic Devices
CPU	Central Processing Unit
DDR	Double Data Rate
DSP	Digital Signal Processor
FPGA	Field-Programmable Gate Array
GPS	Global Positioning System
GUI	Graphic User Interface
HDL	Hardware Description Language
IDE	Integrated Device Electronics
IEEE	Institute of Electrical and Electronics Engineers
IOE	I/O Element
IP	Intellectual Property
IT	Information Technology
KICA	Kernel Independent Component Analysis
LAB	Logic Array Block
LCD	Liquid Crystal Display
LC	Logic Cell
LE	Logic Element
LED	Light Emitting Diode
LSI	Large Scale Integrated
LUT	Look-up Table
OE	Output Enable
OS	Operating System
PC	General Purpose Computer

PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PID	Proportional-Integral-Derivative
PLL	Phase Locked Loop
PPIR	Perspective Projection Image Ratio
RAM	Random-Access Memory
RF	Radio Frequency
RFID	Radio Frequency Identification
ROI	Region of Interested
ROM	Read-Only Memory
RTL	Register-Transfer Level
RSS	Received Signal Strength
SBALA	Slope Based Arc-Line-Arc
SDRAM	Synchronous Dynamic Random Access Memory
SIFT	Scale-Invariant Feature
SOC	System on Chip
SRAM	Static RAM
SXGA	Super Extended Graphics Array
TFT-LCD	Thin Film Transistor-Liquid Crystal Display
TOF	Time-of-Flight
UA	User Agent
UC	Ubiquitous Computing
USB	Universal Serial Bus
VGA	Video Graphics Array
VHDL	Very High speed Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VR	Virtual Reality