

FPGA–Based Formation Control of Multiple Ubiquitous Indoor Robots

by
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CERTIFICATE OF AUTHORSHIP/ORIGINALITY

I certify that the work in this thesis has not been previously submitted for a degree nor has it been submitted as a part of the requirements for a degree except as fully acknowledged within the text.

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Ying-Hao Yu

Abstract

This thesis explores the feasibility of using Field-Programmable Gate Array (FPGA) technology for formation control of multiple indoor robots in an ubiquitous computing environment. It is anticipated that in the future, computers will become integrated with people's daily lives. By way of a hub of surrounding sensors, computers and embedded systems, indoor robots will receive commands from users and execute tasks such as home and office chores in a cooperative manner. Important requirements for such scenarios are power efficiency and computation reliability. The focuses of this project are on exploiting the use of the System-on-Programmable Chip technology and ambient intelligence in developing suitable control strategies for the deployment of multiple indoor robots moving in desired geometric patterns.

After surveying the current problems associated with computing systems and robotics, this research was determined to design an ubiquitous robotics system using Field-Programmable Gate Array (FPGA) technology, a serial of the Register-Transfer Level (RTL) and gate level hardware for image processing, and control implementation. Work was done to develop novel, FPGA-feasible algorithms for colour identification, object detection, motion tracking, inter-robot distance estimation, trajectory generation and formation turning. These algorithms were integrated on a single FPGA chip to improve energy efficiency and real-time reliability. With the use of infrared sensors and a global high-resolution digital camera for environment sensing, all computation required for data acquisition, image processing, and closed-loop servo control was then performed on an FPGA chip as an external server. Battery-powered miniature mobile robots, Eyebots, were used as a test-bed for experiments. For realization, all the proposed algorithms were implemented and demonstrated via real-life video snapshots as shown on a PC monitor. These live images were captured from the on-board digital camera and then directly output to the monitor from a VGA interface of the FPGA platform. These together serve as the main contributions of this thesis, in both algorithm development and chip design verified by experiments.

The digital circuit designs in the chip were simulated using software specifically developed for FPGAs in order to show the timing waveforms of the chip. Experimental results demonstrated the technical feasibility of the proposed architecture for initialization and maintenance of a line formation of three robots. Effectiveness was verified through the percentage usage of the chip capacity and its power consumption. The prototype of this ubiquitous robotic system could be improved for promising applications in home robotics or for concrete finishing in construction automation.

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Contents

1. INTRODUCTION	1
1.1 MOTIVATION	1
1.2 RESEARCH OBJECTIVES	2
1.3 RESEARCH METHODOLOGY AND JUSTIFICATION.....	4
1.4 MAIN CONTRIBUTIONS OF THE THESIS.....	6
1.4.1 <i>Energy efficiency</i>	7
1.4.2 <i>Real-time computing feasibility</i>	7
1.4.3 <i>Security reliability</i>	8
1.5 STRUCTURE OF THESIS.....	9
1.6 LIST OF PUBLICATIONS.....	10
1.6.1 <i>Award:</i>	10
1.6.2 <i>Journal papers accepted/published:</i>	10
1.6.3 <i>Peer-reviewed conference papers:</i>	10
2. LITERATURE REVIEWS AND PROPOSED METHODOLOGIES	12
2.1 UBIQUITOUS COMPUTING.....	12
2.1.1 <i>Origins</i>	13
2.1.2 <i>Ambient intelligence (Aml)</i>	18
2.1.3 <i>Ubiquitous robots</i>	19
2.2 CLASSIFICATION OF UBIQUITOUS ROBOTS.....	23
2.2.1 <i>Survey of control schemes</i>	23
2.2.2 <i>Survey of tracking media</i>	24
2.2.2.1 <i>Passive sensors</i>	24
2.2.2.2 <i>Active sensors</i>	25
2.3 BRIEF DISCUSSION OF FIELD-PROGRAMMABLE GATE ARRAY.....	27
2.3.1 <i>Overview</i>	27
2.3.2 <i>FPGA architecture</i>	28
2.3.2.1 <i>Configurable logic blocks</i>	29
2.3.2.2 <i>FPGA-interconnection</i>	33
2.3.2.3 <i>Configurable I/O block</i>	34
2.4 FPGAS IN ROBOTIC DESIGN.....	36
2.5 PROPOSED APPROACHES.....	37
3. SYSTEM ARCHITECTURE AND DEVICES.....	40
3.1 SYSTEM ARCHITECTURE.....	40

3.2	FPGA DEVELOPING PLATFORM.....	44
3.3	DIGITAL CAMERA MODULE	47
3.4	MOBILE ROBOT EYEBOT	49
3.5	WIRELESS REMOTE SIGNAL.....	52
3.6	FPGA DEVELOPMENT KITS.....	53
4.	COLOUR BASED REAL-TIME OBJECT TRACKING	57
4.1	INTRODUCTION	58
4.1.1	<i>Colour discrimination review</i>	<i>58</i>
4.1.2	<i>Motion detection review.....</i>	<i>62</i>
4.2	CAPTURING IMAGES FROM THE DIGITAL SENSING ARRAY.....	64
4.3	COLOUR DISCRIMINATION	71
4.4	DEMOSAICKING AND COLOUR DISCRIMINATION TESTS.....	75
4.5	LOCALIZATION	81
4.6	MOTION DETECTION	84
4.6.1	<i>One-page-comparison algorithm</i>	<i>84</i>
4.6.2	<i>Image comparison</i>	<i>87</i>
4.6.3	<i>Noise filter and time delay reduction</i>	<i>90</i>
4.7	MOTION DETECTION TEST	92
4.8	DISCUSSION.....	95
4.9	CONCLUSION.....	97
5.	RELATIVE DISTANCE ESTIMATION FOR ROBOTS CONTROL USING MONOCULAR DIGITAL CAMERA ...	99
5.1	INTRODUCTION	99
5.2	PPIR ALGORITHM.....	104
5.2.1	<i>Estimation of longitudinal distance</i>	<i>104</i>
5.2.2	<i>Estimation of lateral distance</i>	<i>109</i>
5.2.3	<i>Estimation of Euclidean distance.....</i>	<i>110</i>
5.3	EXPERIMENTAL RESULTS.....	111
5.3.1	<i>Static estimation</i>	<i>111</i>
5.3.2	<i>Dynamic estimation</i>	<i>113</i>
5.4	DISCUSSION.....	118
5.5	CONCLUSION.....	119
6.	SLOPE-BASED POINT PURSUING MANOEUVRES OF NONHOLONOMIC ROBOTS	121
6.1	INTRODUCTION	121
6.2	ROBOTIC PATH PLANNING WITH DUBINS' CAR.....	125
6.3	SLOPE-BASED ARC-LINE-ARC ALGORITHM.....	130
6.3.1	<i>SBALA algorithm.....</i>	<i>130</i>

6.3.2 <i>General cases of the SBALA algorithm</i>	132
6.4 SBALA IMPLEMENTATION ON AN FP GA.....	136
6.5 EXPERIMENTAL RESULTS AND DISCUSSION	142
6.6 CONCLUSION.....	147
7. LOW-POWER VISION-BASED APPROACH TO MULTI-ROBOT FORMATION CONTROL	149
7.1 INTRODUCTION	149
7.2 EXTENDED SBALA	153
7.3 FORMATION CONTROL WITH SBALA	155
7.4 IMPLEMENTATION AND EXPERIMENTS.....	160
7.5 DISCUSSION	163
7.6 CONCLUSION.....	169
8. SUMMARY AND FUTURE DEVELOPMENTS	170
8.1 INTRODUCTION	170
8.2 RESOURCE USAGE AND POWER DISSIPATION REVIEW.....	173
8.3 THESIS CONTRIBUTIONS OVERVIEW.....	175
8.3.1 <i>Energy efficiency and real-time feasibility</i>	175
8.3.2 <i>Security reliability</i>	176
8.3.3 <i>Inter-robot distance estimation using PPIR</i>	176
8.3.4 <i>Improvement in behaviour-based steering and formation</i>	176
8.3.5 <i>Real-time colour discrimination and motion object tracking</i>	177
8.4 FUTURE DEVELOPMENTS	177
8.5 CONCLUSION.....	179
BIBLIOGRAPHY	181
APPENDIX A. SP-URC-81 TV CODES LIST	195
APPENDIX B. MANCHESTER ENCODING	196
APPENDIX C. THE REGISTER-TRANSFER LEVEL (RT-LEVEL) ABSTRACTION	197
APPENDIX D. BRIEF STRUCTURES OF VHDL AND VERILOG LANGUAGE.....	198
D.1 <i>Structures of VHDL</i>	198
D.2 <i>Structures of Verilog</i>	205
APPENDIX E. STARTING A NEW PROJECT AND DESIGN WITH QUARTUS II.....	209
Appendix F. LIST OF ATTACHED VIDEOS	
.....	219

List of Figures

Fig. 2.1. The comparison between traditional and ubiquitous computing.....	15
Fig. 2.2. Vacuum cleaner Roomba	21
Fig. 2.3. Guarding robot MDARS	21
Fig. 2.4. Kiva carrying things	22
Fig. 2.5. Architecture of FPGAs	28
Fig. 2.6. Structure of a CLB block on Xilinx SPARTAN-3.....	30
Fig. 2.7. Architecture of Altera Cyclone II	32
Fig. 2.8. Configurable IOE on Cyclone II	35
Fig. 3.1. Multiple robot formation control scheme with chip design	43
Fig. 3.2. Whole system installation.....	43
Fig. 3.3. DE2-70 FPGA developing platform.....	46
Fig. 3.4. TRDB-D5M digital camera module	48
Fig. 3.5. The Eyebot.....	50
Fig. 3.6. Schematic of Eyebot.....	51
Fig. 3.7. Driving control scheme of Eyebot.....	52
Fig. 3.8. TV remote code “0” with modulation and Manchester encoding	56
Fig. 4.1. Bayer pattern arrangements	65
Fig. 4.2. Nearest-neighbour interpolation for pixel number 4 with different image directions	66
Fig. 4.3. Simplified linear demosaicking	70
Fig. 4.4. Snap shot of simulated timing waveform of colour interpolation	71
Fig. 4.5. Green colour discrimination with adjustable threshold	74
Fig. 4.6. Time sequence of green colour discrimination.....	74

Fig. 4.7. Demosaicking effects.....	77
Fig. 4.8. Colour discrimination with the self-shadow and diffuse reflection cases	79
Fig. 4.9. Colour discrimination with specular reflection and cast shadow tests.....	80
Fig. 4.10. Noise filter for the output marks of adjustable multi-threshold	81
Fig. 4.11. Eyebots with bull's-eye label.....	82
Fig. 4.12. Colour tracking scenarios for moving Eyebots as seen on a monitor	83
Fig. 4.13. Flow chart of OPC processes	86
Fig. 4.14. OPC timing diagrams	87
Fig. 4.15. Image comparison algorithm.....	89
Fig. 4.16. Motion detection.....	94
Fig. 4.17. Motion detection with mobile Eyebots.....	95
Fig. 5.1. Image projection in a global camera system with 2D labels in single direction view	102
Fig. 5.2. Deployed robots and their perspective images	108
Fig. 5.3. Extended PPIR estimation in the lateral direction.....	111
Fig. 5.4. Different scenarios in static testing.....	115
Fig. 5.5. PPIR estimation in dynamic testing.....	116
Fig. 5.6. Timing waveform of the PPIR algorithm	117
Fig. 6.1. Simple car model with velocity space in two-dimensions	126
Fig. 6.2. Examples of Dubins' turning	128
Fig. 6.3. A representation of SBALA on 2D plane	131
Fig. 6.4. Examples of the SBALA algorithm.....	134
Fig. 6.5. Point pursuing for different locations of point D	134
Fig. 6.6. Possible conditions of trajectory BD driving to point A	135
Fig. 6.7. Test scenario for the SBALA algorithm	138

Fig. 6.8. Point pursuing for line formation with two Eyebots	144
Fig. 6.9. Timing waveform of point A	147
Fig. 7.1. Improved SBALA algorithm	155
Fig. 7.2. Depiction of two robots in a line formation driving	156
Fig. 7.3. Two-robot formation control flowchart	160
Fig. 7.4. Installation of multiple robot formation test	161
Fig. 7.5. Two robots leader-following in line formation	167
Fig. 7.6. Three robots in line formation	168
Fig. B.1. Manchester encoding	196
Fig. C.1. Levels of abstraction with relative behaviour view	197
Fig. D.1. Circuit of a structural model example	204
Fig. E.1. New project wizard page 1 of 5	209
Fig. E.2. New project wizard page 2 of 5	210
Fig. E.3. New project wizard page 3 of 5	211
Fig. E.4. New project wizard page 4 of 5	211
Fig. E.5. Opening a project	212
Fig. E.6. List of new functions	213
Fig. E.7. Component libraries	214
Fig. E.8. A design example	214
Fig. E.9. Resource usage of circuit	215
Fig. E.10. Plain timing diagram	215
Fig. E.11. Node finder window	216
Fig. E.12. Simulated timing	217
Fig. E.13 Packed new symbol	218
Fig. E.14. Block circuit with conduit connection	218

List of Tables

Table 3.1. Cyclone II family features	44
Table 3.2. Different operating modes of TRDB-D5M digital camera module	48
Table 4.1. Linear Demosaicking	68
Table 4.2. OPC design resource usage	91
Table 4.3. Thermal power dissipation of motion detection	93
Table 5.1. PPIR test results with different degrees of n	113
Table 6.1. Three motion primitives	129
Table 6.2. Shortest turning rules for the first arc toward point D	135
Table 6.3. Turning rules for the second arc toward to point A	136
Table 7.1. Formation chip designs resource usage	164
Table 7.2. Power Dissipation of Three Robot Formation Design	166
Table 8.1. Total FPGA resource usage	173
Table 8.2. Power consumptions between motion detection and other designs	174
Table A.1. SP-URC-81 TV codes list	195

List of Symbols

Symbols	Nomenclature	Unit
α	Ratio between perspective label width and virtual label	-
δ_h	Adjustable ratio of perspective width of leader and follower	-
δ_v	Adjustable ratio of perspective length of leader and follower	-
δ_x	Ratio of perspective width of leader and follower	-
δ_y	Ratio between perspective length of leader and follower	-
θ_0	Camera tilting angle	rad
a	Maximum number in RTL square rooting	-
b	Minimum number in RTL square rooting	-
d	Relative longitudinal distance between objects	m
d'	Relative perspective longitudinal distance between objects	m
f	Focal length of lens	m
g_n	Tolerance of green colour range in n thresholds	bit
h	Camera installation height	m
h_0	Object's height front lens	m
h_0'	Image height	m
m	Orientation of robot represented in 2D slope	-
m_2	Orientation of follower toward to point D in SBALA	-
m'	Perpendicular slope of m	-
m_R, m_G, m_B	RGB magnitude of pixel strength	-
n	Index of δ_v and δ_h	-
n_R, n_{R2}, n_{R3}	Multiple of label width	-
p	Projected distance from image sensor to lens	m
s	Lateral relative distance between objects	m
s'	Lateral perspective relative distance between objects	m
t_n^*	Adjustable pixel strength in thresholds	bit
v_{speed}	Robots' normal speed	m/sec
x	Distance from object to lens	m
x_0	Following robot's width	m
x_1	Leading robot's width	m
x_0'	Following robot's perspective width	m
x_1'	Leading robot's perspective width	m

y	Projected distance from image sensor to lens	m
y_0	Following robot's length in longitudinal	m
y_1	Leading robot's length in longitudinal	m
y_0'	Following robot's perspective length	m
y_1'	Leading robot's perspective length	m
$D_{P(T)},$ $D_{P+I(T)}$	Recorded dynamic pixels data	bit
$I(i,j)$	Full colour pixel strength	bit
$M_{ln(T)}$	Moving detection marks on different image rows	-
R_h	Real lateral relative distance in ratio	-
$R_{n(i,j)},$ $G_{n(i,j)}, B_{n(i,j)}$	RGB pixel strength in n thresholds	bit
R_s	Real relative distance in ratio	-
$R_{sat}, G_{sat},$ B_{sat}	Saturated RGB pixel strength	bit
R_v	Real longitudinal distance in ratio	-
T_E	Execution time for moving detecting computing	sec
T_{OPC}	Motion detecting time of OPC	sec
T_P	Pixel data reading time	sec
$T_{reaction}$	Time of a Eyebot's reaction	sec
T_{reset}	Maximal reset interval of pursuing	sec
T_{Tr}	Motion detecting time in traditional computer	sec

Abbreviations

ADC	Analog to Digital Converter
AI	Artificial Intelligence
ALU	Arithmetic Logic Unit
AmI	Ambient Intelligence
ASICs	Application Specific Integrated Circuits
BIOS	Basic Input/ Output System
BNF	Braking Nervous Factor
CAD	Computer-Aided Design
CCDs	Charge Coupled Devices
CMOS	Complementary Metal Oxide Silicon
CPLDs	Complex Programmable Logic Devices
CPU	Central Processing Unit
DDR	Double Data Rate
DSP	Digital Signal Processor
FPGA	Field-Programmable Gate Array
GPS	Global Positioning System
GUI	Graphic User Interface
HDL	Hardware Description Language
IDE	Integrated Device Electronics
IEEE	Institute of Electrical and Electronics Engineers
IOE	I/O Element
IP	Intellectual Property
IT	Information Technology
KICA	Kernel Independent Component Analysis
LAB	Logic Array Block
LCD	Liquid Crystal Display
LC	Logic Cell
LE	Logic Element
LED	Light Emitting Diode
LSI	Large Scale Integrated
LUT	Look-up Table
OE	Output Enable
OS	Operating System
PC	General Purpose Computer

PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PID	Proportional-Integral-Derivative
PLL	Phase Locked Loop
PPIR	Perspective Projection Image Ratio
RAM	Random-Access Memory
RF	Radio Frequency
RFID	Radio Frequency Identification
ROI	Region of Interested
ROM	Read-Only Memory
RTL	Register-Transfer Level
RSS	Received Signal Strength
SBALA	Slope Based Arc-Line-Arc
SDRAM	Synchronous Dynamic Random Access Memory
SIFT	Scale-Invariant Feature
SOC	System on Chip
SRAM	Static RAM
SXGA	Super Extended Graphics Array
TFT-LCD	Thin Film Transistor-Liquid Crystal Display
TOF	Time-of-Flight
UA	User Agent
UC	Ubiquitous Computing
USB	Universal Serial Bus
VGA	Video Graphics Array
VHDL	Very High speed Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
VR	Virtual Reality