Heavy Load Simulation Model of Flyback Switching DC-DC Converters and Its Application for Reliability Improvement

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***Abstract*—This paper presents the simulation model of flyback switching DC-DC converters operating in heavy load modes, and the application of the model in the converter design for improving the system reliability. To derive the simulation model, different operational modes and atomic circuit blocks (ACB) are established first. Then, the state-machine of the system is studied. Finally, the transfer function of each ACB is determined, and according to the relationship among the ACBs, the complete simulation model is built, which can be used for transient analysis during starting, the operation in the under-voltage mode or over-current mode. Furthermore, the heavy load simulation model is applied to calculate the maximum steady-state power loss of the output diode, one of the key factors for thermal analysis which is crucial for the system reliability. The effect of time delay is also considered. By modifying the parameters of a physical flyback converter according to the simulation results, the converter reliability is significantly improved. The theoretical analysis is verified by experimental results.**

Keywords-flyback switching DC-DC converter; simulation model; heavy load; reliability; state machine; atomic circuit block; power loss; time delay

I. INTRODUCTION

Flyback switching converters are commonly used as small power converters because of their simple structure. A great amount of work has been done on the operational principle, design methodology, modeling, and control of the flyback converter [1-4]. However, in the development of new converters, the analysis of system characteristic in heavy load mode is rarely conducted due to the lack of appropriate models. Although the converters have good performances such as the steady-state performance and output ripple coefficient under the rated load, they may have serious problems under a heavy load, which can damage the converters permanently. Therefore, in order to evaluate and improve the reliability of the converter, it is essential to develop an effective and accurate simulation model for characteristic analysis in the heavy load mode in the design stage.

There are three existing methods for building the simulation models: the state-space averaging technique and linearization [5], linear circuit technique [6], and nonlinear design technique [7]. In a flyback switching converter, the transfer functions of some blocks are highly nonlinear, because of the optical parts and pulse width modulated (PWM) integrated circuits (ICs), etc. The accuracy of simulation by the first two methods relies heavily on the modeling process of the optical parts and PWM ICs. In order to increase the simulation accuracy, the third method was employed. However, it is also of high complexity. To overcome these difficulties, a new approach to simulating the flyback switching DC-DC converter operating in heavy load mode based on the state-machine is presented [8]. It is a mixed circuit model based on the SIMULINK of MATLAB, which contains both linear and non-linear circuit blocks. The model is easy to be understood and its parameters can be easily modified. The model can be used for the transient analysis during the system starting, as well as when the system operates in the under-voltage mode or over-current mode, even short-circuited output mode.

Besides the under-voltage and over-current protections, the converter reliability depends upon the heat generation and dissipation. Obviously, the effective and proper determination of power loss is crucial for designing the converter with a high performance/cost ratio and high reliability. However, due to the complex mechanism, thermal analysis in the converter mainly relies on experience and/or empirical formulae. In this paper, the power loss of the output diode is investigated by the proposed heavy load simulation model, including the calculation models of the average steady-state loss under different operational modes (voltage control, under-voltage, and over-current modes), the models of the maximum steady-state loss, and the relation of diode power loss versus the input voltage and output voltage. The effect of time delay is also taken into account. These models are applied to calculate the output diode loss of an existing flyback converter.

II. A FLYBACK SWITCHING DC-DC CONVERTER

Fig. 1 shows the typical topology of a flyback switching DC-DC converter with a single output port, where dashed lines connect control block to the main circuit.

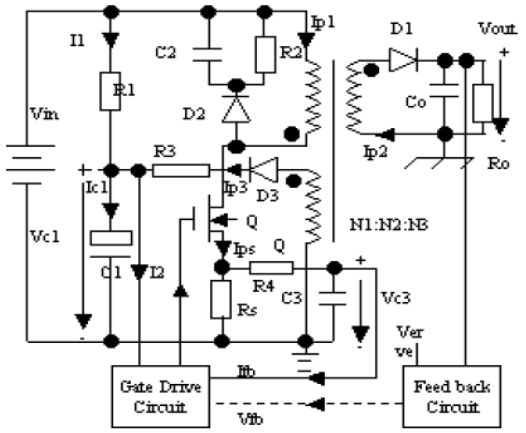

Figure 1. Typical topology of a flyback converter

A. Assumption and Simplification

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B. Operational Modes with Heavy Load

Besides the main input-output circuit and electromagnetic interference (EMI) filter, there are three main blocks including the output voltage control block (VCB), the over current protection (OCP) block, and the under voltage protection (UVP) block. As the load increases, the three blocks will be activated in order. When the load is increased to a certain value, and the output voltage becomes lower than the rated value, the VCB block stops and the OCP block is activated. When the load continues to be increased to a large value or even short circuit the output port, because the output voltage of winding N3 is too small to support the power consumption for the gate drive IC, such as UC3842, both the OCP and UVP blocks are activated. Both the OCP and UVP modes belong to the heavy load mode, and will be studied in detail in this paper. Table I lists the on/off states of each block corresponding to the operational modes. The equivalent circuits for the OCP mode and UVP mode are shown in Figs.2 (a) and (b), respectively.

As there is a huge capacitor across the output port, the process of system start-up has the same characteristic as that of the system operating in the OCP mode. As the transformer is easy to saturate, many converters are damaged during the OCP or UVP mode, mostly in the latter mode.

TABLE I. ON/OFF STATE OF THREE MAIN BLOCKS

Block / Operational mode	VCB Block	OCP Block	UVP Block
VCB Mode	On	Off	Off
OCP Mode	Off	On	Off
UVP Mode	Off	On	On

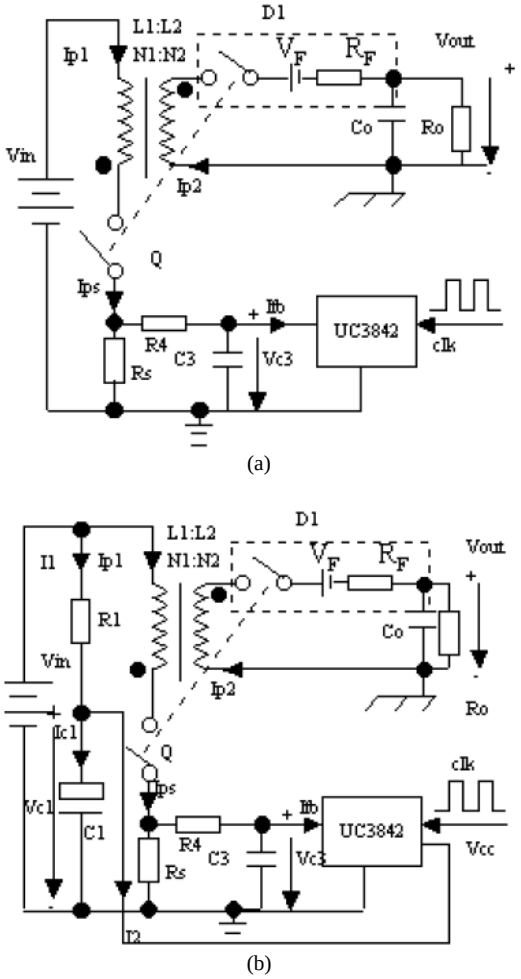


Figure 2. Equivalent circuit: (a) in OCP mode, (b) in UVP mode.

C. Atomic Circuit Blocks

In order to build the simulation model, it is necessary to find out the relations between different components in the system in advance. However, as there are so many components in the converter, it is very difficult for the simulation model to be set up in a simple step. The system may be disassembled to several atomic circuit blocks (ACBs), defined as the possible minimum unit with a complete function, and then the relations among these blocks are built for simulation of the complete system. The components in the same ACB work or stop simultaneously, and perform a task together. According to this principle and the above assumptions, several ACBs of the system operating in heavy load can be obtained, as shown in Table II. The main components of the ACBs are also listed.

TABLE II. ACBS AND MAIN COMPONENTS

No.	ACBs	Components
1	VC1 Charger	R1, C1, R_{ICON}, R_{ICOFF}
2	UVP	U_{START}, U_{STOP}
3	RC FILTER	R4, Rs, C3
4	OCP	1V Comparator, T_{DELAY}
5	RC OUT	C_o, R_o
6	Transformer	Lm1, Lm2, R_{INF}
7	Equivalent Source	D1: V_F, R_F
8	Synchronizer	CLK

D. Analysis of IC-UC3842 in Heavy Load

The functional block diagram of UC3842 is illustrated in Fig. 3 [4]. The voltage of VCC (V_{C1}) for starting is U_{START} = 16 V, and it will be turned off when the voltage decreases to U_{STOP} = 10V. There are two methods which can cause the system into the OCP mode by using either the COMP (1), or the ISENSE (6). Under heavy load, according to Table I, because the output voltage is lower than the rated value and the voltage of COMP (1) is above 4.4 V, only the 1 V voltage of ISENSE (6) can cause the system into the OCP mode.

Based on the energy conservation, UC3842 in the ON state is modeled by a resistance of R_{ICON} = 1360 Ω, and in the OFF state by a very large resistance, $R_{ICOFF,}$ e.g. 2 MΩ. The typical rise time and fall time of the output section of UC3842, according to the manual, are both 50 ns, maximum 150 ns. In order to maximize the system safety when operating in the heavy load mode, the rise time, T_{RISE} is chosen as 50 ns, and the fall time, T_{FALL} is chosen as 150 ns. The electric circuits of these processes can be easily realized.

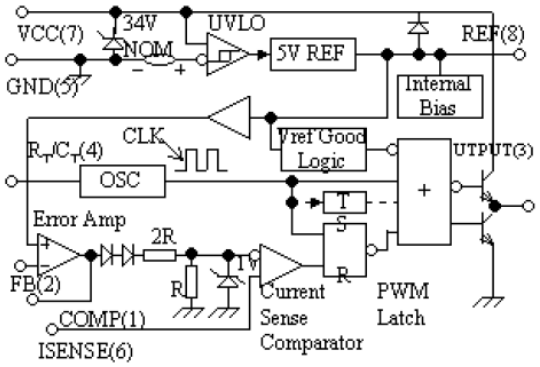


Figure 3. Functional block diagram of UC3842

III. SYSTEM STATE-MACHINE

The state-machine can decide the switching mode in which the system operates. When the output load increases gradually the flyback switching converter can go into different modes and the minimal energy which the transformer can hold is from zero, i.e. the discontinuous current model (DCM), to a certain non-zero value, i.e. the continuous current model (CCM). According to the working principle of this converter and UC3842, the system level state-machine can be obtained and the states of OCP, UVP and PWM are shown in Table III.

As to the current mode (CM), its state depends upon Ip2 only while PWM=0. According to the working principle of the converter, the following function and the state-machine of CM can be obtained.

$$CM^{n+1} = (I_{P2} < 0) * \overline{PWM} + CM^{n} * PWM \qquad (1)$$

where CM=1 corresponds to the DCM, and CM=0 corresponds to the CCM. This is also illustrated in Fig. 4. Similarly, the corresponding logical expression and electric circuit realization of the OCP, UVP and PWM state-machines can be obtained.

TABLE III. STATE-MACHINE OF SYSTEM LEVEL (UVP, OCP, PWM)

(a) UVP^{n+1} state

UVP^n / V_{CC}	0	1
V_{CC}<10	0	0
$10 \le V_{cc} < 16$	0	1
$V_{cc} \ge 16$	1	1

(b) OCP^{n+1} state

OCP^n / UVP^n,Vc3	0	1
00	0	0
01	0	0
11	$\begin{cases} 1 : t \ge T_{delay} \\ 0 : t < Tdelay \end{cases}$	1
10	0	$\begin{cases} 1 : t \ne CLK \uparrow \\ 0 : t = CLK \uparrow \end{cases}$

(c) PWM^{n+1} state

PWM^n / UVP^n,OCP^n	0	1
00	0	$\begin{cases} 1 : t < T_{FALL} \\ 0 : t \ge T_{FLL} \end{cases}$
01	0	$\begin{cases} 1 : t < T_{FALL} \\ 0 : t \ge T_{FLL} \end{cases}$
11	0	$\begin{cases} 1 : t < T_{FALL} \\ 0 : t \ge T_{FLL} \end{cases}$
10	$\begin{cases} 1 : t \ge T_{RISE} \\ 0 : t < T_{RISE} \end{cases}$	1

Note: n stands for the current state, and n+1 stands for the next state.

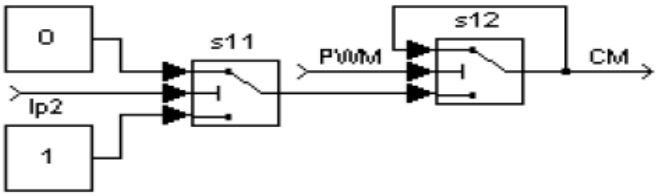


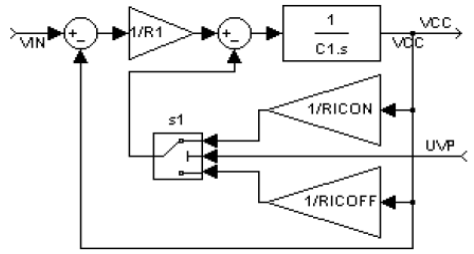
Figure 4. Electric circuit realization of the CM state-machine

IV. ACB SIMULATION MODEL

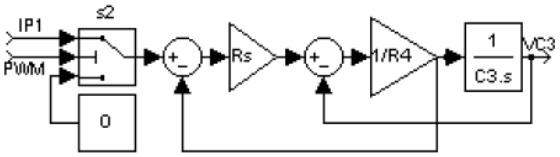
Table IV lists several ACBs and their corresponding input, output and state signals. According to Fig. 2, Table II, Table IV and the working principle of the flyback converter, the SIMULINK/MATALB based simulation model of each ACB can be obtained, as illustrated in Fig. 5.

TABLE IV. ACBS AND CORRESPONDING OUTPUT SIGNAL, INPUT SIGNAL, AND STATE SIGNAL

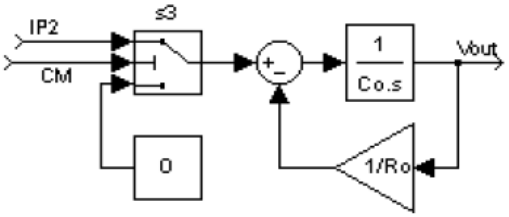
ACB	Input signal	Output signal	State signal
VCC charger	V_{IN}	V_{C1}	UVP
RC filter	I_{P1}	V_{C3}	PWM
RC OUT	I_{P2}	V_{OUT}	PWM, CM
Transformer	V_{C1}, V_D, V_{OUT}	I_{P1}, I_{P2}	PWM, CM



(a)



(b)



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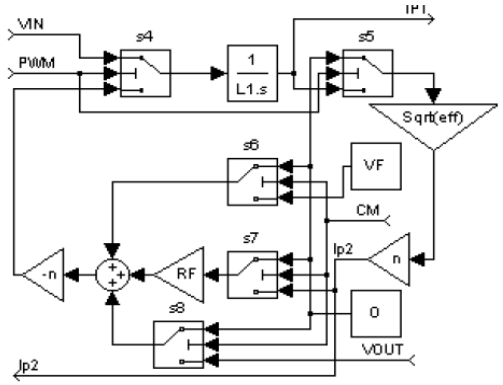


(d)

Figure 5. Electric circuit realization of simulation models of ACBs: (a) VCC charger, (b) RC filter, (c) RC OUT, and (d) transformer

V. COMPLETE SIMULATION MODEL AND IMPLEMENTATION

Based on the previous analysis, a complete simulation model of the flyback converter can be achieved, as shown in Fig. 6.

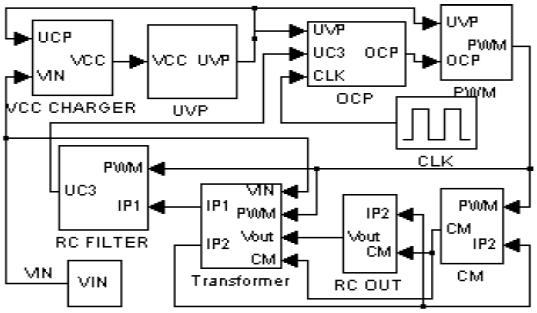
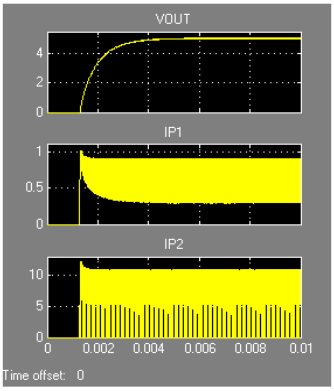


Figure 6. Complete simulation model of the converter

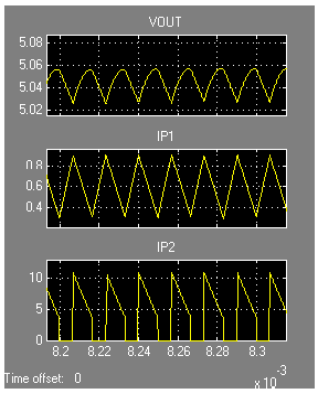
The simulation model is applied to analyze an existing flyback DC-DC converter, which has good performance in the rated load, but was once damaged in the experiment due to a short circuit output at an input voltage of 370 V DC. The major data of the converter include: input voltage: 102-370 VDC; nominal output voltage: 5 VDC; rated output current: 3.6 A; switching frequency: 60 kHz; and maximum duty ratio: 0.414.

The transformer has a primary winding inductance of 1.186 mH, and the numbers of turns of three windings are 96:8:17. Other parameters include: R1=160 KΩ/1W, C1=47 μF/35V, R_S=1.3 Ω, R4=1.2 KΩ, C3=1.0 nF, MOSFET: SSS6N60A, R3=0 Ω, D1: MUR1620, D2: UF4006, D3: 1N4148, R2=100 KΩ/1W, C2=3.3 nF/1000V, and Co=1000 μF/25V.

Fig. 7(a) illustrates the simulated operation process of the converter with the rated load while V_{IN}=102 VDC, and V_F and R_F are chosen as 0.7 V and 0.05 Ω. Fig. 7(b) shows the enlarged steady state. It can be seen that Ip1 has an obvious overshoot at starting, which may cause the transformer into the state of saturation and may damage the converter.



(a) Complete process



(b) Steady state

Figure 7. Simulated results at the rated load (existing converter)

According to the transformer PC40 (Bs=500 mT; t=100 °C) and this converter's characteristic, the rated operating point is 290 mT at Ip1=0.9 A. The margin to the maximum Bs is 210 mT, which corresponds to 0.65 A of Ip1, and hence the maximum Ip1 allowed is 1.55 A. In the rated condition, the maximum current during start-up is 1.2 A, which is less than 1.55 A, so that the converter can work safely. This is consistent to this actual condition.

Under heavy load, e.g. V_{IN}=370 VDC, Ro=0.001 Ω, the operating process of the converter is analyzed by the proposed model, as shown in Fig. 8, where V_F=0.7 V, R_F=0.05 Ω, R1=1600 Ω, R_{ICON}=30 Ω. From the simulation results, one can get V_{OUT}≈0 V, Ip1max=2.16 A, Ip1min=1.96 A, Ip2max=25.92 A and Ip2min=23.52 A. The primary current Ip1 goes over the allowed value, and the converter could be damaged instantly. This is consistent to the actual case that the converter was once damaged in the experiment of short circuit output.

The converter is re-designed by adding the UVP and OCP circuits. Fig. 9 illustrates the simulated results of the new converter under heavy load (V_{IN}=370 VDC, Ro=0.00 1Ω). New parameters include: R_S=1.15 Ω, R4=100 Ω, C3=470 pF. The new simulation results are Ip1max=0.98 A, Ip1min=0.8 A, Ip2max=11.76 A, Ip2min=9.6 A. As Ip1max is less than the allowed value, it will not cause the transformer into the saturation state.

Fig. 10 plots the simulation results of the new converter at the rated condition (V_{IN}=102 VDC, Ro=1.39 Ω), which is similar to that of the old converter (Fig. 7). The only difference between them is that there is no overshoot in Fig. 10, implying that the new converter also has higher safety than the existing one during the process of start up.

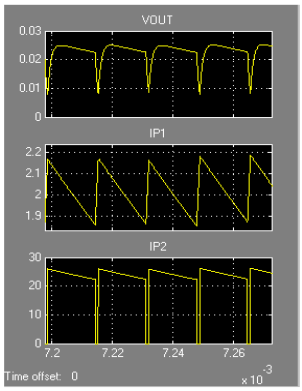


Figure 8. Process under short circuit output (existing converter)

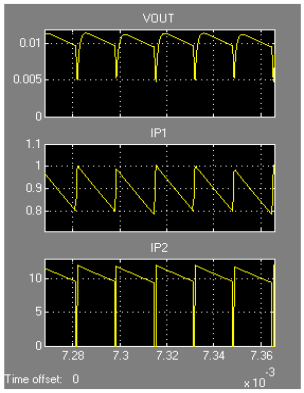
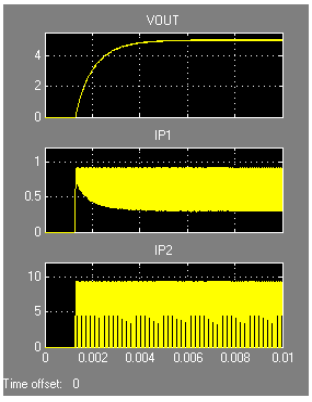
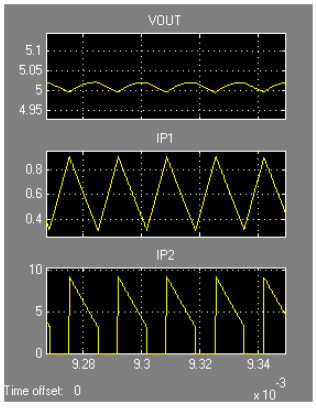


Figure 9. Process under short circuit output (new converter)



(a) Complete process



(b) Steady state

Figure 10. Simulated results at the rated load (new converter)

VI. Power Loss of the Output Diode

The heavy load simulation model can also be applied to investigate the steady-state power loss of the output diode [9], one of key factors for thermal analysis of the converter and improvement of the system reliability. Fig. 11 shows the equivalent electrical circuits of the converter under heavy load modes, derived from Fig. 2. The diode resistance is ignored, as well as the effect of time delay caused by various components and the RC filter circuit (R4 and C3). For the analysis of the diode loss in the normal operational mode, an equivalent electrical circuit is shown in Fig. 12. The parameters of the secondary winding N2 are referred to the primary side by

$$V_F' = \frac{N1}{N2}V_F, \quad C_o' = \left(\frac{N2}{N1}\right)^2 C_o, \quad V_{out}' = \frac{N1}{N2}V_{out} \tag{2}$$

where N1 and N2 are the numbers of turns of the primary and the secondary windings of the transformer, respectively.

A. Output Diode Loss in the VCB mode

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When the converter operates in the VCB mode, the output voltage is a constant. According to [1] and Fig. 12, the following equation can be obtained:

$$dIp1 = \frac{Vin}{L1}DT = \frac{V_{out}' + V_F'}{L1}(1-D)T \tag{3}$$

where L1 is the primary winding inductance of the transformer, D the duty ratio and T the time period of a duty cycle. From (3), the duty ratio can be calculated by

$$D = \frac{V_{out}' + V_F'}{V_{out}' + V_F' + Vin} \approx \frac{V_{out}'}{V_{out}' + Vin} \tag{4}$$

The duty ratio of PWM depends on the equivalent input and output voltages only and it is not affected by the load. According to the output equation during one period, i.e. $dV_{out}' = 0$, one can get:

$$\frac{i_{p1} - i_o'}{C_o'}(1-D)T = \frac{i_o'}{C_o'} * DT \tag{5}$$

$$i_{p1} = i_o' / (1-D) \tag{6}$$

$$P_{DT} = V_F' * i_{p1} * (1-D) = V_F' * i_o' \tag{7}$$

The steady-state power loss of output diode under the normal operational mode, P_{DT}, increases linearly with respect to the load.

As the converter may work at different voltages, the rated output power is designed as the maximum average power that the converter can deliver at any voltage within the whole range

(*Vmin* to *Vmax*). The rated output power, *Pe*, corresponds to the highest output power when *Vin*=*Vmin*, and the maximum output power of the converter, *Pem*, happens when *Vin*=*Vmax*, and they can be calculated by

$$\begin{cases} P_e = V_{\min} D_{\max} (I_{p1\max} - \Delta I_{p1e}) \\ P_{em} = V_{\max} D_{\min} (I_{p1\max} - \Delta I_{p1\max}) \end{cases} \quad (8)$$

where *Ip1max*=1/*Rs* is the allowed maximum primary current, and

$$\begin{cases} \Delta I_{p1\max} = \dfrac{V_{\max}}{2L1} D_{\min} T \\ \Delta I_{p1e} = \dfrac{V_{\min}}{2L1} D_{\max} T \\ D_{\min} = \dfrac{V'_{out} + V'_F}{V'_{out} + V'_F + V\max} \\ D_{\max} = \dfrac{V'_{out} + V'_F}{V'_{out} + V'_F + V\min} \end{cases}$$

Obviously, the converter output power increases when the input voltage increase, and *Pem* > *Pe*. To maximize the safety of the system under the VCB block, the calculation of the maximum power loss is conducted at the highest input voltage. According to (7), the maximum average steady-state power loss of the output diode in the VCB mode can be computed by

$$P_{DTM} = \frac{V'_F}{V'_{out} + V'_F} P_{em} \quad (9)$$

B. Output Diode Loss in the OCP mode

The OCP mode can be considered as a normal operational mode (VCB) with Ip1=Ip1max and Vout ≠ constant. From section VI(A), it has been concluded that for a certain output voltage, the maximum average steady-state power loss of the output diode under the VCB mode happens with the highest input voltage. Therefore, the relation of the diode loss against output voltage should be understood first. According to Fig. 11, the following equations can be obtained:

$$\begin{cases} P_o = V_{in} D (I_{p1\max} - \Delta I_{p1}) \\ \Delta I_{p1} = \dfrac{V_{in}}{2L1} DT \end{cases} \quad (10)$$

Then, the output diode loss in the OCP mode can be computed by

$$\begin{aligned} P_{DC} &= \frac{V'_F}{V'_{out} + V'_F} P_o \\ &= \frac{V'_F V_{in}}{V'_{out} + V'_F} D (I_{p1\max} - \frac{V_{in}}{2L1} DT) \end{aligned} \quad (11)$$

From (4), (10) and (11), it can be seen that for a certain input voltage, when the output voltage decreases, both the duty ratio of PWM and output power decreases as well, but the output diode loss increases. When the output is short-circuited, the equivalent output current is close to Ip1max. In the OCP mode, when the system is with the highest input voltage and short-circuited output, the power loss of the output diode reaches the maximum value as

$$P_{DCM} = V'_F I_{p1\max} \quad (12)$$

Comparing (9) and (12) reveals:

$$P_{DCM} >> P_{DTM}$$

C. Output Diode Loss in the UVP mode

The UVP mode is activated when the output voltage of the converter is lower than the rated value, so that the output voltage of the assistant winding N3 is too small to support the power consumption for the gate drive IC, such as UC3842. The UVP operation is an oscillation process with a large time period, as reported in [4]. Fig. 13 shows the simulated waveform of Vc1, where Ts is the oscillation period, T_C the rise time, and T_D the fall time. By assuming the highest operational voltage of the PWM control hysteresis loop is V_H, and the lowest voltage is V_L, referring to Fig. 11 and considering Vin >> Vc1, T_C can be calculated by

$$T_C = \frac{(V_H - V_L) R_1 C_1}{Vin} \quad (13)$$

Since R1 is much larger than the equivalent resistance of UC3842, R_{IC}, the fall time T_D and the oscillating duty ratio D_s can be obtained by

$$T_D = R_{IC} C_1 \ln \frac{V_H}{V_L} \quad (14)$$

$$D_s = \frac{T_D}{T_s} = \frac{T_D}{T_D + T_C} \quad (15)$$

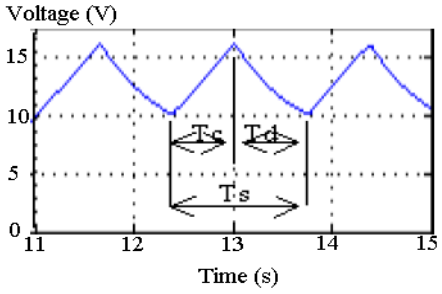

Figure 11. Simulated waveform of Vc1 under the UVP mode

According to (10), (11) and (15), the average steady-state power loss of the output diode in the UVP mode is

$$\begin{aligned} P_{DV} &= P_{DC} D_s \\ &= \frac{V'_F V_{in}}{V'_{out} + V'_F + V_{in}} (I_{p1\max} - \frac{V_{in}}{2L1} DT) D_s \end{aligned} \quad (16)$$

From (13) – (16), it can be found that when the input voltage goes up, the system oscillating frequency and the oscillating duty ratio increase, as well as the power loss P_{DV}. When the input voltage reaches the allowed maximum value, the diode loss will also reach the maximum for a given output voltage, and if at the moment the output is short-circuited (the output voltage is zero), the diode loss is the highest by

$$P_{DVM} \approx V_F' I_{p1\max} D_{sm}$$
$$D_{sm} = \frac{T_D}{(V_H - V_L)R1C1/V\max + T_D} \quad (17)$$

Comparing P_{DV} and P_{DC} reveals that it is very important to choose appropriate operational point of UVP and value of R1 for the high system efficiency. This can be done by the above models.

D. Calculation of the Output Diode Loss in a Practical Flyback Converter

The proposed models are applied to calculate the power loss of the output diode of the existing flyback switching DC-DC converter. According to (8) and (9), the relations of the duty ratio of PWM and the maximum steady-state power loss of output diode against the input voltage in the VCB mode can be obtained, as shown in Fig. 14. When Vin=370 V, the power loss reaches the highest value as P_{DTM}=3.5 W.

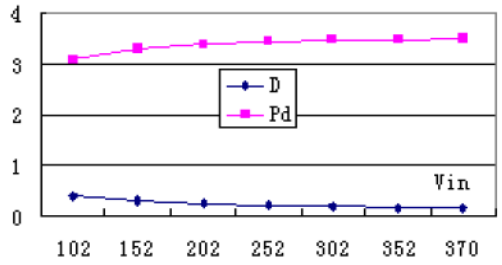

Figure 12. Duty ratio and diode loss versus input voltage under VCB mode

According to (10) – (12), in the OCP mode, the relations of the maximum steady-state power loss of output diode against the input and output voltages are acquired and plotted in Fig. 15. The diode loss will increase if the input voltage increases or the output voltage decreases. When Vin=370 V, and Vout=0.05 V (almost short-circuited), the diode loss reaches the highest value P_{DCM}=6.87 W.

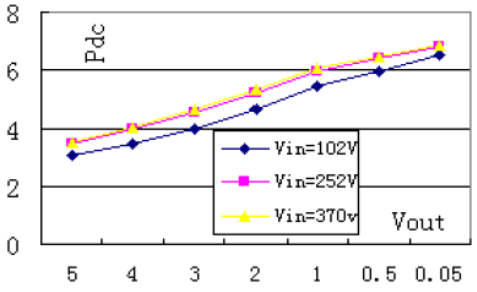

Figure 13. Diode loss versus input and output voltages under OCP mode

From (13) – (17), it can be found that when the converter switches from the OCP mode to the UVP mode, the output voltage at the corresponding operational point is Vout=4.0 V. At this operational point, the diode loss is studied with various input voltages, as illustrated in Fig. 16. Fig. 17 shows the diode loss against input voltage with the short-circuited output (Vout=0.05 V).

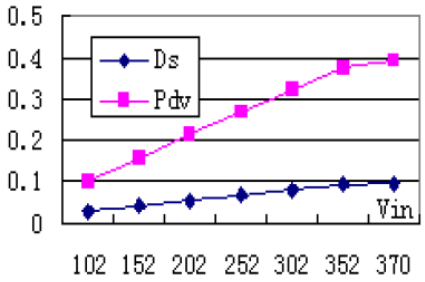

Figure 14. Curves of diode loss versus input voltage at the switching point from the OCP mode to UVP mode (Vout=4.0 V)

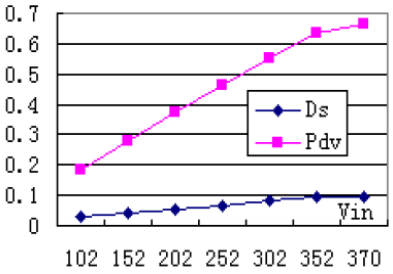

Figure 15. Curves of diode loss versus input voltage in the UVP mode with short-circuited output (Vout=0.05 V)

At the switching point (Vout=4 V) from the OCP mode to UVP mode, the maximum diode loss is found from Fig. 15 to be: P_{DCM}=4.0 W. Because P_{DTM}=3.5 W (Fig. 14) and P_{DVM}=0.66 W (Fig. 17), the maximum diode losses at different operational modes satisfy: $P_{DCM} \geq P_{DTM} \geq P_{DVM}$.

E. Output Diode Loss Considering Time Delay

Because of the high operational frequency, the time delay caused by converter components, such as the PWM control circuit and RC filter (R4 and C3) will affect the diode loss. This phenomenon is studied in this paper by the proposed Matlab/Simulink-based heavy load simulation model. The simulated results are shown in Figs. 18 –20. The time delays of UC3842 are 300 ns for protection, 150 ns for switching off, and 50 for switching on, respectively.

Fig. 18 shows the simulated waveform of Vout, Ip1 and PWM, which agree well with the previous design. Figs. 19 and 20 illustrate the relations of the steady-state diode loss versus input voltage in the VCB and the OCP modes, respectively. Fig. 14 and Fig. 19 have similar curves, but the maximum diode loss when considering time delay (4.0 W) is larger than that without time delay (3.5 W). The curves of Fig. 15 and Fig. 20 are also similar, but the time delay causes higher diode loss (4.44 W vs. 4.0 W), when Vout=4.0 V. Therefore, thermal

design should take the maximum diode loss of in the OCP mode considering the effect of time delay. It is also noted that by choosing the appropriate switching point (Fig. 20), the diode loss can be reduced.

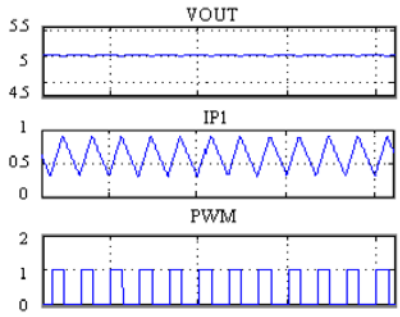

Figure 16. Simulated waveforms of Vout, Ip1 and PWM (Vin=102 V, switching frequency: 60 KHz)

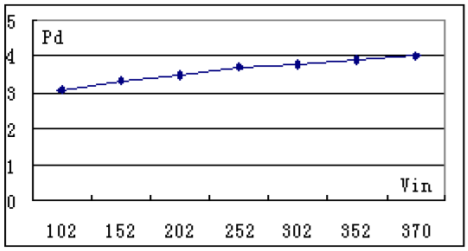

Figure 17. Curve of diode loss against input voltage in the VCB mode (Vout=5 V)

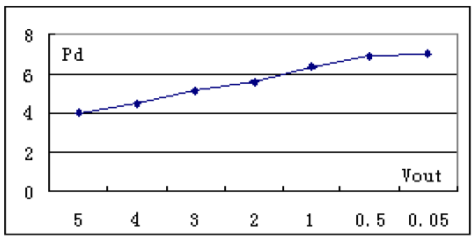

Figure 18. Curve of diode loss against output voltage in the OCP mode (Vin=370 V)

VII. CONLUSION

This paper has systematically presented a procedure to simulate flyback switching DC-DC converters under heavy loads based on the atomic circuit blocks and state-machine. An existing converter is analyzed by the presented simulation model and is found to be likely damaged under a heavy load. The converter is redesigned by adding the under-voltage and over-current protections and it can work safely in both steady state and heavy load modes, so that the converter reliability is significantly improved. This is consistent with the practical cases.

The proposed heavy load simulation model can also been applied for the calculation of power loss, e.g. the maximum steady-state power loss of the output diode under different operational modes. For thermal design, the output diode loss should take the larger of P_{DTM} and P_{DCM}. In the under-voltage mode, the system has large time period and low duty ratio, so that the diode loss P_{DVM} is much smaller than P_{DCM} and can be neglected. Furthermore, the effect of time delay is studied and is found that the diode loss is larger than or equal to that without time delay. The thermal design should be conducted based on the power losses considering time delay.

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