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Quantum electrical characteristics of nanocapacitors

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Abstract—Current integrated circuit miniaturization will soon require device sizes at atomic scale. Recent work has proposed many Coulomb blockade, and tunneling devices as active devices. However, among passive components, capacitors are extremely critical circuit elements in all electronic circuits with wide range applications. In this work, we present the operational criteria that will govern the feasibility of nanocapacitors for future nanoelectronic circuits.

Keywords—Capacitor, MIM Devices, Nanotechnology, Tunneling.

I. INTRODUCTION

C everal nanoelectronic devices have recently been proposed S of which Coulomb blockade [1], [2], and tunneling [3], [4] transistors are the most prominently investigated. However capacitors are critical circuit elements in modern microelectronics and electronic systems, and potential nanoelectronic circuits will be no exception. One can use interconnect capacitances, and metal-insulator-semiconductor (MIS) structures such as MOSFETs to store charge, however these capacitances are highly non-linear [5-7], and are sensitive to ambient conditions [5], [7] due to various factors including defect densities in the dielectric layers, interfacial space charge accumulation, and thermal drift of electrochemical potentials in the semiconductor layers. Hence there will be a need for integrable nanoscopic metal-insulator-metal (MIM) capacitors, for both nanoelectronic integrated circuits, and discrete devices. The longitudinal dimensions (relative to an applied electric field) of layered gate oxides of many existing planar devices can already be between 0.9 and 1.4 nm [8], but their transverse dimensions must remain relatively macroscopic to maintain the desired capacitances. However our proposed nanocapacitor is a MIM device in which the transverse dimensions are also in the nanometer scale.

Capacitance is, now, a sufficiently critical physical quantity, the US National Institute for Standards and Technology (NIST) is developing methods for metrology of a new capacitance standard based on the elementary charge of an electron, using single electron tunneling transistors (SETT), and a low-loss cryogenic capacitor [9-13]. Maccuci [14], [15] presented modeling of differential capacitance of radial quantum dots, and Wang *et al.* presented work on non-linear quantum capacitance [16] and capacitance of atomic junctions [17]. We propose our nanocapacitor as a device that might have applications in nanoelectronic circuits, hybrid (microelectronicnanoelectronic) systems, and low charge store-pump applications. In section II, we present the hybrid capacitance model of a nanocapacitor, and compare it to the classical model. We use a radial parallel-plate (RPP) configuration, for simplicity and ease of presenting the concepts explored herein. In section III, we discuss the implications of dielectric strength on the maximum charge storage capacity, thus operating voltage range, and charge quantization effects in the capacitor. In section IV, we look at tunneling charge leakage, and discharge time of the capacitor. We use MKS units in this work.

II. HYBRID CAPACITANCE MODEL

A. Correction to capacitance model

The longitudinal and transverse dimensions of our nanocapacitor mean there is a quantum mechanical (QM) component in addition to the classical capacitance,

$$C_C = \frac{\varepsilon_r \varepsilon_0 A}{d} \tag{1}$$

where ε_r and ε_0 are the dielectric constant and absolute permittivity respectively, A (m²) is the cross-sectional area of the dielectric, and d (m) is its thickness. The QM component is a manifestation of the density of states (DoS) of the metal electrodes, and their Thomas-Fermi screening lengths. Hence the hybrid capacitance of any nanocapacitor architecture is

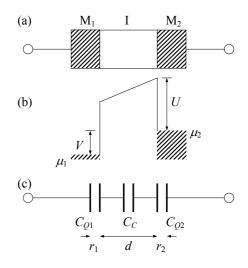


Fig. 1. (a) Structure of a MIM capacitor, (b) its band diagram under applied bias V(V), and (c) the schematic of (equivalent) hybrid capacitance due to the classical RPP capacitance, and quantum capacitance due to Thomas-Fermi screening lengths of the metal electrodes.

given as

$$C = \left(\frac{1}{C_{Q1}} + \frac{1}{C_C} + \frac{1}{C_{Q2}}\right)^{-1}$$
(2)

where *C* (F) is the total capacitance of the nanocapacitor, C_C is the classical (geometric) capacitance, C_{Q1} and C_{Q2} are the quantum capacitances due to the finite DoS of the metal electrodes M₁, and M₂, respectively, as illustrated in Fig. 1. At the semi-classical limit where our nanocapacitor has thousands of atoms in its electrodes despite its size, and accounting for the Thomas-Fermi screening due to penetration of the applied electric field into the surface of the metal electrodes, (2) can be further written as

$$C = \left(\frac{2}{C_Q} + \frac{d}{\varepsilon_r \varepsilon_0 A}\right)^{-1}$$
(3a)

where [18]

$$C_Q \equiv C_{Q1} = C_{Q2} = \frac{\varepsilon_m \varepsilon_0 A}{r_{TF} \sqrt{\varepsilon_m}}$$
, and (3b)

$$r_{TF} = \left(\frac{\varepsilon_0}{e^2 D(\mu_F)}\right)^{1/2} = \frac{(r_s/a_0)^{1/2}}{2.95 \cdot 10^{10}}$$
(3c)

provided the electrodes are made of the same metal, \mathcal{E}_m is the dielectric constant of the metal electrodes, e is the elementary charge of an electron, $D(\mu_F) = dn/d\mu_1 = dn/d\mu_2$ $((J \cdot m^3)^{-1})$ is the DoS at the Fermi level [19], [20] of either electrode, and $r_s/a_0 = 3.01$ for gold (Au) [20] which is the ratio of the sphere-radius of conduction electrons to Bohr radius of the ground-state Hydrogen atom ($a_0 = 52.9$ pm), where $r_{TF} = r_1 = r_2 \sim 58.8$ pm are the Thomas-Fermi screening lengths (radii) for the identical electrodes M₁ and M₂, with electrochemical potentials μ_1 and μ_2 respectively. Hence the hybrid capacitance due to the composition of both classical and quantum capacitances is

$$C = \frac{1}{(2\alpha + 1)} C_C, \alpha = \frac{r_{TF}}{d} \frac{\varepsilon_r}{\sqrt{\varepsilon_m}}.$$
 (4)

This shows that the hybrid capacitance due to Thomas-Fermi screening is a quotient of the classical capacitance by the factor, $(2\alpha+1)^{-1}$. We emphasize that this model applies to DC operating conditions [18]. Figure 2a shows the capacitance density of a nanocapacitor designed using silicon dioxide as the dielectric with $\varepsilon_r(\text{SiO}_2) = 3.9$, and Au electrodes with dielectric constant $\varepsilon_r(\text{Au}) \sim 5$. Despite high- κ dielectrics if prepared qualitatively, SiO₂ has very desirable properties such as band gap, $\phi_g(x)$, of ~9 eV, dielectric strength, \mathbf{E}_{BD} , of 9 MV/cm [21], and effective electron mass, m^* , of ~0.52 m_e [22], where m_e is the free electron mass.

It is evident in Fig. 2a that the difference of hybrid capacitance to classical capacitance is inversely proportional to dielectric thickness. In fact, for the above properties, at d = 1 nm, the difference is ~17%, but decreases with increasing dielectric thickness for a constant applied potential difference. At the above thickness however, the hybrid capacitance density is ~29 fF/µm² relative to ~35 fF/µm² in the classical case, which is still quite comparable to currently researched microelectronic high- κ capacitors. It is also evident in Fig. 2b,

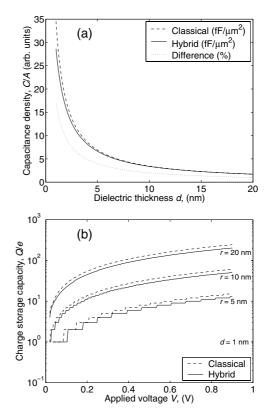


Fig. 2. (a) Capacitance density to dielectric thickness, showing classical capacitance (broken line), hybrid capacitance due to Thomas-Fermi screening (solid line), and the percent difference between the former two (dotted line). (b) Charge storage capacity of a RPP capacitor in (a), with d = 1 nm, and radii of r = 5, 10, and 20 nm.

the charge storage capacities of the RPP nanocapacitor when operated near $\mathbf{E_{BD}}$ for d = 1 nm, and radii r = 5 nm and r = 20nm, is ~10e C and ~200e C of charge corresponding to ~7 eV and ~110 eV of energy respectively by the Coulomb energy $E = Q^2/2C$, where Q is the total charge stored, compared to ~240e C for the classical case. In Fig. 2b, quantum electrical charging effects are clearly visible for dielectric radii of r = 5 nm, and 10 nm.

B. Electrostatics of the nanocapacitor

We simulated and investigated the 2D electrostatics of the RPP nanocapacitor to examine the degree of electric field fringing when compared to macroscopic capacitors, by solving the self-consistent two-dimensional linear Poisson's equation

$$-\varepsilon(\mathbf{r})\nabla\cdot\nabla V(\mathbf{r}) = \rho(\mathbf{r})$$
⁽⁵⁾

with Dirichlet boundary conditions specified for the contact potentials of the electrodes, using finite-difference discretization and simple iterative technique, where **r** is the two-dimensional spatial vector in Cartesian coordinates, $V(\mathbf{r})$ denotes the equipotentials emanating from the charged electrodes, $\rho(\mathbf{r})$ is the charge density distribution (source function), $\varepsilon(\mathbf{r})$ is the relative permittivity ($\varepsilon_r(\mathbf{r}) \cdot \varepsilon_0$) of the material in focus. Here we ignore the effects of electron wave function penetration between the MI junctions, which requires further investigation. Figure 3 shows the simulation of the equipotential lines of a RPP nanocapacitor with plate radii of 5

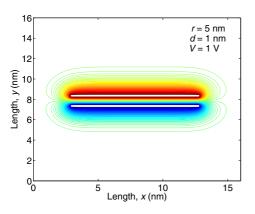


Fig. 3. Center cross-sectional equipotential lines of a RPP nanocapacitor for plate radius r = 5 nm, with dielectric thicknesses of d = 1 nm, demonstrating degree of fringing at nanoscale for SiO₂ at an applied bias of V = 1 V.

nm and 10 nm, and thickness set at 0.3 nm (a monolayer of Au).

As shown in Fig. 3, it is obvious that field fringing can affect the electrostatics of nanocapacitors, but can be minimized by keeping the dielectric thickness small. In this simulation we use an even distribution of $10^6 e$ C/m² of space charge in the dielectric layer to simulate average defects, and SiO₂ as the dielectric, because high- κ dielectrics tend to have reduced dielectric strengths, increased loss tangent, relaxation and heat absorption [23].

III. DIELECTRIC STRENGTH AND OPERATING VOLTAGE

Dielectric strength, E_{BD} , is a critical lattice property that determines the operational electric field range of the nanocapacitors. It is known that the dielectric strength is a function of thickness, called the "thickness effect", and behaves according to the power law [24], [25]

$$\mathbf{E}_{\mathbf{B}\mathbf{D}} = E_0 d^{-y} \mathbf{u} \tag{6}$$

where E_0 is a proportionality constant, y is the index and is typically between 0.3 and 0.4, and **u** is the unit vector, provided the electric field is continuous at nanoscale. This relationship can be justified by the occurrence of lower space charge accumulation densities due to lesser defect sites such as unpassivated surface traps, dangling bonds, charge traps at grain boundaries, and impurities in the dielectric. It could also be that in thin-film dielectrics, the mean free-path of an electron is comparable to the thickness of the dielectric, and its scattering has lesser probability of ejecting further electrons with sufficient energy to produce avalanches that can lead to breakdown. These factors effectively increase E_{BD} in thin dielectrics. Figure 4 shows an extrapolation from known dielectric strengths for SiO₂ using a breakdown voltage of 350 V (DC) for a 950 μ m thick sample [26]. This extrapolation, from microscopic data to predict nanoscopic dielectric strengths, is in good agreement with other published dielectric strengths for SiO₂ [27], [28]. We can predict from Fig. 4, a nanocapacitor with a SiO₂ thickness of 1 nm should be operated below its breakdown voltage of ~2.8 V.

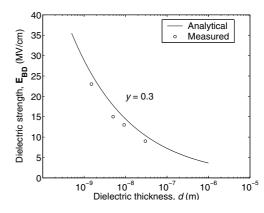


Fig. 4. Dielectric strengths of SiO_2 for varying thicknesses, extrapolated from known strengths using the thickness effect. The prediction is in good agreement with measured dielectric strengths in the nanometer scale.

IV. QUANTUM MECHANICAL TUNNELING LEAKAGE

Tunneling charge leakage is a main constraint on retention time. However, we can reduce tunneling leakage by selecting appropriate dielectrics with larger band gaps (thus larger band offsets). The electrons have a Fermi-Dirac distribution in the metal electrodes, which are connected to the ambient via contacts (leads) that can be viewed as electron reservoirs. The charge stored in the capacitor at any instant is solved for, using

$$\frac{\partial q(V,t)}{\partial t} \delta t + q(V,t) = q_0 \tag{7}$$

where q(V, t) is the instantaneous charge, q_0 is the initial (remaining) stored charge, and $\partial q/\partial t$ is the tunneling current flowing to reduce the band-tilting bias produced by the stored potential. The tunneling current reduces as the stored charge leaks at $\partial q/\partial t$, which itself is a function of the remaining charge. We extrapolate our tunneling currents for d = 1 nm, from published measured data [29].

Figure 5 shows the simulation using the extrapolated experimental tunnel currents for the nanocapacitor with d = 1 nm, and r = 5 nm. The capacitor is initially charged to 0.9 V prior to simulating the discharge time. Initially, it discharges

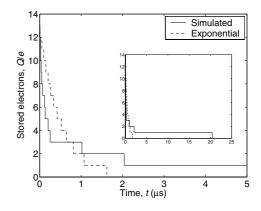


Fig. 5. Charge leakage time (solid line) of the nanocapacitor for d = 1 nm, r = 5 nm, V = 0.9 V, relative to first-order (exponential) discharge (broken line) with time constant $\tau = 0.5 \,\mu$ s, until discharge to zero stored electrons (inset).

rapidly, then retards, which is a consequence of the tunneling current characteristic at low bias potentials. We note that the discharge time per electron in Fig. 5 is a most probable quantity subject to statistical variation of electron retention time. In Fig. 5, the first-order (exponential) discharge with time constant $\tau = 0.5 \,\mu$ s, shows a comparison to classical capacitor discharge.

The inset in Fig. 5 shows the discharge time to reach zero stored electrons ($\sim 20 \ \mu s$) in the capacitor, thus reaching equilibrium of the electrochemical potentials of the electrodes. This single-electron charging and discharging is similar to the Coulomb staircase in SETTs, but at room temperature.

CONCLUSION

We have presented the quantum electrical operational criteria of our nanocapacitor, and discussed the main characteristics that will affect its operability. In particular, we have emphasized the reduction of capacitance as longitudinal, and transverse dimensions approach nanoscale due to low DoS of nanometer-sized electrodes, and the consequent Thomas-Fermi screening effects. We have examined the degree of fringing at the edges of the dielectric that can affect the electrostatics of the nanocapacitor. It is clear keeping the electrode separation small, even at the nanoscale, can minimize fringing. We have explored the increase in dielectric strength in nanoscale dielectrics, and discussed the effects of tunneling leakage on a charged nanocapacitor.

We predict, our nanocapacitor could be utilized in applications, which require charge sensitivities close to the elementary charge of the electron, such as very-high sensitivity proximity sensors, motion detectors, nanoelectromechanical systems, and tip-electronics of scanning capacitance microscopes. It could also be used in novel telemetry nanocircuits powered by low-power sources such as plant or animal metabolisms, where cell potentials are on the order of ~0.5 V [30]. Such telemetry nanocircuits will be vital in medical technologies, radio frequency identification (RFID) systems, behavioral studies such as swam intelligence, and investigating spaces where conventional electromechanical systems cannot reach such as the interior of live tissue.

References

- D. H. Kim, S.-K. Sung, K. R. Kim, and J. D. Lee, "Fabrication of singleelectron tunneling transistors with an electrically formed Coulomb island in a silicon-on-insulator nanowire," *J. Vac. Sci. Technol. B*, vol. 20, pp. 1410-1418, 2002.
- [2] C. S. Wu, C. D. Chen, S. M. Shih, and W. F. Su, "Single-electron transistors and memory cells with Au colloidal islands," *Appl. Phys. Lett.*, vol. 81, pp. 4595-4597, 2002.
- [3] G. L. Timp, *Nanotechnology*. New York: Springer-Verlag New York, Inc., 1999.
- [4] F.-C. Wang, et al., "A tunneling field-effect transistor with 25 nm metallurgical channel length," Appl. Phys. Lett., vol. 70, pp. 3005-3006, 1997.
- [5] H. Samavati, A. Hajimiri, A. R. Shahani, G. N. Nasserbakht, and T. H. Lee, "Fractal Capacitors," *IEEE J. Solid-State Circuits*, vol. 33, pp. 2035-2041, 1998.
- [6] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, "Germanium MOS Capacitors Incorporating Ultrathin High-k Gate Dielectric," *IEEE Electron Device Lett.*, vol. 23, pp. 473-475, 2002.

- [7] K. Matocha, T. P. Chow, and R. J. Gutmann, "Positive Flatband Voltage Shift in MOS Capacitors on n-Type GaN," *IEEE Electron Device Lett.*, vol. 23, pp. 79-81, 2002.
- [8] Semiconductor Industry Association, (2002), International Technology Roadmap for Semiconductors, International SEMATECH, Available: <u>http://public.itrs.net</u>.
- [9] M. W. Keller, A. L. Eichenberger, J. M. Martinis, and N. M. Zimmerman, "A Capacitance Standard Based on Counting Electrons," *Science*, vol. 285, pp. 1706-1709, 1999.
- [10] M. W. Keller, J. M. Martinis, A. H. Steinbach, and N. M. Zimmerman, "A Seven-Junction Electron Pump:Design, Fabrication, and Operation," *IEEE Trans. Instr. Measurement*, vol. 46, pp. 307-310, 1997.
- [11] A. F. Clark, et al., "Application of single electron tunneling: Precision capacitance ratio measurements," Appl. Phys. Lett., vol. 66, pp. 2588-2590, 1995.
- [12] M. W. Keller, J. M. Martinis, N. M. Zimmerman, and A. H. Steinbach, "Accuracy of electron counting using a 7-junction electron pump," *Appl. Phys. Lett.*, vol. 69, pp. 1804-1806, 1996.
 [13] N. M. Zimmerman, "Capacitors with Very Low Loss: Cryogenic
- [13] N. M. Zimmerman, "Capacitors with Very Low Loss: Cryogenic Vacuum-Gap Capacitors," *IEEE Trans. Instr. Measurement*, vol. 45, pp. 841-846, 1996.
- [14] M. Macucci, "Differential capacitance between circular stacked quantum dots," *Physica E*, vol. 1, pp. 7-14, 1997.
- [15] M. Macucci, K. Hess, and G. J. Iafrate, "Electronic energy spectrum and the concept of capacitance in quantum dots," *Phys. Rev. B*, vol. 48, pp. 17354-17363, 1993.
- [16] B. Wang, X. Zhao, J. Wang, and H. Guo, "Nonlinear quantum capacitance," *Appl. Phys. Lett.*, vol. 74, pp. 2887-2889, 1999.
- [17] J. Wang, et al., "Capacitance of Atomic Junctions," Phys. Rev. Lett., vol. 80, pp. 4277-4280, 1998.
- [18] C. T. Black and J. J. Welser, "Electric-Field Penetration Into Metals: Consequences for High-Dielectric-Constant Capacitors," *IEEE Trans. Electron Devices*, vol. 46, pp. 776-780, 1999.
- [19] J. Mulak, "The Thomas–Fermi Type Screening of the Crystal Field Multipole Moments," *Journal of Solid State Chemistry*, vol. 124, pp. 182-189, 1996.
- [20] N. W. Ashcroft and N. D. Mermin, *Solid state physics*, College ed: Saunders College Publishing, 1976.
- [21] D. Landheer, L.-Å. Ragnarsson, and S. Belkouch, "Physical and electrical analysis of silicon dioxide thin films produced by electroncyclotron resonance chemical-vapour deposition," *Microelectronic Engineering*, vol. 36, pp. 53-60, 1997.
- [22] L. F. Mao, J. L. Wei, C. H. Tan, and M. Z. Xu, "Determination of the effective mass of ballistic electrons in thin silicon dioxide films using tunneling current oscillations," *Solid-State Communications*, vol. 114, pp. 383-387, 2000.
- [23] J. J. O'Dwyer, *The theory of dielectric breakdown of solids*. Oxford: Clarendon Press, 1964.
- [24] S. R. Ekanayake, M. B. Cortie, and M. J. Ford, "Design of nanocapacitors and associated materials challenges," *Curr. Appl. Phys.*, 2003, in press.
- [25] J. M. Herbert, *Ceramic dielectrics and capacitors*, vol. 6. New York: Gordon and Breach Science Publishers, 1985.
- [26] L. Larcher, A. Paccagnella, and G. Ghidini, "Gate Current in Ultrathin MOS Capacitors: A New Model of Tunnel Current," *IEEE Trans. Electron Devices*, vol. 48, pp. 271-278, 2001.
- [27] J. Suñé, P. Olivo, and B. Riccò, "Quantum-Mechanical Modeling of Accumulation Layers in MOS Structures," *IEEE Trans. Electron Devices*, vol. 39, pp. 1732-1739, 1992.
- [28] H. S. Momose, et al., "Study of the Manufacturing Feasibility of 1.5-nm Direct-Tunneling Gate Oxide MOSFET's: Uniformity, Reliability, and Dopant Penetration of the Gate Oxide," *IEEE Trans. Electron Devices*, vol. 45, pp. 691-700, 1998.
- [29] K. A. Bowman, L. Wang, X. Tang, and J. D. Meindl, "A Circuit-Level Perspective of the Optimum Gate Oxide Thickness," *IEEE Trans. Electron Devices*, vol. 48, pp. 1800-1810, 2001.
- [30] N. Mano, F. Mao, and A. Heller, "Characteristics of a Miniature Compartment-less Glucose-O₂ Biofuel Cell and its Operation in a Living Plant," J. Am. Chem. Soc., vol. 125, pp. 6588-6594, 2003.