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Experimental investigation of ultracapacitor impedance characteristics

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Abstract

Ultracapacitors (UCs) are being increasingly studied and deployed as a short-term energy storage device in various energy systems including uninterruptible power supplies, electrified vehicles, renewable energy systems, and wireless communication. They exhibit excellent power density and energy efficiency. The dynamic behavior of a UC, however, strongly depends on its impedance characteristics. In this paper, the impedance characteristics of a commercial UC are experimentally investigated through the well-adopted Electrochemical Impedance Spectroscopy (EIS) technique. The implications of the UC operating conditions (i.e., state of charge (SOC) and temperature) to the impedance are systematically examined. The results show that the impedance is highly sensitive to temperature and SOC; and the temperature effect is more significant. The experimental design and multi-condition impedance analysis provides prudent insights into UC system integration, dimensioning, and energy management strategy synthesis in advanced energy systems.

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1. Introduction

Energy storage systems are used in a wide variety of industrial applications, e.g., uninterruptable power supplies (UPS), electrified vehicles (EVs), renewable energy systems, and wireless communication, etc. [1]. Ultracapacitors (UCs), also known as Double-layer Electric Capacitor (DLEC) and Supercapacitors (SCs), are being actively studied and increasingly deployed since they represent a promising energy storage technology. Generally, they are characterized by high power density, fast charging, low internal resistance, high efficiency, and exceptionally long cycle lifespan [2]. These advantageous merits render them ideal for high-power ESSs and complementary components for high-ESSs (e.g., batteries) which turn out to form advanced hybrid energy storage systems (HESSs) [3], [4]. UCs with two electrodes and an ion-permeable separator store charge largely by electrostatic charge transfer and incidental faradaic reactions [5], [6]. When a small potential is applied to the terminals, a double-capacitor structure is formed instantly at the interface between the solid electrode material surface and the liquid electrolyte. High specific surface area electrodes contribute to a significantly increased energy density when compared to conventional capacitors [7]. However, a pseudo-capacitance can also be observed, which results in a nonlinear relationship between the state-of-charge (SOC) and open-circuit voltage. The power sourcing/delivery capability of a UC is highly dependent on its impedance, to which the charge/discharge energy loss is directly proportional. As a result, a systematic examination of such impedance behavior is critical to the development of control/management systems ensuring a safe, reliable, and durable operation of UCs. The concomitant challenge is, however, considerable, because the UC impedance may vary significantly with respect to dynamic operating conditions, in terms of temperature and SOC.

The Electrochemical Impedance Spectroscopy (EIS) technique has been used to characterize UCs, and a class of UC models has been put forward as results in [8] and [9]. A further example was discussed by Buller *et al*. who presented an equivalent circuit model to mimic the phenomenological behavior of UCs [10]. The impedance values at five temperatures and four open-circuit voltages were obtained through the EIS method, and further used to estimate the model parameters. Kötz *et al.* employed the EIS technique to determine the equivalent series resistance and the capacitance at voltages between 2.5V and 3.0 V and temperatures between -40°C and +70°C [11]. Bohlen *et al.* investigated the aging behavior of UCs via impedance spectroscopy analysis [12], where an impedance model composed of pore impedance, and a series resistance and inductance, was proposed. Gualous *et al.* utilized the EIS approach to characterize UCs at their rated voltage and a fixed ambient temperature [13]. All the aforementioned studies, nevertheless, merely take the open-circuit voltage variation of UCs into account, without explicitly assessing the SOC effect on impedance characteristics. In contrast to open-circuit voltage, SOC is clearly more indicative of available energy inside UCs. Unlike conventional capacitors, the UC SOC is largely a nonlinear function of open-circuit voltage, which often cannot be trivially evaluated due to its volatility with operating circumstances. Hence, a direct inclusion of SOC as an influencing factor for impedance analysis and modeling could lead to a more aggressive yet effectual control scheme sufficiently leveraging the potential of a UC pack. In addition, limited levels of influencing factors were considered, incurring the absence of a precise impedance dependency upon operating conditions. Moreover, the coupling impact of the temperature and SOC on the UC impedance has been constantly overlooked in the foregoing work.

The primary purpose of this article is to overcome the above downsides. The impedance characteristics of a UC under various temperatures and SOC values are analyzed through the EIS method. To carry out this work, a test rig was developed, upon which both EIS tests were performed. The EIS tests cover a wide SOC range from 10% SOC to 100% SOC and a broad temperature range from -40°C to +40°C. The impedance dependency on the temperature and SOC is systematically examined, including the interactive effect of both factors. In particular, the high-efficiency SOC window at each temperature is highlighted.

2. EIS technique

The EIS technique is a well-established approach to investigating energy storage devices such as batteries and UCs [14], [15]. It provides a deeper insight into the internal processes of the system by exploring the impedance characteristics under a broad range of frequencies. This is done by injecting a small sinusoidal current signal into the device and measuring the response voltage, or vice versa (galvanostatic and potentiostatic approaches). The complex impedance can be calculated as the quotient of the detected voltage and the injected current at each sampled frequency. The Nyquist diagram is often plotted to depict the evolution of the real and imaginary parts of the impedance under the sampled frequencies. Equivalent circuit models can be further extracted by analyzing and interpreting the derived impedance spectra with basic circuit elements. It can be noted that the impedance changes throughout the service life of the device, where the impedance basically increases with aging. One definition of the End-of-Life (EoF) of a UC is a pre-defined impedance increase from its nominal operation impedance. However, compared with the impedance variation due to temperature and SOC, the impedance varies much more slowly with aging. Therefore, it is reasonable to firstly ignore the impact of aging on the UC impedance in a relatively large time scale. The aging issue needs further work in order to address it, which is well beyond the scope of this paper.

3. Experimental setup

In order to perform the EIS tests, a test rig was set up as shown in Fig. 1. It consists of a battery test system (BTS), a thermal chamber, an electrochemical workstation, a host computer, and a test UC. The BTS is used to load the UC in accordance with pre-defined loading profiles. It has the capability of recording the test parameters, such as accumulated capacity, loading current and terminal voltage. Accuracies of the current and voltage measurements are up to 1 mA and 1 mV, respectively. This guarantees the reliability of the measured data. The recorded data can be further relayed to the host computer through a CAN network, which serves as a reliable and fast-response communication between the host computer and the power cycler. The thermal chamber accommodates the UC and provides the thermostatic ambience for all the tests. The temperature can be set at any point between -40°C to +60°C. The electrochemical workstation is able to measure the impedance of the UC at a given frequency range with high precision. The host computer is used to develop the loading profiles and store the test data fetched from the BTS and the electrochemical workstation. A Maxwell BCAP3000 P270 K04 was selected to conduct all the tests, which allows a maximum current up to 1900 A. The detailed specifications as stated in the manufacturer sheet are shown in Table 1. The tests covered a temperature range from -40°C to 40°C and for a SOC from 10 % up to 100 %.

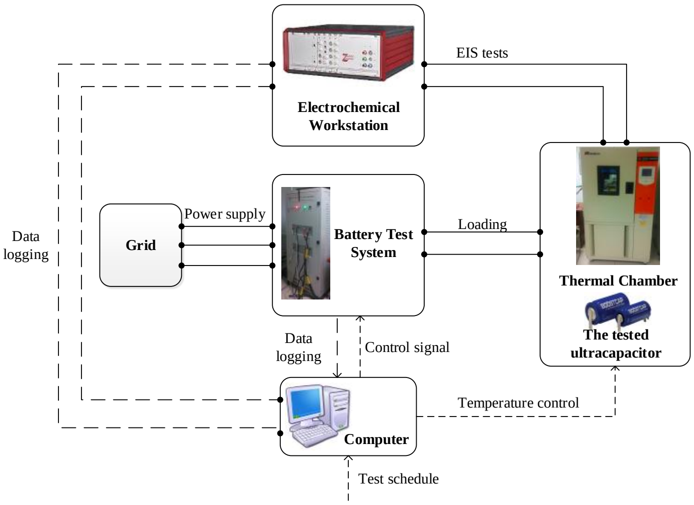

Fig. 1. Configuration of the test rig.

Table 1. Ultracapacitor specifications.

Nominal capacity (*F*)	Rated voltage (*V*)	ESR$_{DC}$ (*mOhm*)	Leak current (*A*)	Operating Temperature (℃)
3000	2.7	0.29	5.2	-40 ~ +65

4. Experimental results

4.1 Temperature Dependency of Impedance

Using the results from the executed EIS tests, the dependency of the UC impedance on temperature was studied in detail. Five temperature points were selected, and these cover the typical thermal operating conditions from extremely low to high temperatures. Fig. 2 shows the temperature influence in more detail in Nyquist plots. Semi-circles can be found in all the plots for the lower temperatures. This phenomenon is due to the slower reaction processes at low temperature, which result in lower frequency threshold for a UC to exercise inductive effects. It is also evident that the real part of the impedance dramatically increases with the decreasing temperature, and the change seems to increase at relatively low temperatures. Furthermore, the temperature dependency of the UC impedance is even greater at temperatures below 0°C. This may be attributed to the reduced solubility of the conducting salt and the increased viscosity of the electrolyte for temperatures below the freezing point. Both of these effects result in dramatically reduced electrolyte conductivity. As a consequence, the power capability of the UCs would be severely compromised under low operating temperature.

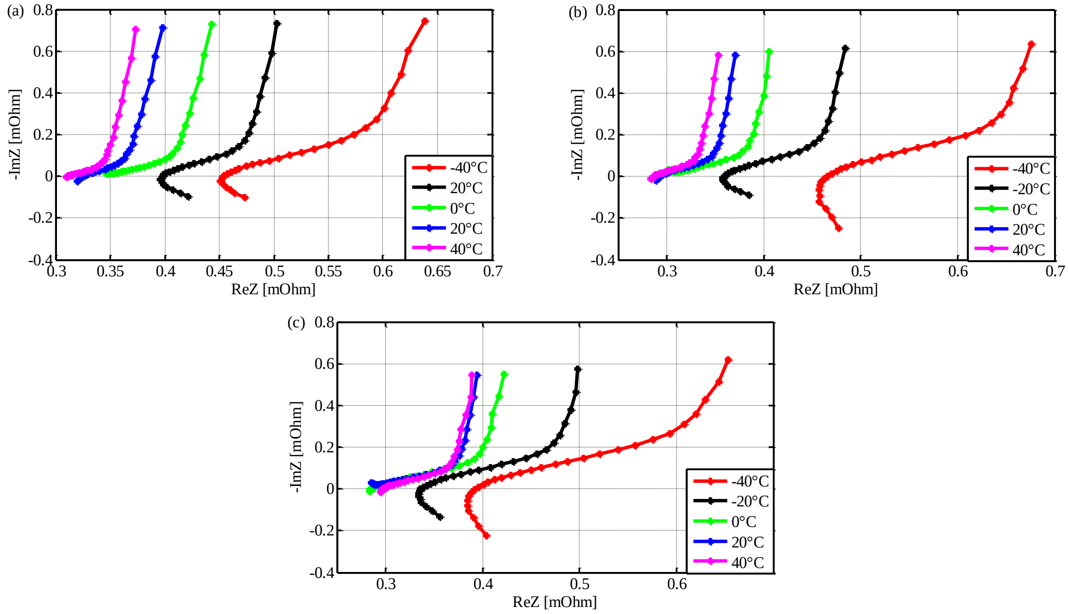

Fig. 2. Schematic impedance spectrum in Nyquist plots under different temperatures with (a) 10% SOC; (b) 50%SOC; (c) 90%SOC.

4.2 SOC dependency of Impedance

The SOC influence on the impedance characteristics of the UC was also investigated. Fig.3 illustrates how the impedance fluctuates with the SOC variation under all the temperatures. Compared to the impedance variation caused by temperature, the SOC factor seems to be less dominant. Upon a closer examination, it is noted that extreme temperatures (as low as -40°C and as high as 40°C) intensify the SOC influence on the impedance, especially in the low frequency region. For example, as shown in Fig. 4, at 40°C, the average impedance firstly reduces as the SOC increases until about 60%, and then the impedance increases when further raising the SOC. Instead, in the case of 20°C, there is constantly decreasing impedance with increasing SOC. Under temperatures below 0°C, the SOC dependency even exhibits an opposite trend to that at 40°C. These observations in turn illustrate the coupling impact of the temperature and SOC on the UC impedance. The SOC range corresponding to low impedance at each temperature can be easily identified from the results in Fig. 4, which represents the high-efficiency SOC window. This is much beneficial to designing control strategies for efficiently diminishing energy losses in realistic operations of UC storage systems.

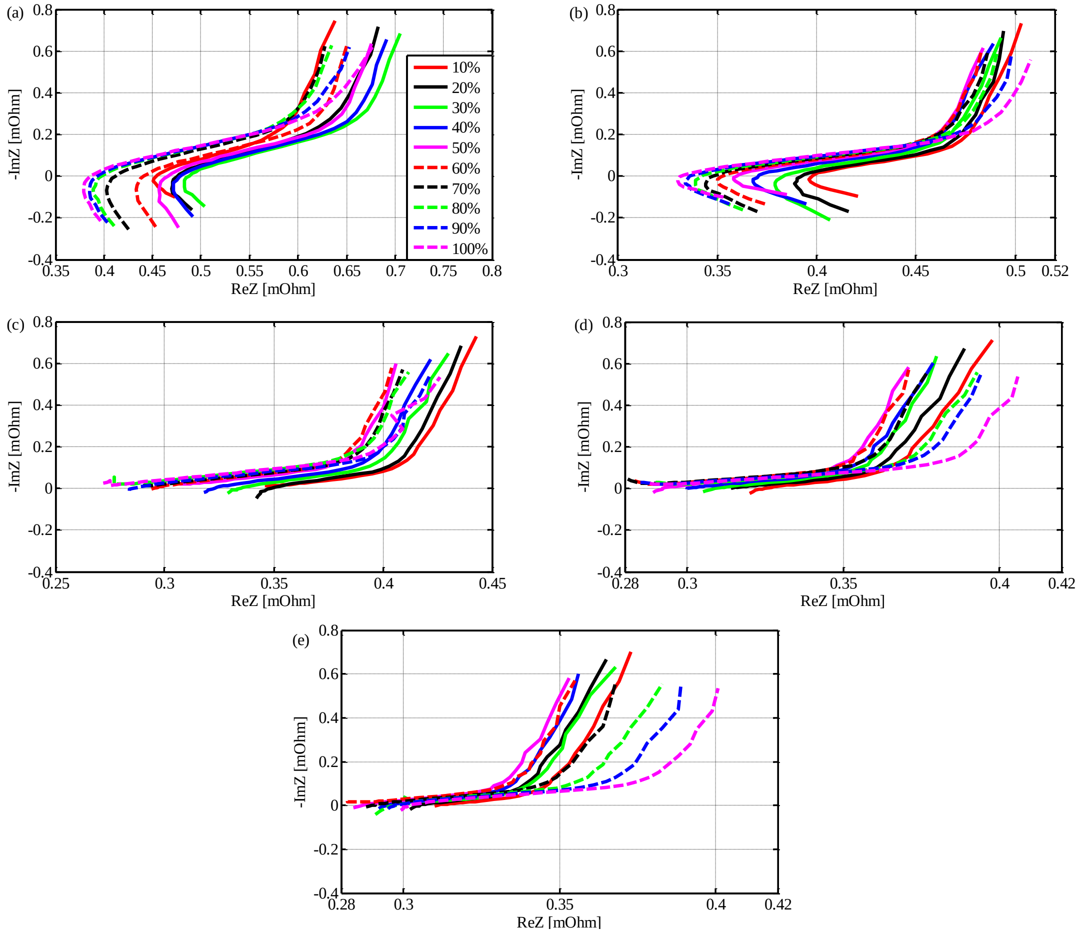

Fig. 3. Schematic impedance spectra in Nyquist plots with different SOC values under the temperature of (a) -40 °C; (b) -20 °C; (c) 0°C; (d)20°C; (e) 40 °C.

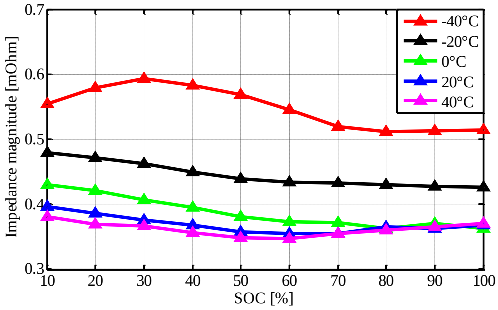

Fig. 4. Evolution of average impedance magnitude with SOC under different temperatures.

5. Conclusions

This paper presents a systematic experimental study of the UC impedance characteristics under different operating conditions (wide ranges of temperature and SOC) through the EIS technique. To this end, a special test rig was established and used to perform the EIS tests. The experimental results indicate that the impedance magnitude exhibits an exponential increase as the temperature decreases. These impedance changes will inevitably compromise the ultracapacitor efficiency and power capability in low-temperature applications, which should be seriously considered in system integration and control design. The analysis of the SOC dependency of impedance highlights the high-efficiency SOC window of the tested UC. Such a window varies with temperature, which reflects the interactive effect of the temperature and SOC on the UC impedance. It is valuable to take this into consideration when optimizing the UC system performance.

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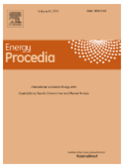

Biography

Lei Zhang received the B.S degree in automotive engineering from South China University of Technology in 2010. He is working towards the Ph. D degree as a dual-degree student with University of Technology, Sydney and Beijing Institute of Technology. His research interests include modeling and optimal control of energy storage systems.

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