Capacitor Voltage Natural Balance Multilevel Converter for High Power Applications

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Abstract: Capacitor voltage balance control has attracted increasing attention in the studies of cascaded multilevel converters and modular multilevel converters. This paper proposes a novel multilevel converter topology based on diode clamped half-bridge cascaded converter for medium/high voltage and high power applications. The capacitor voltages of this converter are self-balanced and only two voltage sensors are required for the capacitor voltage control. Therefore, the control of the converter can be designed as simple as that of a two-level converter. A pulse width modulation (PWM) method based on phase shifted PWM and a control strategy of the converter utilized as astatic Var generator (SVG) are also presented. The proposed converter and control strategy were simulated with PSIM. Experiments were also carried out with a laboratory prototype. Both the simulation and experiment results validated the performance of the proposed converter. The capacitor voltage natural balancing is realized with the new topology, and the applied PWM and control method also work effectively.

1. Introduction

Multilevel converter is popularly used in static Var generator (SVG) [1-2] or active power filter (APF) [3-5] in medium voltage networks, high voltage direct current (HVDC) transmission system [6-9], high voltage motor drive [10] and so on. There are several kinds of multilevel converters widely used, such as diode-clamped multilevel converter, flying-capacitor multilevel converter, cascade H-bridge multilevel converter, and modular multilevel converter (MMC) [11-13]. Recently, MMC has attracted significant interest for high voltage applications [7-8, 14-21]. The major advantages of MMC include the modularity and the capability of high voltage output. The voltage rating of a commercial semiconductor switch, for example, the insulated gate bipolar transistor (IGBT), is limited by the manufacturing technology. Tens or even hundreds of switches may be required in the applications of MMC [14], and there are also numerous capacitors needed in the converter [21]. The voltage of each capacitor in the converter should be controlled to keep the capacitor and the switches from over voltage. Thus the capacitor voltage balance control has become a very hot topic in the studies of MMC [15-20].

Both hardware and software methods can be applied to balance the capacitor voltage. The auxiliary energy exchanging circuits can be used to balance the capacitor voltages as a hardware method. However, the auxiliary circuit is usually very complex and requires extra control circuit, which greatly increases the cost.

Theoretically, the voltage of a capacitor will rise when the current flows into it and will drop when the current flows out of it, which depends on the circuit topological mode of the converter. The topological mode changes when the switching is triggered, and hence the capacitor voltage can be balanced by regulating the switching duty cycle with a pulse width modulation (PWM) strategy or a capacitor voltage balance

control algorithm. More and more attention is being focused on how to balance the capacitor voltage of MMC by using software programming without affecting its outputs, system control stability and so on. A disposition PWM method proposed by Fan *et al.* [18] was employed in the MMC, and improved with a simple capacitor voltage balance algorithm which keeps the merit of low calculation when the number of sub-modules is fairly large. Since the balancing action is only applied to the sub-modules with the highest and lowest voltages, the voltage balance capability may become weak in a high power MMC with large number of sub-modules. Accordingly, many switches are needed in a phase arm of the MMC. The phase voltage redundant states can be used to balance the capacitor voltages [15-16]. The capacitor voltage balance control can also be achieved in the modulation by regulating the phase of the carrier wave or the amplitude and phase of the modulation reference [9]. Similar investigations of capacitor voltage balance control for MMC have been reported in [22]. Although no extra auxiliary power circuit is required to balance the capacitor voltage with software control, the voltage of each capacitor has to be measured, e.g. a voltage sensor, an analog to digital data converting circuit and a communication circuit are required in each sub-module of MMC. When the quantity of sub-modules is very large, there will be a large scale of control circuit, increasing the cost of the converter and deteriorating the simplicity of the system. Furthermore, the computational cost of the capacitor voltage balance control is so high that it becomes a key issue of concern [20].

Topology with capacitor natural balancing capability has also attracted attention. A universal multilevel converter was proposed by Peng, *et al.* in 2000 [13], which had the capability of capacitor voltage natural balance. However, the quantity of the

power switches is much larger than that of other multilevel converter topologies, e.g. MMC.

A novel diode clamped modular multilevel converter was proposed by Gao, *et al.* in [4]. Capacitor voltage balance has been achieved by using an auxiliary diode in each sub-module and a simple energy feedback circuit in a phase cluster. Thus only the overall control of the capacitor voltage in a phase arm and the control of the energy feedback circuit are required, which reduces the computational cost greatly. Furthermore, only four voltage sensors are used to control the capacitor voltages in the whole system. However, an energy feedback circuit together with its control is still required.

This paper proposes an improved diode clamped modular multilevel converter topology with the merits of capacitor voltage natural balancing, very few voltage sensors and high power capacity. The converter topology analysis is presented in Section 2. In Section 3, the modulation method and the control of the proposed converter utilized as a static Var generator are demonstrated. Then simulations and experiments are carried out to validate the capacitor voltage natural balancing capability and the control effectiveness of the proposed multilevel converter in Section 4.

2. Topology and Analysis

2.1 Working principle of the topology

The sub-module of the MMC is a half-bridge converter, and the dc-link capacitor is floating. The basic diode clamped modular multilevel converter topologies as shown in Fig. 1 (*a*) ~ (*b*) were originally proposed by Gao, *et al.* in [4]. The topology of Fig.

1 (*a*) is named as upward clamping topology (UCT), and the other as shown in Fig. 1 (*b*) is named as downward clamping topology (DCT). When the voltage across the diode is positive, it will switch on naturally. Thus the capacitor voltage in a phase cluster can be clamped, upward or downward. However, an energy feedback circuit has to be added to overcome the drawback of capacitor voltage unidirectional clamping.

Based on the basic diode clamped modular multilevel converter topology, an improved topology is proposed as shown in Fig. 1 (*c*). There are *N* stages in this topology and the two sub-modules in the same stage can be taken as a unit. The left arm of the new topology is a UCT and the right arm is a DCT. The negative terminals of left and right arms are connected together as the negative terminal. The positive terminals of the left and right arms are also connected through inductors L_1 and L_2, as the positive terminal of the new topology. Another inductor (L_3) is used to connect the cathodes of the capacitors (C_{L1} and C_{R1}) in the top unit as shown in Fig. 1 (*c*). A diode (D_M) is used to connect the anodes of C_{LN} and C_{RN} in the bottom unit.

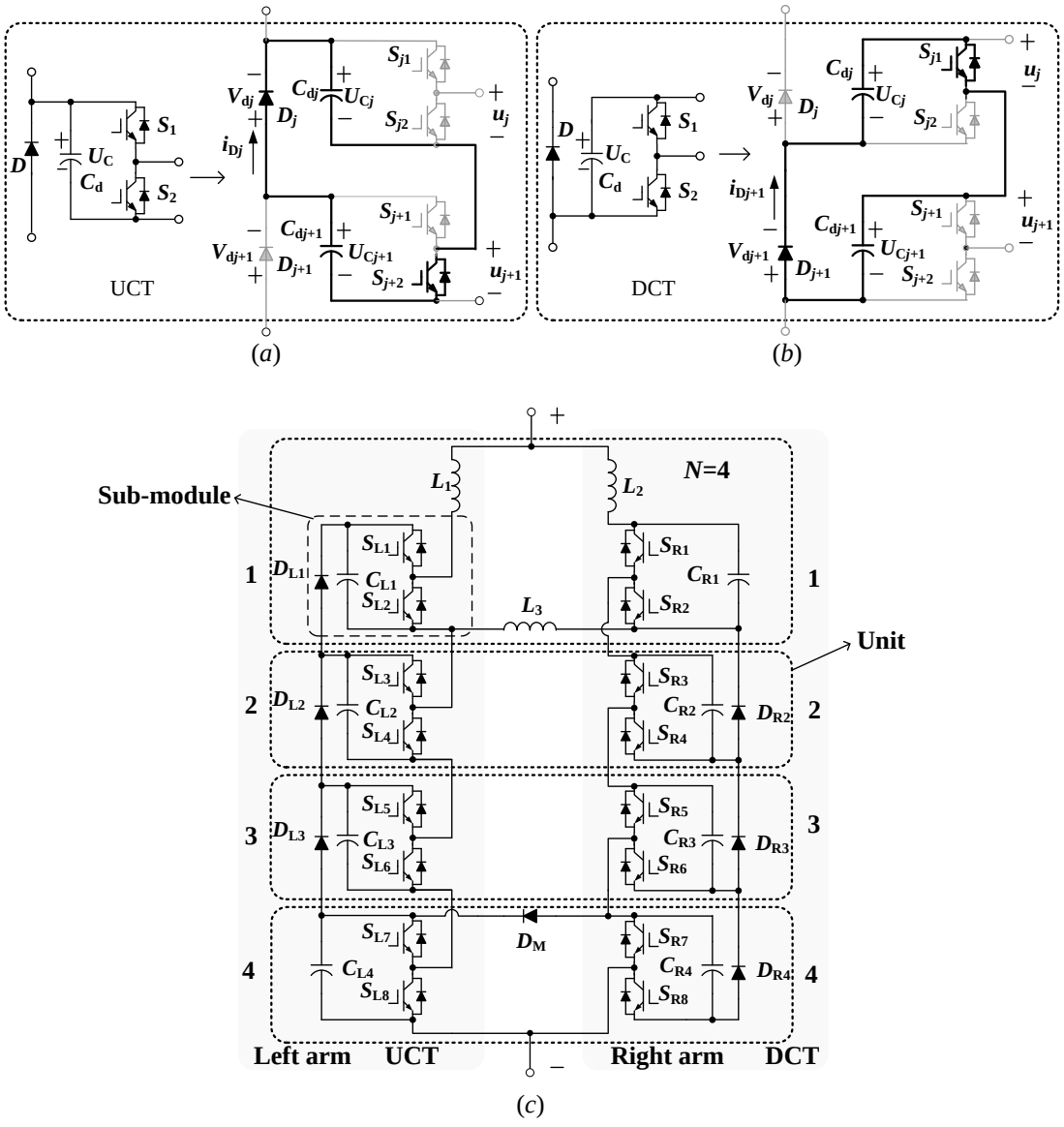


Fig. 1. Diode clamped modular multilevel converter topology: (*a*) ~ (*b*) basic topologies, (*c*) proposed topology

Because the capacitor voltages are clamped when the converter runs, we have $U_{CLj} \leq U_{CLj\text{-}1}$ in the left arm of the proposed topology, while $U_{CRj} \geq U_{CRj\text{-}1}$ in the right arm. Then,

$$U_{CL1} \geq U_{CL2} \geq \ldots U_{CLj\text{-}1} \geq U_{CLj} \geq \ldots U_{CLN\text{-}1} \geq U_{CLN} \tag{1}$$

$$U_{CR1} \leq U_{CR2} \leq \ldots U_{CRj\text{-}1} \leq U_{CRj} \leq \ldots U_{CRN\text{-}1} \leq U_{CRN} \tag{2}$$

If $U_{CLN} \geq U_{CRN}$ and $U_{CL1} \leq U_{CR1}$ can be achieved, the capacitor voltage will be all balanced as follows,

$$U_{CL1}=U_{CL2}=\ldots U_{CLj-1}=U_{CLj}=\ldots U_{CLN}=U_{CRN}=\ldots U_{CRj-1}=U_{CRj}\ldots U_{CR2}=U_{CR1} \quad (3)$$

In the proposed converter, $U_{CLN} \geq U_{CRN}$ and $U_{CL1} \leq U_{CR1}$ are achieved in the bottom unit and the top unit, respectively.

2.2 Analysis of the bottom unit in the topology

There are four topological modes for the bottom unit as shown in Fig. 2. In Fig. 2 (*a*) ~ (*b*) the switch S_{R8} is on. If $U_{CR4}>U_{CL4}$, the diode D_M will switch on and current i_{DM} will flow from C_{R4} into C_{L4}. Consequently, U_{CR4} will drop while U_{CL4} will rise, i.e. U_{CR4} is clamped by U_{CL4}. Thus, $U_{CL4}\geq U_{CR4}$. Although S_{R8} and D_M are both off ($i_{DM}=0$) in the topological modes of Fig. 2 (*c*) ~ (*d*), $U_{CL4}\geq U_{CR4}$ could also be achieved because S_{R8} switches on and off frequently during the normal operation.

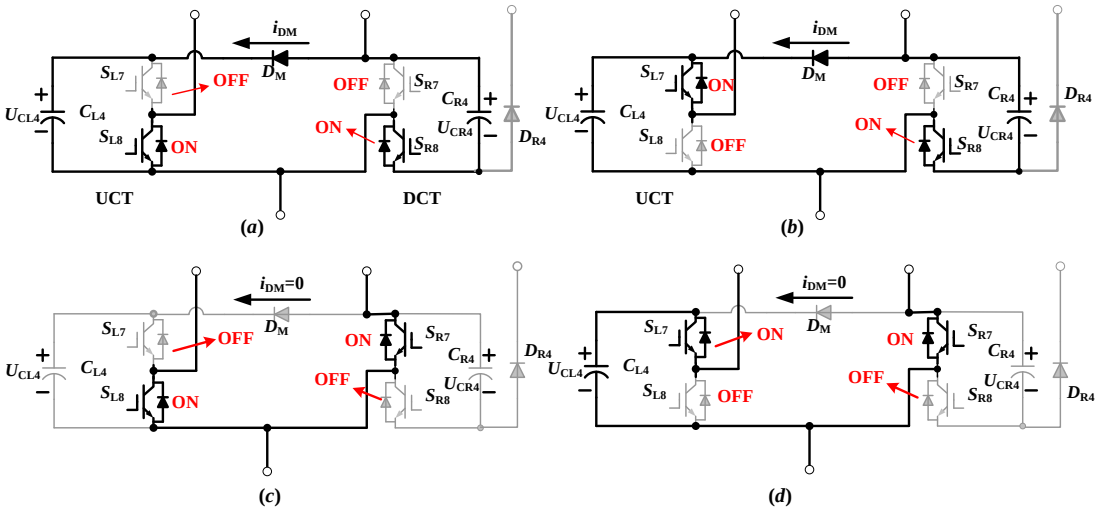


Fig. 2. Typical topological modes of the bottom unit

2.3 Analysis of the top unit in the topology

The top unit of the topology is shown in Fig. 3, which consists of two half-bridge sub-modules. The relationship between the current i_{circul} and the output voltages (u_{L1}, u_{R1}) of the sub-modules is,

$$(L_1+L_2+L_3)\frac{di_{circul}(t)}{dt}=u_{L1}(t)-u_{R1}(t) \tag{4}$$

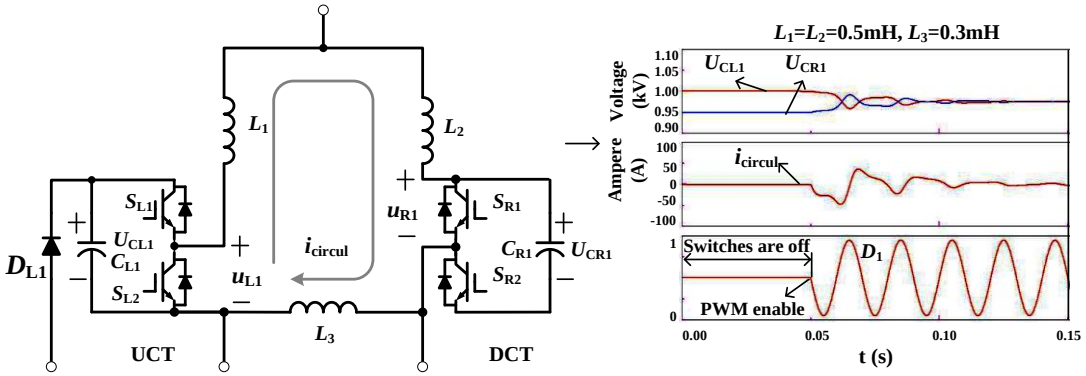


Fig. 3. Topology of the top unit and simulation of the capacitor voltage dynamic process

Assume T_S is the switching cycle ($T_S = t_1 - t_0$, where t_0 is the starting time of a switching cycle and t_1 is the ending time.) and D_1 is the duty cycle of S_{L1} and S_{R2} (The PWM strategy will be presented in Section 3), then,

$$\begin{aligned} i_{circul}(t_1)-i_{circul}(t_0) &= \int_{t_0}^{t_1}\frac{u_{L1}(t)-u_{R1}(t)}{(L_1+L_2+L_3)}dt \\ &= \frac{\int_{t_0}^{t_1}u_{L1}(t)dt-\int_{t_0}^{t_1}u_{R1}(t)dt}{L_1+L_2+L_3} \\ &= \frac{(U_{CL1}-U_{CR1})D_1T_S}{L_1+L_2+L_3} \end{aligned} \tag{5}$$

When the converter runs in steady state,

$$\xrightarrow{t_1-t_0=T_S} i_{circul}(t_1)=i_{circul}(t_0) \tag{6}$$

Then,

$$U_{CL1}-U_{CR1}=0,\rightarrow U_{CL1}=U_{CR1} \tag{7}$$

The simulation of the dynamic process of capacitor voltage balancing for the top unit is also presented in Fig. 3.

2.4 *Topology for AC applications*

The topology of an *M*-level (*M* = 11) capacitor voltage natural balancing multilevel converter utilized as an SVG is shown in Fig. 4. There are two parts in this converter, the positive part and the negative part, and both of them are based on the topology in Fig. 1 (*c*). Each part has *N* units (*N*=5 in Fig. 4) and two arms. The output voltages of the converter are u_{OL} and u_{OR}. Only half of the output current of the converter flows through each arm. Thus this topology is suitable for large power applications.

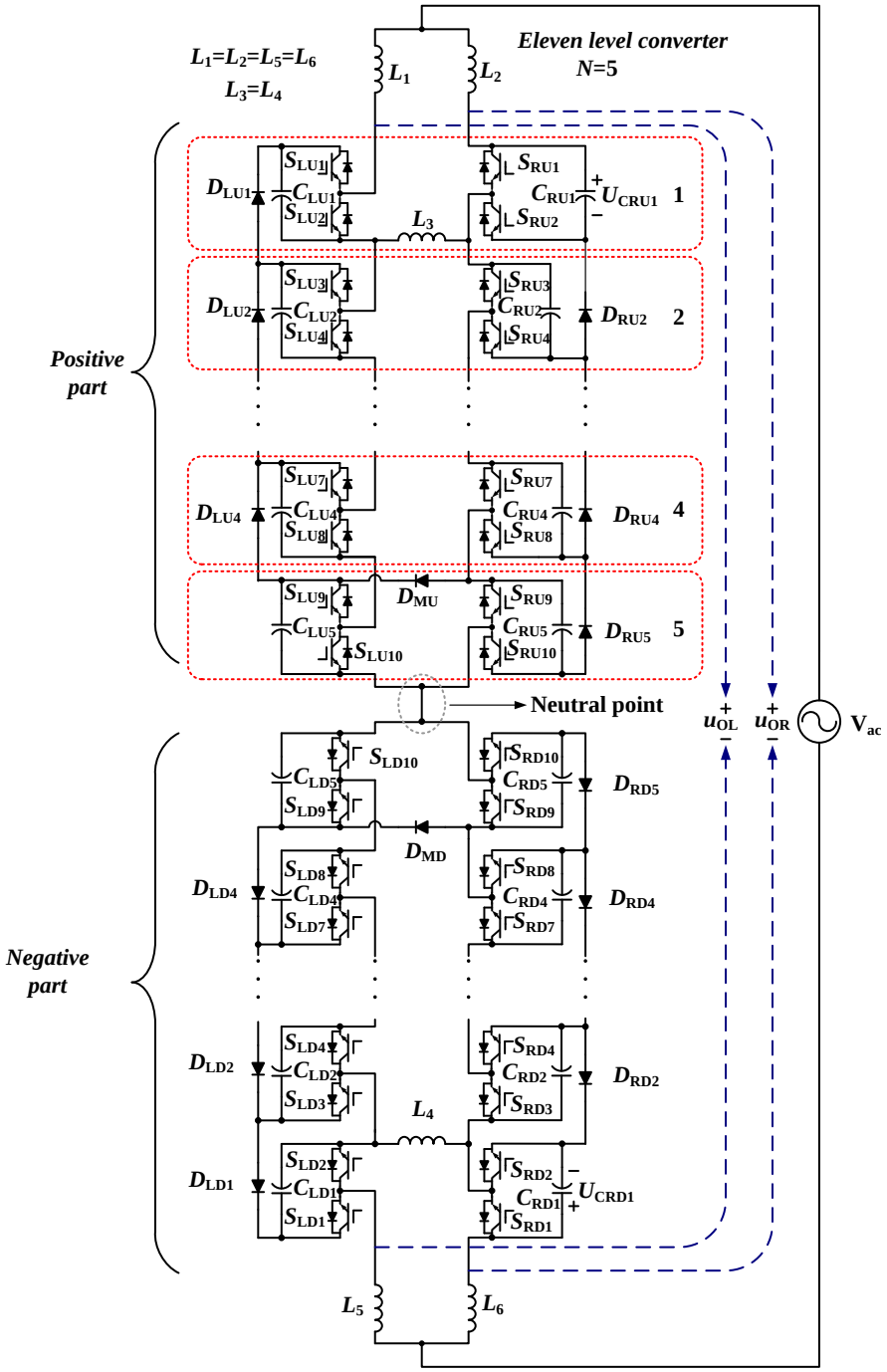


Fig. 4. Topology of capacitor voltage natural balancing multilevel converter

Considering the requirement of voltage clamping, fast diode is necessary. Besides that, a small rating inductor can be connected to each diode in series in order to limit the current pulse during the recovery from a serious unbalance of capacitor voltages.

3. Pulse Width Modulation and Control

3.1 Phase shifted pulse width modulation method

The topology of a unit in this proposed converter is shown in Fig. 5(*a*). The output voltage of the left sub-module is u_{Lj}, and u_{Rj} is the voltage of the right sub-module. Table 1 lists the relationship between the unit output and the switch states.

Table 1. Relationship between the output and the switch states of a unit

No.	$S_{\mathrm{L}k}$	$S_{\mathrm{L}k+1}$	$S_{\mathrm{R}k}$	$S_{\mathrm{R}k+1}$	$u_{\mathrm{L}j}$	$u_{\mathrm{R}j}$
1	0	1	0	1	0	$U_{\mathrm{CR}j}$
2	1	0	0	1	$U_{\mathrm{CL}j}$	$U_{\mathrm{CR}j}$
3	0	1	1	0	0	0
4	1	0	1	0	$U_{\mathrm{CL}j}$	0

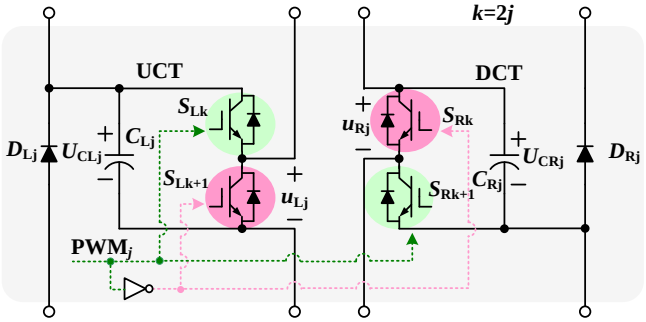
Since the two arms in the converter are symmetrical, the states of Nos. 2 and 3 (in Table 2) are selected in the switch modulation strategy. $S_{\mathrm{L}k}$ and $S_{\mathrm{R}k+1}$ are triggered by the same PWM signal which is interlocked with that used to trigger $S_{\mathrm{L}k}$ and $S_{\mathrm{R}k+1}$ (Fig. 5 (*a*)).

The PS-PWM (Phase shifted pulse width modulation) [23] is applied in this converter. Fig. 5 (*a*) and (*b*) show the principle of PS-PWM (N=3). v_{ref} is the

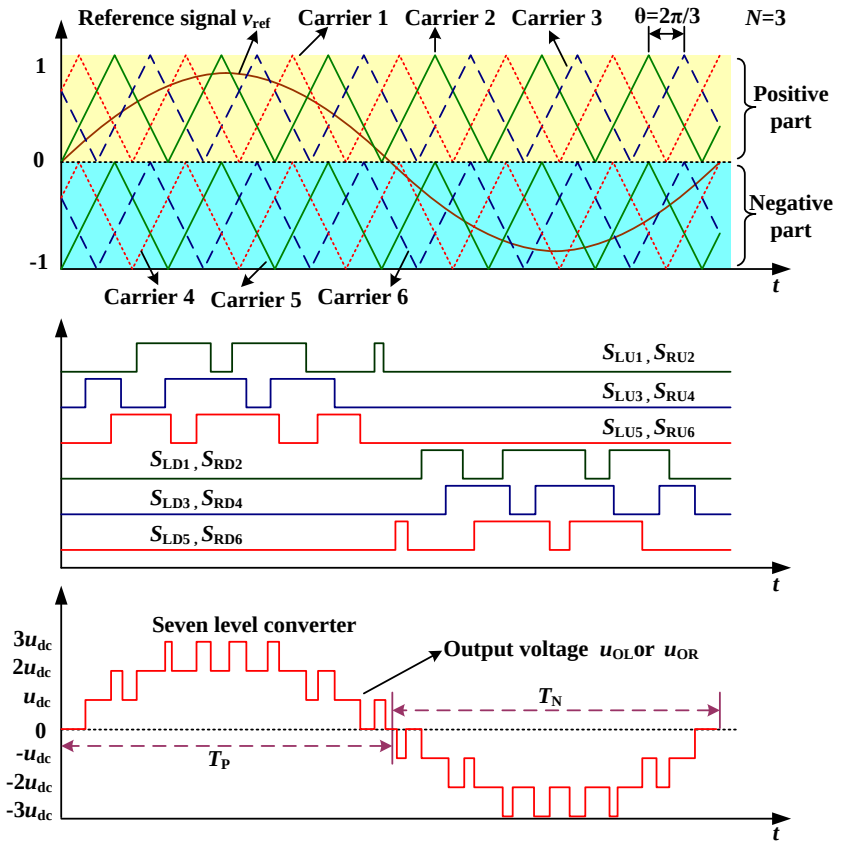
reference signal, and there are six triangular carriers. The phase shift θ between consecutive carriers is

$$\theta = 2\pi/N \tag{8}$$

During the modulating process, when v_{ref} is higher than the carrier, S_{Lk} and S_{Rk+1} are switched on, while S_{Lk+1} and S_{Rk} are switched off. If v_{ref} is lower than the carrier, S_{Lk+1} and S_{Rk} are switched on, while S_{Lk} and S_{Rk+1} are switched off. With the PS-PWM, the converter output voltage u_{OL} or u_{OR} is shown in Fig. 5 (*b*) (N=3). u_{dc} is the capacitor voltage in each sub-module when the capacitor voltages are all balanced.



(*a*)



(*b*)

Fig. 5. Principle of the PS-PWM for the converter

3.2 Control method of the proposed converter applied as a single phase SVG

The proposed converter can be directly connected to the grid without a transformer. With the advantage of capacitor voltage natural balancing the control of the converter can be simplified significantly. The dc-link voltage control algorithm is as simple as that of a two-level converter. Furthermore, much fewer voltage sensors are required to measure the capacitor voltage in this proposed converter. Thus, only the gate driving circuit is required in a sub-module. By contrast, in the traditional MMC, capacitor voltage control has to be used for each sub-module, resulting in a high computational cost. Moreover, each sub-module requires a voltage sensor, a measuring circuit (e.g. A/D converter) and a controller.

Fig. 6 shows the proposed control method for the converter which is applied as a single-phase SVG. The system control mainly consists of a single-phase PLL (Phase Lock Loop), a reactive current detector, a current controller, a capacitor voltage controller and a PWM generator. A voltage sensor is used to measure the grid voltage (u_{Line}) and the PLL will compute the line voltage phase (ωt). The reactive current (i_{Qref}) is detected with the instantaneous reactive power theory.

The line current (i_{Line}) is used in the reactive current detection, and the closed-loop reactive power compensation control is realized by using a PI controller. Besides that, two voltage sensors are used to measure the capacitor voltages in the positive part and the negative part, respectively. Since the capacitor voltages are self-balanced in the proposed converter, only one sub-module in each part of the converter needs to be controlled and the voltage sensor can be placed in any sub-module of one arm. The capacitor voltage control scheme is shown in Fig. 6 (*b*). For simplicity two voltage sensors are placed in the top unit and the bottom unit respectively to measure U_{CRU1} and U_{CRD1} for the capacitor voltage control.

There are two parts in the capacitor voltage control, one for the positive part and the other for the negative part of the converter. The control of two parts should be decoupled. An idea of time-sharing control in Fig. 6 (*b*) is presented. The current $\boldsymbol{I}_{\mathrm{SVG}}$ is controlled by regulating the output voltage $\boldsymbol{U}_{\mathrm{SVG}}$ of the SVG as follows,

$$\boldsymbol{I}_{SVG} = \frac{\boldsymbol{U}_{SVG} - \boldsymbol{U}_{Line}}{X_L} = \frac{\Delta \boldsymbol{U}}{X_L} \tag{9}$$

where, X_L is the inductive impedance of the inductor of SVG.

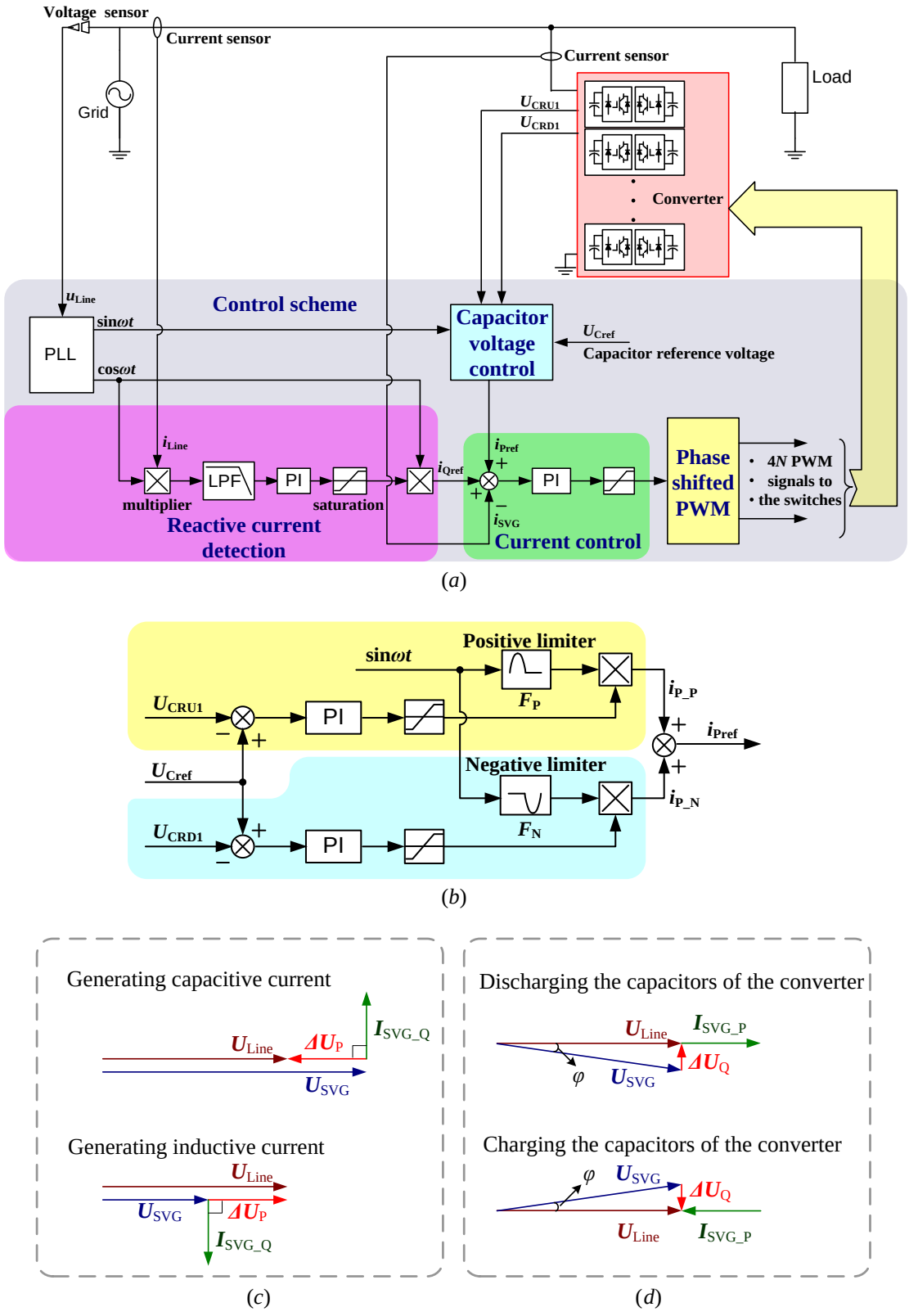


Fig. 6. Control principles: (*a*) system control scheme (SVG), (*b*) capacitor voltage control scheme, (*c*) vector diagram of the reactive current control, (*d*) vector diagram of the active current control

The analysis of SVG current control is shown in Fig. 6 (*c*) ~ (*d*). The angle φ between $\boldsymbol{U}_{\mathbf{SVG}}$ and $\boldsymbol{U}_{\mathbf{Line}}$ is only affected by the active component $\boldsymbol{I}_{\mathbf{SVG\_P}}$ of $\boldsymbol{I}_{\mathbf{SVG}}$, and $\boldsymbol{I}_{\mathbf{SVG\_P}}$ is much smaller than the rating current of SVG. Therefore, in most time of the positive half-line-cycle (0~π), the output voltage of SVG is positive, and the output voltage of the negative part is almost zero. Conversely, the output voltage of SVG is negative in most time of the negative half-line-cycle (π~2π), and the output voltage of the positive part is almost zero. Then the time-sharing control in Fig. 6 (*b*) can be described as: the capacitor voltage control of the positive part of SVG is enabled in the positive half-line-cycle and disabled in the negative half-line-cycle, while the control of the negative part is enabled in the negative half-line-cycle and disabled in the positive half-line-cycle. Two data limiters are used in the time-sharing control as follows：

$$F_P(x)=\begin{cases} x & (x>0) \\ 0 & (x\le 0) \end{cases} \tag{10}$$

$$F_N(x)=\begin{cases} x & (x<0) \\ 0 & (x\ge 0) \end{cases} \tag{11}$$

The proposed time-sharing capacitor voltage control consists of two PI regulators, two data limiters and two multipliers (Fig. 6 (*b*)). U_{CUR1} and U_{CDR1} are used for the capacitor control. The reference active current (i_{P_P}, i_{P_N}) is the product of the output of the PI regulator and the phase signal which is adjusted by the data limiter. The sum of i_{P_P} and i_{P_N} is the reference active current i_{Pref}. The sum of the reference reactive current i_{Qref} and i_{Pref} is the reference current i_{SVG}. Another PI regulator is used to control the current of the SVG, and the pulse width modulation method is the PS-PWM as described above.

4. Simulations and Experiments

The power circuit of the SVG based on the proposed multilevel converter (Fig. 4) has been simulated, where a laboratory prototype has been also implemented for experimental validation.

4.1 Simulations

Simulations were carried out using PSIM and the specifications and parameters of the multilevel SVG are listed in Table 2. The number of units in the converter is 10. Specifically, there are 5 units in the positive part of SVG and another 5 units in the negative part. Each unit consists of two sub-modules. The reference dc-link voltage of each sub-module is 1 kV. The control strategy shown in Fig. 6 is used for the simulations.

Table 2. Specifications and parameters used for simulations

Parameters	***Symbol***	***Rating***
Line voltage	u_{Line}	3 kV(RMS)
SVG capacity	S_{SVG}	425 kVA
Number of units in the converter	$2N$	10
Capacitance in each sub-module	C	4.7 mF
Dc-link voltage of each sub-module	U_{Cref}	1 kV
Inductors	L_1, L_2, L_5, L_6	1 mH
Auxiliary inductor	L_3, L_4	0.3 mH
Switching frequency	F_s	5 kHz

With the PWM strategy shown in Fig. 5, an eleven-level SVG was simulated. The simulation results of the output voltages u_{OL} and u_{OR} are shown in Fig. 7 (*a*). The bottom curve in Fig. 7 (*a*) is the reference signal for PWM and the modulation index is 0.9.

The initial capacitor voltage of each sub-module is 1 kV. The load is inductive with inductance of 70 mH and resistance of 1 Ω. The simulation lasts for 0.6 s. At 0.2 s, the reactive current compensation function of the SVG is enabled. The waveforms of the grid voltage u_{Line}, current i_{Line}, the output current of SVG i_{SVG} and the load current i_{Load} are presented in Fig. 7(*b*).

The simulations of inductor currents (i_{L1}, i_{L2}) are presented in Fig. 7(*c*). i_{L1} and i_{L2} are almost the same and are equal to half of i_{SVG}.

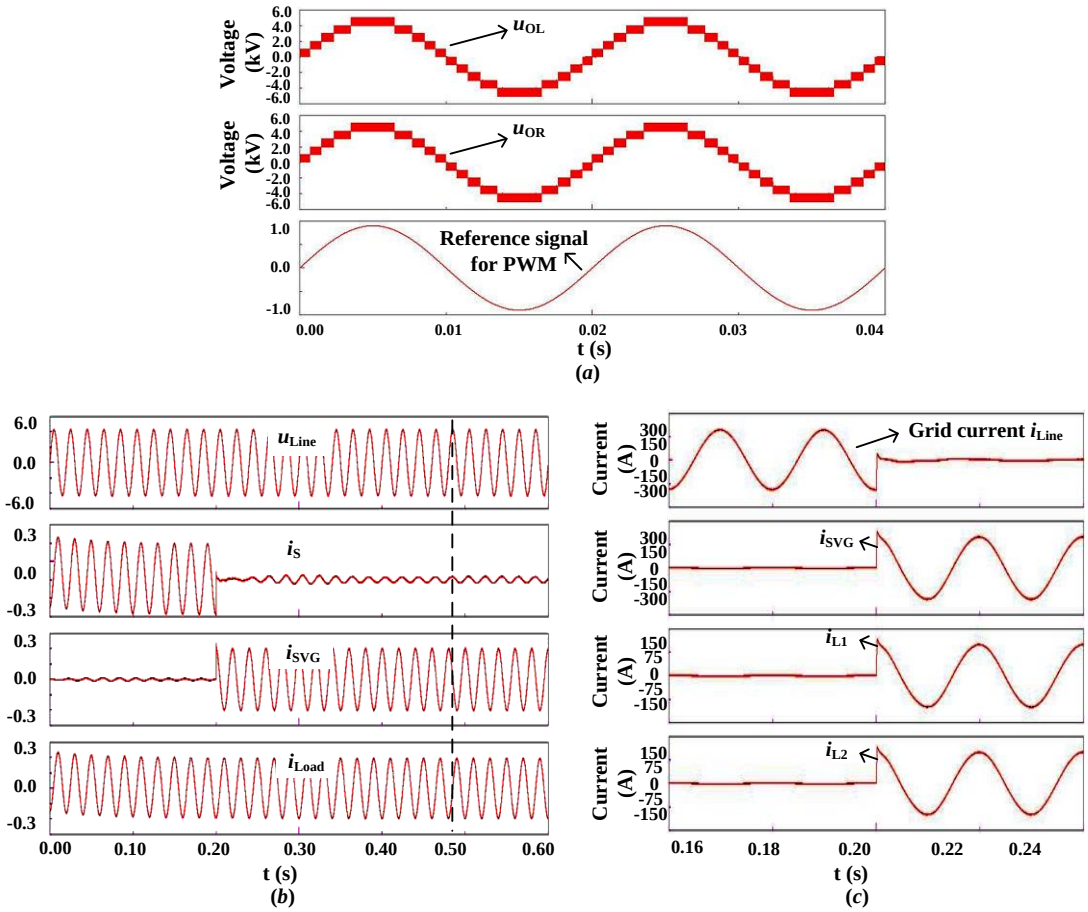


Fig. 7. Simulations of the eleven-level SVG: (*a*) output voltages of the eleven-level multilevel converter, (*b*) reactive current compensation simulation, and (*c*) simulation of currents of the inductors i_{L1}, i_{L2} in the SVG

In applications, the loss difference, the leakage current difference, the time delay of the gate driving pulse signals, the PWM strategy and so on could affect the capacitor voltage balance. In order to simulate the voltage unbalance of the capacitors, a discharging resistor is connected to the capacitor in parallel in each sub-module. The different discharging power was simulated by using different rating resistors, of which the parameters are listed in Table 3. The discharging power P_{loss} is

$$P_{loss} = i_R U_C = \frac{U_C^2}{R} \tag{12}$$

Table 3. Parameters of the discharging resistors.

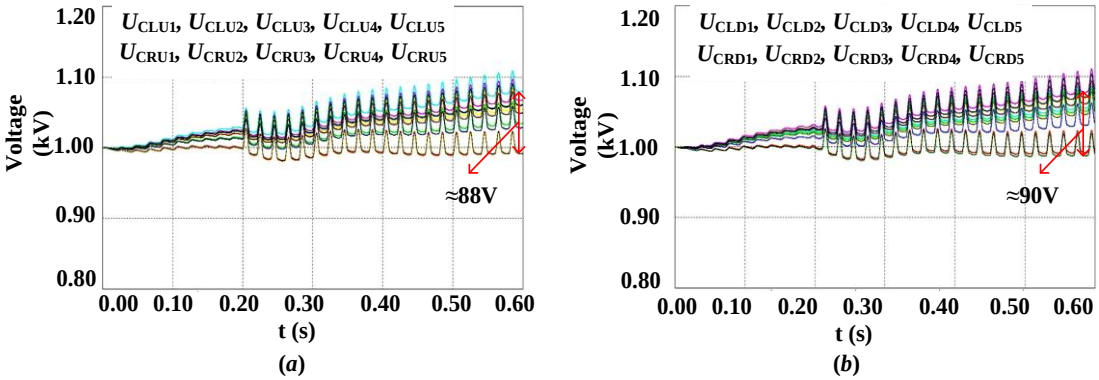
Symbol	***Rating***	***Symbol***	***Rating***
R_{LU1}	2 kΩ	R_{RU1}	3.5 kΩ
R_{LU2}	2.5 kΩ	R_{RU2}	2.0 kΩ
R_{LU3}	1.5 kΩ	R_{RU3}	2.5 kΩ
R_{LU4}	2.2 kΩ	R_{RU4}	1.5 kΩ
R_{LU5}	1.0 kΩ	R_{RU5}	1.0 kΩ
R_{LD1}	2.8 kΩ	R_{RD1}	2.5 kΩ
R_{LD2}	3.5 kΩ	R_{RD2}	2.8 kΩ
R_{LD3}	2.0 kΩ	R_{RD3}	1.0 kΩ
R_{LD4}	1.5 kΩ	R_{RD4}	3.0 kΩ

R_{LD5}	1.0 kΩ	R_{RD5}	2.0 kΩ

Note: The denotation of the subscripts is the same as that of the capacitors in Fig. 4.

For comparison, the simulation of the capacitor voltages in the eleven-level SVG without clamping diodes and auxiliary inductor (L_3, L_4) was carried out and the results are shown in Fig. 8 (*a*) ~ (*b*). The initial voltage for all capacitors was 1 kV but the voltages became unbalanced quickly. The maximum voltage difference reached about 88 V at 0.6 s in the positive part of the converter in Fig. 8 (*a*). The voltages of the capacitors in the negative part of the converter exhibited similar variations in Fig. 8 (*b*). Without specialized capacitor voltage control, the voltage unbalance would become so serious that the SVG would not work properly.

Then, the SVG based on the proposed topology was simulated where the discharging resistors listed in Table 3 were also used. The results are shown in Fig. 8 (*c*) ~ (*d*). The maximum voltage difference in all the sub-modules was no more than 8 V. With the new topology, the voltage balance is realized and it is rarely affected by the current of SVG.



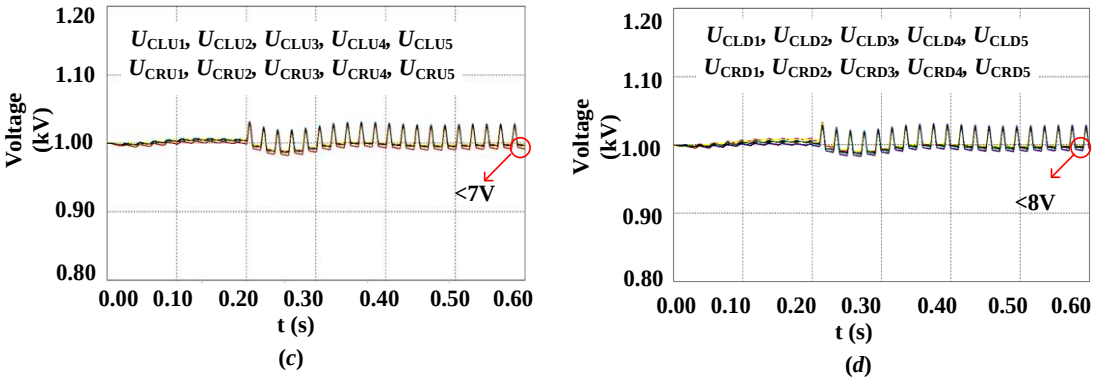


Fig. 8. Simulation results of the capacitor voltages: (*a*) ~ (*b*) converter without clamping diodes, (*c*) ~ (*d*) converter with clamping diodes.

The simulation results show that the proposed multilevel converter topology is capable of balancing the capacitor voltage effectively.

4.2 Experiments

A laboratory prototype was implemented with the topology in Fig. 4 where N=3. The prototype parameters are listed in Table 4. There are six units in this seven-level converter. The line voltage is 120 V (RMS) and the electrolytic capacitors with the rating voltage of 100 V are used as the dc-link capacitors in each sub-module. The capacitor reference voltage is 65 V. The power switches are IRF640 (International Rectifier Company) and the diodes are FR307. Hardware setup of the prototype for the experimental work is shown in Fig. 9. The control unit is designed with DSP (TMS320F28335, Texas Instruments) and FPGA (EP4CE22F17I7N, Altera). The PWM method shown in Fig. 5 is implemented in the FPGA which sends the PWM signals to the gate driving circuit with isolation. The control strategy presented in Fig. 6 is uploaded in the DSP where the PWM duty cycle is calculated, and the calculation result is sent to FPGA. One voltage sensor is used to measure the line voltage. Only

two voltage sensors are used to measure the capacitor voltage U_{CRU1} and U_{CRU1} respectively.

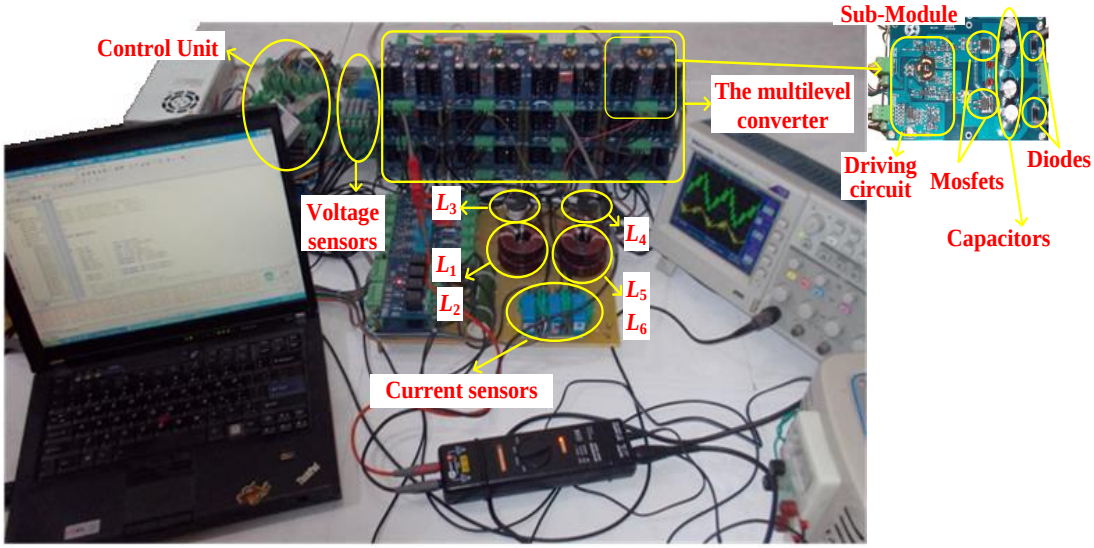


Fig. 9. The laboratory prototype

Table 4. Parameters of the prototype

Parameters	***Symbol***	***Rating***
Line voltage	u_{Line}	120 V (RMS)
SVG capacity	S_{SVG}	1200 VA
Number of units in the converter	$2N$	6
Capacitor	C	4.0 mF
Dc-link voltage	U_{Cref}	65 V
Inductors	L_1, L_2, L_5, L_6	2.1 mH
Auxiliary inductor	L_3, L_4	0.32 mH
Switch	S	IRF640 (18 A/200 V)
Clamping Diode	D	FR307 (3 A/1000 V)

Switching frequency	F_s	10 kHz
Control ICs	DSP, FPGA	TMS320F28335, EP4CE22F17I7N

The experiment results of the output voltages of the converter are shown in Fig. 10 (*a*). With the PS-PWM method in Fig. 5, u_{OL} and u_{OR} are the seven-level voltage. Fig. 10 (*b*) presents the line voltage u_{Line} and the current i_{SVG} of the SVG. The output current is capacitive and its amplitude is about 10 A. Because the PS-PWM strategy is used, the current ripples are suppressed effectively. The currents (i_{L1}, i_{L2}) of the two arms in the positive part of the SVG are presented in Fig. 10 (*c*). The amplitude of i_{L1} and i_{L2} is about 5 A. The currents of the two arms are balanced naturally.

The capacitor voltages of the converter are shown in Fig. 11. Fig. 11 (*a*) and (*b*) demonstrates the capacitor voltages of the left and right arms respectively in the positive part of the SVG, while Fig. 11 (*c*) and (*d*) presents the voltages in the negative part. All the capacitor voltages are balanced and the maximum difference between them is less than 3 V. The experimental results are well aligned with the simulation ones.

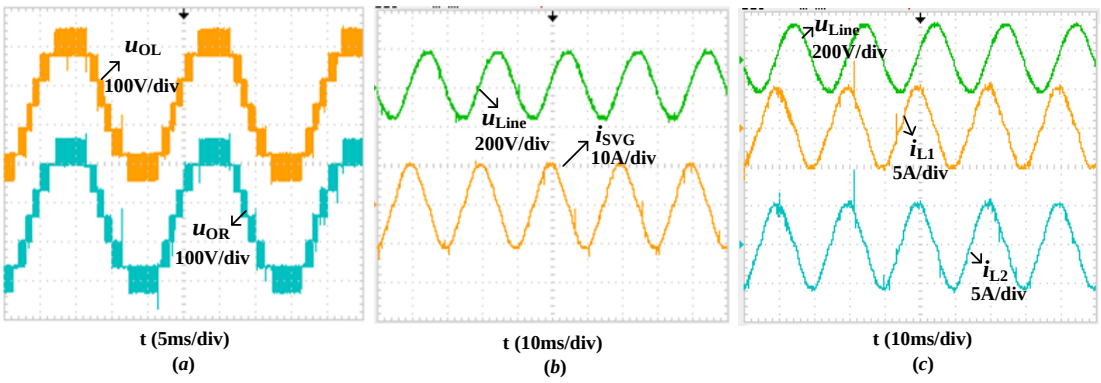


Fig. 10. Experiment results of the proposed seven-level SVG: (*a*) output voltage of the seven-level SVG, (*b*) output current of the seven-level SVG, (*c*) currents of the two arms of the positive part in the converter

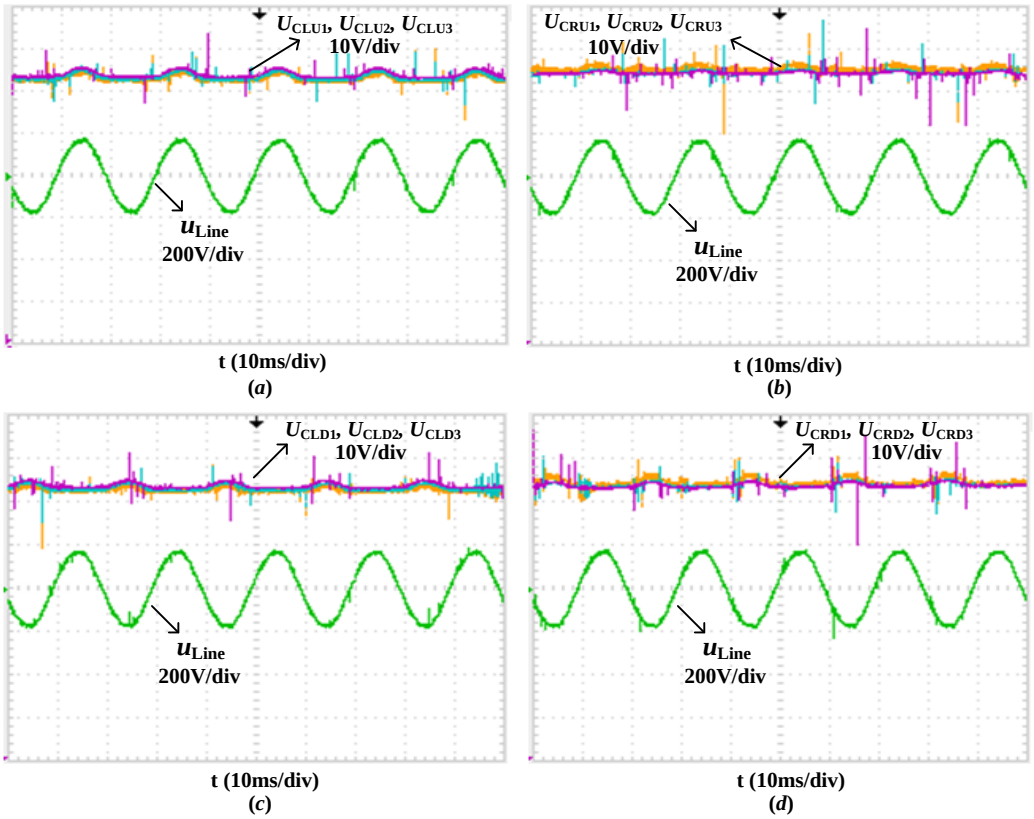


Fig. 11. Capacitor voltages of the seven-level SVG

In Fig. 12, the dynamic balancing process of capacitor voltage is presented. The initial voltages of the left arm in the positive part of the converter were 47, 58 and 62 V, respectively, for U_{CLU3}, U_{CLU1} and U_{CLU2} in Fig. 12 (*a*). The SVG was started at t^* and the capacitor voltages were quickly balanced. Fig. 12 (*b*) demonstrates the balancing process of the capacitor voltage of the right arm.

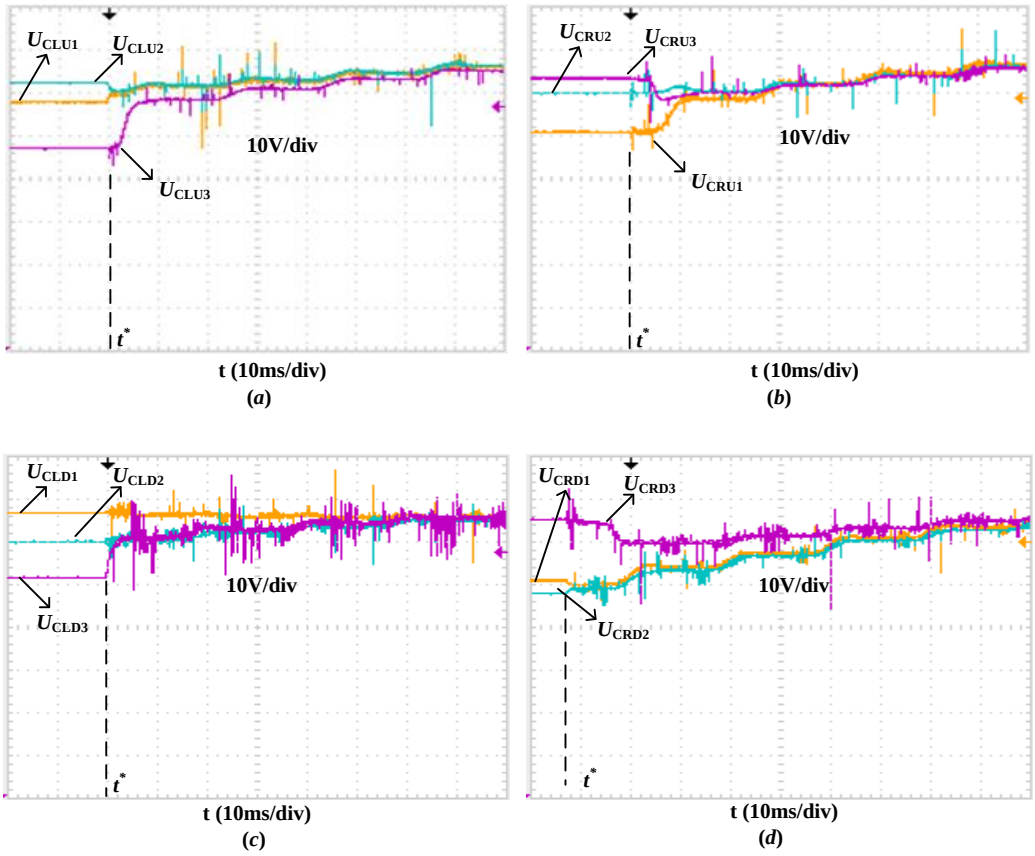


Fig. 12. Dynamic balancing process of the capacitor voltage

5. Conclusions

A novel multilevel converter topology has been proposed in this paper. The capacitor voltage self-balancing is achieved in this topology by using small power rating clamping diodes and a parallel structure consisting of an upward clamping arm and a downward clamping arm. No extra auxiliary circuits are required in this topology. The capacitor voltage control of the proposed topology is as simple as that of a two-level converter and the control computational cost is reduced greatly. The capacitor voltage balancing is independent from the output current of the converter, and only two voltage sensors are required to control the capacitor voltage, much less than that of the traditional MMC. The PS-PWM method and the control proposed in the paper are both effective.

The proposed converter topology is suitable for high power and high voltage applications, such as medium-voltage SVG, medium-voltage APF, HVDC and high voltage motor drive.

6. Acknowledgement

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7. References

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