Design of deep-nanometer-scale capacitors and associated materials challenges

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Abstract

The International Technology Roadmap for Semiconductors (ITRS) projects that the spatial resolution of features in integrated circuits will eventually be well at nanoscopic dimensions. As a result, there is, presently, an active interest in the design of nano-scale circuit elements such as transistors, resistors, and "capacitors". As with all circuit elements, the materials for fabrication of nano-scale capacitors are an important factor. We analyse these requirements for engineering nanoscopic capacitors, and show that, at deep-nanometer-scales, dielectric properties such as dielectric constant, dielectric strength, and dielectric relaxation determine the practicality of such capacitors. These properties, in turn, are closely linked to the structure, purity, method of fabrication, and dimensions of the capacitor components and materials.

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1. Introduction

The resolution of lithography used for very large-scale integrated circuit (IC) fabrication has followed Moore's law consistently since 1970, and the ITRS since 1992 [1], and is fast approaching 90nm as projected. The current commercial state-of-the-art is 125nm, attained using deep-ultra-violet (DUV) lithography at λ = 193nm [2]. The capacitor is one of the four fundamental circuit elements required to design a functional and feasible nano-scale IC, and is a critical component in electronic circuits [3], [4]. Increasing IC densities will drive component sizes to deep-nanometer-scales and the capacitor is no exception.

There are several conceptual architectures capable of storing sufficient charge at the nano-scale, such as individual metallic clusters [5], large molecules, electrolytic charged double layers [6], nano-wires and nano-tubes, interdigital or fractal-like arrangements [7], and of course parallel-plates. In this paper we present the critical material properties that would determine the practicality of such capacitors, and use a parallel-plate capacitor as a basis to do so, for simplicity.

2. Design of nano-scale parallel-plate capacitors

The capacitors we consider here consist of two disk-shaped electrodes separated by a thin layer of dielectric. We deliberately omit discussing the leads of the capacitor, as here we are interested in the properties mentioned above. For a classical macroscopic parallel-plate capacitor, the capacitance is given by

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d} \qquad (1)$$

and the electrical potential energy stored by

$$U_e = \frac{1}{2} C(\Delta v)^2 . \qquad (2)$$

We can use expressions (1), (2), and associated electrostatic equations, correctly at nano-scales because electrostatic phenomena can be considered scale invariant [7]. We note that at these dimensions, the quantised nature of charge, and stored electrical energy, becomes apparent. Our capacitors are at least a few hundred atoms in size. Hence we can assume that a mobile single electron (hole) will appear delocalised about an electrode because the Fermi-velocity of electrons (holes) in a conductor is very high (~10^6m/s) relative to the polarization angular velocity of the dielectric dipoles. So even a single electron (hole) will appear, relative to the dielectric, as a charge density distribution rather than a point charge.

Evaluating for a parallel-plate capacitor fabricated with focused ion-beam (FIB) lithography, using SiO_2 as a dielectric (ε_r = 3.9), a plate radius, r = 1nm, and dielectric thickness, d = 0.5nm, we can obtain a capacitance of ~$0.22 \cdot 10^{-18}$F (or 0.22aF). The potential difference produced across the capacitor due to one stored electron is given by

$$\Delta v = \frac{q}{C} \qquad (3)$$

and is ~0.73VDC. The stored electrical energy of this capacitor is therefore ~0.36eV. However, being mindful of our emphasis of the scale-invariance of electrostatics, the electric field produced by this configuration is ~1.46GV/m (14.6MV/cm) and is at the threshold, or exceeds, the dielectric strength of currently known dielectrics. Hence a single electron is all that could be stored in such a nano-scale (quantum) capacitor: a single-electron capacitor (SEC).

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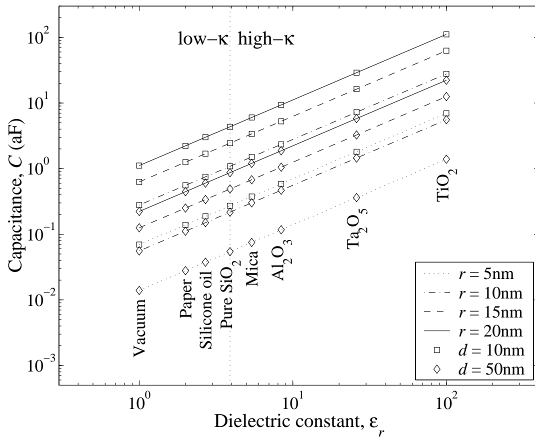

Fig. 1 Capacitance of a parallel-plate capacitor as a function of dielectric constant ε_r, dielectric radius r (nm), and dielectric thickness d (nm), fabricable with modern focused ion-beam (FIB) lithography. The perforated line distinguishes low-κ dielectrics from high-κ dielectrics.

3. Dielectric properties

1.1. Dielectric constant

The dielectric constant is a critical parameter in nano-scale capacitor design, as evident from Fig. 1, and, is the only parameter we can manipulate to vary the capacitance, independent of architecture. Dielectrics must have ε_r on the order of 4 to 10^4 (high-κ) to implement feasible nano-scale capacitors. Although using high-κ dielectrics can readily increase capacitance, consequent problems such as lower dielectric strength, and higher loss factor and heat absorption of such materials prevent their use. This renders the design of systems containing such capacitors challenging, hence low-κ dielectrics are currently, and widely, favoured. We have considered some primary dielectrics for nano-scale capacitor design, which are Ta_2O_5, certain ceramics, glass, polymers, and titanates (of Ba, Ca, Mg, Pb, Sr). The selection of these dielectrics is further constrained by their ability to be deposited on substrates using currently available techniques of epitaxy and lithography.

1.2. Dielectric strength

The dielectric strength, $\mathbf{E_{BD}}$, is another factor that is currently not understood in sufficient detail, however is a critical material property in the design of nano-scale capacitors. The $\mathbf{E_{BD}}$ of most bulk ceramics is listed as only 1.5 to 15MV/m [8], [9] but that of defect free dielectric thin-films is usually considered to be as high as 1GV/m (10MV/cm) [10].

The dependence of $\mathbf{E_{BD}}$ on thickness is a known phenomenon [11], [12] referred to as the "thickness effect" [13], but it appears to have not been investigated in sufficient detail. This effect shows that in thin-film dielectrics individual defects don't occur in sufficient density to cause correlated and coordinated electrical breakdown [14]. Furthermore, for dielectric thicknesses smaller than the electron mean free path, on the order of a few nanometers [15], consecutive electron-atom impact-ionisations that can avalanche have considerably lower probability of occurring, dramatically increasing the dielectric strength of the thin-film material. This allows nanoscopic thin-films to be subjected to considerably greater electric fields than macroscopic sheets of the same material with the same crystallography. The thickness effect is expressed as [13]

$$\mathbf{E_{BD}} = E_0 d^{-y} \tag{4}$$

where E_0 is the constant of proportionality, and $3 \leq y \leq 4$. Using a macroscopic dielectric with breakdown voltage of 380VDC applied over a SiO_2 dielectric of 950nm thickness [7], we can get a coefficient of proportionality of

$$E_0 = \mathbf{E_{BD}} / d^{-0.35} \approx 3.12 \cdot 10^6 \tag{5}$$

where $\mathbf{E_{BD}}$ is in MV/m and d is in m. Equations (4) and (5) predicts that the $\mathbf{E_{BD}}$ of a 1mm film of pure SiO_2 could be ~35MV/m, while that of a 1nm layer could be as high as ~4.41GV/m. This is an approximation of the thickness effect, but explains how it will be possible to operate nano-scale capacitors at higher electric fields than observed in those using macroscopic dielectrics.

1.3. Large band-gap dielectrics and breakdown

Increasing the band-gap of the dielectric also contributes to increasing the dielectric strength of a material. Avalanche breakdown occurs when electrons in the occupied valence band receives sufficient energy to move to the empty conduction band [13]. Hence the larger the band-gap the higher the electric field strength required to move an electron to the conduction band, hence the higher the dielectric strength. However, intrinsic breakdown can occur if, *inter alia,* electrons accumulate in the empty conduction band by tunnelling from the occupied valence band, under an applied electric field [13]. This also occurs due to ion production through electron-atom collisions, and impurity induced charge traps and defect sites.

1.4. Dielectric relaxation

Dielectric relaxation (absorption) is a fundamental limitation in high precision applications based on charging and discharging capacitors, such as sample-and-hold circuits, integrators, analog-to-digital and digital-to-analog converters, high-Q circuits such as voltage controlled oscillators (VCOs), and active filters [16-18]. Particularly in analog-to-digital converters consisting of sample-and-hold circuits, dielectric relaxation can dramatically hinder dynamic range [17].

A symptom of dielectric relaxation is the propensity of a capacitor to regain a percentage of its original charge after a momentary short-circuit of its terminals [17]. The amount of dielectric relaxation a capacitor exhibits is a highly dependent function of the dielectric material. Silicon dioxide exhibits about 0.1% dielectric relaxation, placing its performance in the middle of the dielectric candidate set [16], [19], [20]. Fig. 2 illustrates the basic electrical model of dielectric relaxation.

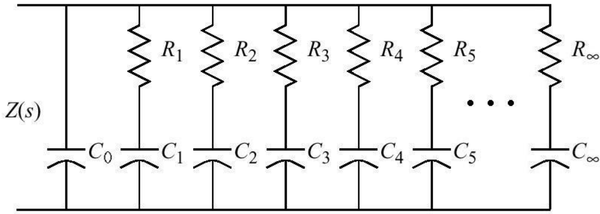

Fig. 2 The basic model for dielectric relaxation in a capacitor [16], [18].

In Fig. 2, each series RC-pair, connected in parallel with the main capacitance, C_0, contributes to a time constant. As the terminals momentarily short-circuit, C_0 discharges completely but the absorptive R_nC_n-pairs discharge relative to their time constants. Once the circuit opens, residual charge stored in the R_nC_n-pairs trickles into C_0 over time to recharge C_0 to a percentage of its original charge. The capacitances, C_n, in these RC-pairs have very small values hence don't store as much charge as C_0. This is the reason for a small percentage rise in potential difference rather than a recharge close to the original potential difference of C_0.

Table 1 Example data for model of Fig. 2 with n = 5 [16].

n	R_n (GΩ)	C_n (pF)	C_n/C_0	R_nC_0	$\tau_n = R_nC_n$ (s)
0	0	10^6	1	0	0
1	3600	140	$1.4\cdot10^{-4}$	$3.6\cdot10^6$	500
2	250	200	$2.0\cdot10^{-4}$	$2.5\cdot10^5$	50
3	20	270	$2.7\cdot10^{-4}$	$2.0\cdot10^4$	5.4
4	3	190	$1.9\cdot10^{-4}$	$3.0\cdot10^3$	0.58
5	0.33	120	$1.2\cdot10^{-4}$	$3.3\cdot10^2$	0.04

As shown in Table 1, the time constants reduce as n increases, causing the resonant frequency of the nth RC network to increase. Also note that dielectric relaxation has an inherent dissipative and memory effect as modelled by the resistances and capacitances of Fig. 2, respectively. It is the wide range of time constants that causes the memory and dissipative effects of dielectric relaxation to manifest in a capacitor's entire operating frequency band [16].

Dielectric relaxation electromigration of low mobility defects, such as protons and vacant sites, which are displaced towards either electrode by an applied electric field and drift back to an equilibrium distribution when the electric field is removed. The return to equilibrium may be hastened by an increase in temperature so that sizeable discharge may occur on heating specimens that have been subjected to electric fields for a prolonged period [13].

4. Materials for electrodes

Since the overall dimensions of the capacitor are expected to be nanoscopic, there are interesting implications for the metal electrodes as well. If we assume that the capacitor is comprised of two parallel-plates, of radius r and thickness d, and the plates are fabricated from Au atoms nominally packed at 70% density, it can be shown the number of Au atoms per plate electrode is

$$n_{Au} \approx 176 r^2 d \qquad (6)$$

where, for convenience both r and d are in nm. Hence a Au electrode, with a nominal radius of 1nm, a plate thickness of 0.5nm, is composed of 88 atoms. This electrode is sufficiently small that its physical properties are different to those of macroscopic structures. It is expected the melting point of such a plate will be reduced by about 200°K due to its size alone [21]. As a result, the plate material behaves as if the temperature is much higher than it actually is, producing increased diffusion at hetero-interfaces, high mobility of surface atoms, and chemical reaction with the environment. This latter issue is a serious problem for metallic circuit components in the nano-scale domain, since even copper will be completely oxidised under equilibrium atmospheric conditions. This is the reason noble metals such as Au are such prominent materials for fabrication of proposed nano-scale electronic circuits; Au is the least likely of all metals to oxidise in such conditions, is a good conductor of electricity and heat, and is readily fabricable using electroplating and lithography techniques [22].

5. Operation at ultra-high frequencies

It is possible that circuits containing nano-scale capacitors will be operated at unprecedentedly high frequencies provided their self-resonant frequencies are much higher than the bandwidth of the circuit. The current state-of-the-art appears to offer capacitors with self-resonant frequencies as high as 40GHz [7] but there are future applications in which signals will have tera-Hertz and higher frequencies [23], [24] in which case the capacitors must also follow the same advances. Hence it is critical to analyse the frequency response of nano-scale capacitors, and their constituent materials. Given the importance of ε_r in determining capacitance, it therefore becomes paramount to consider the extent to which ε_r itself is influenced by frequency. The Cole-Cole model [25] for complex dielectric constant is

$$\varepsilon_r(\omega) = \varepsilon_H + \frac{\varepsilon_L - \varepsilon_H}{1 + (j\omega\tau_0)^{1-\alpha}}, \quad 0 \le \alpha \le 1 \qquad (7)$$

where α is the frequency constant, τ_0 is the charging time constant, ω the radian frequency, ε_L the low frequency dielectric constant, and ε_H the high frequency dielectric constant. Given (7), we can express the admittance of the capacitor as

$$Y(\omega) = s\left(C_H + \frac{C_L - C_H}{1 + (s\tau_0)^{1-\alpha}}\right)\Bigg|_{s=j\omega}, \quad 0 \le \alpha \le 1 \qquad (8)$$

where $Y(\omega)$ is the frequency response of the capacitor, C_L is the low frequency capacitance, C_H is the high frequency capacitance [16], [25]. The reason the dielectric constant of a material varies with frequency is, various mechanisms within the dielectric are excited at different frequencies [16], [26]. As an electric field impinges on a dielectric material, the charged particles (molecules, atomic nuclei, electrons) will rearrange themselves to align their dipole moments with the field. Fig. 3 illustrates these phenomena in better detail.

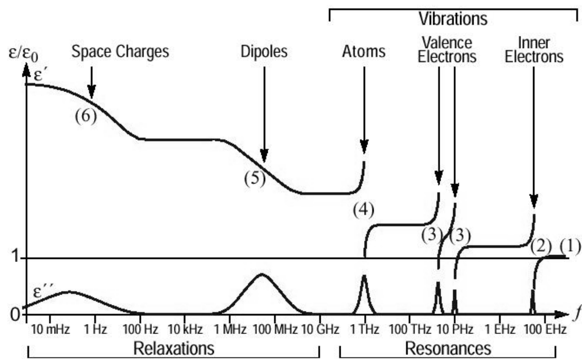

Fig. 3 Frequency response of complex dielectric constant, $\varepsilon_r(\omega) = \varepsilon' + j\varepsilon''$, of polar dielectrics [16].

Region (1) in Fig. 3 is in the X-ray and gamma radiation frequency range. At these frequencies there is no interaction between the material and the wave, hence $\varepsilon_r(\omega)$ is the same as that of free space, ε_0. As frequency of the alternating electric field decreases the inner electrons (2), the valence electrons (3), and eventually the atoms (4) themselves successively resonate and make their contributions [16]. As the frequency descends, polar molecules (5), which are in some materials electric domains, become excited and increase the $\varepsilon_r(\omega)$, greatly. For polar molecules this is called dipole relaxation, for electric domains it is ferroelectric relaxation. These two represent the mechanisms behind dielectric relaxation. The last process that affects $\varepsilon_r(\omega)$ is called space-charge relaxation (6). This is caused by charges that are free to move about but not to recombine at the electrodes. At low frequencies, these charges behave like macroscopic dipoles that reverse their direction each half period [16].

6. Conclusions

Nano-scale capacitors have potential application in the highly miniaturised ICs, and discrete devices of the future. We can envisage parallel-plate capacitances as minuscule as a few aF, designed or arranged in particular architectures if higher capacitances are desired. The performance of these hypothetical devices will be strongly controlled by the materials' properties used to make them. The maximum electrical energy that can be stored will depend on the values of ε_r and $\mathbf{E_{BD}}$, and seems to be of the order of several eV, with currently available materials. We have presented our analysis of some critical material properties that will affect the design and fabrication of such nanoscopic capacitors. We have also proposed the possibility of implementing a quantum capacitor (SEC) for advanced applications such as ultra-high density electrostatic memories, tera-Hertz and higher frequency antennae for continuous and pulsed electromagnetic communications, and capacitive arrays for high-efficiency macroscopic capacitors.

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