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RESEARCH ARTICLE

Optimized Interleaved Ultra-High Gain DC–DC Power Converter With Low Ripple Input Current and Voltage Stress for Fuel Cell Systems

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ABSTRACT This paper presents an ultra-high voltage gain power converter designed to address the challenges posed by the inherently low output voltage and high output current of fuel cell systems. The proposed converter features a two-stage integrated design, comprising a two-phase interleaved boost converter and a high-gain switched capacitor coupled inductor boost converter. The interleaved design divides the current equally between two phase legs, minimising conduction losses and enhancing efficiency. Additionally, this technique significantly reduces input current ripple, leading to lower fuel cell degradation and improved performance. The switched capacitors and coupled inductor in the high gain boost converter enhance the voltage gain while minimising voltage stress on the active switches and diodes. This approach enables the utilisation of low voltage rated switches and diodes, reducing costs and minimising conduction and switching losses. Additionally, the converter features a common input and output ground to mitigate electromagnetic interference and uses low-side switches to simplify gate circuitry and reduce costs. To validate the proposed design, a 500W prototype is developed and tested in a laboratory environment. The prototype achieves a peak efficiency of 95.52%, a peak-to-peak input current ripple of less than 1.5%, and a voltage gain of 27.8 at a 50% duty cycle.

INDEX TERMS DC-DC boost converter, coupled inductor, switched capacitor, ultra-high voltage gain, fuel cell, low input ripple current, interleaved boost converter.

I. INTRODUCTION

In recent years, the imperative to address climate change has intensified efforts towards developing and implementing renewable energy generation systems aiming to replace their fossil fuel-based counterparts [1]. In tandem with advancements in energy generation, significant attention has been given to developing clean energy storage systems to maximise the utilisation of energy harnessed from these renewable sources [2]. Fuel cells, when used as an energy storage system, offer the ability to store substantial quantities of renewable fuel, such as hydrogen, that contain a high power density and emit zero emissions [3], [4]. The versatile application of fuel cells is particularly advantageous in sectors such as transportation, remote micro-grid power supply, and auxiliary and backup power generation, where a high quantity of uninterrupted energy is required for extended time periods [5]. Fig. 1 illustrates the various applications of fuel cells.

Despite the advantages of fuel cell use in various applications, the inherent challenges of the low output voltage and high output current create difficulty when directly interfacing with loads or buses of varying voltage levels [6], [7]. The use of fuel cells can also greatly influence an electrical systems efficiency due to the high electrical losses caused by the fuel cells high output current [8]. The low output voltage and high output current is a result of the low voltage potential between cells within a fuel cell stack, typically between 0.6-0.8V per

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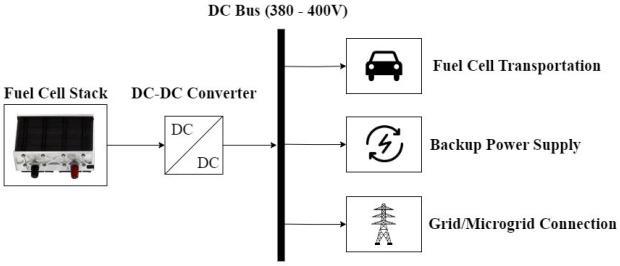


FIGURE 1. Fuel cell stack connection to various applications through DC-DC boost converter.

cell [9], [10]. To overcome the low cell potential, fuel cell systems contain stacks that are made up of many cells in series. Increasing the number of cells in a stack can, however, cause difficulties when attempting to control the fuel and oxidant flows, cell temperature, and cell humidification (for PEM systems), leading to a faster degradation of the fuel cell stack [8], [11]. One faulty cell within a series stack will also deem the stack inoperable, whilst a higher number of cells increases the overall cost of the system. Methods such as connecting multiple fuel cell stacks externally have been used to overcome issues when increasing the cell count per stack, however, if each stack is required to contain its own monitoring and control, the cost of the overall system can be greatly increased [6]. Load variations can also affect the fuel cells output voltage, therefore requiring the need for voltage controllers to maintain system voltage levels [12]. Fuel cells are also sensitive to variations in the current, and therefore require to be connected to systems with a low ripple DC current. Experiments by B. Wahdame et. al [13] have shown the negative effects of DC current with a high ripple content on fuel cell systems. The importance of a power converter with low input ripple current, and that can reach ultra-high voltage gains is therefore identified, since such a converter can minimise the cell count within the stack to prolong the fuel cell life and minimise costs, introduce voltage control to the fuel cell's output, and ultimately make the use of fuel cell systems more practical within modern society.

Various designs of DC-DC power converters have previously been proposed, each focusing on achieving specific goals for a diverse range of applications [6]. A typical DC-DC boost converter backbone utilised for fuel cell interconnection is the interleaved design, which has been used in [10], [14], [15], [16], [17], [18], [19], and [20]. Experiments in [10], [14], and [17] showed the benefit of using a high number of interleave phases to enhance efficiency and reduce input ripple current for high current applications. However, the interleave design can only produce voltage gains of up to two, and is therefore inappropriate for reaching ultra-high voltage gains. This problem has attempted to be overcome in [15], through the addition of voltage lift and multiplier cells into the conventional two-phase interleave converter. A significant increase in voltage gain was achieved for this design, although the requirement of adding lift and multiplier cells in each phase significantly increases the number of components required in the converter. Similar problems were encountered in [18] and [20] when adding multiplier cells and in [19] when adding coupled inductors and multiplier cells to increase the voltage gain. Quadratic boost topologies are also a popular design for significantly increasing voltage gain capabilities. The conventional quadratic boost converter and variations to this topology specifically designed for fuel cell applications have been proposed in [21], [22], [23], and [24]. Since a single inductor is directly connected to the input in these designs, a trade-off between converter efficiency and input ripple current occurs when attempting to size the input inductor. Other converter designs have also emphasised producing a wide input voltage range [25], [26], [27], enhanced efficiency through soft switching [28], [29], and utilisation of cascading [30], multiplier\lift cells and switched capacitors\inductors to enhance the voltage gain capabilities [31], [32], [33]. Although these converters possess merit for the purpose in which they were designed, none exhibit ultra-high voltage gain (>20) capabilities, with the highest experimental voltage gain recorded as 16.67 from [19]. Therefore, the need for an ultra-high gain converter designed specifically for fuel cells is made apparent.

Various methods for achieving high voltage gains have been extensively discussed in [34]. However, not all of these methods are suitable for fuel cell applications due to the unique requirements fuel cell systems possess. While the ultra-high gain converters presented in [35] and [36] may not be directly suitable for fuel cell systems, they demonstrate the advantages of integrating coupled inductor and switched capacitor techniques into designs to produce ultra-high voltage gains.

In light of these challenges, there arises a clear need for an ultra-high gain converter (>20) specifically tailored for fuel cells. This paper addresses this gap by proposing a novel converter design that effectively incorporates a two-phase interleaved boost converter with integrated switched capacitor and coupled inductor techniques. The proposed design aims to overcome the limitations observed in existing converters, providing a solution that enables an ultra-high voltage gain while maintaining efficiency and mitigating issues related to input ripple current.

The remainder of the paper is organised as follows: Section II describes the methodology for developing the proposed converter and its characteristics. Section III provides insight into the theoretical and simulation analysis of the proposed converter and details the procedure for the development of the prototype. Experimental analysis and results of the developed prototype are presented in Section IV. A comparison of performance with the proposed converter and other converters designed specifically for fuel cell systems is provided in Section V. Finally, Section VI provides conclusions about the design process and performance of the developed prototype.

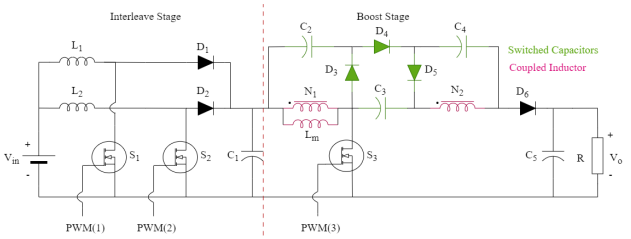


FIGURE 2. The proposed converter.

II. DESCRIPTION OF THE PROPOSED CONVERTER

The proposed converter is presented in Fig. 2, and employs a two-stage cascaded design, integrating interleaved techniques, as well as switched capacitors and coupled inductors. The interleaved design is chosen for its proven effectiveness in enhancing efficiency and minimising input ripple current for high output current fuel cells.

The interleave converters do, however, suffer from a limited duty cycle of 50%, decreasing the capabilities of reaching a high voltage gain. Integrating voltage lift and multiplier cells into interleave designs further raises the component count, as these cells are required in all phases of the interleaved design. Therefore, a cascaded design is chosen as an optimal alternative approach to keep the component count low, whilst retaining the ability to reach an ultra-high voltage gain. Since high currents are to be dealt with by the interleaving stage, the second stage is designed to optimise voltage gain and reduce voltage stress. A coupled inductor boost converter is chosen as a starting point to achieve this goal. Switched capacitors are then optimally incorporated into the coupled inductor boost converter design to efficiently utilise both switching cycles, resulting in the development of an efficient, high-gain converter.

The proposed converter, employing an optimised switched capacitor and coupled inductor configuration integrated with an interleaved technique, presents several distinctive advantages, particularly for fuel cell applications: 1) ultra-high voltage gain, 2) low input current ripple, 3) high efficiency, 4) low voltage stress on active switches, 5) common ground between input and output and potentially low electromagnetic interference issues, and 6) simplified gate drive circuit requirements.

III. THEORETICAL ANALYSIS

A. CONVERTER OPERATIONAL PRINCIPLE

There are two switch cycles, corresponding to switching modes I and II, as shown in Fig. 3(a) and Fig. 3(b), respectively. During switch mode I, inductor L_1 and the coupled inductor are discharged along with capacitor C_3, to supply the load at the output voltage, V_o. Capacitors C_2, C_4, and C_5 are charged to their corresponding voltage levels through the forward biasing of diodes D_3, D_5, and D_6, whilst inductor L_2 is charged due to the on-state of switch S_2. In mode II, L_1 and L_m are charged due to the on-state of switches S_1 and S_3, respectively. Capacitor C_1 is partially

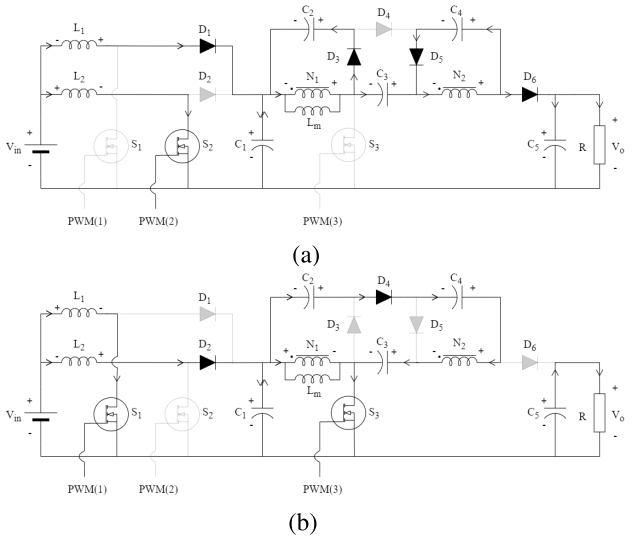


FIGURE 3. Switch modes of the proposed converter under CCM operation. (a) Mode I, (b) Mode II.

discharged to provide sufficient current for the charging of the coupled inductor, whilst the load is supplied through the discharging of C_5 to the output voltage level. Capacitor C_3 is charged as a result of the discharging of capacitors C_2 and C_4, due to the forward biasing of diode D_4. Inductor L_2 is discharged through the forward biased diode D_2. Key waveforms of the switching modes described are presented in Fig. 4. Note this operation proposes the PWM signals of switches S_1 and S_3 are synchronised, however, the converter is designed such that each stage may operate independently. This is due to the presence and sizing of the decoupling capacitor C_1. The synchronisation of the interleave and boost stage PWM signals is therefore not required.

B. VOLTAGE GAIN DERIVATION

To facilitate circuit analysis, the following assumptions are made:

- Capacitors are sufficiently large such that their voltage is constant.
- Inductors are sufficiently large to ensure CCM operation under all conditions.
- Equal power sharing is exhibited in each of the interleave phases.
- All components are ideal.

According to the converter's operational principles, the voltage gain can be determined as follows:

During switch mode I, the output voltage may be defined as,

$$V_o = V_{int} + V_{N1(d)} + V_{C3} + V_{N2(d)} \tag{1}$$

where $_d$ represents the discharging of the respective inductor, and the intermediate voltage, V_{int}, is the voltage of capacitor C_1 as defined in (2),

$$V_{int} = V_{in} + V_{L1(d)} = V_{in} + V_{L2(d)} = V_{C1} \tag{2}$$

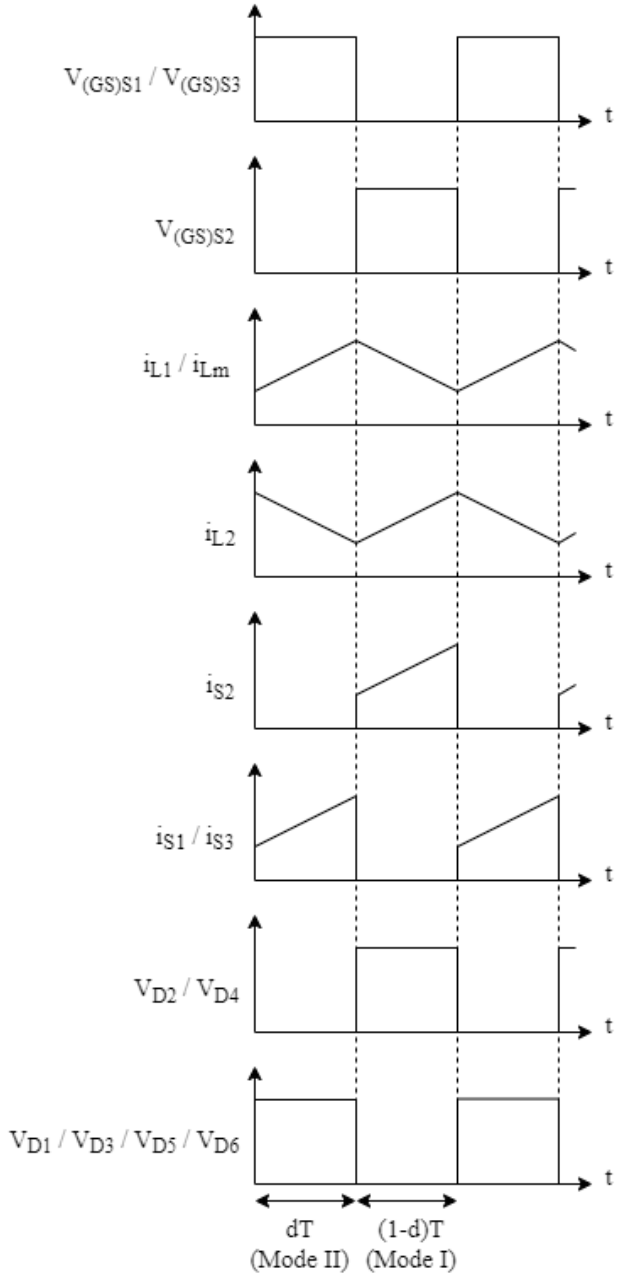


FIGURE 4. Key voltage and current waveforms.

Inductor L_2, and capacitors, C_2 and C_4 are charged in this switch mode according to (3), (4) and (5),

$$V_{L2(c)} = V_{in} \tag{3}$$
$$V_{C2} = V_{N1(d)} \tag{4}$$
$$V_{C4} = V_{N2(d)} \tag{5}$$

where $_c$ represents the charging of the respective inductor. In switch mode II, inductor L_1 and the coupled inductor are charged according to (6) and (7) respectively, whilst capacitor C_3 is charged according to (8),

$$V_{L1(c)} = V_{in} \tag{6}$$
$$V_{N1(c)} = V_{int} = \frac{V_{N2(c)}}{n} \tag{7}$$
$$V_{C3} = V_{int} + V_{C2} + V_{C4} + V_{N2(c)} \tag{8}$$

where n represents the coupled inductor turns ratio. Using Volt-Second Balance Theory, the intermediate voltage may be determined as,

$$V_{int} = V_{in}\frac{1}{1-d_1} \tag{9}$$

where d_1 is the duty cycle of the interleave stage switches. From (9), (7) may be rewritten to give (10),

$$V_{N1(d)} = V_{in}\frac{d_2}{(1-d_1)(1-d_2)} = \frac{V_{N2(d)}}{n} \tag{10}$$

where d_2 is the duty cycle of switch S_3. The voltage levels of capacitors C_2 and C_4 may then be rewritten to (11) and (12) respectively,

$$V_{C2} = V_{in}(\frac{1}{1-d_1})(\frac{d_2}{1-d_2}) \tag{11}$$
$$V_{C4} = nV_{in}(\frac{1}{1-d_1})(\frac{d_2}{1-d_2}) \tag{12}$$

Rewriting the voltage for capacitor C_3 in terms of (7), (9), (11) and (12) gives (13),

$$V_{C3} = V_{in}\frac{1+n}{(1-d_1)(1-d_2)} \tag{13}$$

Finally, the voltage output can be rewritten combining equations (9), (10), and (13) into equation (1) to give (14),

$$\frac{V_o}{V_{in}} = \frac{2+n+nd_2}{(1-d_1)(1-d_2)} \tag{14}$$

Since the interleave stage possesses a maximum PWM duty cycle of 50%, an alteration to the circuit operation may be to set the interleave duty cycle to a constant 50%, and control voltage through the PWM of S_3 only. This operation leads to a voltage gain described in (15),

$$\frac{V_o}{V_{in}} = \frac{4+2n+2nd_2}{1-d_2} \tag{15}$$

C. VOLTAGE AND CURRENT STRESS ANALYSIS

The semiconductor current and voltage stresses are determined through the use of Amp-Second Balance Theory, and similar methods to those used in Section III-B. Stresses are then confirmed through simulation of the proposed converter in MATLAB Simulink. Table 1 provides the voltage and current stresses for all semiconductor components within the proposed design. The maximum voltage stresses exhibited by components D_4 and D_6 are shown to be considerably less than the output voltage. This unique characteristic is due to the optimal use of coupled inductor and switched capacitor techniques that aid in lowering the voltage stress, especially for the output diode D_6.

TABLE 1. Semiconductor voltage and current stresses.

Component	Voltage Stress (V)	Current Stress (A)
D_1	$\frac{(1-d_2)}{2+n+nd_2}V_o$	$\frac{2+n+nd_2}{2(1-d_2)}I_o$
D_2	$\frac{(1-d_2)}{2+n+nd_2}V_o$	$\frac{2+n+nd_2}{2(1-d_2)}I_o$
D_3	$\frac{1}{2+n+nd_2}V_o$	I_o
D_4	$\frac{(1+n)}{2+n+nd_2}V_o$	I_o
D_5	$\frac{n}{2+n+nd_2}V_o$	I_o
D_6	$\frac{(1+n)}{2+n+nd_2}V_o$	I_o
S_1	$\frac{(1-d_2)}{2+n+nd_2}V_o$	$\frac{2d_1+nd_1+nd_1d_2}{2(1-d_1)(1-d_2)}I_o$
S_2	$\frac{(1-d_2)}{2+n+nd_2}V_o$	$\frac{2d_1+nd_1+nd_1d_2}{2(1-d_1)(1-d_2)}I_o$
S_3	$\frac{1}{2+n+nd_2}V_o$	$\frac{2+n+nd}{1-d_2}I_o$

The maximum current stress is exhibited by switch S_3, and equates to half the input current when the interleave stage contains a switch duty cycle of 50%. The use of the interleave design also proves to effectively halve the current in each of the phases, resulting in a low current stress for all components in each interleave phase.

D. DYNAMIC MODELLING AND CONTROLLER DESIGN

In this section, a small-signal model is formulated to determine the control-to-output transfer function. The proposed converter features a two-stage design: an initial boost converter followed by a coupled inductor converter. The transfer functions for these two stages are derived separately and can be integrated for the purpose of controller design.

The boost converter incorporates two energy storage components: the inductor current and the capacitor. The circuit equations for on-state can be represented by 16 and 17,

$$L_1\frac{di_{L1}}{dt} = V_{in} \tag{16}$$

$$C_1\frac{dv_{c1}}{dt} = -\frac{P_o(1-D_1)^2}{V_{in}^2}v_{c1} \tag{17}$$

The circuit equations for off-state can be represented by 18 and 19,

$$L_1\frac{di_{L1}}{dt} = V_{in} - v_{c1} \tag{18}$$

$$C_1\frac{dv_{c1}}{dt} = i_{L1} - \frac{P_o(1-D_1)^2}{V_{in}^2} \times v_{c1} \tag{19}$$

The state-space averaging method is employed to develop the mathematical model. Through this technique, the behavior of the converter is averaged over a switching cycle, effectively eliminating high-frequency switching ripples. Despite this averaging, the resulting model accurately captures the critical dynamics of the converter essential for control design. Subsequently, the small-signal model is derived through linearization. The control-to-output transfer function, representing the small-signal dynamics of the boost converter, is determined as follows,

$$G_B(s) = \frac{K_o(-\beta_1 s+1)}{s^2+2\xi\omega_n+\omega_n^2} \tag{20}$$

where,

$$K_o = \frac{(1-D_1)V_{c1}}{L_1C_1}, \quad \beta_1 = \frac{I_{L1}L_1}{(1-D_1)V_{c1}}$$

$$\omega_n = \frac{(1-D_1)}{\sqrt{L_1C_1}}, \quad \xi = \frac{P_o(1-D_1)}{2V_{in}^2}\sqrt{\frac{L_1}{C_1}}$$

The coupled inductor converter includes four energy storage elements, comprising of a coupled inductor and four capacitors. The voltages across the intermediate capacitors C_2, C_3, and C_4 are constant and dependent on either the input or output voltage, hence they are not considered as state variables [37]. The state variables are the coupled inductor and the output capacitor. Consequently, the small-signal model is simplified to a second-order system. For the coupled inductor stage, the output voltage v_o and the current through the primary side of the coupled inductor i_L are the two state variables. Thus, the circuit equations for the on switching states can be expressed by 21 and 22,

$$L_m\frac{di_L}{dt} = V_{c1} \tag{21}$$

$$C_5\frac{dv_o}{dt} = -\frac{v_o}{R} \tag{22}$$

The circuit equations for off state can be represented by 23 and 24,

$$L_m\frac{di_L}{dt} = V_{c1} + V_{c3} + V_{c4} - v_o \tag{23}$$

$$C_5\frac{dv_o}{dt} = \frac{i_L}{2+n+nD} - \frac{v_o}{R} \tag{24}$$

By applying the state-space averaging method and linearization process, the control to the output transfer function is obtained as,

$$G_c(s) = \frac{\tilde{v}_o(s)}{\tilde{d}_3(s)} = \frac{K_o(-\beta_1 s+1)}{s^2+2\xi\omega_n s+\omega_n^2} \tag{25}$$

where,

$$K_o = \frac{V_o(1-D_3)-V_{c1}(1+n+nD_3)}{L_mC_5(2+n+nD_3)(1-D_3)}$$

$$\beta_1 = \frac{I_LL_m}{V_o(1-D_3)-V_{c1}(1+n+nD_3)}$$

$$\omega_n = \left(\frac{1-D_3}{2+n+nD_3}\right)\sqrt{\frac{2+n+nD_3}{L_mC_5}}$$

$$\xi = \frac{1}{2R(1-D_3)}\sqrt{\frac{L_m(2+n+nD_3)}{C_5}}$$

In the proposed converter, the interleaved stage primarily minimizes the input current ripple and reduces the current

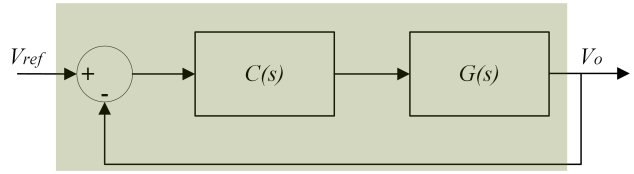


FIGURE 5. Proposed converter control block diagram.

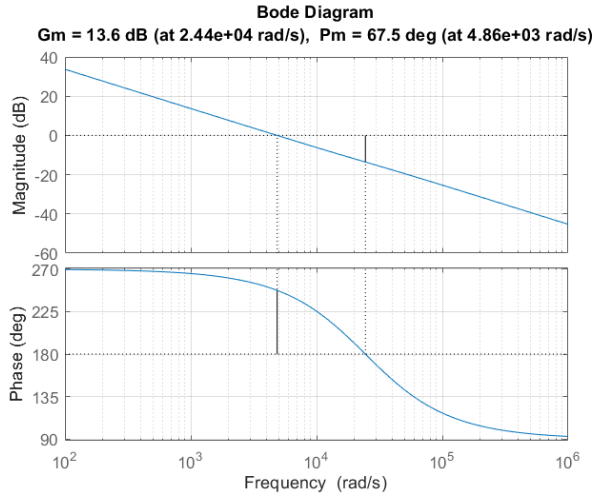


FIGURE 6. Proposed converter bode diagram.

stress. This stage operates at a constant maximum allowable duty cycle of 0.5 for optimal performance. Additionally, the decoupling capacitor C_1 isolates the dynamics of the interleaved stage from the second stage. Moreover, the output voltage is regulated by the coupled inductor converter. As a result, the overall converter dynamics are predominantly governed by the coupled inductor converter.

The control block diagram of the proposed converter is illustrated in Fig. 5. The controller $C(s)$ is designed using the Affine parameterization approach [38]. This design leverages the desired closed-loop system performance by specifying the close-loop undamped natural frequency ω_{cl} and the damping ratio ζ_{cl}. The controller is implemented in PID format for execution in a digital microcontroller.

$$C(s) = \frac{s^2 + 2\xi\omega_n s + \omega_n^2}{K_o s(\alpha_2 s + \alpha_1)} \tag{26}$$

where,

$$\alpha_1 = \frac{2\xi_{cl}}{\omega_{cl}}, \quad \alpha_2 = \frac{1}{\omega_{cl}^2} \tag{27}$$

To ensure a stable closed-loop system, the relative stability of $C(s)G(s)$ is ensured. Higher phase and gain margins are indicative of relative stability, as these quantify the distance from the point of instability. The Bode diagram of the closed-loop system is presented in Fig. 6. The Bode plot demonstrates a solid phase margin of 67.5Â°, ensuring control system stability.

TABLE 2. Experimental parameters.

Parameter	Value
Input Voltage (V_{in})	14.4V
Output Voltage (V_o)	400V
Rated Power	500W
Switching Frequency (f_{sw})	50kHz
S_1/S_2	N0604N-S19-AY
S_3	CSD19535KCS
D_1/D_2	STPS30M60ST
D_3	DSTF30100S
D_4	FFSP3065A
D_5/D_6	STPSC12H065D
C_1	Electrolytic, 4000uF, 50V
C_2	Film, 47uF, 63V
C_3	Film, 40uF, 400V
C_4	Film, 33uF, 160V
C_5	Electrolytic, 220uF, 600V
L_1/L_2	33uH
Coupled Inductor	50uH, $N_1 : N_2$ = 1:3.5

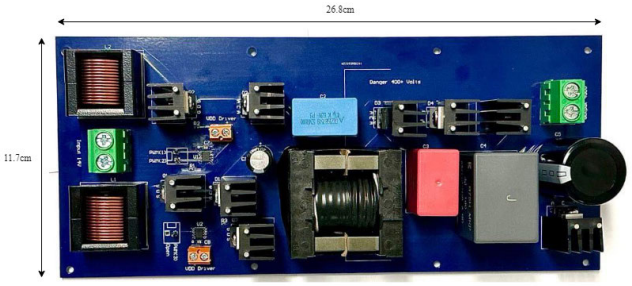


FIGURE 7. The developed prototype.

E. DEVELOPMENT OF THE PROTOTYPE

The development of the prototype is achieved through theoretical and simulation analysis of the proposed converter. The prototype's voltage, frequency and power characteristics are provided in Table 2, along with characteristics of the chosen capacitors and inductors, and part numbers for the chosen semiconductor components. The prototype's final design is depicted in Fig. 7.

Semiconductor components are sized based on their current and voltage stresses calculated in Table 1, and through analysis of the converter in MATLAB Simulink.

Since the interleave converter exhibits a theoretical input ripple current of zero, the inductors are sized according to the CCM requirement under all operating conditions. As the

TABLE 3. Theoretical loss in each component at 105W and 500W operating conditions.

Component Loss	Loss (W) @ 105W	Loss (W) @ 500W
L_1, P_{cond}	0.04	0.58
L_2, P_{cond}	0.04	0.51
$L_{N1/N2}, P_{cond}$	1.59	20.54
P_{core} Total	0.05	0.24
S_1, P_S Total	0.09	0.77
S_2, P_S Total	0.08	0.67
S_3, P_S Total	0.29	1.78
D_1, P_{Vfd}	0.7	2.75
D_2, P_{Vfd}	0.69	2.61
D_3, P_{Vfd}	0.09	1.04
D_4, P_{Vfd}	0.21	0.74
D_5, P_{Vfd}	0.21	0.74
D_6, P_{Vfd}	0.21	0.74
Capacitor, P_{cond} Total	0.06	0.64
Total	**4.35**	**34.34**

coupled inductor is not directly connected to the input, its ripple current content is also not of a concern, and is therefore sized based on the CCM requirement. The inductors and coupled inductor are sized according to (28),

$$L_{min} = \frac{Vd}{2If_{sw}} \tag{28}$$

where V is the input voltage or intermediate voltage when calculating the inductor or coupled inductor inductances, respectively, I is the average current at the minimum operating condition and f_{sw} is the converter switch frequency.

Capacitor C_5 is sized based on the output voltage ripple requirement of 0.5V, and determined by (29),

$$C_{min} = \frac{Vd}{R\Delta Vf_{sw}} \tag{29}$$

where ΔV is the peak-to-peak output voltage ripple, and R is the load resistance at the maximum power rating of 500W.

Capacitor C_1 is sized to ensure decoupling between the boost and interleave stages, whist capacitors C_2, C_3 and C_4 are sized to ensure minimal voltage ripple across the circuit. The input voltage is set as 14.4V to align with the commercially available 500W fuel cell from Horizon Technologies [39]. According to (15), a coupled inductor turns ratio of 3.5 is chosen to obtain the required voltage gain at 50% duty cycle.

An Arduino microcontroller is used to generate the PWM signals to drive the converter. Two 2EDN7524FXTMA1 low-side MOSFET gate drivers are sourced to drive the gates of the interleave and boost stage switches.

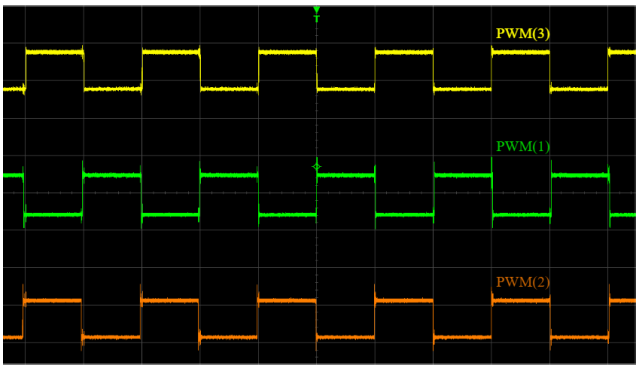


FIGURE 8. PWM switching scheme for experimental analysis.

For experimental analysis, the prototype is powered with a 2100W high current Aligent 6573A DC source, and the gate drivers with a GW Instek GPC-3030D DC source. The converter is connected to Maynuo M9712B 300W programmable load, with all waveforms and measurements captured using a Rohde and Schwarz RTB2004 Digital Oscilloscope.

IV. EXPERIMENTAL RESULTS

A. OPERATION AND PERFORMANCE

The PWM switching scheme is shown in Fig. 8, where the interleave PWM signals are 180^o out of phase, operating at a 50% duty cycle. The boost stage PWM signal also operates at 50% duty cycle and in phase with switch S_2 of the interleave stage. Fig. 9 - 11 show key waveforms of the interleaved stage. Inductor L_1 and L_2 waveforms shown in Fig. 9 coincide with the 180^o phase shift between PWM signals, aligning with the theoretical analysis. As a result of the interleaving, the sum of current in each of the phases results in a near constant input current. The input ripple current is shown in Fig. 15, and is measured as 1.5%. The currents of switches S_1 and S_2 shown in Fig. 10(a) and Fig. 10(b), respectively, show near equal current sharing, implying the operation of equal power sharing between phases. The interleave stage diode voltages in Fig. 11 are shown to be equal to the intermediate voltage when operating at 400V, aligning with the theoretical analysis.

Key waveforms from the boost stage are provided in Fig. 12 - 14. The coupled inductor primary and secondary current waveforms in Fig. 12 show the direction of current flow throughout this stage of the circuit. The current is shown to travel through the primary windings consistently in one direction, whilst the current travels through the secondary winding in opposite directions for the switch, S_3, on-state and off-state. During the charging of the coupled inductor, current flows through the secondary winding in the opposite direction, causing the charging of capacitor C_3. During the switch S_3 off-state, current travels in the same direction as the primary windings and to the load, as predicted by

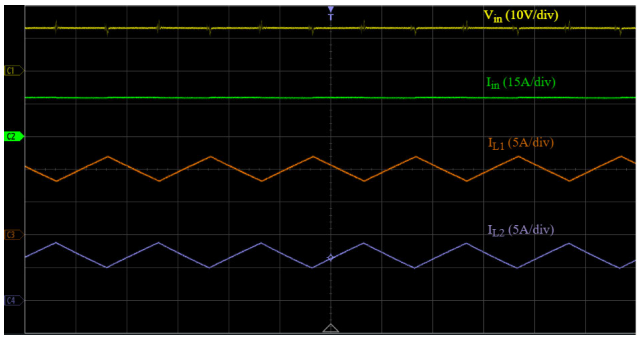
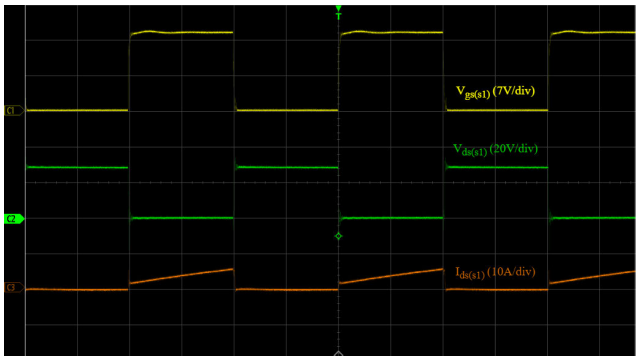
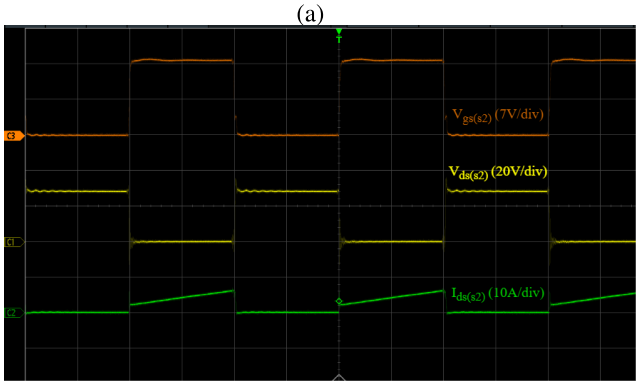


FIGURE 9. Interleave stage input current and voltage, and inductor currents waveforms.



(a)



(b)

FIGURE 10. Interleave stage switch voltage and currents waveforms. (a) S_1, (b) S_2.

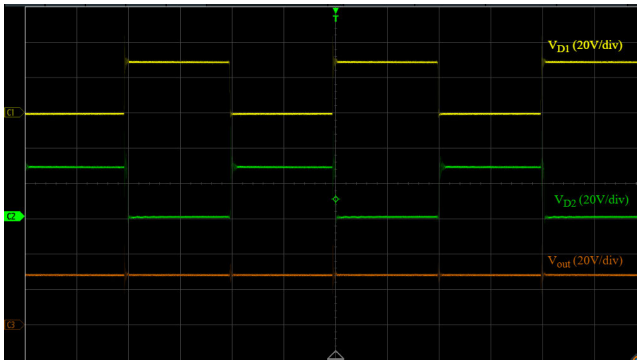


FIGURE 11. Interleave stage output voltage and diode voltages at 400V output voltage operating condition.

the theoretical analysis and simulation. Fig. 13 shows the operation of the switch S_3, whilst Fig. 14 shows the voltage levels of diodes D_3, D_4, and D_5, and capacitor C_4. Voltage and

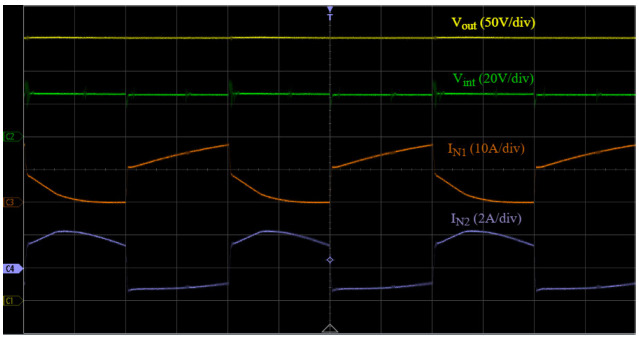


FIGURE 12. Boost stage input and output voltages, and coupled inductor currents.

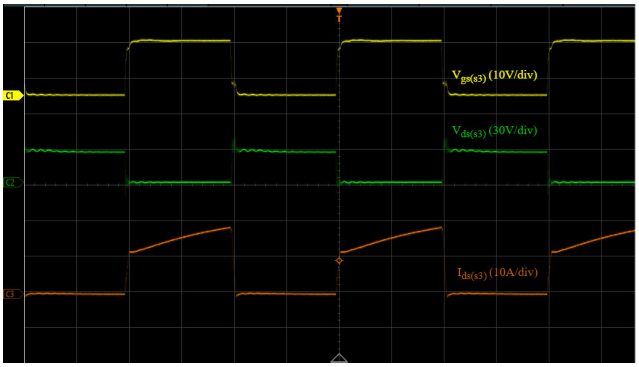


FIGURE 13. Boost stage switch voltage and currents.

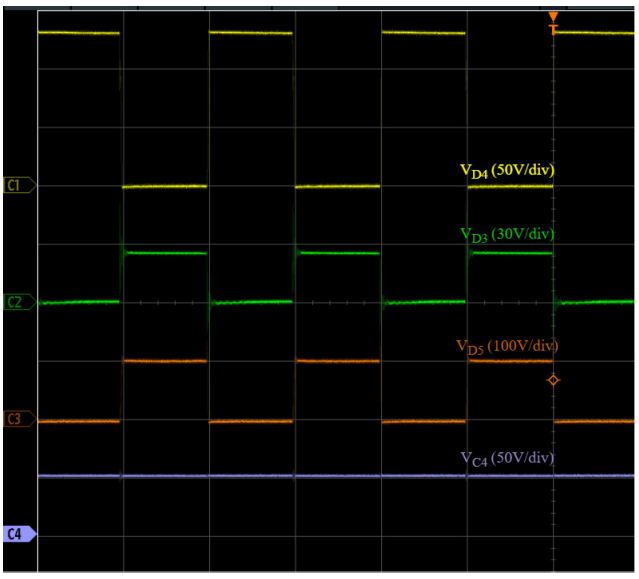


FIGURE 14. Boost stage diode and capacitor voltages waveforms.

current levels here are shown as near equal to their predicted current and voltage stresses from the converter theoretical analysis.

Fig. 9 and 12 show the input and output voltage, respectively, of the proposed converter. The input voltage is shown to remain constant at 14.4V, whilst the output voltage is 400V under a 50% duty cycle for all switches. The resultant voltage gain is equal to 27.8 at a low-duty cycle, realising the proposed converter's ability to reach

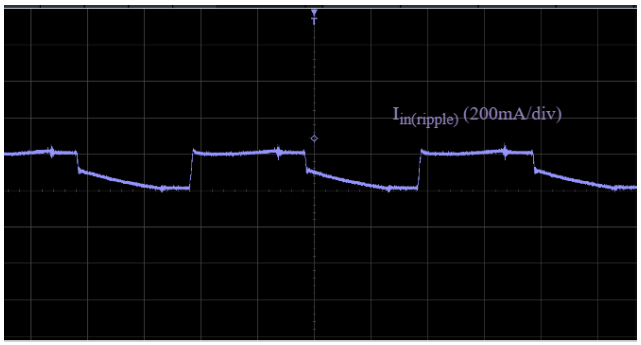


FIGURE 15. Ripple in the input current.

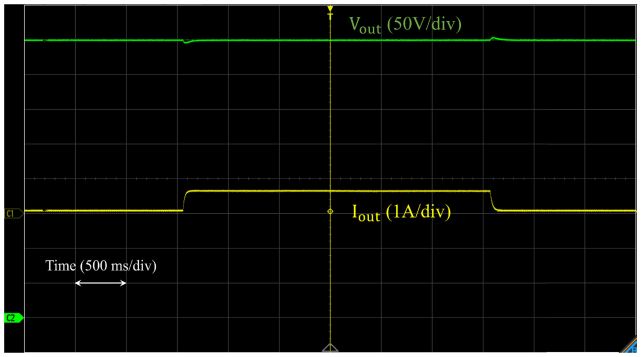


FIGURE 16. Dynamic response of the proposed converter under sudden changes in load.

an ultra-high voltage gain. All measured waveforms are consistent with the theoretical analysis.

The dynamic response of the converter to sudden load changes is illustrated in Fig. 16. The output load current varies from 0.1A to 0.7A at 400V. As observed, the output voltage is effectively regulated at 400V despite the step change in load. The output voltage exhibits a minimal overshoot of 1% and stabilizes within 100 ms. Overall, the converter demonstrates satisfactory closed-loop performance, maintaining a stable output voltage under step load changes.

The theoretical and experimental conversion efficiency curves are depicted in Fig. 17. Simulation analysis showed a maximum efficiency of 95.85% at an input power of 105W, whilst maximum experimental efficiency is recorded as 95.52% at an input power of 110.8W. Both efficiency curves exhibit a similar trend, although the practical efficiency is slightly diminished compared to the theoretical values due to PCB conduction losses and other non-ideal factors.

B. LOSS ANALYSIS

Theoretical loss analysis is conducted to determine the primary sources of power consumption within the converter. Conduction losses are calculated using (30),

$$P_{cond} = I_{RMS}^2 R \tag{30}$$

where R denotes the components series DC resistance and I_{RMS} is the components root mean square current, determined

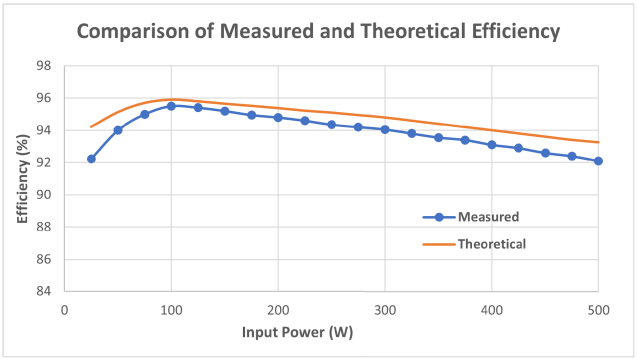


FIGURE 17. Experimental and theoretical efficiency curves.

through (31),

$$I_{RMS} = \sqrt{\frac{1}{T}\int_0^T i(t)^2 dt} \tag{31}$$

For the switching time period, T, and instantaneous current $i(t)$. Diode forward voltage conduction losses were calculated using (32),

$$P_{Vfd} = I_{ave} V_{fd} \tag{32}$$

where V_{fd} is the diode forward voltage drop at that operating condition, and I_{ave} is the diode average current determined through (33),

$$I_{ave} = \frac{1}{T}\int_0^T i(t) dt \tag{33}$$

Inductor core losses are calculated using the Generalised Steinmetz Equation in (34),

$$P_{core} = K f_{sw}^{\alpha} B_{max}^{\beta} A_c l_c \tag{34}$$

where f_{sw} is the switching frequency, B_{max} is the inductor peak flux density, A_c is the core cross-sectional area, l_c is the core mean path length, and K, α, and β are the Steinmetz coefficients, found as typical values in inductor datasheets.

Switching losses for the active switches are calculated using (35) and (36),

$$P_{S(on)} = \frac{1}{2} V_{S(rise)} I_{S(fall)} t_{rise} f_{sw} \tag{35}$$

$$P_{S(off)} = \frac{1}{2} V_{S(fall)} I_{S(rise)} t_{fall} f_{sw} \tag{36}$$

where V_S and I_S are the respective switch rise and fall voltage and current magnitudes, t_{rise} and t_{fall} are the rise and fall times, respectively, and $f\,sw$ is the switching frequency.

The total power loss within the circuit is therefore calculated via (37), with the efficiency calculated through (38).

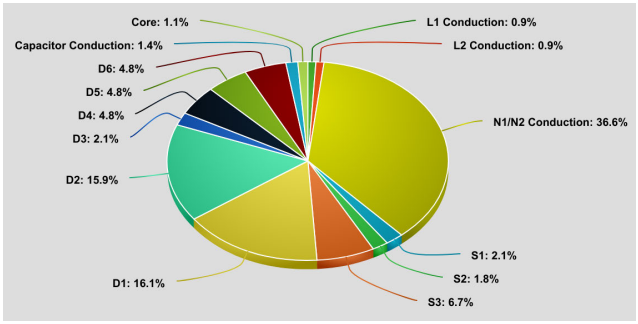
$$P_{loss} = P_{cond} + P_{Vfd} + P_{core} + P_{S(on)} + P_{S(off)} \tag{37}$$

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} * 100\% \tag{38}$$

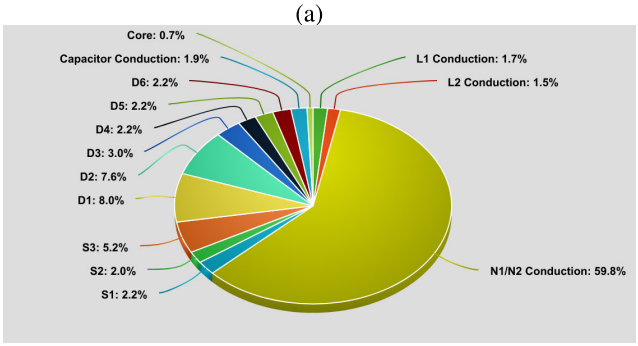
Individual component losses are listed in Table 3, and a visual representation of the power losses for the theoretical maximum efficiency and rated converter output power are

TABLE 4. Comparison of the proposed converters power rating, peak efficiency, input ripple current, voltage gain, and number of components with other converters. All data is obtained from each converters experimental results.

[Ref]	Rated Power (W)	Peak Efficiency (%)	I_{in} Ripple (%)	Voltage Gain	Switch/Diode/Inductor/Capacitor
[14]	1430	97.99	0.7	1.6	12/0/6/1
[15]	150	92.6	unspecified	14	2/10/4/4
[22]	200	94.02	9.52	6	1/5/2/4
[23]	300	95.01	12.5	10	2/5/2/5
[24]	200	94.07	25	8.33	1/4/3/4
[25]	400	95.13	50	10	1/5/2/5
[28]	1000	95.4	3.5	8	3/3/1/3
[31]	1000	96.56	unspecified	11	2/4/3/5
[32]	100	95.8	25.6	10	1/3/2/4
[33]	50	92	22.8	4.5	1/5/2/4
Proposed	**500**	**95.52**	**1.5**	**27.8**	**3/6/3/5**



(a)



(b)

FIGURE 18. Theoretical percentage of component power loss for the operational cases of (a) 105W (b) 500W.

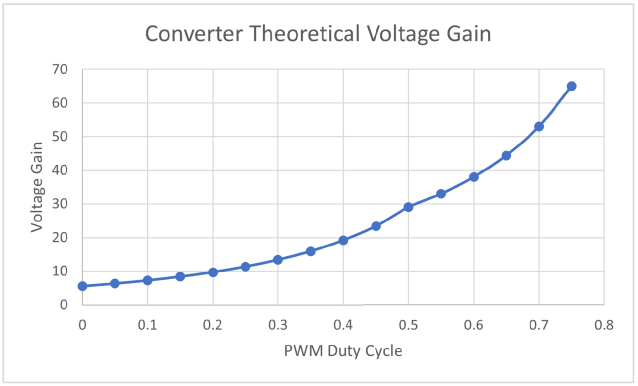


FIGURE 19. Theoretical voltage gain of the proposed converter.

provided in Fig. 18(a) and Fig. 18(b), respectively. As a result of the high winding resistance, the coupled inductor contributes to a high percentage of power loss within the circuit. Interleave diodes contribute to a high power loss percentage as a result of their high associated operational currents, whilst the switches also share a majority of the power loss, especially from the single switch in the boost stage, S_3.

Since the coupled inductor is the primary source of power loss under all operating conditions, optimising this component would be the first step towards improving efficiency. The high winding resistances observed are due to the use of a handmade coupled inductor with standard wire. A manufacturer sourced coupled inductor with litz wire may aid in reducing the resistances and associated power losses to further enhance the converter efficiency.

V. COMPARISON WITH OTHER CONVERTER DESIGNS

Table 4 provides a detailed comparison of the proposed converter and other converters from the literature designed for fuel cell applications. As shown, the proposed converter has the capability of achieving a significantly higher voltage gain than all other converters when operating at a 50% duty cycle. Fig. 19 also shows the converter's theoretical voltage gain capability, where a potential voltage gain as high as 65 is possible for switch, S_3, duty cycles up to 75% and switches S_1/S_2 duty cycles maintained at 50%. The use of the interleaving technique has also shown merit in achieving a low input ripple current with respect to

other converters. The peak efficiency is comparable with respect to the other designs and may be further enhanced by sourcing an alternative coupled inductor with lower winding resistances. The proposed converter component count is also high with respect to most other converter designs, although it is significantly lower than the converters from [14] and [15], which contain the lowest ripple current and highest voltage gain from literature, respectively. The proposed design is, therefore, competitive with respect to similar designs in all fields of interest, whilst achieving a significantly higher voltage gain than any other converter explored for this application.

VI. CONCLUSION

This paper presents a novel interleaved, cascaded DC-DC boost converter specifically designed for fuel cell applications. The proposed converter leverages interleaving techniques in the input stage to significantly reduce input ripple current while efficiently boosting the input voltage. The second stage integrates a switched capacitor coupled inductor boost converter to achieve an ultra-high voltage gain of 27.8 at a 50% switch duty cycle, with a minimal input ripple current of just 1.5%. The prototype demonstrated a peak efficiency of 95.52%, with losses primarily attributed to a high coupled inductor winding resistance. Additionally, the converter exhibits low voltage stress on semiconductor devices, with the maximum switch voltage stress measuring only 14% of the output voltage. The key achievements are as follows:

1) The interleaved design achieves a significant reduction in input ripple current, which enhances the performance and reliability of fuel cell systems.

2) The cascaded DC-DC boost converter achieves an ultra-high voltage gain of 27.8, demonstrating its capability to meet high voltage requirements for various applications.

3) The converter reaches a peak efficiency of 95.52%.

4) The design ensures that the maximum switch voltage stress is only 14% of the output voltage, contributing to reduced losses and increased reliability of semiconductor components.

5) The converter benefits from a common input and output ground configuration and simplified gate driver circuitry, making it easier to implement in practical applications.

Despite these significant advancements, the proposed converter does not incorporate soft-switching techniques. Future research could focus on exploring soft-switching strategies, such as zero-voltage switching (ZVS) and zero-current switching (ZCS), to further enhance the efficiency and power density of the converter. Additionally, the design of coupled inductors can be improved to reduce conduction losses and improve efficiency.

Overall, the proposed converter demonstrates significant potential for fuel cell applications and provides a foundation for future developments aimed at optimizing high-gain DC-DC converters for a variety of practical applications, including hydrogen fuel cells and renewable energy systems.

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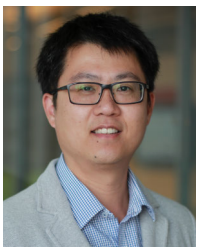

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