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ORIGINAL RESEARCH

A new soft-switching high gain DC/DC converter with bipolar outputs

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Abstract

This paper introduces a new single-input multi-output step-up DC/DC converter with soft-switching performance and low input current for renewable energy applications. The proposed topology uses a three-winding coupled-inductor (TWCI) and voltage multiplier circuits to achieve high voltage gains. The bipolar output voltages of the proposed converter can be varied independently by tuning the turns ratios of the TWCI. Due to the semi-trans-inverse specification of the suggested topology, high voltage gains can be obtained under a lower number of turns ratio in the magnetic device. Furthermore, a regenerative passive clamp technique mitigates the voltage stress on the single power switch. Additionally, the power dissipations are further reduced by considering a resonant tank in the circuit. In the converter, the parasitic leakage inductances of the TWCI windings help to provide the soft-switching conditions for the switch and also to eliminate the reverse-recovery loss for all converter diodes. The operating mode of the presented converter has been introduced and the steady state, along with the main operating equations have also been derived. Finally, the theoretical analysis is verified by a sample prototype 235 W at the input voltage 25 V and outputs of 200 V and −200 V.

1 | INTRODUCTION

In recent years, with the development of power electronics, the low-voltage DC distribution system based on renewable energy sources has become a proper alternative to replace the conventional ac distribution system [1]. For this purpose, DC-DC switched-mode converters have drawn particular attention to the use of renewable energy sources (RES) such as photovoltaic. For such applications, high voltage gain ratio, low input current ripple, minimum voltage stress, and compact design are the main performance indicators that are required for DC-DC power converters [2]. So far, many high step-up converters have been introduced to increase the low voltage level of renewable DC resources. To enhance the voltage gains, voltage boosting methods, including voltage lift, switched capacitors/inductors, voltage multipliers, and cascaded connections, are often used [1–4]. However, most of these structures suffer from hard-switching performance and large component count, which compromise the efficiency and power density of the converter. For low-power applications, the non-isolated circuits give often better performance at a lower cost [1, 4].

Generally, lots of low-power equipment such as LED lighting, computers, gadgets, appliances, medical devices, energy harvesting, UPS, portable devices, and data centres need DC power. For this purpose, single-input multi-output (SIMO) DC-DC structures are an effective way to feed several DC loads under higher power density and compact design [5, 6].

One of the popular multi-output topologies in the DC bus frameworks is the bipolar structure. It has a three-wire system, which is able to provide three different voltage levels, including positive (V_p), negative (V_n) outputs, and the sum of them (V_p+V_n) for DC units to easily interface with the DC microgrids and for DC-AC application such as mid-point clamped Multilevel converters. In such systems, if a fault happens in one of the poles, the other pole can operate to increase the reliability of the system [7]. Adjustable output DC voltage with a wide range of variety from negative to positive is one of the benefits of the bipolar converters, which makes their applications wider.

Several types of SIMO with bipolar outputs have been presented in recent years. In [5], [8], and [9], some different transformer-less structures of bipolar DC-DC structures based on combinations of the SEPIC and CUK converters with low

input current ripple are proposed. Ideally, the voltages of the positive and negative poles of the output are equal. However, the output voltages are adjusted only with the help of the duty cycle at different load conditions, where it is challenging to balance the bipolar voltage levels. Also, a new single-switch boost-based DC-DC converter with multi-output voltages is proposed in [10]. This simple structure can provide two equal negative and positive output voltages for a DC bus. However, hard-switching performance and limited voltage gains are considered as its disadvantages. A new bipolar DC-DC converter with high voltage gains is introduced in [11]. Although this converter offers high output voltages with a small duty cycle, and voltage gains, the steep slope of voltage gain, making the control more complex. Furthermore, in [12], a new non-isolated high voltage gain DC-DC converter with interleaving and switched-capacitor techniques with bipolar outputs is suggested. Although soft-switching performance, in this circuit, high voltage gains are achieved using a large component counts. In addition, three new multi-output DC-DC converters with simple structure and low DC input current ripple are presented in [13–15]. The impossibility of balancing the output poles is the main defect of these converters. Also, in [16] and [17], new bipolar DC-DC converters with discontinuous input current are introduced.

Today, magnetically coupled devices and other voltage boosting techniques are widely adopted to improve the performance of multi-output DC-DC converters. In these topologies, the turns ratio of the coupled-inductor, as an additional freedom degree, further enhances the voltage gains without needing an extreme duty cycle [1, 18, 19]. In such converters, to restrict the high voltage spike, the active/passive clamp circuits can be used [19]. Moreover, soft-switching operation is one of the key performance indicators for switched-mode DC-DC converters, which is applicable in three ways including zero current switching (ZCS), zero voltage switching (ZVS), zero voltage transition (ZVT) and zero current transition (ZCT). Since the main power switch/switches in high step-up DC-DC converters withstand the highest current value; therefore, soft switching techniques have a significant effect on reducing or eliminating the switching losses, which leads to efficiency improvement of the circuit. This means that the step-up circuit can operate at higher frequencies, which decreases the size and weight of the passive components, and cooling requirements. However, the main disadvantage of some soft switching techniques such as ZVS, ZVT, and ZCT often increase the complexity and cost of the power electronics design and control. In [20], a new family of symmetrical bipolar output converters with ZVS performance is suggested. However, in this topology, many power switches should be used to achieve ZVS performance, which limits its applications. Also, two new types of single-output ZVT step-up DC-DC converter based on CI are introduced [21] and [22]. Nevertheless, they require additional circuit components, including active-switch, coupled-inductor, and resonant capacitors and inductors, to create the desired soft switching conditions for the power switches. In addition, in [23], a zero-voltage zero-current transition network for a dual-phase interleaved converter is suggested. In this topology, with the help of an additional CI along with an active switch, the proposed circuit is able to perform is soft-switching operation. It is worth noting that in some DC-DC converters, soft switching performance ZCS is created intrinsically without the need for additional elements, which can be considered as an advantage [2, 3].

So far, several bipolar DC-DC converters using coupled-inductor have been introduced. In [24] and [25], two new bipolar high voltage gain DC-DC converters using coupled-inductor and cascaded techniques are provided. In this topology, adjusting the negative pole can be done by the turns ratio of the coupled-inductor. Thus, two balanced outputs can be achieved in this converter under unbalanced power flow conditions in the bipolar DC bus. However, this simple structure give limited voltage gains, and high input current ripples, which are demerits of this topology. Moreover, a new coupled-inductor-based non-isolated SEPIC DC-DC converter with two different negative and positive voltage gains is suggested in [26]. Since both output poles of the converter are a function of the turns ratio and duty cycle, their balancing is not easily implemented. In addition, in [27, 28], a ZVS high voltage gain converter based on boost-CUK topology is presented. In this double-switch converter, an active clamp circuit is used to transfer the energy of the leakage inductor. However, the series connection between the input DC source and the primary side of the three-winding coupled-inductor makes a high input current ripple. In addition, in [29], a new high step-up DC-DC Converter based on three-winding CI with three outputs is suggested. However, the series connection between the input DC source and the primary side of the three-winding coupled-inductor makes a high input current ripple, which limits their applications for renewable energy sources. Also, in [30], a new type of transformerless bipolar DC-DC converter is introduced. However, the steep slope of voltage gain changes in this converter leads to its more complicated control. Moreover, a transformerless symmetric bipolar quadratic Buck-Boost converter is introduced in [31]. However, in this circuit, three switches along with three magnetic cores need to consider. In addition, new coupled-inductor high-gain DC/DC converter with bipolar outputs with low input current ripple is presented in [32]. Nevertheless, using two power switches can be considered as demerits of the mentioned topology.

Regarding the merits and demerits of the discussed step-up converters, this paper presents a new type of bipolar DC-DC converter based on a TWCI. The novelties of the introduced topology are:

1. High voltage gains for three outputs as a function of duty cycle of the single switch and turns ratio of the coupled-inductor.
2. The semi-trans-inverse manner leads to voltage gain enhancement under reduced turns number.
3. Low input current ripple.
4. Low voltage stress on the main power switch.
5. Soft-switching performance ZCS for the single power switch of the circuit.
6. No reverse recovery problem for all diodes.

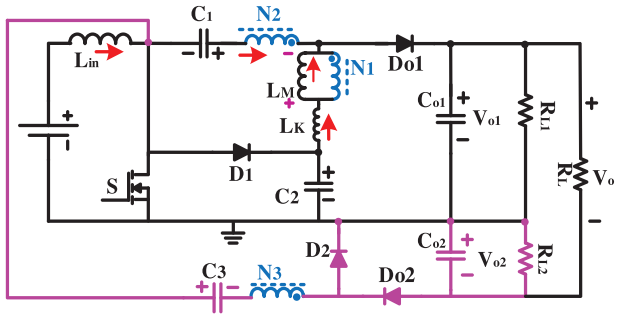


FIGURE 1 The circuit configuration of the proposed converter.

7. Considering a resonant tank to decrease the switch power loss.

This paper is organized as follows: introducing the proposed circuit topology, the steady-state analysis, along with mathematical derivation are given in Sections 2 and 3. In Section 4, the advantages of the introduced circuit are compared with other similar converters. Sections 5 and 6 provide the parameters design and experimental verifications for a sample prototype and finally concludes in Section 7.

2 | PRINCIPLES OF OPERATION OF THE PROPOSED CONVERTER

The proposed topology is depicted in Figure 1. This circuit is formed by a power switch (S), an input inductor (L_{in}), a TWCI, four diodes (D_1, D_2, D_{o1}, and D_{o2}), and five capacitors (C_1, C_2, C_3, C_{o1}, and C_{o2}). In Figure 1, R_{L1}, R_{L2} and R_L are the load resistors connected between the output DC terminals of the proposed converter. V_{o1} and V_{o2} are the positive and negative DC output voltages, respectively. Thanks to the clamp circuit (C_2 and D_1), the voltage rate across the power switch is restricted. Due to considering a resonant tank among the capacitors C_1, C_2, and TWCI, the current waveforms of the switch and diode D_{o2} change into a sinusoidal form, which decreases the switch turn-off and reverse recovery losses. In this circuit, the leakage inductances of the TWCI help to alleviate the reverse recovery loss of the diodes.

All switching components are supposed to be ideal for simplifying the presented circuit analysis in continues conduction mode (CCM) condition. Moreover, the voltages of the converter capacitors are considered to be a constant value. Furthermore, the TWCI is modelled as an ideal transformer with turns ratios $n_{21} = N_2/N_1$ and $n_{31} = N_3/N_1$, along with a magnetizing (L_M) and a merged leakage (L_k) inductances. Figure 2 shows the theoretical main key waveforms in six states of the proposed topology. Furthermore, the equivalent circuits of each mode are depicted in Figure 3.

Mode-1 [$t_0 - t_1$]: At $t = t_1$, the MOSFET switch starts to conduct at ZCS conditions. From Figure 3a, the Diode D_2 is also conducting, while other converter diodes are reverse biased. In this mode, the input DC source provides energy to the input inductor L_{in} during this transient mode. Because of the effect of the reflected leakage inductor on the tertiary side of the TWCI, the current of the Diode D_2 reaches zero with a low reverse recovery (LRR) problem at the end of this state.

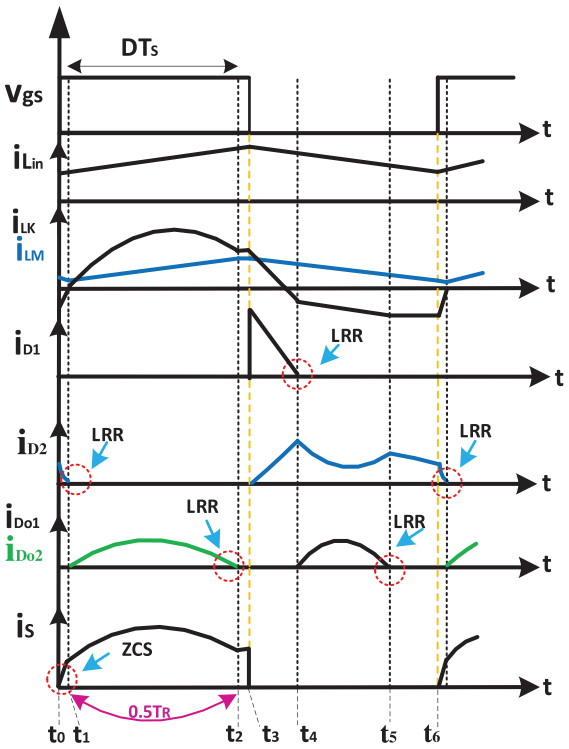


FIGURE 2 Typical main key waveforms of the proposed converter in CCM operation.

Mode-2 [$t_1 - t_2$]: In the second operating mode, the power switch still is on, and at $t = t_1$, the output diode D_{o2} begins to conduct with a low slope. Same as Mode-1, L_{in} is charged by the input DC source. The energy stored in the Capacitor C_2 and the TWCI are delivered to the balancing Capacitor C_1. Because of the positive induced across the magnetizing inductor, L_M gets charged. During this interval, to alleviate the switch current value at the turn-off time, a resonant tank between the TWCI windings and the Capacitors C_1, and C_2 are considered. According to Figure 3b, the mentioned resonant performance forms the current waveforms of the switch and diode Do_2 into a sinusoidal shape. This decreases the switch loss and diode reverse recovery issue. The resonant frequency (f_{R2}) based on LC resonant tank is obtained as:

$$f_{R2} = \frac{1}{T}_{R2} = \frac{1}{2\pi\sqrt{L_k\,(C_1 \| C_2)}} \tag{1}$$

It is noteworthy that the best case of the resonant tank operation for alleviating the power losses is in the critical mode

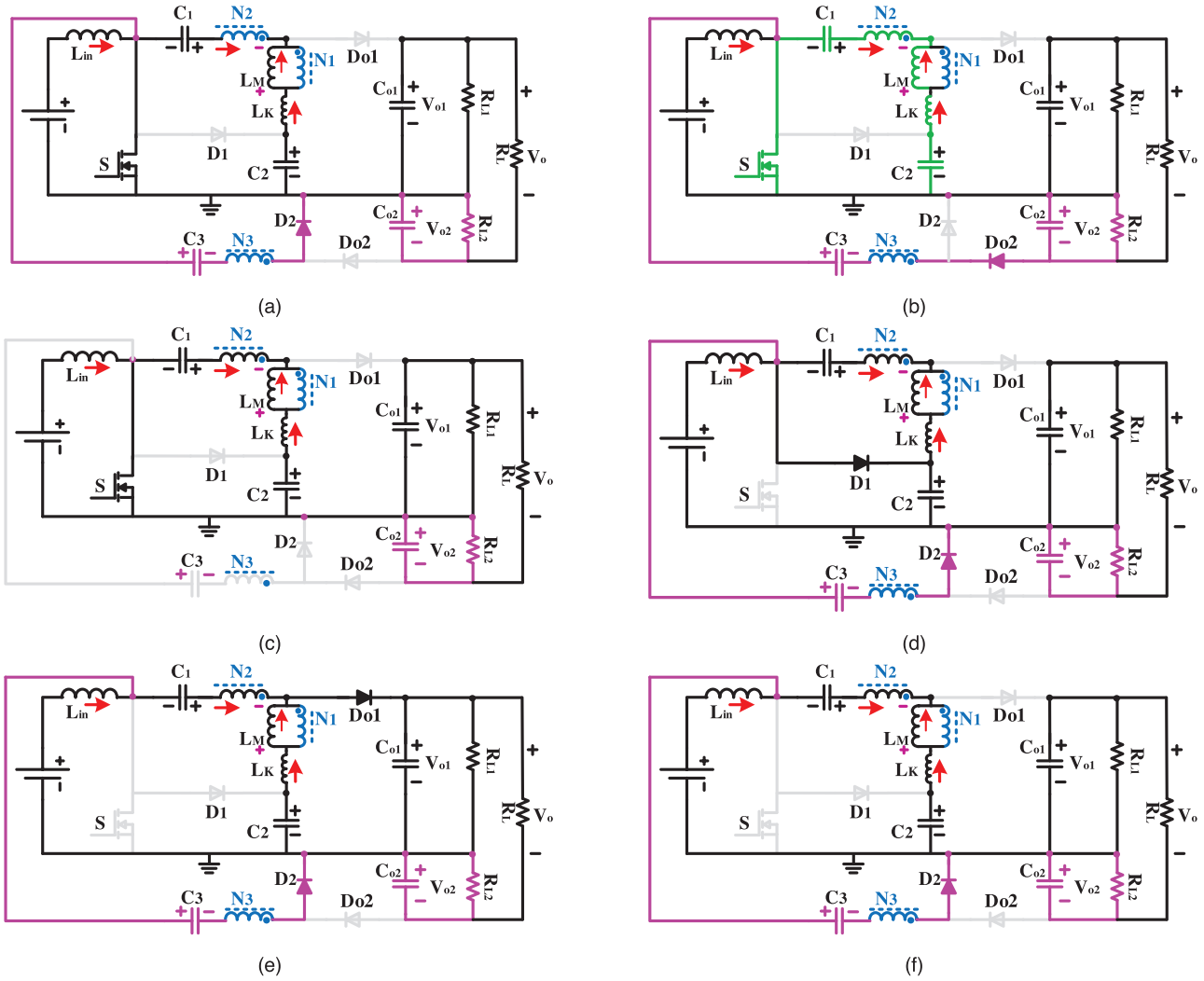


FIGURE 3 Operation modes of the proposed circuit: (a) Mode-1, (b) Mode-2, (c) Mode-3, (d) Mode-4, and (e) Mode-5, and (f) Mode-6.

($T_R/2 \approx DT_S$). In this state, the following equations can be written:

$$v_{Lin} = V_{in} \tag{2}$$

$$v_{LM} = \frac{v_{C2} - v_{C1}}{1 - n_{21}} \tag{3}$$

$$v_{C3} = v_{Co2} - n_{31}.v_{LM} \tag{4}$$

Also, the current passing through the switch is calculated as:

$$i_s = i_{in} + i_{Do2} + i_{LK} \tag{5}$$

During this state, the magnetic energy stored in the tertiary side of the TWCI is released to the output capacitor C_{o2}. This interval complete when the current value of the output diode Do_2 reaches zero at a gentle slope without reverse recovery. Thus, it can be expected that the switching noises of the output DC voltage will be removed.

Mode-3 [$t_2 - t_3$]: according to Figure 3c, after D_{o2} is turned OFF, the currents of the secondary and primary sides of the TWCI are identical. During this time interval, the current of the coupled-inductor charges the capacitor C_1. In this short interval, the current passes from the switch, which is derived as:

$$i_S = i_{in} + i_{LK} \tag{6}$$

Mode-4 [$t_3 - t_4$]: At the beginning of this mode, the single power switch is OFF. In this mode, the Diode D_2, along with clamp Diode D_1 begins to conduct. Thus, the voltage across the switch is clamped. (Figure 3d). Also, the capacitor C_2 starts to get energy from L_{in}. Furthermore, the energy of the magnetizing inductor charges the Capacitor C_3. Therefore, i_{Lin} and i_{LM} start to decrease linearly. This state ends when the current of the clamp diode D_1 reaches zero under a low reverse recovery issue. The following equations for the voltage can be achieved in this mode:

$$v_{Lin} = V_{in} - v_{C2} \tag{7}$$

$$v_{LM} = \frac{-v_{C1}}{1 - n_{21}} \tag{8}$$

$$v_{C3} = v_{C2} + n_{31} v_{LM} \tag{9}$$

$$D_4 \approx \frac{2}{M\left(I_{o1} + I_{o2}\right) + \frac{I_{o1}}{1-n_{21}}} \tag{10}$$

Here D_4 is the time duration of the operating mode-4.

Mode-5 $[t_4 - t_5]$: In this mode, the Diode D_2 is still ON, and D_{o1} begins to conduct under a gentle slope (Figure 3e). Meanwhile, the Capacitor C_3 still receives energy from the secondary side of the TWCI. During this mode, the energies of L_m and L_{in} are released to the output Capacitor C_{o1}. This mode is finished when the output Diode Do_1 turns OFF with low reverse recovery. In this interval, the following equations can be obtained:

$$v_{Co1} = v_{C2} + v_{LM} \tag{11}$$

$$v_{C3} = v_{C2} - v_{C1} + v_{LM}\left(n_{21} - n_{31} - 1\right) \tag{12}$$

$$D_5 = \frac{\pi I_o}{i_{Do1(peak)}} \tag{13}$$

$$f_{R5} = \frac{1}{T}_{R5} = \frac{1}{2\pi\sqrt{L_k\left(C_2 \| (n_{31} - n_{21})^2 C_3 \| C_1\right)}} \tag{14}$$

where D_5 and f_{R5} are the time interval and the resonant frequency of Mode-5.

Mode-6 $[t_5 - t_6]$: As it is shown in Figure 3f, same as in the previous mode, the Capacitor C_3 receives energy from the TWCI. Moreover, the energies of the magnetizing inductor and Capacitor C_1 are delivered to the Capacitor C_2.

$$v_{C3} = v_{C2} - v_{C1} + v_{LM}\left(n_{21} - n_{31} - 1\right) \tag{15}$$

$$D_6 = 1 - \mathrm{D} - D_4 - D_5 \tag{16}$$

Here D_6 denotes the time interval of Mode-6.

3 | STEADY-STATE ANALYSIS OF THE PROPOSED STRUCTURE

3.1 | Voltage gain

Using the KVL on the input and magnetizing inductances, the following equations can be expressed:

$$V_{C2} = \frac{V_{in}}{1 - D} \tag{17}$$

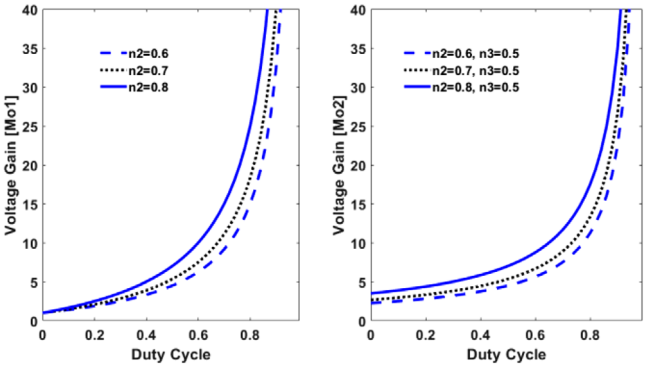


FIGURE 4 The voltage gain of the presented converter versus the duty cycle and several n_{21} and n_{31}.

$$V_{C1} = \frac{D.V_{in}}{1 - D} \tag{18}$$

where D represents the duty cycle of the switch. Using (8), (9), (17), and (18), the voltage of the Capacitor C_3 is determined as:

$$V_{C3} = \frac{1 + Dn_{31} - n_{21}}{\left(1 - n_{21}\right)\left(1 - D\right)} .V_{in} \tag{19}$$

Moreover, using (12) and (4), the averaged values of the positive (M_{o1}) and negative (M_{o2}) voltages can be obtained as:

$$M_{o1} = \frac{V_{C01}}{V_{in}} = \frac{(1 + D - n_{21})}{(1 - n_{21})(1 - D)} \tag{20}$$

$$M_{o2} = \frac{V_{C02}}{V_{in}} = \frac{1 + n_{31} - n_{21}}{(1 - n_{21})(1 - D)} \tag{21}$$

Thus, the overall voltage gain of the presented converter in CCM operation is obtained as:

$$M = \frac{V_o}{V_{in}} = M_{o1} + M_{o2} = \frac{2 + \mathrm{D} + n_{31} - 2n_{21}}{(1 - n_{21})(1 - D)} \tag{22}$$

Equations (20) and (21) show the positive and negative DC output voltages of the presented converter, which can be regulated in a wide range by three parameters D, n_{21}, and n_{31}. Figure 4 depicts the voltage gains M_{o1} and M_{o2} of the proposed circuit versus the duty cycle under some n_{21} and n_{31}. From this figure, the regulation of the M_{o1} and M_{o2} can be made separately. Also, the 3D plot of the overall voltage gain M in the function of n_{21} and n_{31} is illustrated in Figure 5. It is clear that the voltage gains M_{o1}, M_{o2}, and M are more sensitive to increasing n_{21} towards unity $(n_{21} \rightarrow 1)$. Hence, a higher output voltage can be obtained at fewer turns ratios of the TWCI, which alleviates the power loss.

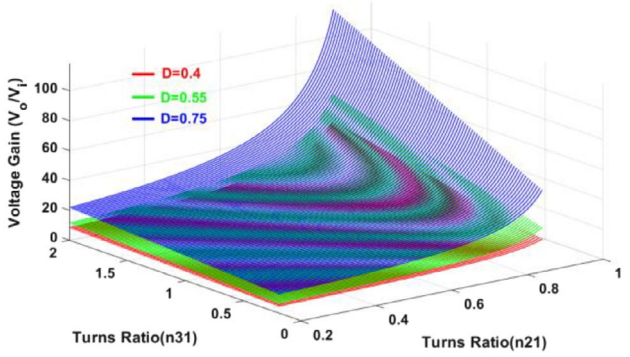


FIGURE 5 3D plot of the voltage gain M versus n_{21} and n_{31}.

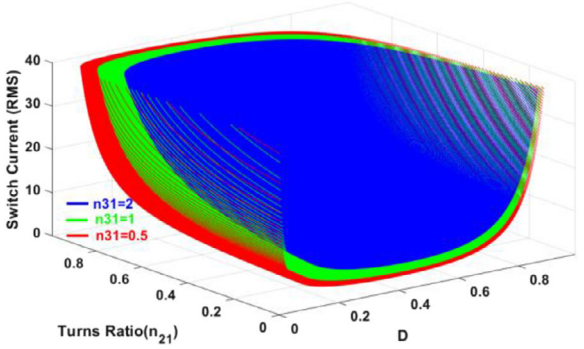


FIGURE 6 RMS current of the power switch versus D and n_{21}.

3.2 | Voltage and current stresses

Concerning the suggested topology operation, the voltage stresses of the single power switch and the converter diodes are derived as given in (23)–(25).

$$V_{S(Peak)} = V_{D1(Peak)} = \frac{V_{in}}{1-D} = \frac{(1-n_{21})}{2+D+n_{31}-2n_{21}} V_o \tag{23}$$

$$V_{Do1} = \frac{1}{2+D+n_{31}-2n_{21}} V_o \tag{24}$$

$$V_{D2} = V_{Do2} = \frac{1+n_{31}-n_{21}}{2+D+n_{31}-2n_{21}} V_o \tag{25}$$

By assuming the critical mode for the Mode-2, ($0.5T_R \approx DT_S$) and the sinusoidal form of current, the peak current value of the output Do_2 can be approximated as:

$$i_{Do2_{peak}} = \frac{\pi}{2D} I_{o2-o} \tag{26}$$

Here $I_{o2\text{-}o}$ is defined as:

$$I_{o2-o} = \frac{V_{o2}}{R_{L2}} + \frac{V_o}{R_L} \tag{27}$$

The maximum current value of D_2 and D_{o1} can be estimated as:

$$i_{D2(peak)} \approx \frac{I_{o2-o}}{1-D} \tag{28}$$

$$i_{Do1(peak)} \approx (1-n_{21})\, I_{Lin} \tag{29}$$

Regarding the State-2 of the proposed topology, the maximum and RMS values of the currents passed through the switch are approximated as follow:

$$I_{S(Peak)} \approx I_{in} + \frac{\frac{\pi}{2D} I_{o2-o}(1+n_{31}-n_{21}) + I_{o1-o}}{1-n_{21}} \tag{30}$$

$$I_{S(RMS)} = \sqrt{DH^2 + \frac{DX^2}{2} + \frac{4DHX}{\pi}} \tag{31}$$

where M and H are defined as:

$$H = I_{in} + \frac{I_{o1-o}}{1-n_{21}} \tag{32}$$

$$X = \frac{\pi I_{o2-o}}{2D}\left(\frac{1+n_{31}-n_{21}}{1-n_{21}}\right) \tag{33}$$

$$I_{in} = M_{o1}\frac{V_{o1}}{R_{L1}} + M_{o2}\frac{V_{o2}}{R_{L2}} + M\frac{V_o}{R_L} \tag{34}$$

From Mode-3, the current of the power switch at the turn-off time is estimated as follows:

$$i_{SW}^{t=off} = i_S^{t=t_3} = H \tag{35}$$

In addition, the peak current value of the clamp Diode D_1 at the start of the operating Mode-4 is expressed as:

$$i_{D1(peak)} = i_S^{t=t_3} \tag{36}$$

Figure 6 depicts a 3D plot of the RMS of the power switch current as a function of the duty cycle and n_{21} under some values of n_{31}. From this figure, a proper duty cycle range to achieve better performance is about $0.3 < D < 0.7$.

Moreover, the RMS current values of the circuit components of the introduced topology are estimated as follows:

$$i_{D1_{(RMS)}} = H\sqrt{\frac{D_4}{3}} \tag{37}$$

$$i_{D2_{(RMS)}} = I_{o2-o}\sqrt{\frac{1}{1-D}} \tag{38}$$

$$i_{Do1_{(RMS)}} = \frac{(1-n_{21})\, I_{in}}{2}\sqrt{\frac{T_{R5}}{T_s}} \tag{39}$$

$$i_{Do2_{(RMS)}} = \frac{\pi}{2} I_{o2-o}\sqrt{\frac{1}{2D}} \tag{40}$$

Moreover, the RMS current values of the converter capacitors are calculated as follows:

$$I_{C1(RMS)} = \sqrt{\left(\frac{\pi n_{31} I_{o2-o}}{4D(1-n_{21})}\right)^2 . D + \left(\frac{I_{o2-o}}{1-D} - I_{in}\right)^2 . (1-D)} \tag{41}$$

TABLE 1 The parasitic parameters of the switched-mode converter.

Parameter	Description
$r_{DS(ON)}$	ON-state resistance of the switch
t_{on}, t_{off}	Turn-off and turn-on times of the switch
T_s	The switching cycle time of the power switch
ESR_i	Equivalent series resistance of the capacitors
V_F	Voltage drop of the diode
C_{oss}	Output capacitance of the MOSFET
r_D	Conduction resistance of the diode
r_{Lin}, r_{Ni}	Parasitic resistances of the input inductor and CI windings

$$I_{C2(RMS)} \approx I_{C1(RMS)} \tag{42}$$

$$I_{C3(RMS)} = I_{o2-o}\sqrt{\frac{\pi^2}{8D} + \frac{1}{1-D}} \tag{43}$$

$$I_{Co1(RMS)} = \sqrt{(I_{o1-o})^2.D + \left(\frac{(1-n_{21})\,I_{in}}{2}\right)^2.\frac{T_{R2}}{T_s}} \tag{44}$$

$$I_{Co2(RMS)} = I_{o2-o}\sqrt{\frac{\pi^2}{8D} + 1 - D} \tag{45}$$

In addition, the RMS current values of the three sides of the TWCI are estimated as:

$$I_{N1(RMS)} = \sqrt{(1-D)\,H^2 + \frac{DX^2}{2}} \tag{46}$$

$$I_{N2(RMS)} \approx I_{N1(RMS)} \tag{47}$$

$$I_{N3(RMS)} = I_{o2-o}\sqrt{\frac{\pi^2}{8D} + \frac{1}{1-D}} \tag{48}$$

3.3 | Efficiency estimation

This section evaluates the power loss mechanism of the proposed topology. The main parasitic components of the switch-mode converters are given in Table 1.

The ZCS operation of the single power switch of the proposed converter eliminates the power loss at turn-on instant.

Also, the resonant tank of the operating Mode-2 alleviates the switch-off loss. Therefore, the power dissipation of the power switch in the presented circuit can be estimated as:

$$P_S = \frac{1}{2T_s}.V_{DS}\left(i_S^{t=off}.t_{off}\right) + \frac{1}{2T_s}\left(C_{oss}.V_{DS}^2\right) + r_{DS(on)}.I_{S(RMS)}^2 \tag{49}$$

Here, $i_S^{t=off}$ and $I_{S(RMS)}$ are the switch current of turn-of time and RMS values given by (31) and (36).

As described, in the proposed converter, all diodes turn off without reverse recovery loss. Thus, the conduction power loss of the diodes of the presented topology can be calculated as follows:

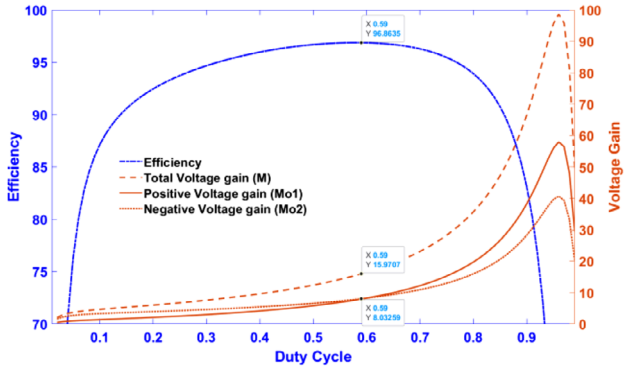


FIGURE 7 Non-ideal voltage gains and efficiency of the proposed converter versus duty cycle.

$$P_{Di} = V_F.I_{D(AVG)} \tag{50}$$

where $I_{D(AVG)}$ is the averaged value of the diode current. The capacitor losses can be determined as:

$$P_{Cap.i} = ESR_i.I_{C(RMS)}^2 \tag{51}$$

Finally, the magnetic components losses can be estimated by:

$$P_{Mag.} = r_{L_{in}}.I_{L_{in}(RMS)}^2 + r_{N1}.I_{lk1(RMS)}^2 + r_{N2}.I_{N2(RMS)}^2 + r_{N3}.I_{N3(RMS)}^2 + P_{Core(Lin,\ TWCI)} \tag{52}$$

Figure 7 shows the theoretical efficiency along with the non-ideal voltage gains (Total (M), Positive (M_{o1}), and Negative (M_{o2})) of the proposed converter at V_{in} = 25 V, R_{L1} = 1000 Ω, R_{L2} = 700 Ω, R_L = 1200 Ω, n_{21} = 0.75, n_{31} = 0.6, and f_s = 50 kHz. In this condition, at D = 0.59, two output voltages are equal $V_{o1} = V_{o2}$ = 200 V. Also, the values of the parasitic components of the circuit are selected as: r_{DS} = 3.7 mΩ, t_{off} = 88 ns, C_{oss} = 670 pF, $r_{C1} = r_{C2} = 7 = r_{C3}$ = 7 mΩ, $r_{Co1} = r_{Co2}$ = 0.1 Ω, $V_{FD1} = V_{FD2}$ = 0.67 V, $VF_{Do1} = VF_{Do2}$ = 0.65 V, $r_{D1} = r_{D2}$ = 5 mΩ, $r_{Do1} = r_{Do2}$ = 7 mΩ, r_{Lin} = 12 mΩ, r_{N1} = 15 mΩ, r_{N2} = 10 mΩ, r_{N3} = 14 mΩ).

Regarding this figure, due to the high voltage and current levels at higher duty cycles, the maximum power-handling capability and actual voltage are limited, which also happens in other step-up topologies. However, converters such as the proposed converter, which have a high voltage gain and soft-switching performance, can provide higher power-handling capacities and voltage gain.

Moreover, the theoretical efficiency along with the non-ideal voltage gain of the proposed converter as a function of the duty cycle under several values of n_{21}, n_{31} is depicted in Figure 8. According to this figure, considering higher values for n_{21} to a small amount value towards unity ($n_{21}\rightarrow 1$) (increasing this value does not have much effect on increasing their parasitic resistance) can cause proper efficiency in the proposed converter.

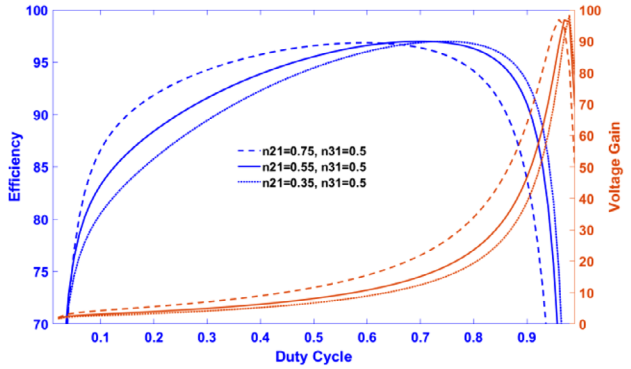


FIGURE 8 Calculated efficiency under various n_{21}.

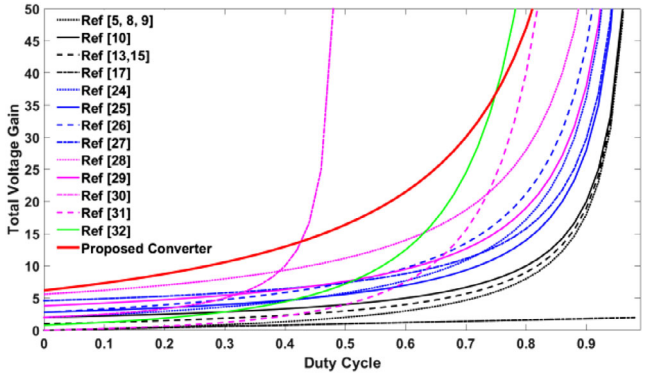


FIGURE 9 Total voltage gain comparison.

4 | PERFORMANCE COMPARISON

Table 2 compares some typical performance indicators including components count, voltage gains, device stresses, switching performance, and input current ripple of the proposed and other converters mentioned in the literature.

From Table 2, only the proposed and converters in [17], and [26–29] act under soft-switching condition along with a very low reverse recovery problem. At turns ratio $n_{21} = 0.75$, $n_{31} = 1.05$ (for TWCI), $n = 1.8$ (for two-winding CI), Figure 9 shows the total voltage gain comparison of the converters specified in Table 2. It can be seen that the proposed converter, along with

TABLE 2 Performance comparison of the proposed converter with different converters with bipolar output voltage capability.

Converter topology	No. of components S/D/C/CI+L/T	Voltage gain Positive (M_{o1})	Voltage gain Negative (M_{o2})	L.I.C.R.	Voltage stress on main switch (V_s/V_o)	Maximum voltage stress on diodes (V_D/V_o)	Soft-switching (main switch)	Reverse recovery loss
[5]	1/2/4/0+4/11	$\frac{D}{(1-D)}$	$\frac{D}{(1-D)}$	Yes	$\frac{V_o}{2D}$	$\frac{V_o}{2D}$	–	High
[8]	1/2/4/0+3/10	$\frac{D}{(1-D)}$	$\frac{D}{(1-D)}$	Yes	$\frac{V_o}{2D}$	$\frac{V_o}{2D}$	–	High
[9]	1/2/4/0+3/10	$\frac{D}{(1-D)}$	$\frac{D}{(1-D)}$	Yes	$\frac{V_o}{2D}$	$\frac{V_o}{2D}$	–	High
[10]	1/3/3/0+1/8	$\frac{1}{(1-D)}$	$\frac{1}{(1-D)}$	Yes	$\frac{V_o}{2}$	$\frac{V_o}{2}$	–	High
[13]	1/2/3/0+2/8	$\frac{1}{(1-D)}$	$\frac{D}{(1-D)}$	Yes	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$	–	High
[15]	1/2/3/0+2/8	$\frac{1}{(1-D)}$	$\frac{D}{(1-D)}$	Yes	$\frac{V_o}{1+D}$	$\frac{V_o}{1+D}$	–	High
[17]	2/2/4/0+2/10	D	D	No	$\frac{V_o}{2D}$	$\frac{V_o}{2D}$	ZVS	High
[24]	1/3/3/1^{2w}+0/8	$\frac{1+nD}{(1-D)}$	$\frac{1}{(1-D)}$	No	$\frac{V_o}{2+nD}$	$\frac{(1+n)V_o}{2+nD}$	–	Very low
[25]	1/4/4/1^{2w}+0/10	$\frac{n}{(1-D)}$	$\frac{1}{(1-D)}$	No	$\frac{V_o}{1+n}$	$\frac{nV_o}{1+n}$	–	Very low
[26]	1/4/4/1^{2w}+0/10	$\frac{1+n}{(1-D)}$	$\frac{nD}{(1-D)}$	No	$\frac{V_o}{1+n+nD}$	$\frac{(1+n)V_o}{1+n+nD}$	ZCS	High
[27]	2/3/5/1^{2W}+1/12	$\frac{1+n}{(1-D)}$	n	No	$\frac{V_o}{1+n(2-D)}$	$\frac{(1+n)V_o}{1+n(2-D)}$	ZVS	Very low
[28]	2/4/5/1^{2W}+0/12	$\frac{1+n}{(1-D)}$	$\frac{1+n}{(1-D)}$	No	$\frac{V_o}{2(1+n)}$	$\frac{V_o}{2}$	ZVS	Very low
[29]	1/5/5/$1^{3\ W}$+0/12	$\frac{2+n_{21}}{(1-D)}$	$-\frac{n_{31}}{(1-D)}$	No	$\frac{V_o}{2+n_{21}+n_{31}}$	$\frac{(1+n_{21})V_o}{2+n_{21}+n_{31}}$	ZCS	Low
[30]	2/5/4/0+1/12	$\frac{1}{(1-2D)}$	$-\frac{1}{(1-2D)}$	Yes	$\frac{V_o}{2}$	$\frac{V_o}{2}$	–	High
[31]	3/4/4/0+3/14	$\frac{D}{(1-D)^2}$	$\frac{D}{(1-D)^2}$	Yes	$\frac{(1-D)V_o}{2D}$	$\frac{V_o}{2D}$	–	High
[32]	2/4/4/1^{3W}+1/12	$\frac{D}{(1-D)^2}$	$\frac{n+D-1}{(1-D)^2}$	Yes	$\frac{(1-D)V_o}{2D+n-1}$	$\frac{(n+D-1)V_o}{2D+n-1}$	QR	Low
Proposed converter	1/4/5/$1^{3\ W}$+1/12	$\frac{1+D-n_{21}}{(1-n_{21})(1-D)}$	$\frac{1+n_{31}-n_{21}}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+D+n_{31}-2n_{21}}$	$\frac{1+n_{31}-n_{21}}{3+D+n_{31}-3n_{21}}$	ZCS+QR	Very low

S = Switch, D = Diode, C = Capacitor, CI = Coupled-inductor, L = Inductor, T = Total device count, L.I.C.R. = Low input current ripple.

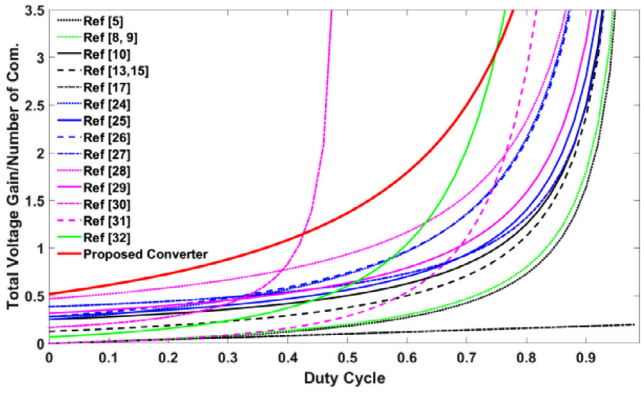


FIGURE 10 The comparison of total voltage gain per number of components.

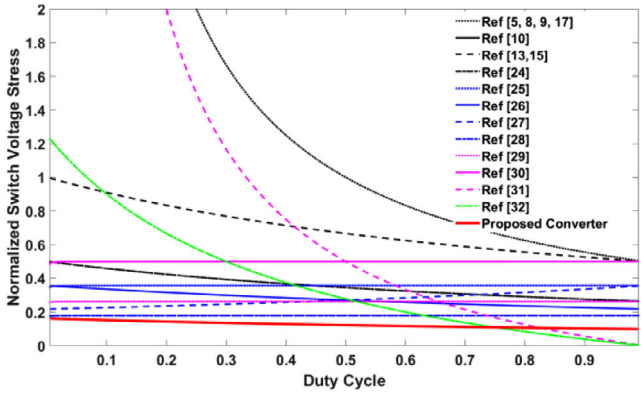


FIGURE 11 Comparison of normalized voltage stress on the main power switch.

the converter in [30] can provide higher output voltages than the others. However, the steep slope of voltage gain changes in the converter [30] leads to its more complicated control. Furthermore, the ratio of the voltage gain ratio to the whole number of circuit components (M/N) is a reasonable indicator to evaluate the power density of the converter. Therefore, a comparison of the voltage gain to the number of components for the converters referred to in Table 2 is demonstrated in Figure 10. Based on this figure, just the introduced circuit in this article and the converter in [28] (with the steep slope of voltage gain changes) have a higher value of M/N at a full range of duty cycle.

Also, Figure 11 illustrates the normalized switch voltage stress of the converters mentioned in Table 2. From this figure, the proposed topology has the lowest voltage stress among the competitors. Similarly, Figure 12 indicates the normalized maximum diode voltage stress of the converters in Table 2. Here, the maximum voltage stress of the diodes of the proposed topology is at a low level.

In addition, the estimated costs of the converters at a same working point (200 W, 25 V/400 V, $n_{21} = 0.8$, $n_{31} = 0.54$, $n = n_{21}+n_{31} = 1.34$ and 50 kHz) given in the comparison Table 2 are taken from Mouser, Digikey and nz.rs-online websites, which are summarized in Table 3. Regarding this table,

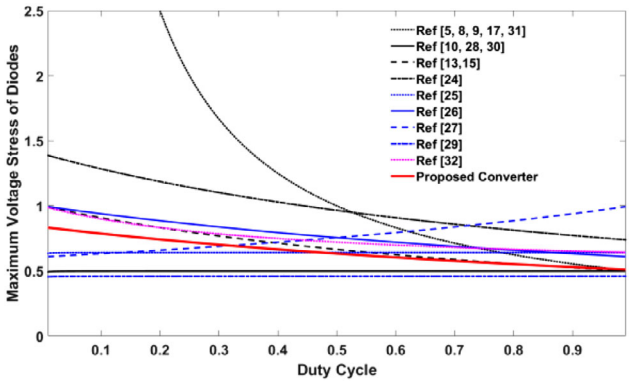


FIGURE 12 Comparison of normalized maximum voltage stress of the diodes of the converters in Table 2.

TABLE 3 Summarized of cost comparison of the converters.

	Cost of components				
Converter	**Cores**	**Switches**	**Capacitors**	**Diodes**	**Total**
[5]	$9.32	$8. 4	$8.95	$2.46	$29.13
[8]	$7.71	$8. 4	$8.95	$2.46	$27.52
[9]	$7.71	$8. 4	$8.95	$2.46	$27.52
[10]	$2.57	$8. 4	$8.4	$2.25	$21.62
[13]	$5.14	$8. 4	$8.3	$3.13	$25.97
[15]	$5.14	$6.7	$8.3	$3.13	$25.97
[17]	–	–	–	–	–
[24]	$2.57	$6.7	$4.82	$4.38	$17.47
[25]	$2.57	$6.7	$8.2	$4.53	$22.0
[26]	$2.57	$6.7	$11.61	$3.54	$24.42
[27]	$5.14	$13.2	$17.7	$4.2	$40.25
[28]	$2.57	$11.6	$4.12	$2.79	$21.08
[29]	$2.57	$6.7	$10.9	$5.44	$25.61
[30]	$2.09	$11.4	$11.2	$4.62	$29.31
[31]	$7.23	$17.3	$7.14	$4.16	$35.83
[32]	$4.66	$9.47	$8.15	$4.57	$26.85
Proposed converter	$4.18	$2.38	$8.15	$3.1	$17.81

the total cost of the proposed converter and the converter in [24] are at the lowest level. However, the converter in [24] suffers from high input current ripple and hard switching performance.

The comparisons show that in the proposed structure, higher voltage gain can achieve by a lower number of turns ratios.

Moreover, the semiconductors of the proposed circuit have lower power switch and diode voltage stresses. Therefore devices with lower voltage rated can be selected. In addition, the soft-switching condition, along with very low reverse recovery, make the proposed topology give a high output voltages under enough high efficiency.

5 | PARAMETERS DESIGN

The parameters design includes the magnetic components, resonant tank, and capacitors. The input inductor of the suggested topology is designed to limit the input current ripple at a desirable rate given as:

$$L_{in} = \frac{V_{in}.D}{\Delta I_{Lin}.f_s} \tag{53}$$

Here ΔI_{in} denotes the permitted peak-to-peak ripple of the input current. To guarantee the usage life of the RES, the permitted current ripple of about 20% is recommended. Furthermore, the magnetizing inductance of the TWCI can be obtained as:

$$L_M > \frac{V_{LM}.D}{\Delta I_{LM}.f_s} = \frac{V_{in}.D}{\Delta I_{LM}.(1-n_{21})\,f_s} \tag{54}$$

where ΔI_{LM} is the current ripple rate. It is important to mention that considering a very low ripple rate for the magnetizing inductor raises the wire consumption and an IR^2 loss. The output capacitances C_{o1} and C_{o2} for achieving voltage ripple factor less than 1% can be calculated as follows:

$$C_{o1} = \frac{D}{\Delta V_{co1}.f_s}\left(\frac{V_{o1}}{R_{L1}} + \frac{V_o}{R_L}\right) \tag{55}$$

$$C_{o2} = \frac{1-D}{\Delta V_{co2}.f_s}\left(\frac{V_{o2}}{R_{L2}} + \frac{V_o}{R_L}\right) \tag{56}$$

In addition, the suitable values of the middle capacitors including C_1, C_2, and C_3 can be given as:

$$C_1 = \frac{\mathrm{D}.i_{N2}}{\Delta V_{C1}.f_s} = \frac{n_{31}\pi I_{o2-o}}{\Delta V_{C1}.2\,(1-n_{21})\,f_s} \tag{57}$$

$$C_2 = \frac{\mathrm{D}.i_{N2}}{\Delta V_{C2}.f_s} = \frac{n_{31}\pi I_{o2-o}}{\Delta V_{C2}.2\,(1-n_{21})\,f_s} \tag{58}$$

$$C_3 = \frac{i_{D2}.\mathrm{D}}{\Delta V_{c3}.f_s} = \frac{I_{o2-o}}{\Delta V_{c3}.(1-D)\,.f_s} \tag{59}$$

here ΔV_{Ci} represents the allowable voltage ripple rate of each capacitor. But, calculating the C_2 and C_1 values need extra consideration. Since the middle capacitors C_1 and C_2 play an important role in the resonant tank, so using (1), the proper values of these capacitors to obtain the proper resonant frequency is calculated by:

$$\pi\sqrt{L_{k1}\,(C_2 \| C_1)} = DT_S \tag{60}$$

6 | EXPERIMENTAL VALIDATION

A 235 W prototype with an input DC voltage 25 V and output DC voltages 200 V/−200 V (total 400 V) is established to verify the theoretical analysis of the suggested converter. The specifications of this prototype are summarized in Table 4. Due to adopting a passive clamp circuit, a MOSFET (IRFB4110) with a very low $R_{DS(on}$ is used. To improve the converter efficiency, film capacitors (MKP and MKT series) with very low ESR have been considered. To extract the current shapes with better quality, a high-frequency current probe PA-667 with division rates of 500 and 50 mV/A is used. Moreover, in order to measure the voltage of the circuit elements that do not have a common ground, a differential voltage probe GDP-025 with division coefficients of ×20, ×50 and ×200 is also employed. Also, the magnetic parameters and parasitic resistances of the components are measured using a Hantek 1833C.

TABLE 4 key parameters of prototype setup.

Parameter	Values
Output power (P_{out})	235 W
Input voltage (V_{in})	25 V
Loads (R_{L1}, R_{L2}, R_L)	1000 Ω, 700 Ω, 1200 Ω
Output voltages (V_{o1},V_{o2}, V_o)	+200 V, −200 V, 400 V
Switching frequency (f_s)	50 kHz
Capacitors C_1, C_3	MKP 8.2 μF/250 V
Capacitor C_2	MKP 5.6 μF/250 V
Capacitors C_{o1}, C_{o2}	MKT 5.6 μF/275 V
Power switch S	IRFB4110/$R_{DS(on)}$ = 3.7 mΩ
Input inductor L_{in}	110 μH/T184-52
Magnetizing inductor of the CL (L_m)	250 μH
Turns ratios of the TWCI (n_{21}:n_{31})	(0.77:0.6)/EE42/21/20
Diodes D_2 , D_{o1} and D_{o2}	MUR440
Diode D_1	MBR10100

Figure 13a expresses the experimental results of the MOSFET (i_{sw} and V_{DS}). According this figure, the power MOSFET turns ON under ZCS conditions with low voltage stress (V_{DS} ≈ 60 V). Moreover, with the quasi-resonant performance of the converter during Mode-2, the current value of the MOSFET is decreased at the turn-off instants, which decreases the switching power loss. Regarding Figure 13b,c, the current of all diodes reaches zero with a light slope without having reverse recovery issues.

Moreover, the voltage stress rates at the converter diodes are V_{D1} = 60 V, V_{D2} = V_{Do1} = V_{Do2} ≈ 250 V, which are lower than the output DC voltage (V_o = 400 V). Furthermore, Figure 14 illustrates the input and leakage inductors' currents, which are matched with the given key waveforms in Figure 2. Based on this figure, the input current ripple is limited to about 20%, which is suitable for RES. In addition, the output voltages of the proposed converter, including V_{o1} (positive), V_{o2} (negative), and V_o (V_{o1}+ V_{o2}) are shown in Figure 15. Since the current of the output diodes D_{o1} and D_{o2} reach zero at a very low slope, the DC output voltages are regulated without voltage noises at the switching moments, which is another merit of the proposed topology.

The measured efficiency of the presented topology versus the output power changes at V_{o1} = 200 V, V_{o2} = —200 V, and V_o = 400 V is provided in Figure 16. The full load efficiency of the converter is about 95.2%. Also, Figure 17 shows the

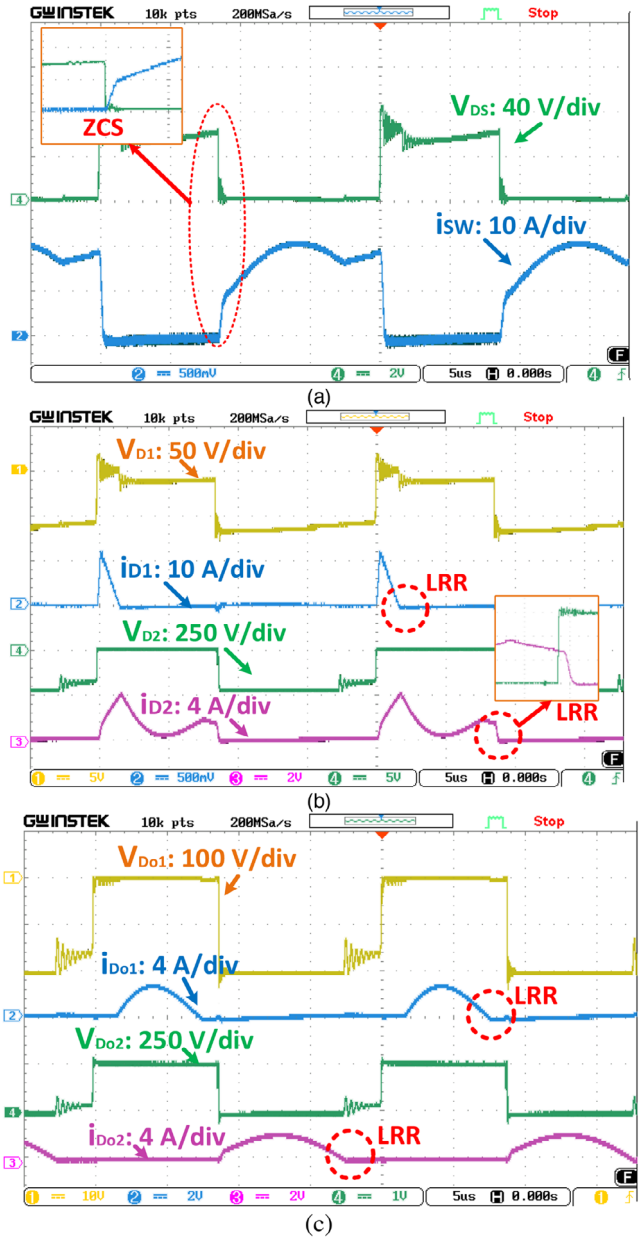


FIGURE 13 Experimental results of the switching components. (a) MOSFET, (b) diodes D_1 and D_2, (b) diodes D_{o1} and D_{o2} (LRR = low reverse recovery).

dissipation loss breakdown profile of the converter at full load conditions. To achieve the power dissipation of each parameter, the parasitic components are measured from the sample prototype. The soft-switching performance, along with the low voltage stresses, makes the share of the semiconductor power losses at a small level compared to the magnetic devices' loss.

Figures 18, 19 show the dynamic responses of the presented converter at the output load and input DC voltage variations. In this test, the output load resistance R_{L1} has been switched from 600 Ω to 1200 Ω. Also, the input DC source has been switched from V_{in} = 20 V to V_{in} = 25 V. From these figures, a simple closed-loop controller (PI) can regulate the output voltages at V_o = 400 V, successfully.

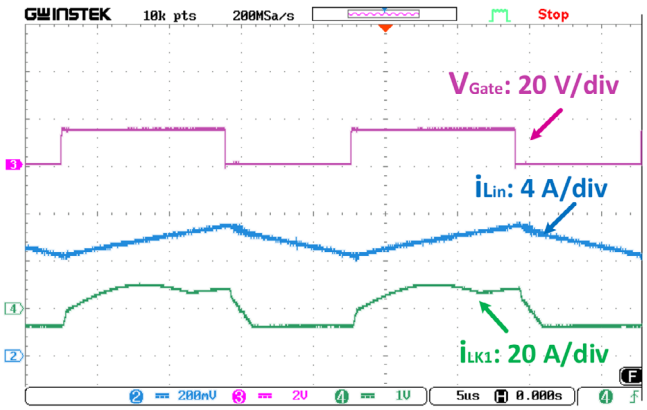


FIGURE 14 Experimental results of V_{gate}, i_{Lin} and i_{Lk1}.

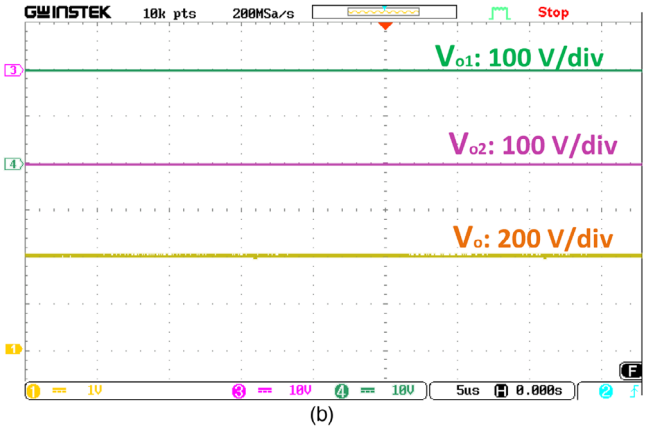


FIGURE 15 Experimental results of V_{o1} (positive output), V_{o2} (negative output), and V_o.

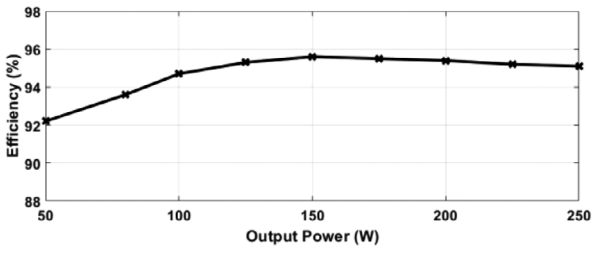


FIGURE 16 Measured efficiency versus output power.

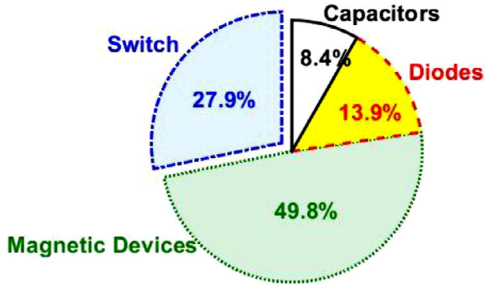


FIGURE 17 Estimated power loss breakdown profile of the converter at full load condition (25 V/(200 V, −200 V, 400 V)/235 W).

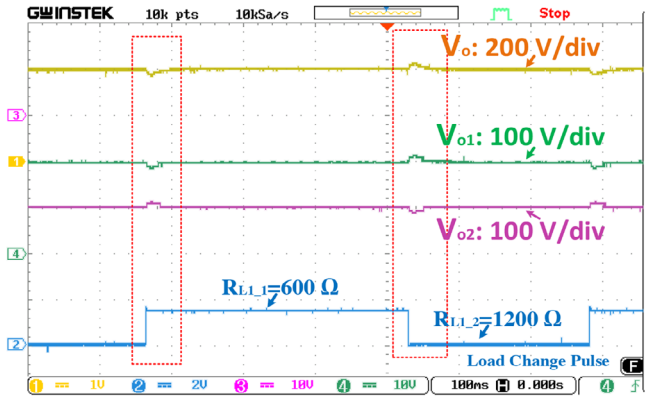
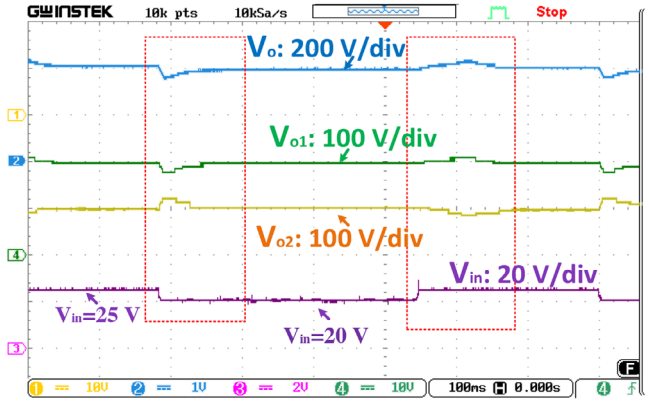


FIGURE 18 Dynamic response. under 100% disturbance in the output load R_{L1}.



(b)

FIGURE 19 Diagram of the dynamic response under 20% disturbance in the input DC voltage.

Also, the power loss distribution of the suggested topology components is listed in Table 5. The values of the parasitic resistances of the CI, and capacitors are measured with the help of a RLC meter Hantek 1833C. Furthermore, the real values of the forward voltage drop (V_F) of the converter diodes are obtained by their instantaneous currents.

It should be mentioned that since the coupled inductor of the proposed converter has semi-trans-inverse property, it does not need a large number of turns. In this case, due to low turns ratios and small parasitic resistance, they do not play a significant role in converter power losses.

7 | CONCLUSION

In this article, a new coupled-inductor-based high voltage gain DC-DC converter with bipolar outputs has been presented. The low input current ripple of the proposed converter is desirable for fuel cell, photovoltaic, and battery applications. In this topology, high voltage gains are achieved using the concepts of three winding coupled-inductor along with the voltage multipliers. The introduced converter can offer three degrees of freedom to set the positive and negative voltage gains. The regenerative passive clamping technique suppresses voltage spikes at the single power switch. In this topology, to further reduce the power loss, a resonant tank is adopted with the parasitic (leakage inductance) and main components of the converter. Since the output diodes of the converter turn off with a little slope, the output DC voltages are free from switching spikes. Due to low voltage stresses, low voltage rated semiconductor devices (switch and diodes) with low parasitic components can be chosen to improve the efficiency. Finally, the experimental results of a sample prototype 235 W (V_{in} = 25 V/ V_{o1} = 200 V , V_{o2} = −200 V, and V_o = 400 V) have justified the feasibility of the suggested circuit design. Therefore, the proposed topology is well suited for high step-up renewable energy applications.

TABLE 5 Loss distributions of the proposed topology.

MOSFET losses

Device	Type	P_{on} (W)	P_{off} (W)	P_{Coss} (W)	$P_{con.}$ (W)	$P_{Total.}$ (W)
MOSFET	IRF4110	–	2.4	0.05	0.6	**3.05 W**

Diode losses

Device	Type	V_F (V)	$P_{Di.}$ (W)
D_1	MBR10100	0.55	0.27
D_2	MUR440	0.83	0.49
D_{o1}	MUR440	0.8	0.4
D_{o2}	MUR440	0.61	0.36
		Total	1.52 W

Capacitor losses

Device	Type	*ESR* (mΩ)	$P_{Ci.}$ (W)
C_1	8.2 uF 250 V (MKP)	7	0.39
C_2	5.6 uF 250 V (MKP)	10	0.49
C_3	8.2 uF 250 V (MKP)	7	0.015
C_{o1}	5.6 uF 275 V (MKT)	4.7	0.0047
C_{o2}	5.6 uF 275 V (MKT)	4.7	0.0030
		Total	0.9 W

Magnetic losses

Device	Type	$P_{Con.}$ (W)	$P_{Core.}$ (W)
L_{in}	T184-52	1.9	1.57
TWCI	EE42/21/20	0.92/0.82/0.05	0.07

AUTHOR CONTRIBUTIONS

Sara Hasanpour: Conceptualization; data curation; formal analysis; investigation; methodology; project administration; resources; software; supervision; validation; visualization; writing—original draft. **Yam Prasad Siwakoti**: Formal analysis; investigation; project administration; supervision; writing—review and editing. **Frede Blaabjerg**: Funding acquisition; investigation; project administration; validation; writing—review and editing.

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The authors declare no conflicts of interest.

DATA AVAILABILITY STATEMENT
The data presented in this study are available on request from the corresponding author.

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